THE DATASHEET OF

LTC4240IGN#PBF

CompactPCI Hot Swap Controller with I²C Compatible Interface

FEATURES

- **Allows Safe Board Insertion and Removal from a Live CompactPCI™ Bus**
- **I²C™ Compatible 2-Wire Interface**
- **PRECHARGE Output Biases I/O Pins During Card Insertion and Extraction**
- Controls 3.3V, 5V, 12V and –12V Supplies
- Foldback Current Limit with Circuit Breaker
- LOCAL_PCI_RST# Logic On-Board
- QuickSwitch® Enable Output
- Status LED Driver
- User Programmable Supply Voltage Power-Up Rate
- Registers Individual Supply Faults
- Available in a 28-Pin Narrow SSOP Package

APPLICATIONS

- Hot Board Insertion into CompactPCI Bus
- Electronic Circuit Breaker

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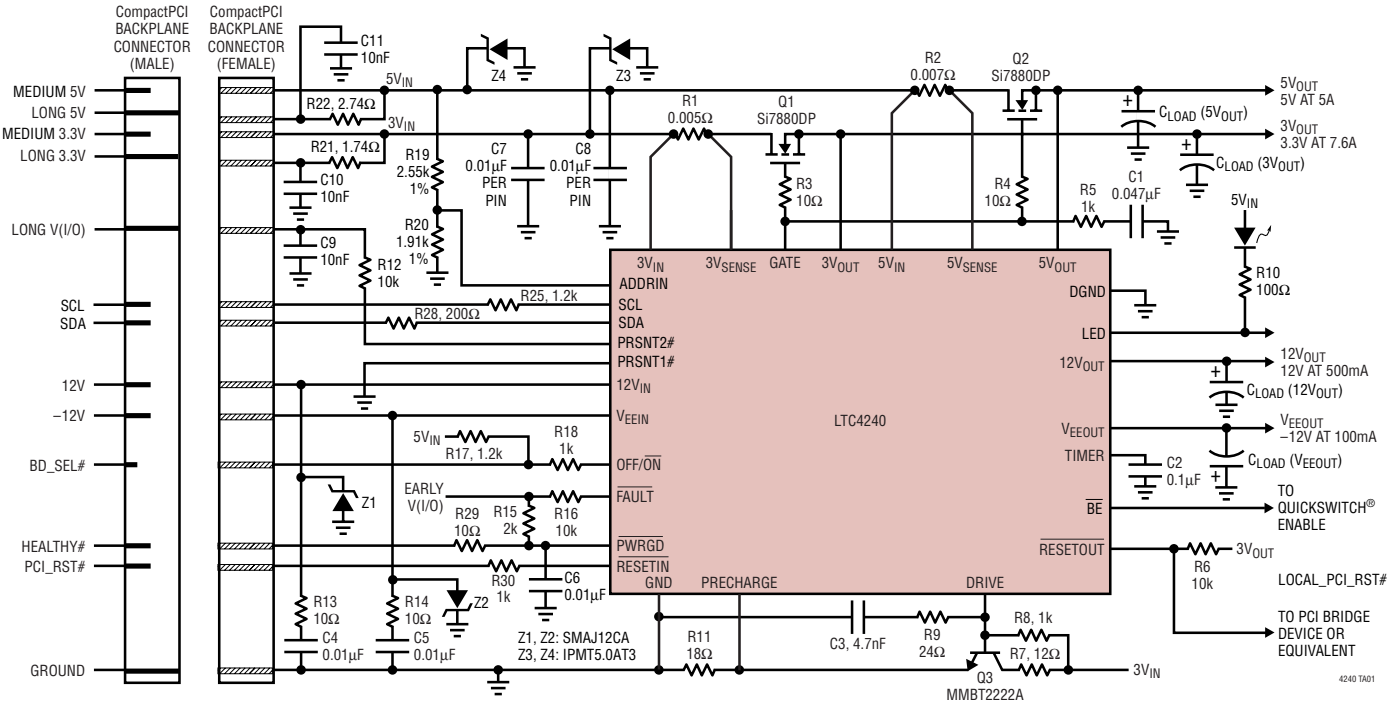
Hot Swap is a trademark of Linear Technology Corporation.
QuickSwitch is a registered trademark of Quality Semiconductor Corp.
CompactPCI is a trademark of the PCI Industrial Computer Manufacturers Group.
I²C is a trademark of Philips Electronics N.V.

DESCRIPTION

The LTC®4240 is a Hot Swap™ controller that allows a board to be safely inserted and removed from a live CompactPCI bus slot. The LTC4240 has a built-in 2-wire I²C compatible interface to allow software control and monitoring of device function and power supply status. Two external N-channel transistors control the 3.3V and 5V supplies, while two internal switches control the –12V and 12V supplies. Electronic circuit breakers protect all four supplies against overcurrent faults. The $\overline{PWRGD}$ output indicates when all of the supply voltages are within tolerance. The OFF/$\overline{ON}$ pin is used to cycle the board power or reset the circuit breaker. The I²C interface allows the user to turn the device off or on, set $\overline{RESETOUT}$, turn on the status LED driver and ignore 12V, –12V faults. It also allows the user to read the status of the $\overline{FAULT}$, $\overline{RESETIN}$, $\overline{RESETOUT}$, $\overline{PWRGD}$, PRSNT1# and PRSNT2# pins. Under a fault condition, the I²C interface can also be used to determine which of the four supplies generated the fault. The LTC4240 is available in a 28-pin narrow SSOP package.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltages
- $5V_{IN}$ ..... –0.3V to 12V
- $12V_{IN}$ ..... –0.3V to 14V
- V_{EEIN} ..... 0.3V to –14V

Input Voltages
- PRSNT1#, PRSNT2#, SCL, $\overline{RESETIN}$, OFF/$\overline{ON}$ ..... –0.3V to 12V
- $5V_{OUT}$, $5V_{SENSE}$, $3V_{IN}$, $3V_{SENSE}$, $3V_{OUT}$ ..... –0.3V to ($5V_{IN}$ + 0.3V)
- ADDRIN, PRECHARGE ..... –0.3V to $5V_{IN}$

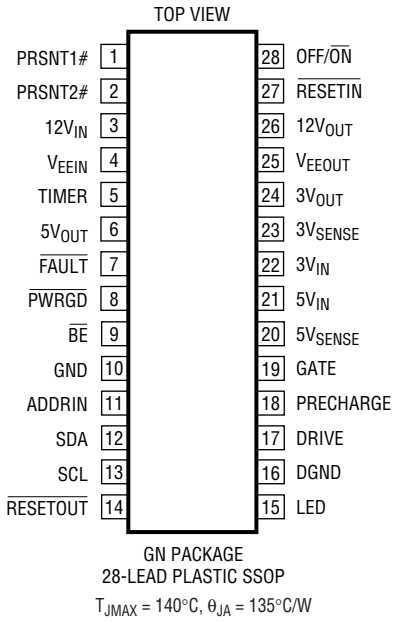
Output Voltages
- TIMER, $\overline{FAULT}$, $\overline{PWRGD}$, SDA, $\overline{RESETOUT}$, LED, DRIVE, GATE, $12V_{OUT}$ ..... –0.3V to 14V
- V_{EEOUT} ..... –14V to 0.3V
- $\overline{BE}$ ..... 0.3V to ($5V_{IN}$ + 0.3V)

Operating Temperature Range
- LTC4240C ..... 0°C to 70°C
- LTC4240I ..... –40°C to 85°C

Storage Temperature Range ..... 65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 140°C, θ_{JA} = 135°C/W

ORDER PART NUMBER
LTC4240CGN
LTC4240IGN

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. $12V_{IN}$ = 12V, V_{EEIN} = –12V, V_{3VIN} = 3.3V, V_{5VIN} = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD}	V_{12VIN} Supply Current	OFF/$\overline{ON}$ = 0V	●		3	8	mA
V_{LKO}	Undervoltage Lockout	$12V_{IN}$	●	7.00	8.00	10.80	V
		$5V_{IN}$	●	4.10	4.3	4.45	V
		$3V_{IN}$	●	2.35	2.45	2.55	V
		V_{EEIN}	●		–9	–10.5	V
V_{FB}	Foldback Current Limit Voltage	V_{FB} = (V_{5VIN} – $V_{5VSENSE}$), V_{5VOUT} = 0V, TIMER = 0V	●	15	25	35	mV
		V_{FB} = (V_{5VIN} – $V_{5VSENSE}$), V_{5VOUT} = 3V, TIMER = 0V	●	55	70	85	mV
		V_{FB} = (V_{3VIN} – $V_{3VSENSE}$), V_{3VOUT} = 0V, TIMER = 0V	●	15	25	35	mV
		V_{FB} = (V_{3VIN} – $V_{3VSENSE}$), V_{3VOUT} = 2V, TIMER = 0V	●	55	65	80	mV
V_{CB}	Circuit Breaker Trip Voltage	V_{TV} = (V_{5VIN} – $V_{5VSENSE}$), V_{5VOUT} = 5V, TIMER = Open	●	50	55	60	mV
		V_{TV} = (V_{5VIN} – $V_{5VSENSE}$), V_{5VOUT} = 0V, TIMER = Open	●	6	11	16	mV
		V_{TV} = (V_{3VIN} – $V_{3VSENSE}$), V_{3VOUT} = 3.3V, TIMER = Open	●	50	55	60	mV
		V_{TV} = (V_{3VIN} – $V_{3VSENSE}$), V_{3VOUT} = 0V, TIMER = Open	●	6	11	16	mV
t_{OC}	Overcurrent Fault Response Time	(V_{5VIN} – $V_{5VSENSE}$) = 100mV, TIMER = Open	●	25	35	55	µs
	Overcurrent Fault Response Time	(V_{3VIN} – $V_{3VSENSE}$) = 100mV, TIMER = Open	●	25	35	55	µs
t_{SC}	Short-Circuit Response Time	(V_{5VIN} – $V_{5VSENSE}$) = 200mV, TIMER = Open	●	25	35	55	µs
		(V_{3VIN} – $V_{3VSENSE}$) = 200mV, TIMER = Open	●	25	35	55	µs
$I_{GATE(UP)}$	GATE Pin Turn-On Current	OFF/$\overline{ON}$ = 0V, V_{GATE} = 0V, TIMER = 0V	●	–20	–65	–100	µA
$I_{GATE(DN)}$	GATE Pin Turn-Off Current	V_{GATE} = 5V, (Note 3)	●	100	200	300	µA
$I_{GATE(FAULT)}$	GATE Pin Fault-Off Current	OFF/$\overline{ON}$ = 0V, V_{GATE} = 2V, TIMER = Open, $\overline{FAULT}$ = 0V	●	2.5	6	8.5	mA
ΔV_{GATE}	External Gate Voltage	ΔV_{GATE} = (V_{12VIN} – V_{GATE}), I_{GATE} = 1µA	●		600	1000	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. $12V_{IN}$ = 12V, V_{EEIN} = –12V, V_{3VIN} = 3.3V, V_{5VIN} = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ΔV_{12V} ΔV_{VEE}	12V Switch Voltage Drop V_{EE} Switch Voltage Drop	$\Delta V_{12V} = (V_{12VIN} - V_{12VOUT})$, I = 500mA $\Delta V_{VEE} = (V_{EEOUT} - V_{EEIN})$, I = 100mA	● ●		300 125	600 250	mV mV
I_{CL}	Current Foldback	$12V_{IN}$ = 12V, $12V_{OUT}$ = 0V V_{EEIN} = –12V, V_{EEOUT} = 0V	● ●	–50 50	–350 250	–800 350	mA mA
I_{TH}	Current Fault Threshold	$12V_{IN}$ = 12V V_{EEIN} = –12V	● ●	–550 225	–1250 500	–1900 800	mA mA
T_{TS}	Thermal Shutdown Temperature	Note 4			150		°C
V_{TH}	Power Good Threshold Voltage	$12V_{OUT}$ $5V_{OUT}$ $3V_{OUT}$ V_{EEOUT}	● ● ● ●	10.8 4.50 2.8 –10	11.1 4.65 2.9 –10.5	11.4 4.75 3.0 –10.8	V V V V
V_{IL}	Input Low Voltage	OFF/$\overline{ON}$, $\overline{RESETIN}$, SCL, SDA, PRSNT1#, PRSNT2#	●			0.8	V
V_{IH}	Input High Voltage	OFF/$\overline{ON}$, $\overline{RESETIN}$, SCL, SDA, PRSNT1#, PRSNT2#	●	2			V
I_{IN}	Input Current PRSNT1#, PRSNT2#, OFF/$\overline{ON}$, $\overline{RESETIN}$, SDA, SCL	OFF/$\overline{ON}$ = $\overline{RESETIN}$ = SDA = SCL = 0V, 5V, PRSNT1#, PRSNT2# = 0V, 5V	● ●		±0.08 ±0.08	±2 ±2	µA µA
	$\overline{RESETOUT}$, $\overline{FAULT}$ Leakage Current	$\overline{RESETOUT}$ = $\overline{FAULT}$ = 12V, OFF/$\overline{ON}$ = 0V, $\overline{RESETIN}$ = 3.3V	●		±0.08	±2	µA
	$\overline{PWRGD}$ Leakage Current	$\overline{PWRGD}$ = 12V, OFF/$\overline{ON}$ = 4V	●		±0.08	±2	µA
	$5V_{SENSE}$ Input Current	$5V_{SENSE}$ = 5V, $5V_{OUT}$ = 0V, GATE = 0V	●		55	100	µA
	$3V_{SENSE}$ Input Current	$3V_{SENSE}$ = 3.3V, $3V_{OUT}$ = 0V, GATE = 0V	●		55	100	µA
	$5V_{IN}$ Input Current	$5V_{IN}$ = 5V, TIMER = 0V, OFF/$\overline{ON}$ = 0V	●		0.8	1.5	mA
	$3V_{IN}$ Input Current	$3V_{IN}$ = 3.3V, TIMER = Open $3V_{IN}$ = 3.3V, TIMER = 0V	● ●		250 250	600 500	µA µA
	$5V_{OUT}$ Input Current	$5V_{OUT}$ = 5V, OFF/$\overline{ON}$ = 0V, TIMER = 0V, GATE = 0V	●		237	400	µA
	$3V_{OUT}$ Input Current	$3V_{OUT}$ = 3.3V, OFF/$\overline{ON}$ = 0V, TIMER = 0V, GATE = 0V	●		120	200	µA
	V_{EEIN} Input Current	TIMER = 0V, OFF/$\overline{ON}$ = 0V	●		–950	–1200	µA
	Precharge Input Current	$V_{PRECHARGE}$ = 1V	●			10	µA
	ADDRIN	ADDRIN = 0V, 5V	●			±0.1	µA
I_{TIMER}	TIMER Pin Current	OFF/$\overline{ON}$ = 0V, TIMER = 0V TIMER = 5V, OFF/$\overline{ON}$ = 2V	● ●	–6 15	–11.5 28	–17 55	µA mA
V_{TIMER}	TIMER Threshold Voltages		●	5	5.5	6.5	V
R_{DIS}	$12V_{OUT}$ Discharge Impedance $5V_{OUT}$ Discharge Impedance $3V_{OUT}$ Discharge Impedance V_{EEOUT} Discharge Impedance		● ● ● ●		430 50 150 650	1000 100 300 1000	Ω Ω Ω Ω
V_{OH}	CMOS Output High Voltage	$\overline{BE}$, I = –100µA	●	$5V_{IN}$ – 0.4			V
V_{OL}	CMOS Output Low Voltage Output Low Voltage Output Low Voltage	$\overline{BE}$, I = 100µA $\overline{PWRGD}$, $\overline{RESETOUT}$, $\overline{FAULT}$, SDA(I = 3mA) LED (I = 10mA)	● ● ●			0.4 0.4 0.8	V V V
V_{PXG}	PRECHARGE Reference Voltage	V_{5VIN} = 5V	●	0.9	1	1.1	V
I^2C Timing (Note 4)							
f_{SCL}	SCL Clock Frequency					100	kHz
t_{SUSTA}	Start Condition Setup Time			4.7			µs
t_{BUF}	Bus Free Time Between Stop and Start			4.7			µs
t_{HDSTA}	Start Condition Hold Time			4			µs

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SUSTP}	Stop Condition Setup Time			4			µs
t_{HDDAT}	Data Hold Time			300			ns
t_{SUDAT}	Data Setup Time			250			ns
t_{LOW}	Clock Low Period			4.7			µs
t_{HIGH}	Clock High Period			4.0			µs
t_f	Clock/Data Fall Time					300	ns
t_r	Clock/Data Rise Time					1000	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

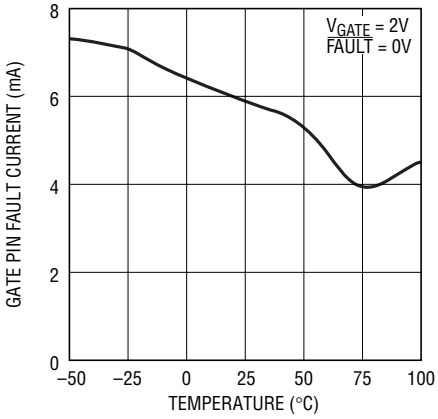
Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 3: OFF/$\overline{ON}$ pin pulled up to 5V by 1.2k resistor.

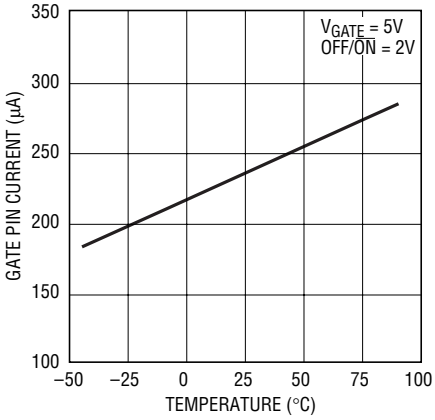
Note 4: Parameters guaranteed by design and not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

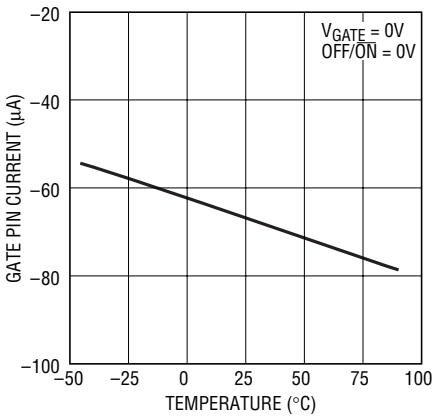
Gate Pin Fault Current vs Temperature



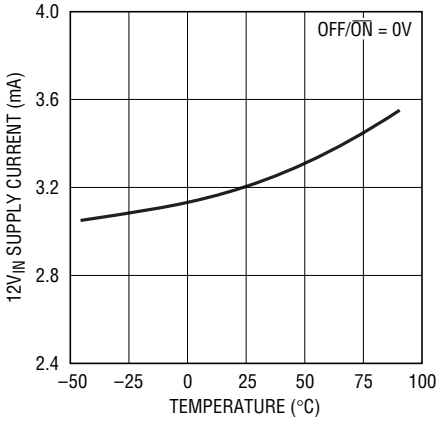
Gate Pin Turn-Off Current vs Temperature



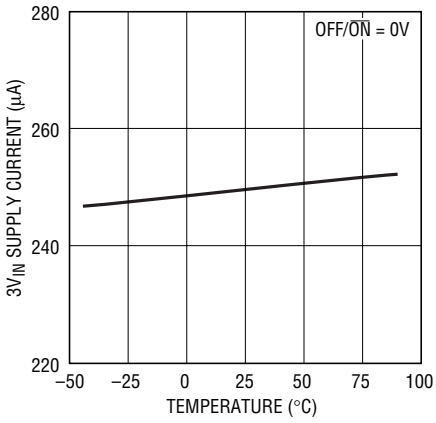
Gate Pin Turn-On Current vs Temperature



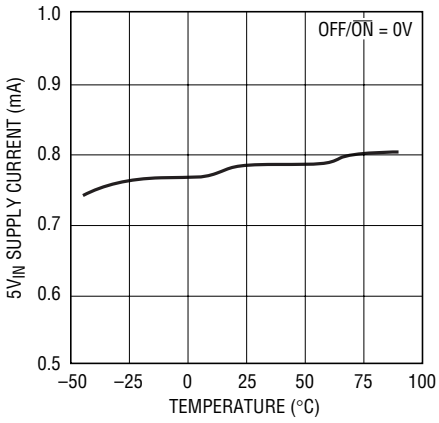
$12V_{IN}$ Supply Current vs Temperature



$3V_{IN}$ Supply Current vs Temperature

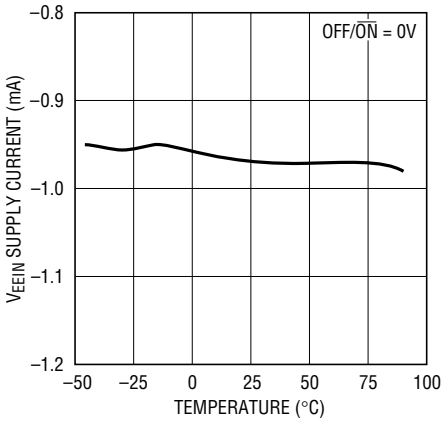


$5V_{IN}$ Supply Current vs Temperature

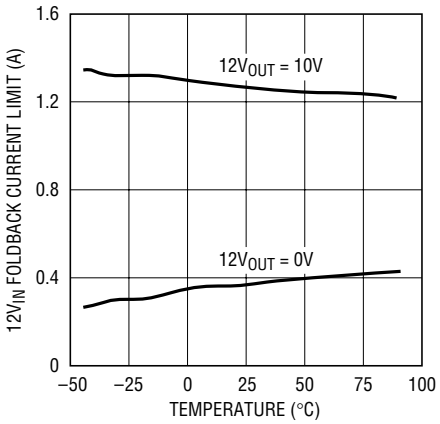


TYPICAL PERFORMANCE CHARACTERISTICS

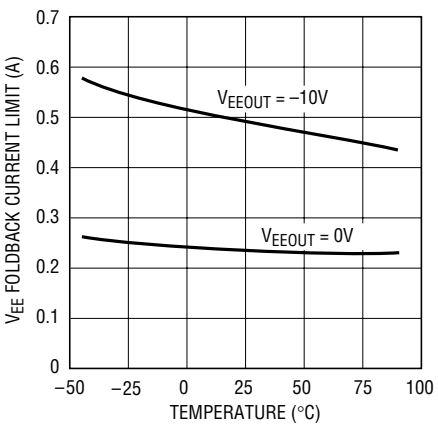
V_{EEIN} Supply Current vs Temperature



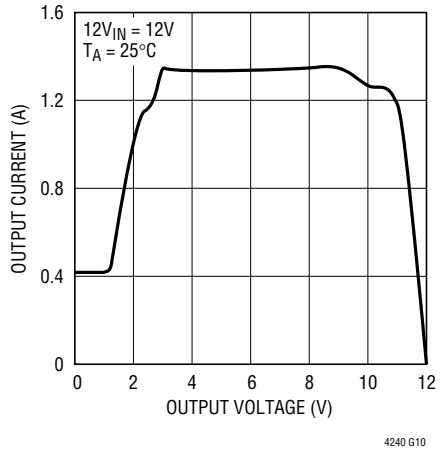
$12V_{IN}$ Foldback Current Limit vs Temperature



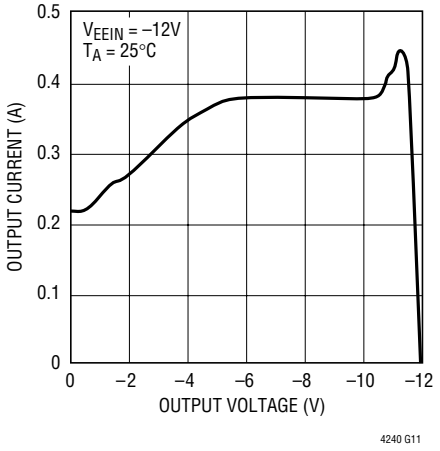
V_{EEIN} Foldback Current Limit vs Temperature



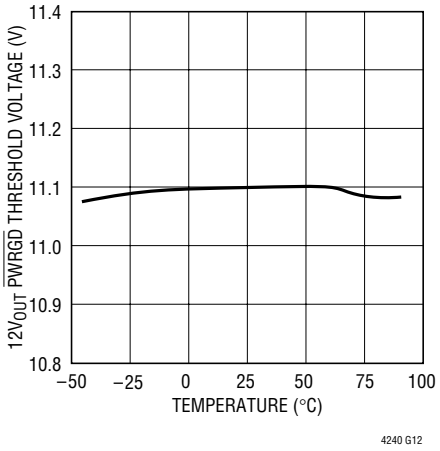
12V Output Current



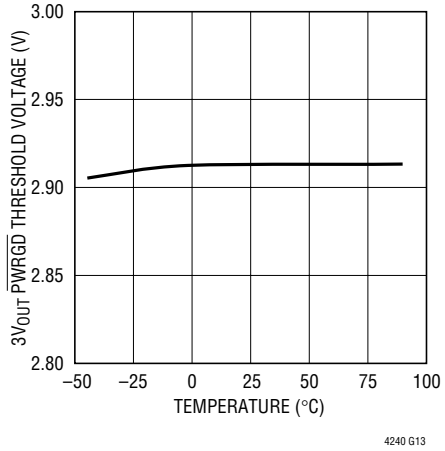
–12V Output Current



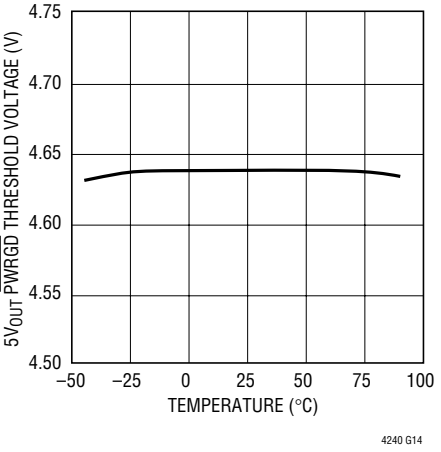
$12V_{OUT}$ $\overline{PWRGD}$ Threshold Voltage vs Temperature



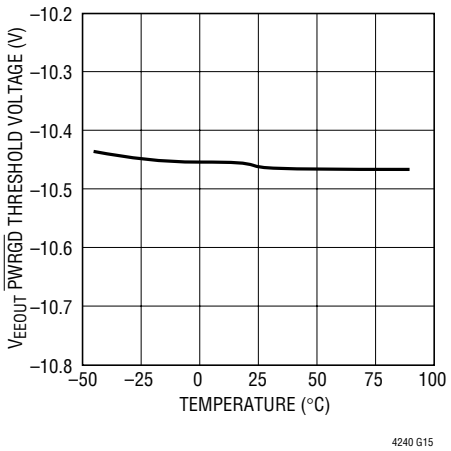
$3V_{OUT}$ $\overline{PWRGD}$ Threshold Voltage vs Temperature



$5V_{OUT}$ $\overline{PWRGD}$ Threshold Voltage vs Temperature

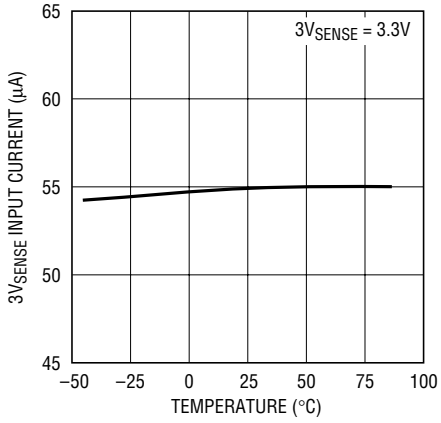


V_{EEOUT} $\overline{PWRGD}$ Threshold Voltage vs Temperature



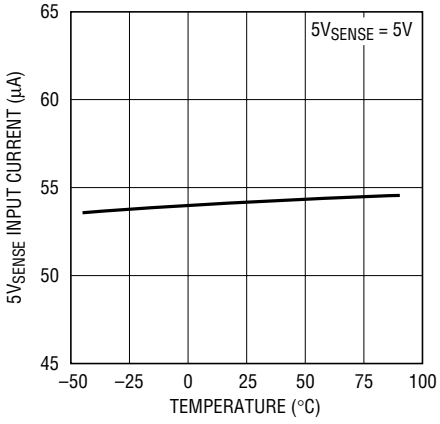
TYPICAL PERFORMANCE CHARACTERISTICS

$3V_{SENSE}$ Input Current vs Temperature



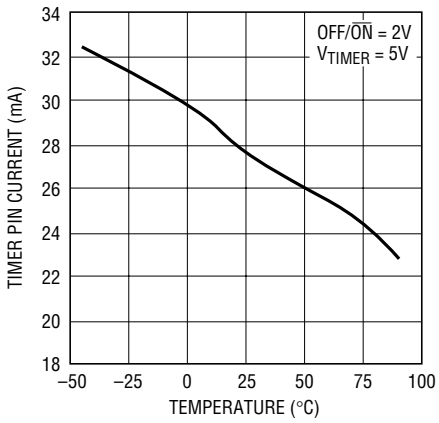
4240 G16

$5V_{SENSE}$ Input Current vs Temperature



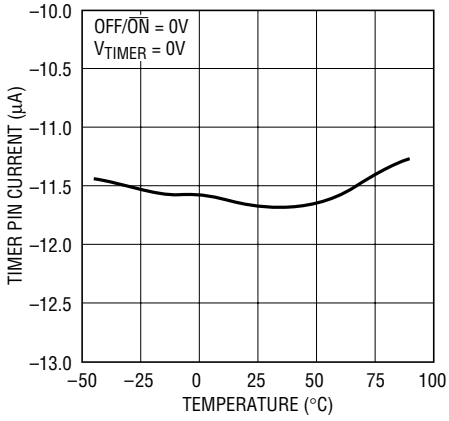
4240 G17

Timer Pin Turn-Off Current vs Temperature



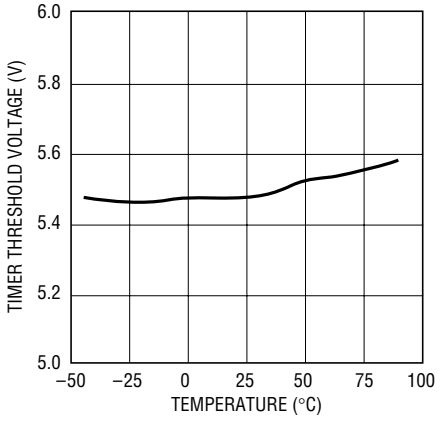
4240 G18

Timer Pin Turn-On Current vs Temperature



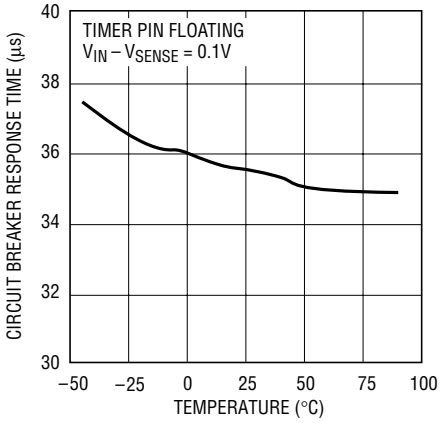
4240 G19

Timer Threshold Voltage vs Temperature



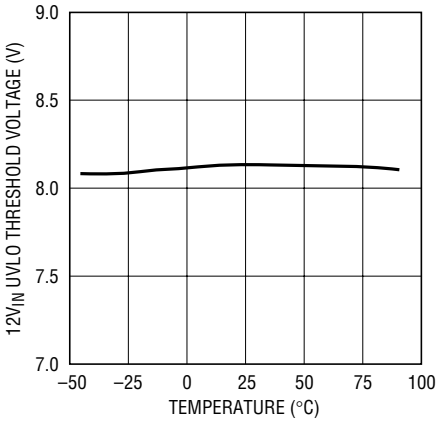
4240 G20

5V/3.3V Circuit Breaker Overcurrent Fault Response Time vs Temperature



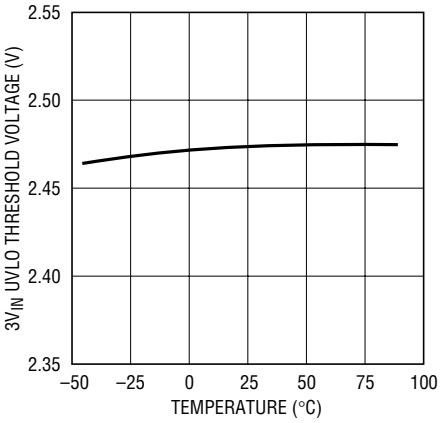
4240 G21

$12V_{IN}$ UVLO Threshold Voltage vs Temperature



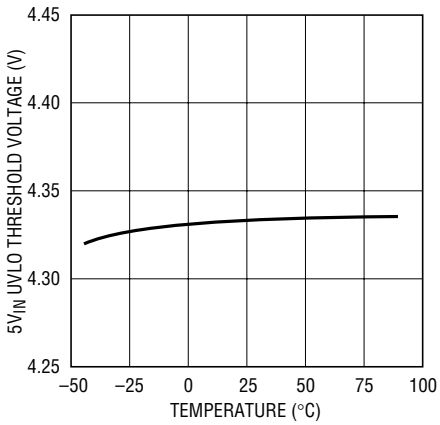
4240 G22

$3V_{IN}$ UVLO Threshold Voltage vs Temperature



4240 G23

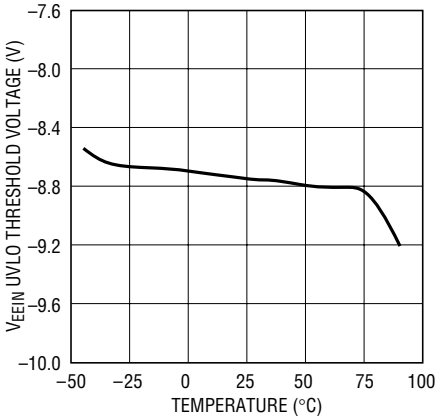
$5V_{IN}$ UVLO Threshold Voltage vs Temperature



4240 G24

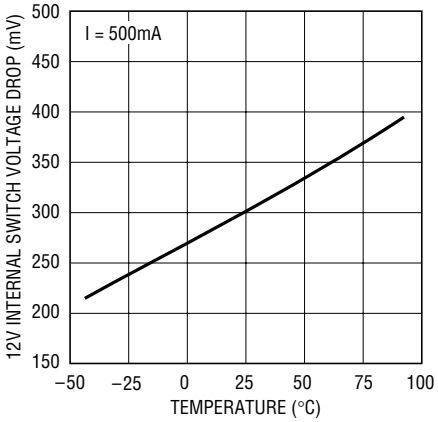
TYPICAL PERFORMANCE CHARACTERISTICS

V_{EEIN} UVLO Threshold Voltage vs Temperature



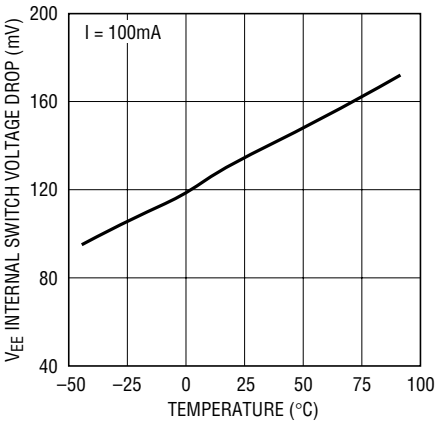
4240 G25

$12V_{IN}$ Internal Switch Voltage Drop vs Temperature



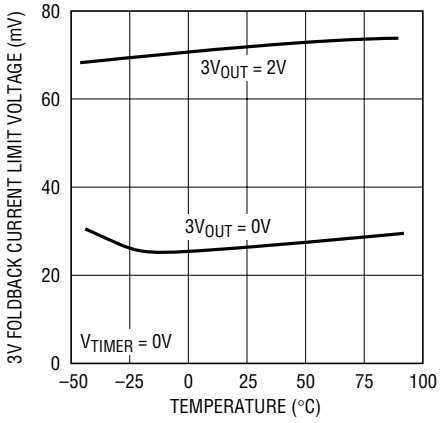
4240 G26

V_{EEIN} Internal Switch Voltage Drop vs Temperature



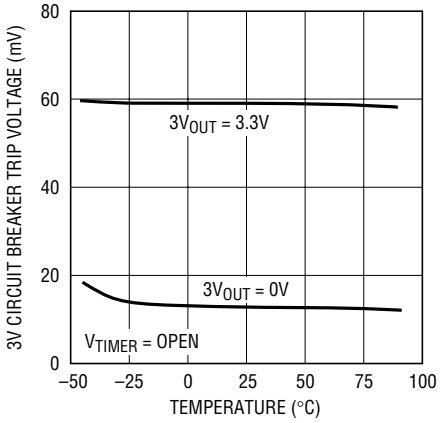
4240 G27

3V Foldback Current Limit Voltage vs Temperature



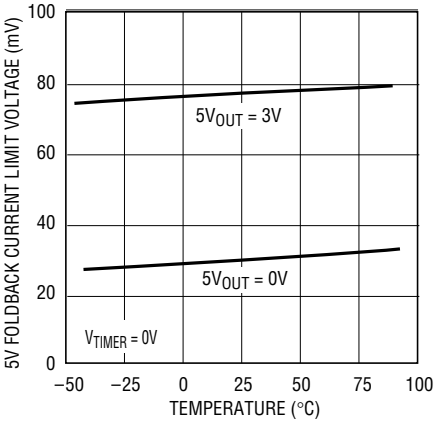
4240 G28

3V Circuit Breaker Trip Voltage vs Temperature



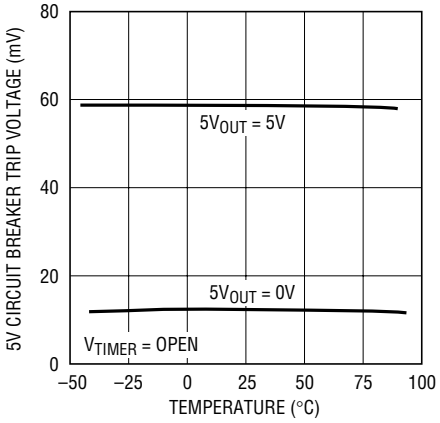
4240 G29

5V Foldback Current Limit Voltage vs Temperature



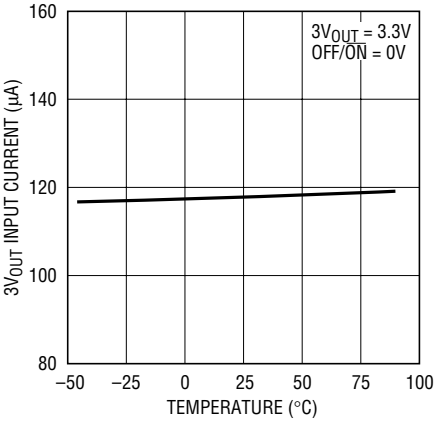
4240 G31

5V Circuit Breaker Trip Voltage vs Temperature



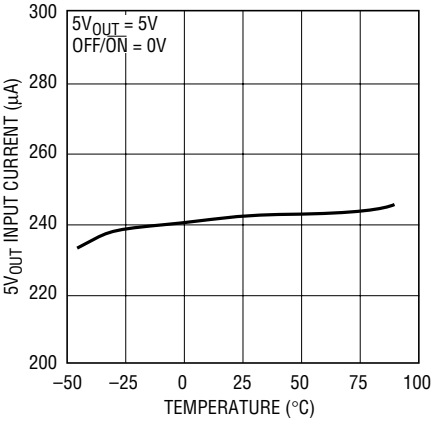
4240 G32

$3V_{OUT}$ Input Current vs Temperature



4240 G33

$5V_{OUT}$ Input Current vs Temperature



4240 G34

PIN FUNCTIONS

PRSNT1# (Pin 1): PCI Present Detect Input 1. PRSNT1# and PRSNT2# are readable over the I²C Bus. PRSNT1# and PRSNT2# indicate the maximum power used by the card. Do not float.

PRSNT2# (Pin 2): PCI Present Detect Input 2. Do not float.

$12V_{IN}$ (Pin 3): 12V Supply Input. A 0.5Ω switch is internally connected between $12V_{IN}$ and $12V_{OUT}$ with foldback current limit. An undervoltage lockout circuit prevents the switches from turning on while the $12V_{IN}$ pin is below 8V. $12V_{IN}$ provides power to some of the LTC4240's internal circuitry. See Input Transient Protection section on how to protect $12V_{IN}$ from large voltage transients.

V_{EEIN} (Pin 4): –12V Supply Input. A 1Ω internal switch is connected between V_{EEIN} and V_{EEOUT} with foldback current limit. An undervoltage lockout circuit prevents the switches from turning on while V_{EEIN} is above –9V. See Connecting V_{EEIN} section for more notes on V_{EEIN} and V_{EEOUT}. Also refer to Input Transient Protection section.

TIMER/AUX $12V_{IN}$ (Pin 5): Current Fault Inhibit Timing Input. Connect a capacitor from TIMER to GND. With the LTC4240 turned off (OFF/$\overline{ON}$ = HIGH), the TIMER pin is internally held at GND. When the device is turned on, an 11.5µA pull-up current source is connected to TIMER. Current limit faults will be ignored until the voltage at the TIMER pin rises above 5.5V. The Timer capacitor also serves as an auxiliary charge reservoir for internal V_{CC} in the event the $12V_{IN}$ pin voltage glitches below the LTC4240 UVL threshold voltage.

$5V_{OUT}$ (Pin 6): 5V Output Sense. The $\overline{PWRGD}$ pin will not pull low until the $5V_{OUT}$ pin voltage exceeds 4.65V. When the power switches are turned off, a 50Ω resistor pulls $5V_{OUT}$ to ground.

$\overline{FAULT}$ (Pin 7): Open-Drain Fault Output . $\overline{FAULT}$ is pulled low when a current limit fault is detected. Current limit faults are ignored until the voltage at the TIMER pin is above 5.5V. Once the TIMER cycle is complete, $\overline{FAULT}$ pulls low and the LTC4240 turns off (in the event of an overcurrent fault lasting longer than 35µs). The LTC4240 will remain in the off state until the OFF/$\overline{ON}$ pin is cycled high then low or power is cycled. Note that the OFF/$\overline{ON}$ cycling can also be performed using I²C bus.

$\overline{PWRGD}$ (Pin 8): Open-Drain Power Good Output. Connect the CPCI HEALTHY# signal to the $\overline{PWRGD}$ pin. $\overline{PWRGD}$ remains low while $V_{12VOUT} \geq 11.1V$, $V_{3VOUT} \geq 2.9V$, $V_{5VOUT} \geq 4.65V$ and $V_{EEOUT} \leq -10.5V$. When any of the supplies drops below its power good threshold voltage, $\overline{PWRGD}$ will go high after a 10µs deglitching time. The switches will not be turned off when $\overline{PWRGD}$ goes high, unless a fault has occurred. The CPCI specification calls for a 0.01µF bypass capacitor on the backplane for HEALTHY#.

$\overline{BE}$ (Pin 9): QuickSwitch Bus Enable Output. The $\overline{BE}$ output remains high until power is good on all supplies. This serves to isolate the I/O data lines during live insertion. This is a CMOS output powered by $5V_{IN}$.

GND (Pin 10): Analog Ground. Connect to analog ground plane.

ADDRIN (Pin 11): I²C Address Programming Input. The I²C address is programmed by connecting the ADDRIN pin to a resistor divider between the $5V_{IN}$ pin and GND. See Table 1 for 1% resistor values and corresponding addresses. Resistors must be placed close to the ADDRIN pin to minimize errors due to stray capacitance and resistance on the board trace. Connect this pin to ground if I²C is not used.

SDA (Pin 12): I²C Data Input and Output. Note that TTL levels are used. Connect this pin to ground if I²C is not used.

SCL (Pin 13): I²C Clock Input, 100kHz Maximum. Note that TTL levels are used. Do not float. Connect this pin to ground if I²C is not used.

$\overline{RESETOUT}$ (Pin 14): Open-Drain Reset Output. Connect the CPCI LOCAL_PCI_RST# signal to the $\overline{RESETOUT}$ pin. $\overline{RESETOUT}$ is the logical combination of $\overline{RESETIN}$, $\overline{PWRGD}$, and I²C $\overline{RESETOUT}$ latch output.

LED (Pin 15): CPCI Status LED. Pulls low to light LED when $\overline{RESETOUT}$ is low or when the I²C LED latch is set.

DGND (Pin 16): Digital Ground. Connect to ground plane.

DRIVE (Pin 17): External transistor's base drive output for bus precharge. Connects to the base of an external NPN emitter-follower which in turn biases the PRECHARGE

PIN FUNCTIONS

node. An external 1k resistor between the transistor's base and $3V_{IN}$ is needed.

PRECHARGE (Pin 18): Precharge Monitor Input. An internal error amplifier servos the DRIVE pin voltage to keep the precharge node at 1V. Becomes valid when long 5V and 3.3V power pins make contact .Tie pins 17 and 18 together if precharge function is unused.

GATE (Pin 19): High Side Gate Drive for the External 3.3V and 5V N-Channel Power Transistors. An external series RC network is required for the current limit loop compensation and to set the maximum ramp-up rate. During power-up, the slope of the voltage rise at the GATE pin is set by the 65µA current source charging the external GATE capacitor or by the 3.3V or 5V current limit and the associated output capacitor. During power-down, a 200µA current source pulls the GATE pin to GND.

The voltage at the GATE pin will be modulated to maintain a constant current when either the 3.3V or 5V supply goes into current limit and the TIMER pin is less than 5.5V. Once the TIMER pin is above 5.5V, and in the event of a current fault condition lasting for longer than 35µs, the GATE pin is immediately pulled to GND.

$5V_{SENSE}$ (Pin 20): 5V Current Limit Sense. A sense resistor placed between $5V_{IN}$ and $5V_{SENSE}$ determines the current limit for this supply. A foldback current feature makes the current limit decrease as the voltage at the $5V_{OUT}$ pin approaches 0V. To disable the current limit, $5V_{SENSE}$ and $5V_{IN}$ must be tied together.

$5V_{IN}$ (Pin 21): 5V Supply Sense Input. An undervoltage lockout circuit prevents the switches from turning on when the voltage at the $5V_{IN}$ pin is less than 4.3V. At least one long pin must be connected to $5V_{IN}$ to ensure precharge output. See Input Transient Protection section.

$3V_{IN}$ (Pin 22): 3.3V Supply Sense Input. An undervoltage lockout circuit prevents the switches from turning on when the voltage at the $3V_{IN}$ pin is less than 2.45V. If no 3.3V input supply is available, connect two series diodes between $5V_{IN}$ and $3V_{IN}$ (tie anode of first diode to $5V_{IN}$ and cathode of second diode to $3V_{IN}$, Figure 15). At least one long pin must be connected to $3V_{IN}$ to ensure precharge output. See Input Transient Protection section.

$3V_{SENSE}$ (Pin 23): 3.3V Current Limit Sense. A sense resistor placed between $3V_{IN}$ and $3V_{SENSE}$ determines the current limit for this supply. A foldback feature makes the current limit decrease as the voltage at the $3V_{OUT}$ pin approaches 0V. To disable current limit, $3V_{SENSE}$ and $3V_{IN}$ must be tied together.

$3V_{OUT}$ (Pin 24): 3.3V Output Sense. The $\overline{PWRGD}$ pin cannot pull low until the $3V_{OUT}$ pin voltage exceeds 2.9V. If no 3.3V input supply is available, tie the $3V_{OUT}$ pin to the $5V_{OUT}$ pin. When the power switches are turned off, a 150Ω resistor pulls $3V_{OUT}$ to ground.

V_{EEOUT} (Pin 25): –12V Supply Output. An internal 1Ω switch is connected between V_{EEIN} and V_{EEOUT}. V_{EEOUT} must exceed –10.5V before the $\overline{PWRGD}$ pin pulls low. When the power switches are turned off, a 650Ω resistor pulls V_{EEOUT} to ground.

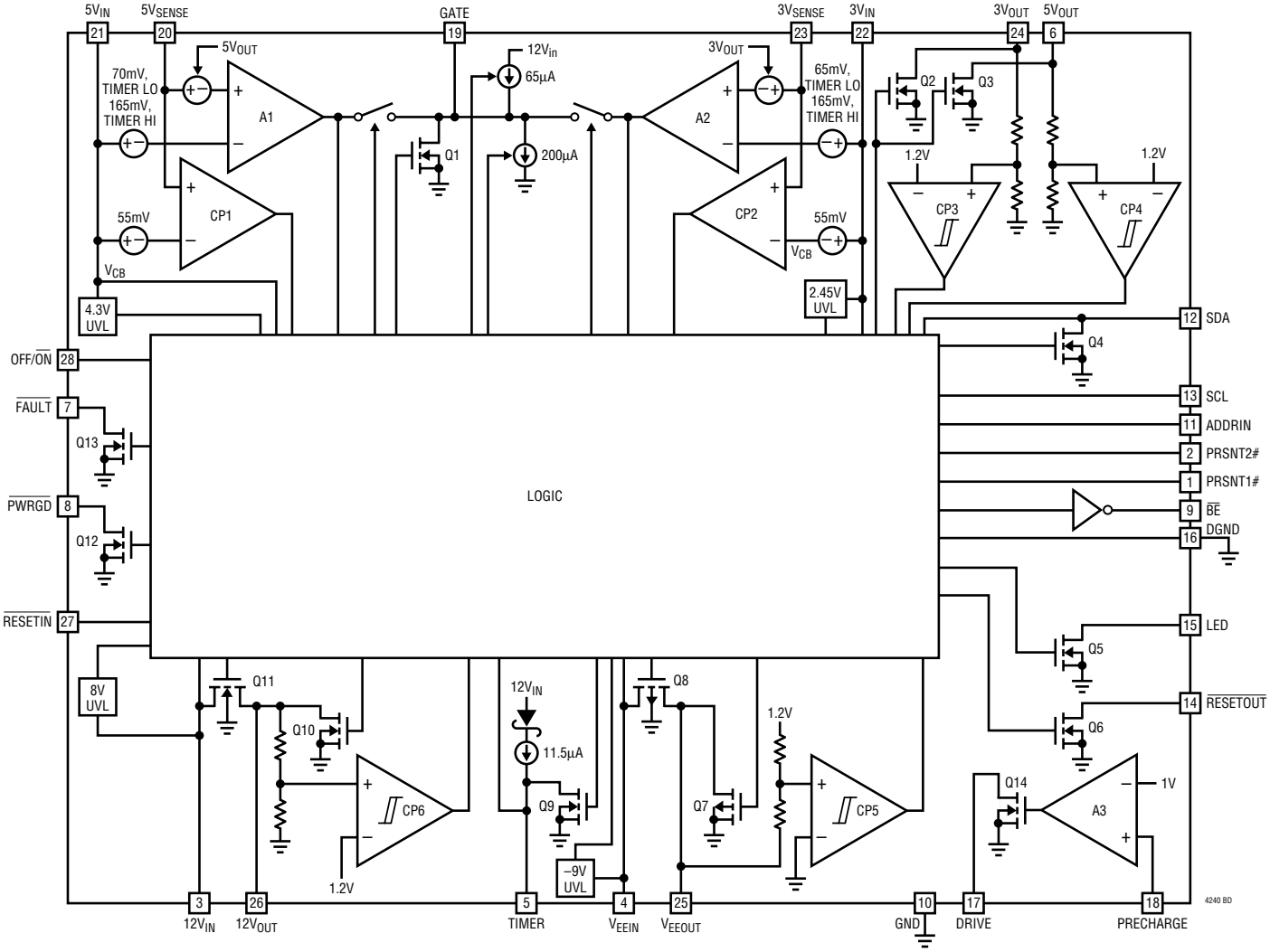
$12V_{OUT}$ (Pin 26): 12V Supply Output. A 0.5Ω switch is connected between $12V_{IN}$ and $12V_{OUT}$. $12V_{OUT}$ must exceed 11.1V before the $\overline{PWRGD}$ pin can pull low. When the power switches are turned off, a 430Ω resistor pulls $12V_{OUT}$ to ground.

$\overline{RESETIN}$ (Pin 27): PCI Reset Input. Connect the CPCI PCI_RST# signal to the $\overline{RESETIN}$ pin. Pulling $\overline{RESETIN}$ low will cause $\overline{RESETOUT}$ to pull low. Note that the I^2C $\overline{RESETIN}$ latch output can also set $\overline{RESETOUT}$. Do not float.

OFF/$\overline{ON}$ (Pin 28): OFF/$\overline{ON}$ Input. Connect the CPCI BD_SEL# signal to the OFF/$\overline{ON}$ pin. When the OFF/$\overline{ON}$ pin is pulled low, the GATE pin is pulled high by a 65µA current source and the internal 12V and –12V switches are turned on. When the OFF/$\overline{ON}$ pin is pulled high, the GATE pin will be pulled to ground by a 200µA current source and the 12V and –12V switches turn off.

Cycling the OFF/$\overline{ON}$ pin high and low will reset a tripped circuit breaker and start a new power-up sequence. The I^2C OFF/$\overline{ON}$ latch output can also be used to reset the electronic circuit breaker. Do not float.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LTC4240 is a Hot Swap controller that allows a board to be safely inserted and removed from a CompactPCI bus slot. The LTC4240 has built-in 2-wire I^2C compatible interface hardware to allow software control and monitoring of device function and power supply status.

Hot Circuit Insertion

When a circuit board is inserted into a live CompactPCI (CPCI) backplane slot, supply bypass capacitors on the board can draw huge supply transient currents from the CPCI backplane power bus. The transient currents can cause glitches on the power bus, thus causing other boards in the system to reset.

The LTC4240 is designed to turn a board's supply voltages on and off in a controlled manner, allowing the board to be safely inserted or removed from a live CPCI slot without disturbing the system power supplies. The device also protects the supplies from shorts, precharges the bus I/O pins during insertion and extraction and monitors the supply voltages. The LTC4240 includes an I^2C compatible interface, which allows software control of device functions.

The LTC4240 is specifically designed for CPCI applications where it resides on the plug-in board. For best results, a well bypassed backplane is recommended.

LTC4240 Feature Summary

- Allows safe board insertion and removal from a CPCI backplane. Status LED visually identifies when a board is ready for removal.
- Controls all four CPCI supplies: –12V, 12V, 3.3V and 5V.
- Foldback current limit: An analog current limit with a value that depends on the output voltage. If the output is shorted to ground, the current limit drops to keep power dissipation and supply glitches to a minimum.
- 12V and –12V circuit breakers: if either supply remains in current limit for more than 35µs, the circuit breaker will trip, the supplies will turn off and the $\overline{FAULT}$ pin pulls low.
- Adjustable 5V and 3.3V circuit breakers: if either supply exceeds current limit for more than 35µs, the circuit breaker will trip, the supplies will be turned off and the $\overline{FAULT}$ pin will be pulled low. In addition, an analog loop will servo the GATE pin to limit the current to three times circuit breaker limit during transient conditions.
- I^2C interface: software control allows user to both write to and read from the device. The user can turn the device off and on, set the status LED, set $\overline{RESETOUT}$ and disable faults on $12V_{IN}$ and V_{EEIN}. The user can also read the device status: $\overline{FAULT}$, $\overline{RESETIN}$, $\overline{RESETOUT}$ $\overline{PWRGD}$, PRSNT1#, PRSNT2#, FAULTCODE0 and FAULTCODE1. If a fault occurs, the FAULTCODE bits identify which supply generated the fault.
- Current limit during power-up: the supplies are allowed to power-up in current limit. This allows the LTC4240 to power-up boards with widely varying capacitive loads without tripping the circuit breaker. The maximum allowable power-up time is programmable using an external capacitor connected to the TIMER pin. See TIMER section
- Internal 12V and –12V power switches.
- $\overline{PWRGD}$ output: indicates the voltage status of the four supply voltages.
- PCI_RST# is combined with HEALTHY# and with the I^2C $\overline{RESETIN}$ latch output to create LOCAL_PCI_RST# output. If HEALTHY# asserts, LOCAL_PCI_RST# is asserted independent of the other two inputs.
- Precharge output: an internal reference and amplifier provide 1V for biasing bus I/O connector pins during CPCI card insertion and extraction.
- Space saving 28-pin SSOP package.

I^2C Interface

The LTC4240 incorporates an I^2C compatible 2-wire (clock and data) interface that allows the user to easily query and control the status of the LTC4240. A single analog input pin selects 1 of 32 allowed addresses. The I^2C bus can be

APPLICATIONS INFORMATION

used to turn off/on the power switches, turn on the status LED (alerting the user that its safe to remove the plug-in board), and assert the LOCAL_PCI_RST# signal. The I²C bus is also used to read the logic signals of several device pins: $\overline{\text{FAULT}}$, $\overline{\text{PWRGD}}$, $\overline{\text{RESETIN}}$, and $\overline{\text{RESETOUT}}$. Additionally, when a supply generates a current fault, the I²C bus can be used to determine which supply generated the fault. See Send Byte and Receive Byte sections for a full description of all I²C features.

The LTC4240 supports Send Byte and Receive Byte protocols. Communication is achieved using the SCL and SDA pins (TTL compatible input thresholds). The SCL pin is the clock input from the I²C bus (host) to the LTC4240 (slave). The maximum SCL frequency is 100kHz. SDA is the bidirectional data transfer line between the I²C bus and the LTC4240. Send Byte and Receive Byte protocols are both comprised of 2 bytes. The first byte for both is the address byte. All communication begins with a START command.

Programming the I²C Address

The voltage on the ADDRIN pin determines the I²C address. The ADDRIN voltage is set externally with a resistor divider from $5V_{IN}$ to ground (resistor placement must be close to the pin, do not place a bypass capacitor on ADDRIN). This voltage is fed to a 5-bit A/D and compared against the address byte clocked in by the I²C bus. The 5-bit A/D allows 32 unique LTC4240 devices to be connected on the same I²C bus. 1% resistors should be used to place the voltage at ADDRIN approximately 0.5 LSB away from each code transition. Table 1 shows recommended resistor values for each of the address code segments. The resistor ratio for each code segment has been optimized for best performance over the specified temperature range. The parallel resistance for the address setting resistors should be kept under 10k.

Table 1. Suggested ADDRIN 1% Resistor Values

ADDR CODE	RECOMMENDED ADDRIN VOLTAGE	ALLOWED ADDRIN VOLTAGE RANGE	$R_{19(TOP)}$ RESISTOR	$R_{20(BOT)}$ RESISTOR
00	0.108125	0.080 to 0.136	8660	191
01	0.264375	0.236 to 0.293	2550	140
02	0.420625	0.393 to 0.449	2550	237
03	0.576875	0.549 to 0.605	2550	332
04	0.733125	0.705 to 0.761	2550	442
05	0.889375	0.861 to 0.918	2550	549
06	1.045625	1.018 to 1.074	3830	1020
07	1.201875	1.174 to 1.230	2550	806
08	1.358125	1.330 to 1.386	2550	953
09	1.514375	1.486 to 1.543	1150	499
10	1.670625	1.643 to 1.699	1020	511
11	1.826875	1.799 to 1.860	8660	4990
12	1.983125	1.955 to 2.021	2550	1690
13	2.139375	2.111 to 2.175	2550	1910
14	2.295625	2.268 to 2.330	1130	1130
15	2.451875	2.424 to 2.488	1370	1330
16	2.608125	2.580 to 2.644	2550	2800
17	2.764375	2.736 to 2.800	2550	3160
18	2.920625	2.888 to 2.950	2550	3570
19	3.076875	3.044 to 3.110	715	1150
20	3.233125	3.200 to 3.262	1150	2100
21	3.389375	3.356 to 3.421	1150	2430
22	3.545625	3.513 to 3.574	1150	2800
23	3.701875	3.669 to 3.731	357	1020
24	3.858125	3.825 to 3.886	2550	8660
25	4.014375	3.981 to 4.041	249	1020
26	4.170625	4.138 to 4.190	1070	5360
27	4.326875	4.294 to 4.349	178	1150
28	4.483125	4.450 to 4.499	133	1150
29	4.639375	4.606 to 4.651	102	1300
30	4.795625	4.763 to 4.805	105	2430
31	4.951875	4.919 to 4.962	100	10000

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START and STOP Commands

The START command is defined as a high to low transition of the SDA line while the SCL line is high. It is an asynchronous event issued by the host, waking up all slave devices and alerting them that a slave address is being written onto the bus. Only the slave device that matches the address will communicate with the host. The STOP command is defined as a low to high transition on the SDA line while SCL is high. It is also an asynchronous event issued by the host to signal the termination of the data transfer. Other than START and STOP commands, the SDA line is allowed to change states only when SCL is low.

Address Byte

Once the LTC4240 has detected a START command, it clocks in the SDA line on the succeeding 9 SCL rising edges. The first 7 bits clocked in contain the address of the slave device targeted by the host. The first (MSB) address bit must be set to low and the second bit must be set to high. The next 5 bits are fed into a digital comparator and compared against the output of an internal 5-bit A/D. If the comparison is true, then there is an address match and the LTC4240 continues to communicate with the host device. The LTC4240 proceeds to acknowledge the address match by pulling the SDA line low while SCL is low, just before the 9th SCL rising edge. Figures 1 and 3 show a timing diagram of the START condition and address byte for both the Send Byte and Receive Byte protocols. Note that the SDA bit clocked in with the 8th SCL edge determines whether the host is sending or receiving information to/from the LTC4240.

Send Byte Protocol

The Send Byte protocol allows a host to write information into the LTC4240 and command the LTC4240 to perform certain predetermined functions. The host initiates communication with a START bit followed by 7 address bits. The address bits are followed by the R/$\overline{W}$ bit, which is low for Send Byte. The 9th bit is asserted low by the LTC4240 to acknowledge when there has been an address match. The only time the LTC4240 writes data onto the SDA bus during a send byte is to acknowledge the address and command bytes. The first 8 bits are referred to collectively as the address byte.

The command byte follows the address byte. The command byte contains the information sent from the host to the LTC4240. After the LTC4240 acknowledges the address byte, each of the next 8 SCL rising edges shifts SDA from the host into a shift register inside the LTC4240. The first 2 bits clocked into the shift register (2 MSBs of the command latch) are not used by the LTC4240. Only the 6 LSBs are stored in the command latch on the falling edge of the 8th clock during the command byte. The output of the command latch remains fixed until the next Send Byte command overwrites it. Note that if power is turned off ($5V_{IN} < 2V$), the command and data latches will be cleared. Figure 1 shows the timing diagram of the entire send byte protocol. Transmission ends when the host issues a STOP command. Table 2 defines the functions of the 6 command bits. Note that some of these functions can override, or can be overridden by, other circuitry and pins of the LTC4240. Figure 2 shows the relationship between bits C1 to C3 and other LTC4240 signals.

Receive Byte Protocol

The Receive Byte protocol is used by the host to read data from the LTC4240 data latch. This protocol begins with a START command, issued by the host, followed by 7 address bits. The address bits are followed by the R/$\overline{W}$ bit, which is high for Receive Byte. The 9th bit is used by the LTC4240 to acknowledge when there is an address match.

The data byte then follows the address byte. This byte contains LTC4240 status information. After the LTC4240 acknowledges the address byte, it shifts 8 bits of data onto the SDA line. Figure 3 shows the entire Receive Byte timing diagram. Note that neither the host or the slave acknowledges the data byte (SDA line stays high during 9th clock edge of the data byte).

APPLICATIONS INFORMATION

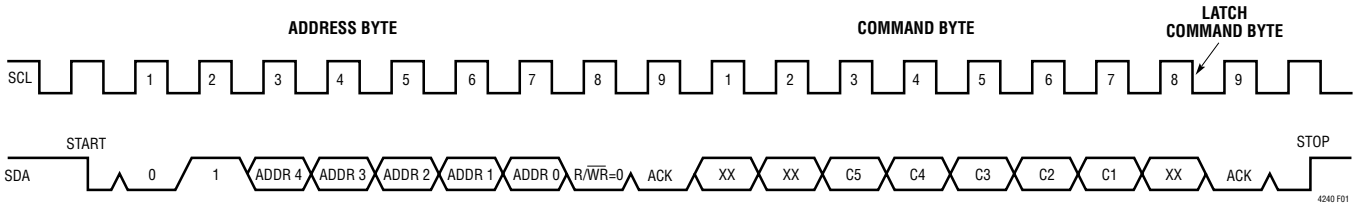

Figure 1. Send Byte Protocol

Table 2. Command Byte Definitions

	HIGH	LOW	POWER-UP STATE
C7	Don't care	Don't care	N/A
C6	Don't care	Don't care	N/A
C5	Ignore V_{EEOUT} faults	Don't ignore V_{EEOUT} faults	LOW
C4	Ignore $12V_{OUT}$ faults	Don't ignore $12V_{OUT}$ faults	LOW
C3	Sets $\overline{RESETOUT}$	Does not set $\overline{RESETOUT}$ low	LOW
C2	Turns OFF/$\overline{ON}$ to OFF Overrides OFF/$\overline{ON}$ pin	Does not set OFF/$\overline{ON}$ Does not override OFF/$\overline{ON}$ pin	LOW
C1	Turns on LED open drain	Does not turn on LED open drain	LOW
C0	Don't care	Don't care	N/A

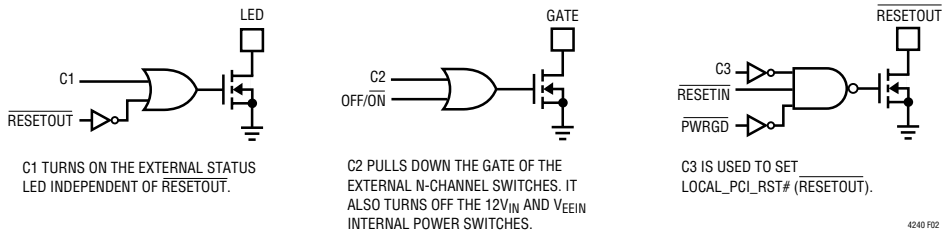

Figure 2. Send Byte Command Latch and Logic

APPLICATIONS INFORMATION

Table 3 shows the definition for each data bit. $\overline{PWRGD}$, $\overline{FAULT}$, $\overline{RESETIN}$, and $\overline{RESETOUT}$ external pins can be monitored. PRSNT1# and PRSNT2# are PCI signals that provide information on the power requirements of the board. Refer to PCI local bus specifications for a detailed description. FAULTCODE1 and FAULTCODE0 are two internal binary encoded signals that, along with $\overline{FAULT}$, indicate which of the four supplies generated a fault. Note that the FAULTCODE signals are valid only when $\overline{FAULT}$ has been asserted low. See Table 4 for description.

Status LED

The main function of the LED is to alert the user when it is permissible to physically extract the board. The LED output of the LTC4240 is an open drain N-channel device capable of sinking 10mA from an externally connected LED. This LED lights up when $\overline{RESETOUT}$ (LOCAL_PCI_RST#) is asserted. Upon application of Early Power, the long 5V pins will power up the LTC4240 and light up the Status LED. It will remain on until $\overline{PWRGD}$ (HEALTHY#) is asserted and $\overline{RESETIN}$ (PCI_RST#) is deasserted, and the board enters normal operation. Note that this LED can also be turned on via the I^2C 2-wire interface.

CPCI Connection Pin Sequence

The staggered length of the CPCI male connector pins ensures that all power supplies are physically connected to the LTC4240 before back-end power is allowed to ramp (BD_SEL# asserted low). The long pins, which include 5V, 3.3V, V(I/O) and GND mate first. The short pins, which includes BD_SEL# (OFF/$\overline{ON}$), mate last. At least one long 5V power pin must be connected to the LTC4240 in order for the PRECHARGE voltage to be available during Early Power. The external components connected to the precharge pin require long 3.3V.

The following is a typical hot plug sequence:

1. ESD clips make contact.
2. Long power and ground pins make contact and Early Power is established (see Early Power section). The 1V PRECHARGE voltage becomes valid at this stage. Power is applied to the pull-up resistors connected to $\overline{FAULT}$, $\overline{PWRGD}$ and OFF/$\overline{ON}$ pins. The status LED is lit, indicating that the plug-in board is in the process of being connected (LOCAL_PCI_RST# is asserted). All power switches are off.
3. Medium length pins make contact. There are six 5V and eight 3.3V medium length power pins, bringing the 5V total to 8 pins and the 3.3V total to 10 pins. The maximum DC current for the 3.3V and 5V supplies is 10A and 8A, respectively. The I^2C command latch is initialized to allow seamless CPCI Hot Swap operation. The LTC4240 can be used as a Hot Swap controller without ever establishing I^2C communication. Both $\overline{FAULT}$ and $\overline{PWRGD}$ continue to be pulled up high at this

Table 3. STATUS Byte Definitions

S7	Logic state of the PRSNT2# pin
S6	Logic state of the PRSNT1# pin
S5	Logic state of the $\overline{PWRGD}$ pin
S4	Logic state of the $\overline{RESETOUT}$ pin
S3	Logic state of the $\overline{RESETIN}$ pin
S2	FAULTCODE1 (see Table 4)
S1	FAULTCODE0 (see Table 4)
S0	Logic state of the $\overline{FAULT}$ pin

Table 4. FAULTCODE Encoding Description for Receive Byte

FAULTCODE0	FAULTCODE1	$\overline{FAULT}$	Supply Causing Fault
LO	LO	LO	$3V_{IN}$
LO	HI	LO	$5V_{IN}$
HI	LO	LO	$12V_{IN}$
HI	HI	LO	V_{EEIN}
X	X	HI	None

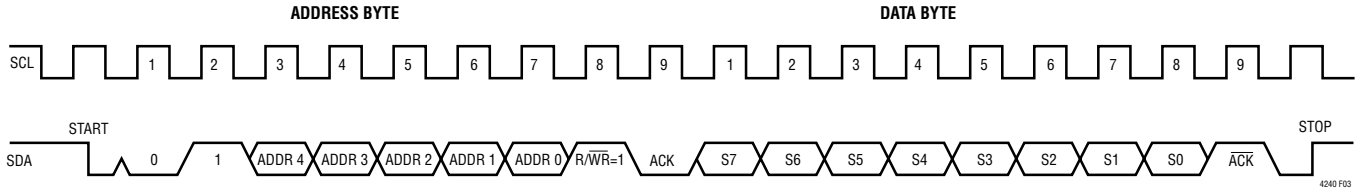

Figure 3. Receive Byte Protocol

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stage in the hot plug sequence, indicating that the LTC4240 is in reset mode with all power switches off (BD_SEL# is still pulled high to long 5V).

The 12V and –12V supplies make contact at this stage. Zener clamps Z1 and Z2 plus shunt RC snubbers R13-C4 and R14-C5 help protect the $12V_{IN}$ and V_{EEIN} pins, respectively, from large transient voltages during hot insertion and short-circuit conditions.

The signal pins also connect at this point. This includes the HEALTHY# signal connecting to the $\overline{\text{PWRGD}}$ pin and the PCI_RST# signal connecting to the $\overline{\text{RESETIN}}$ pin. The $\overline{\text{PWRGD}}$ and $\overline{\text{RESETIN}}$ signals are combined internally with Bit 3 (C3) of the I^2C command latch (see Send Byte protocol) to generate the LOCAL_PCI_RST# signal, which is available at the $\overline{\text{RESETOUT}}$ pin.

4. Short pins make contact. BD_SEL# signal connects to the OFF/$\overline{\text{ON}}$ pin. This starts the electrical part of the connection process. If the BD_SEL# signal is grounded on the backplane, then the electrical connection process starts immediately. Note that the electrical connection process can be interrupted with the Send Byte protocol of the I^2C serial interface.

   System backplanes that do not ground the BD_SEL# signal will instead have circuitry that detects when BD_SEL# has made contact with the plug-in board. The backplane logic can then control the power up process by pulling BD_SEL# low. Figure 4 illustrates the power up sequence. The mating of BD_SEL# is represented by the high to low transition of the BD_SEL# signal.

Power-Up Sequence

Two external N-channel power MOSFETs isolate the 3.3V and 5V power paths, while two internal MOS switches isolate the 12V and –12V power paths. (See front page Application Circuit). Sense resistors R1 and R2 provide current limit and fault detection for the $3V_{IN}$ and $5V_{IN}$ supplies, while R5 and C1 provide current control loop compensation. Current fault detection for the 12V and –12V supplies is done internally.

A high to low transition on BD_SEL# causes the voltages on the TIMER, GATE, $3V_{OUT}$, $5V_{OUT}$, $12V_{OUT}$ and V_{EEOUT} pins to begin ramping (see Figure 4). The TIMER pin capacitance is charged by an 11.5µA current source while the GATE capacitance is charged by a 65µA current source. Concurrently, an internal charge pump turns on the gates of the internal power switches that isolate the 12V and –12V supplies. All faults are ignored during the time that the voltage at the TIMER pin remains below 5.5V. In order to avoid faults due to the charging of the bulk output capacitors, all output voltages must settle before the TIMER pin reaches 5.5V. See TIMER section for more details.

The $5V_{OUT}$ and $3V_{OUT}$ supply outputs will ramp up according to the slowest of the following slew rates:

$$\frac{dV}{dt} = \frac{65\mu A}{C1}, \text{or} = \frac{I_{LIMIT(5V)} - I_{LOAD(5V)}}{C_{LOAD(5VOUT)}}, \quad (1a)$$

$$\text{or} = \frac{I_{LIMIT(3V)} - I_{LOAD(3V)}}{C_{LOAD(3VOUT)}} \quad (1b)$$

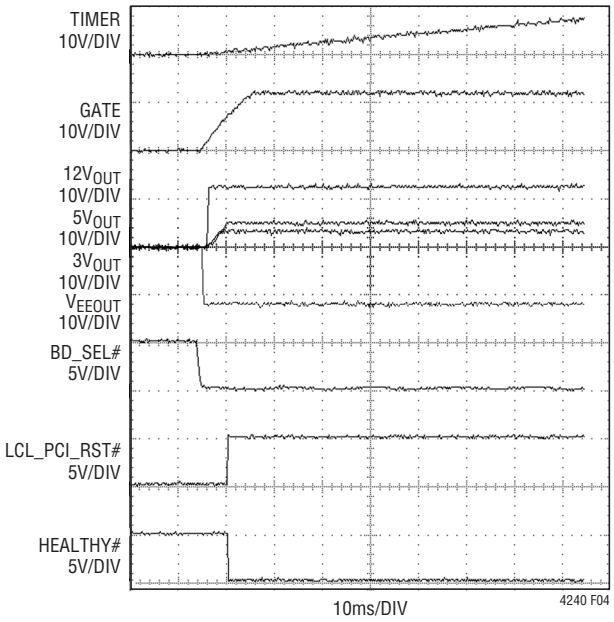

Figure 4. Normal Power-Up Sequence

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Note that capacitor C1 performs dual functions. In addition to controlling the ramp up rates of the 5V and 3.3V outputs, it also compensates the current limit loop. Current limit faults are ignored while the TIMER voltage is less than 5.5V.

Once all four supplies are within tolerance, the $\overline{\text{PWRGD}}$ pin ($\underline{\text{HEALTHY\#}}$) will be pulled low and LOCAL_PCI_RESET# ($\underline{\text{RESETOUT}}$) is free to follow PCI_RST#. Bit 3 of the I^2C command latch powers up low, thus not asserting LOCAL_PCI_RST#.

Power-Down Sequence

When either BD_SEL# (OFF/$\overline{\text{ON}}$) or Bit 2 of the command latch (C2) is set high, a power-down sequence begins (Figure 5).

The TIMER pin is immediately pulled low. The GATE pin (Pin 19) is pulled down by a 200µA current source to prevent the load currents on the 3.3V and 5V supplies from going to zero instantaneously and glitching the power supply voltages. Internal switches are connected to each of the output supply voltage pins to discharge the output bulk capacitors to ground. When any one of the output voltages drops below its $\overline{\text{PWRGD}}$ threshold, the $\underline{\text{HEALTHY\#}}$ signal pulls high, LOCAL_PCI_RST# ($\underline{\text{RESETOUT}}$) is asserted low, and the external status LED turns on.

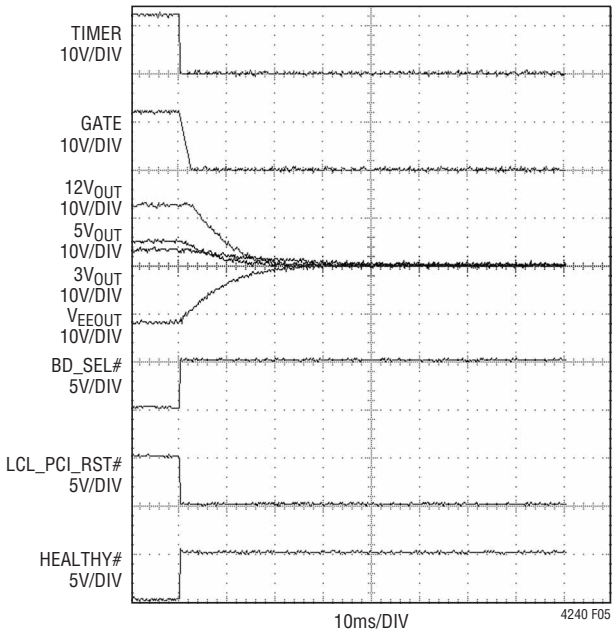

Figure 5. Normal Power-Down Sequence

Once the power-down sequence is complete the status LED will light up and the CPCI card may be removed from the slot. During extraction, the precharge circuit will continue to bias the bus I/O pins at 1V until the long connector pin connections are broken.

Early Power

Early Power usage is restricted by the CompactPCI (CPCI) specification. It is intended to power up the precharge circuit and I/O cells. The CPCI specification allows any of the long power pins (5V, 3.3V, V(I/O)) to be used for Early Power. Since Early Power is not isolated, a resistor should be placed in series with each CPCI connector pin. Note that if any Early Power pin is shorted on the inserted card, the current limiting resistor will dissipate the power.

In order to maximize the DC current available from the 5V supply, all eight 5V connector pins should be tied together on the inserted card. The same applies to the ten 3.3V CPCI connector pins. Early Power should then be drawn from either or both of the two V(I/O) long pins. If either or both of 5V and 3.3V is used for Early Power, then the 5V and 3.3V sense resistor values must be chosen such that the 1A/pin CPCI rule is not violated.

Connecting V_{EEIN}

To lessen the likelihood of faulting on power up, the V_{EEOUT} output pin should be bypassed with a capacitor that is only as large as necessary. A value of 10µF to 47µF is recommended. If a large value bypass capacitor is used (e.g. ≥100µF) on V_{EEOUT}, current limit faults may occur during power-up or during recovery from power failures.

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Timer

During a power-up sequence, an 11.5µA current source is connected to the TIMER pin (Pin 5) and charges up the external TIMER pin capacitor. Current limit faults are ignored until the TIMER voltage ramps to 5.5V. This feature allows the LTC4240 to power-up CPCI boards with widely varying capacitive loads on the back end supplies. The power-up time for either of the two outputs under current limit conditions is given by the slower of:

$$t_{ON}(XV_{OUT}) = 2 \bullet \frac{C_{LOAD(XVOUT)} \bullet XV_{OUT}}{I_{LIMIT(XVOUT)} - I_{LOAD(XVOUT)}} \text{ or} \quad (2a)$$

$$t_{ON}(GATE) = \frac{C1(XV_{OUT} + V_{TH})}{65\mu A} \quad (2b)$$

Where $XV_{OUT} = 5V_{OUT}$ or $3V_{OUT}$. The timer period should be set longer than the maximum supply turn-on time but short enough to not exceed the maximum safe operating area of the pass transistor during a short-circuit. V_{TH} is the threshold voltage of the external power FET (2V – 3V). The timer period will be:

$$t_{TIMER} = \frac{C_{TIMER} \bullet 5.5V}{11.5\mu A} \quad (3)$$

The TIMER pin is immediately pulled low when either OFF/$\overline{ON}$ (Pin 28) or Bit 2 of command latch (C2) goes high.

The TIMER pin also functions as a temporary auxiliary supply for $12V_{IN}$. In the event of a large (greater than 1V) glitch on $12V_{IN}$, the energy stored on the timer capacitor is used as substitute $12V_{IN}$ power. This improves the glitch immunity of the LTC4240.

Thermal Shutdown

The internal switches for the 12V and –12V supplies are protected by current limit and thermal shutdown circuits. When the temperature of the die reaches 150°C, all four switches will be latched off and the $\overline{FAULT}$ pin (Pin 7) will be pulled low. Since there is no automatic retry, power will have to be cycled with the OFF/$\overline{ON}$ pin or the I^2C command latch.

Short-Circuit Protection

In order to lower power dissipation in the pass transistors and to mitigate voltage spikes on the supplies during short-circuit conditions, the current limit on each supply is designed to be a function of the output voltage. As the output voltage drops, the current limit decreases. Unlike a traditional circuit breaker function where huge currents can flow before the breaker trips, the current foldback feature lowers short-circuit current by at least 50% when powering up into a short.

If any supply is in current limit after the TIMER pin voltage has ramped to 5.5V, then all four pass transistors will be immediately turned off and $\overline{FAULT}$ will be asserted low (Figure 6).

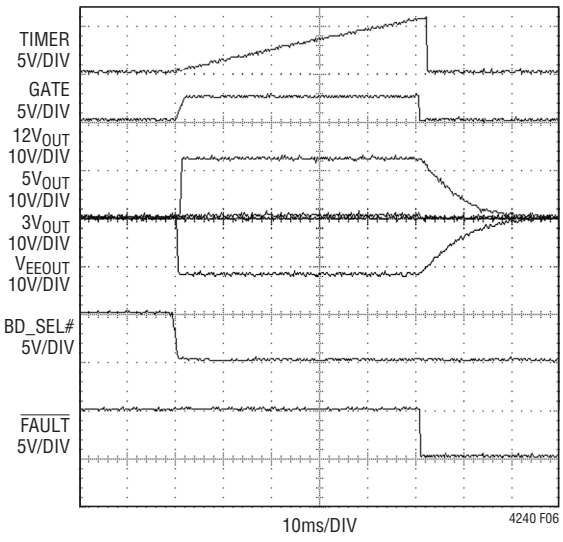

Figure 6. Power-Up into a Short on 3.3V Output

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Once the TIMER voltage has reached 5.5V, all of the supplies will be latched off if any supply enters current limit for at least 35µs. The 35µs delay prevents quick current spikes—for example, from a fan turning on—from causing false trips of the circuit breaker.

During normal operation, the 5V and 3.3V supplies are protected from overcurrent and short-circuit conditions by dual-level circuit breakers. In the event that either supply current exceeds the nominal limit, an internal timer is started. If the supply is still overcurrent after 35µs, the circuit breaker trips and all the supplies are turned off (Figure 7). If a short-circuit occurs on $5V_{OUT}$ or $3V_{OUT}$ and the supply current exceeds three times the set limit, an analog loop will limit the current to 3 times the value set by R_{SENSE} and 55mV. If the short persists for more than 35µs, the LTC4240 latches off (Figure 8). It will stay in the latched off state until it is reset using the OFF/$\overline{ON}$ pin or by using the I^2C interface. The LTC4240 can also be reset by cycling any of the power supplies.

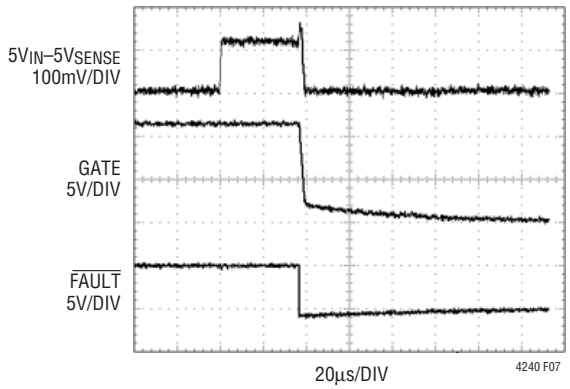

Figure 7. Overcurrent Fault on 5V

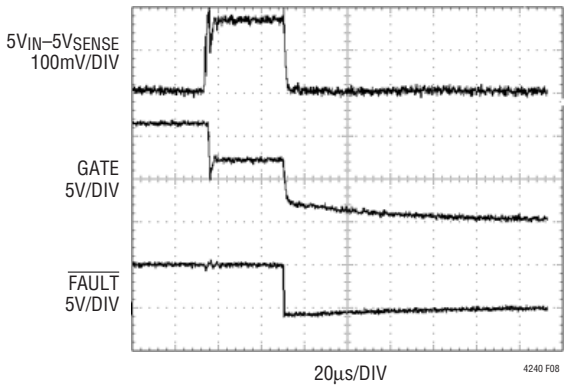

Figure 8. Short-Circuit Fault on 5V

The current limit and the foldback current level for the 5V and 3.3V outputs are both a function of the external sense resistor (R1 for $3V_{OUT}$ and R2 for $5V_{OUT}$, see front page). A sense resistor is connected between $5V_{IN}$ (Pin 21) and $5V_{SENSE}$ (Pin 20) for the 5V supply. For the 3.3V supply, a sense resistor is connected between $3V_{IN}$ (Pin 22) and $3V_{SENSE}$ (Pin 23). The current limit and the current foldback current level are given by Equations 4 and 5:

$$I_{LIMIT(XVOUT)} = \frac{55mV}{R_{SENSE(XVOUT)}} \quad (4)$$

$$I_{FOLDBACK(XVOUT)} = \frac{11mV}{R_{SENSE(XVOUT)}} \quad (5)$$

where $XV_{OUT} = 5V_{OUT}$ or $3V_{OUT}$.

Equation 4 is the current limit for $XV_{OUT} \approx XV_{IN}$. Equation 5 shows the I_{LIMIT} for shorted outputs. Both equations assume voltage on TIMER pin is greater than 5.5V.

$XV_{OUT} = 3V_{OUT}$ or $5V_{OUT}$. Note that since there are only 8 pins connecting $5V_{IN}$, $R_{SENSE} \geq 0.007\Omega$ for $5V_{IN}$.

The current limit for the internal 12V switch is set at –1200mA folding back to –350mA and the –12V switch at 500mA folding back to 250mA.

Selecting R_{SENSE}

An equivalent circuit for the 5V and 3.3V circuit breakers is shown in Figure 9. The sense resistor and the circuit breaker threshold voltage determine the fault current that turns off the external FETs. Sense resistors with a 1% tolerance are recommended. Due to part to part and temperature variations for both the sense resistor value and the circuit breaker threshold voltage, the actual current limit threshold will exhibit some variation. To calculate the smallest value of current that will trip the fault comparator, use the largest value of the sense resistor and the smallest value of the threshold voltage. A 0.005Ω 1% sense resistor (on the 3.3V supply, for example) with typical temperature coefficients would increase to approximately 0.0051Ω (nominal value multiplied by the 1% tolerance and the TC at 70°C). Since the minimum value of the threshold voltage is 50mV, this implies a current limit of 9.8A. To arrive at the largest value of the current limit that will turn off the external FETs, the nominal value of the

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sense resistor drops to 0.0049Ω and the largest value of threshold voltage increases to 60mV. This results in a trip current of 12.2A.

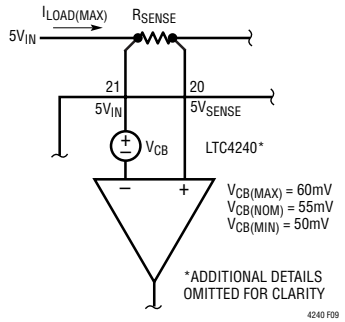

Figure 9. Circuit Breaker Equivalent Circuit for Calculating R_{SENSE}

Plug-in board designers are thus limited to using less than 9.8A when a nominal 0.005Ω resistor is used. Using more than 9.8A runs the risk of turning off the external FET. Since the CompactPCI specification allows a maximum 1A/pin, at least 10 pins must be used to supply 9.8A. This implies that only the 3.3V supply can use a 0.005Ω resistor, since the 5V supply has a maximum of 8 pins available. To adhere to the 1A/pin specification, the 5V sense resistor should be larger than the 3.3V sense resistor. Typical applications show a nominal 0.007Ω resistor, which results in a 7.04A maximum deliverable current to the plug-in board loads. The 7.04A current implies at least 7 pins on the 5V connector. Note that the thermal considerations of the external FET will also place limitations on the maximum allowable current.

5V and 3.3V External FET Selection

The LTC4240 uses external power FETs to limit and modulate the current delivered by the 3.3V and 5V supplies. There are several parameters to consider when selecting the FET:

1. On resistance.
2. Gate and drain breakdown voltage.
3. Steady state and transient power dissipation.

On Resistance

The CompactPCI specification limits the total IR drop of the FET plus the IR drop of the sense resistor to 100mV. For a nominal sense resistor of 0.005Ω, if the user limits the 3.3V supply load current to 8.7A, then the maximum FET resistance should be less than 0.0063Ω. Similarly, for a 6.2A load current on the 5V supply and a 0.007Ω sense resistor, the maximum 5V FET resistance should be 0.0088Ω. Note that above values of FET resistance are worst case over temperature (on the FET's datasheet, find the resistance vs temperature curve and de-rate the room temperature maximum value).

Breakdown Voltage

The maximum DC voltage that can appear across the drain/source of the external power FET is 5V +10%. During transient events and hot swap conditions, parasitic inductances could cause ringing up to 3 times the supply voltage. The use of voltage transient suppressors at the 5V and 3.3V inputs can limit these voltage swings to less than 10V (see front page schematic). Similarly, the largest DC voltage that is likely to appear across the gate is 12V +10%. Voltage suppressors on the $12V_{IN}$ node will also limit the transient spikes on that node. Additionally, the total capacitance on the GATE node will serve to filter fast voltage noise spikes. FETs with a minimum rating of ±20V on both the drain/source and the gate/source are recommended.

Steady State Power Dissipation

For a user selected maximum load current of 8.7A on the 3.3V power supply and a 0.0063Ω maximum FET resistance, the DC power dissipation is:

$$(I_{MAX})^2(R_{DSON,MAX}) = (8.7)(8.7)(0.0063) = 0.477W$$

This is within the SOA limits of most power FETs.

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Transient Power Dissipation

There are certain transient events that can significantly increase the power dissipated by the external FET. If the LTC4240 5V supply (at 5V + 10%) powers up into a 1.5V short (potentially manifested as a short to two diodes in series), then the FET can potentially have 4V across it with 8.8A flowing. This implies a power dissipation of 35.1W. The amount of time the FET will dissipate 35.1W will depend on the relative values of the TIMER and GATE capacitances. For the values specified on the front page application circuit, the GATE pin will ramp high significantly faster than the TIMER pin, hence transient power dissipation will be set by the TIMER pin capacitance.

The dissipated 35.1W, the ramp time of the TIMER pin (50ms will be used for this example), and the FET thermal resistance will determine the internal junction temperature of the FET. Most FETs will specify a maximum internal junction temperature of 150°C. The FET datasheets should have a transient thermal impedance graph. This graph has a family of curves listing the FET transient thermal impedance as a function of duty cycle. The duty cycle refers to what percentage of the time the FET is in the short circuit condition. If we choose the Si7880DP FET and assume that the board on which the FET is placed has minimal heat sinking capability, and further assume that the user will turn on the board every 2.5 seconds (0.02 duty cycle: 50ms on, 2450ms off), then by looking at the junction-to-ambient curve we note that with a 70°C ambient temperature, the Si7880DP internal junction temperature will be 172°C. This is above the absolute maximum rating of the FET, and although operating at this temperature will not damage the FET immediately, it does affect its long term reliability. Conversely, if we assume that there is a perfect heat sink for the Si7880DP package, then we would use the junction-to-case curve and calculate a value of 117°C with a 70°C ambient temperature. The Si7880DP comes in a thermally enhanced package whose drain lead is a large piece of metal that can conduct heat away from the internal junction of the FET. To achieve best performance, the drain of the Si7880DP should be connected to a piece of copper (as large as possible) on the board. Note that if the output is shorted to ground, the current foldback feature will cut the power dissipation by at least a factor of two.

When the LTC4240 is turned on and the large $5V_{OUT}$ output capacitor (2000µF or more) is charged, it is possible that the 5V FET will dissipate as much as the 35.1W described above. If there is no DC load at $5V_{OUT}$, then 8.8A will charge the 2000µF in less than 2ms, which should not pose any thermal problems for the Si7880DP. If the DC load at $5V_{OUT}$ approaches the current limit, then the above analysis should be used to calculate the internal junction temperature of the FET.

Output Voltage Monitor

The DC level of all four supply outputs is monitored by the power good circuitry. When any of the four supply outputs falls below its specified level (see DC electrical specifications) for longer than 10µs, the PWRGD (HEALTHY#) open drain pin will be deasserted and the LOCAL_PCI_RST# signal will be asserted low. This does not generate a fault condition.

The LOCAL_PCI_RST# signal ($\overline{\text{RESETOUT}}$ pin) is derived from the HEALTHY# ($\overline{\text{PWRGD}}$ pin), PCI_RST# ($\overline{\text{RESETIN}}$ pin), and Bit 3 of the command latch (see Table 5).

Table 5. LOCAL_PCI_RST# Truth Table

PCI_RST#	HEALTHY#	Bit 3 (C3) Command Latch	LOCAL_PCI_RST#
LO	X	X	LO
X	HI	X	LO
X	X	HI	LO
HI	LO	LO	HI

Precharge

The PRECHARGE input and DRIVE output pins are used to generate the 1V precharge voltage that biases the bus I/O connector pins during board insertion and extraction (Figure 10). The LTC4240 is capable of generating precharge voltages other than 1V. Figure 11 shows a circuit that can be used in applications requiring a precharge voltage less than 1V. The circuit in Figure 12 can be used for applications that need precharge voltages greater than 1V. Table 6 lists suggested resistor values for R11A and R11B vs precharge voltage for the application circuits shown in Figures 11 and 12.

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Table 6. R1 and R2 Resistor Values vs Precharge Voltages

$V_{PRECHARGE}$	R11A	R11B	$V_{PRECHARGE}$	R11A	R11B
1.5V	18Ω	9.09Ω	0.9V	16.2Ω	1.78Ω
1.4V	18Ω	7.15Ω	0.8V	14.7Ω	3.65Ω
1.3V	18Ω	5.36Ω	0.7V	12.1Ω	5.11Ω
1.2V	18Ω	3.65Ω	0.6V	11Ω	7.15Ω
1.1V	18Ω	1.78Ω	0.5V	9.09Ω	9.09Ω
1V	18Ω	0Ω			

Precharge resistors are used to connect the 1V bias voltage to the CompactPCI connector I/O lines. This allows live insertion of the I/O lines with minimal disturbance. Figure 13 shows the precharge application circuit for 5V signaling environments. The precharge resistor requirements are more stringent for 3.3V and Universal Hot Swap signaling. If the total leakage current on the I/O line is less

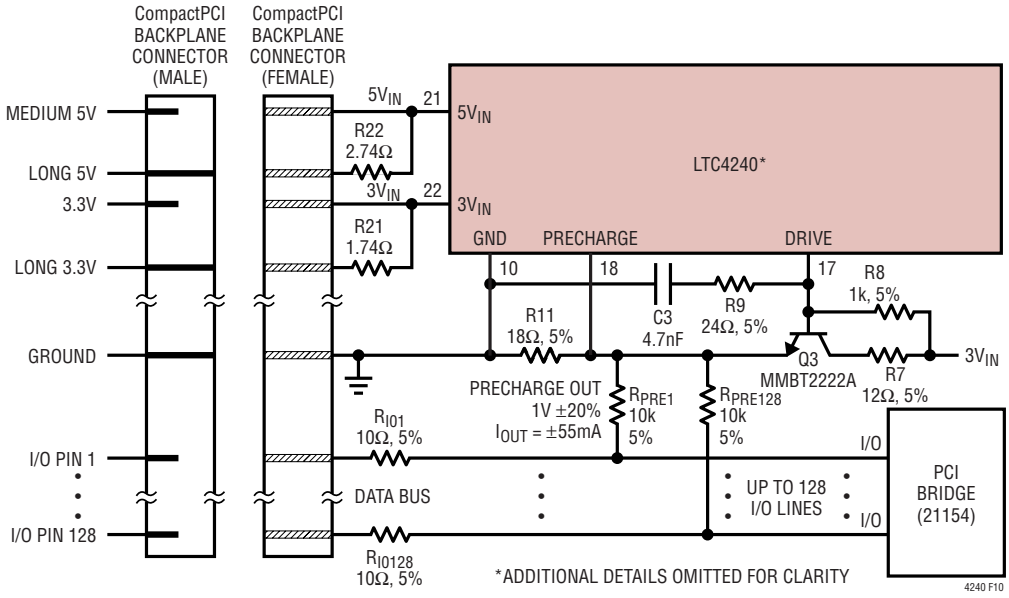

Figure 10. Precharge Application Circuit

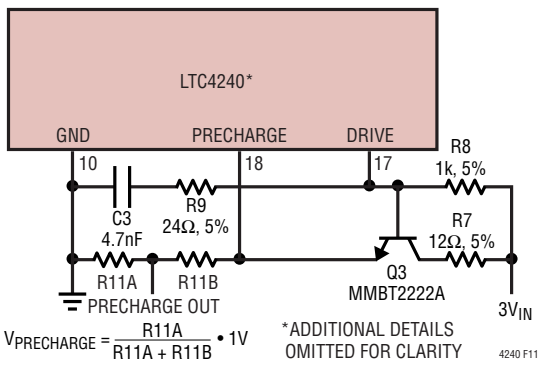

Figure 11. Precharge Voltage Less Than 1V

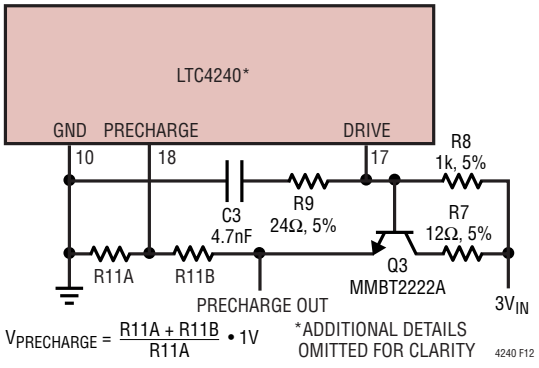

Figure 12. Precharge Voltage Greater Than 1V

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than 2µA, then a 50K resistor can be connected directly from the 1V bias voltage to the I/O line. However, many ICs connected to the I/O lines can have leakage currents up to 10µA. For these applications, a 10k resistor is used but must be disconnected when the board has been seated as determined by the state of the BD_SEL# signal. Figure 14 shows a precharge circuit that uses a bus switch to connect the individual 10k precharge resistors to the LTC4240 1V PRECHARGE pin. The electrical connection is made (bus switches close) when the voltage on the BD_SEL# pin of the plug-in card is above 4.4V, which occurs just after the long pins have made contact. The bus switches are subsequently electrically disconnected when the board connector makes contact with the BD_SEL# pin (bus switch $\overline{OE}$ pin is pulled high by Q4).

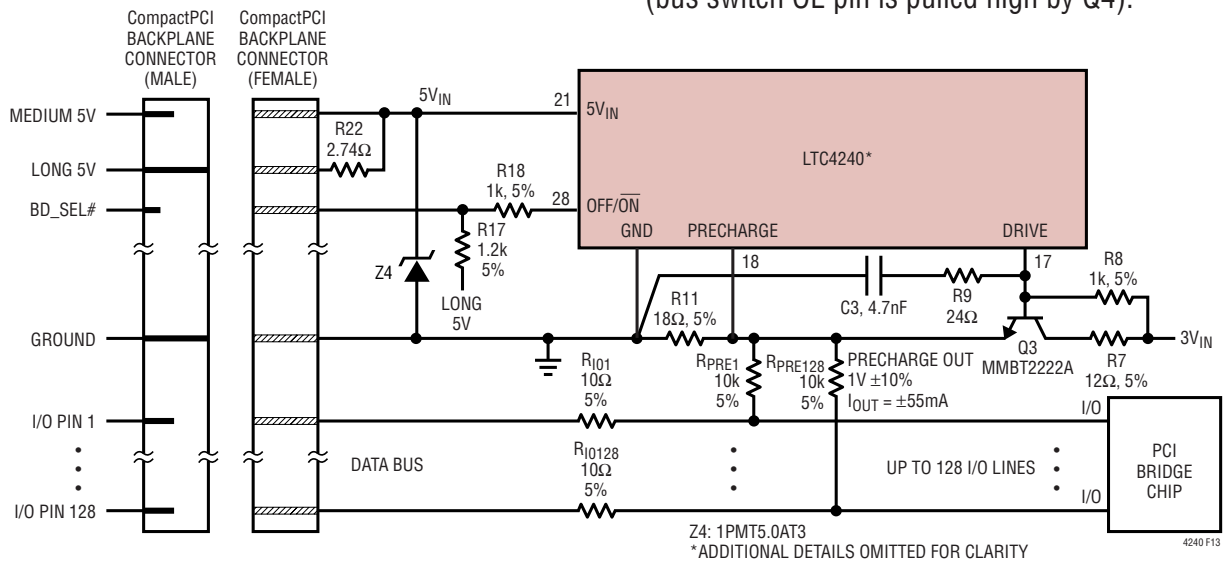


Figure 13.Precharge Application Circuit for 5V Signaling Systems

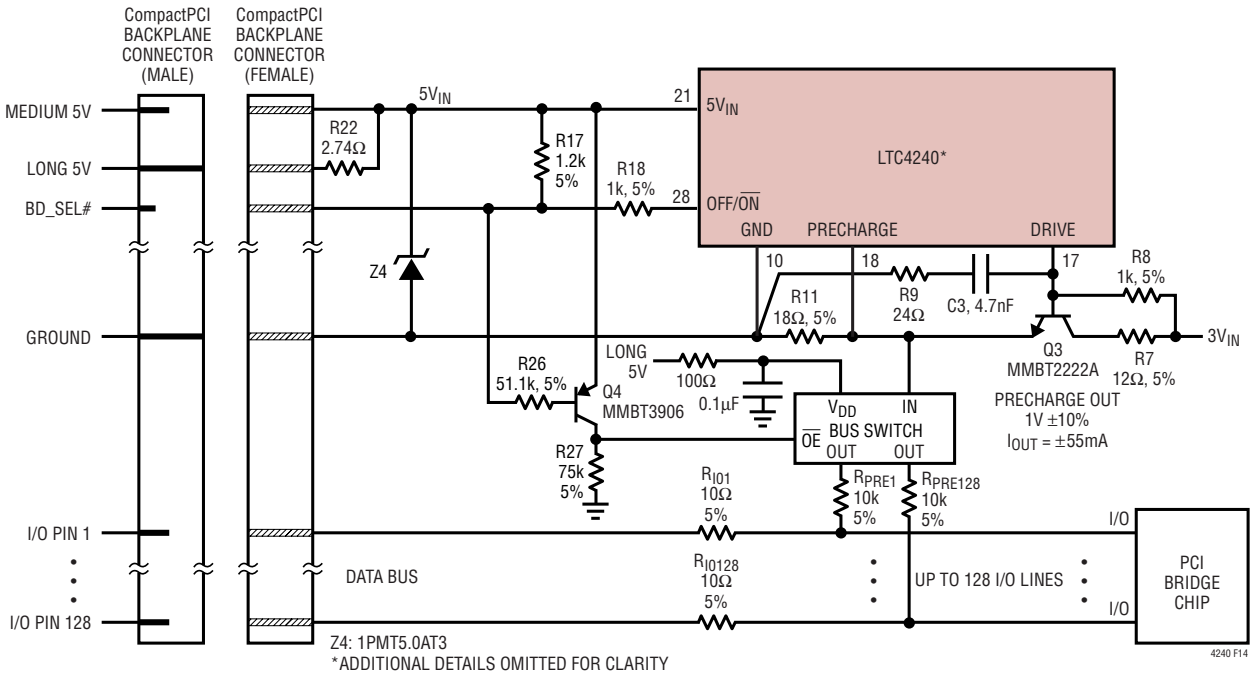


Figure 14. Precharge Bus Switch Application Circuit for 3.3V and Universal Hot Swap Boards

APPLICATIONS INFORMATION

The assumption by the CompactPCI specification is that there is a diode to 3.3V on the circuit that is driving the BD_SEL# pin. The 1.2k resistor pull up to $5V_{IN}$ on the plug-in card will thus be clamped by the diode to 3.3V. If the BD_SEL# pin is being driven high, the actual voltage on the pin will be approximately 3.9V. This is still above the high TTL threshold of the LTC4240 OFF/$\overline{ON}$ pin, but low enough for Q4 to disable the bus switches and thus remove the 10k resistors from the I/O lines. Note that BD_SEL# is ordinarily connected to V(I/O), which in turn is allowed to be driven by either 3.3V or 5V. For applications such as shown in Figure 14, the pull up on BD_SEL# is restricted to the long 5V pins. A bus switch with no internal diode to V_{DD} is preferred. Since the power to the bus switch is derived from one of the unswitched power planes, a 100Ω resistor plus a 0.1µF bypass capacitor should be placed in series with its power supply.

When the plug-in card is removed from the connector, the BD_SEL# connection is broken first, and the BD_SEL# voltage pulls up to 5V. This causes Q4 to turn off, which re-enables the bus switch, and the precharge resistors are again connected to the LTC4240 PRECHARGE pin for the remainder of the board extraction process.

The LTC4240 $\overline{BE}$ pin can alternatively be used to drive the enable input of the bus switch. The $\overline{BE}$ signal would then keep the I/O lines precharged until all supplies reached power good status. The resistor in series with the PRECHARGE pin protects the internal circuitry from large voltage transients during live insertion.

PRSNT1#, PRSNT2#

PRSNT1# and PRSNT2# are PCI signals that convey the plug-in board's power consumption information. These pins should either be shorted to ground or be connected to Early Power with a 10k resistor. The voltage levels (TTL) at the PRSNT#1, 2 pins can be read using the I^2C 2-wire interface.

PRSNT1#	PRSNT2#	Expansion Configuration
Open	Open	No plug in board present
Ground	10k Pull-Up	Plug-in board present, maximum power consumption
10k Pull-Up	Ground	Plug-in board present, nominal power consumption
Ground	Ground	Plug-in board present, minimum power consumption

Other CompactPCI Applications

If no 3.3V supply input is required, Figure 15 illustrates how the LTC4240 should be configured.

For applications where the BD_SEL# connector pin is grounded on the backplane, the circuit in Figure 16 allows the LTC4240 to be reset simply by pressing a pushbutton switch on the CPCI plug-in board. This arrangement allows for manual resetting of the LTC4240's circuit breakers.

Input Transient Protection

Hot-plugging a board into a backplane generates inrush currents from the backplane power supplies. This is due to the charging of the plug-in board bulk capacitance. To reduce this transient current to a safe level, the CPCI Hot Swap specification restricts the amount of unswitched capacitance used on the input side of the plug-in board. Each pin connected to the CPCI female connector on the plug-in board is allowed at most 0.01µF/pin. Bulk capacitors are only allowed on the switched output side of the LTC4240 ($5V_{OUT}$, $3V_{OUT}$, $12V_{OUT}$, V_{EEOUT}). Some bulk capacitance is allowed on the Early Power planes, but only because a current limiting resistor is assumed to separate the connector from the bulk capacitor. Circuits normally placed on the unswitched Early Power (PCI Bridge, for example) need to have a current limiting resistor.

APPLICATIONS INFORMATION

Disallowing bulk capacitors on the input power pins mitigates the inrush current during hot plug. However, it also tends to create a resonant circuit formed by the inductance of the backplane power supply trace and the parasitic capacitance of the plug-in board (mainly due to the large power FET). Upon board insertion, the ringing of this circuit will exhibit peak overshoot as high as 2.5 times the steady state voltage (>30V for 12V).

There are two methods for abating the effects of these high voltage transients: using zener clamps, and using snubber networks. Snubbers are RC networks whose time constants are large enough to damp the inductance of the parasitic resonant circuit. The snubber capacitor should be 10X to 100X the value of the plug-in board parasitic capacitance. The value of the series snubber resistor should be large enough to damp the resulting R-L-C circuit and is typically between 1Ω and 50Ω. These protection networks should be mounted very close to the LTC4240 in order to minimize parasitic inductance. This is shown in Figure 17 for the 3.3V and 5V supplies.

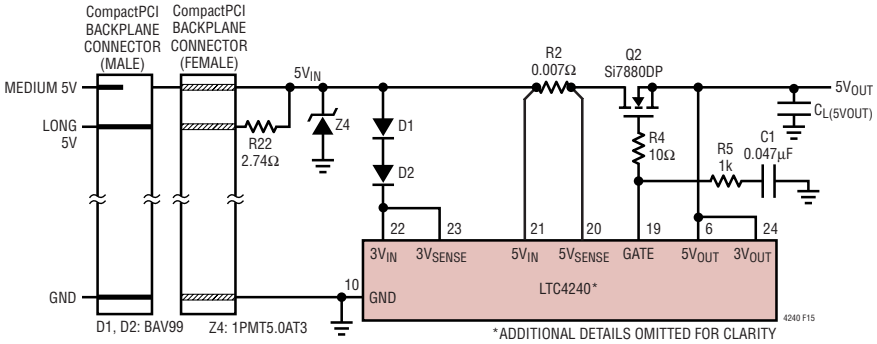


Figure 15. 5V Supply Only Application Circuit

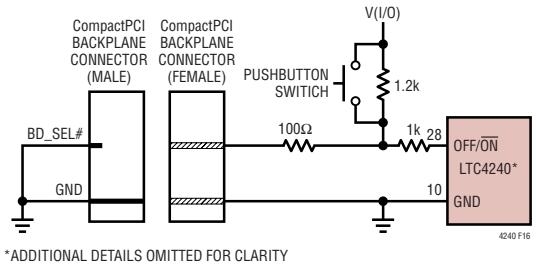


Figure 16. BD_SEL# Pushbutton Toggle Switch

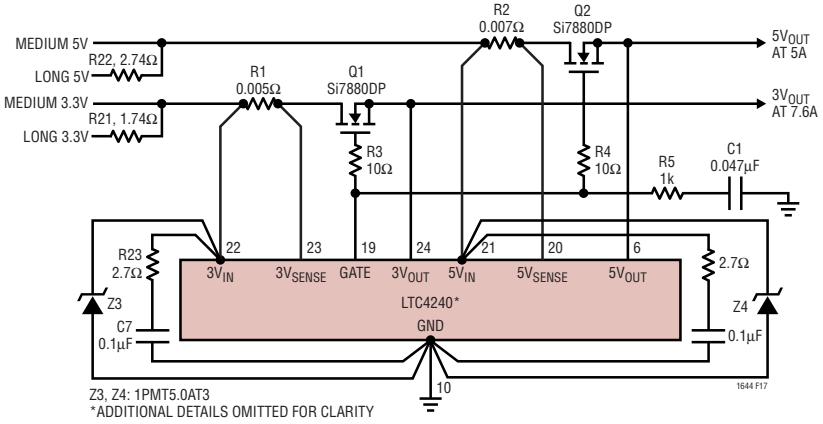
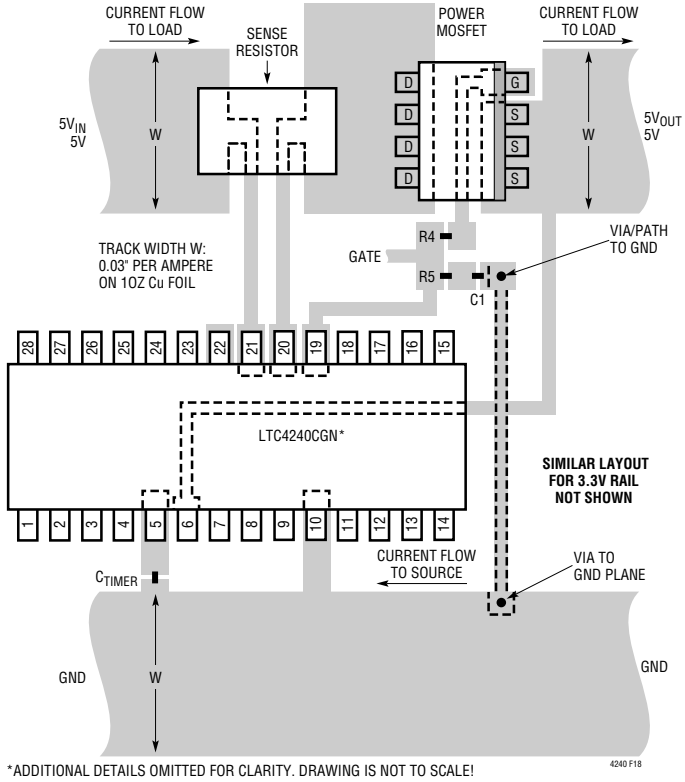


Figure 17. Place Transient Protection Device Close to the LTC4240

APPLICATIONS INFORMATION

Note (see front page schematic) that the 12V and –12V show 0.01µF snubber capacitors. This is consistent with the CPCI specification since we also recommend a 10Ω snubber resistor. The $12V_{IN}$ pin is the most sensitive to high energy large voltage transients. A transient voltage suppressor with a breakdown voltage between 13.2V and 15V is advisable. The TVS should also be able to dissipate at least 150W. The SMAJ12CA can be used for both $12V_{IN}$ and V_{EEIN}. Place the TVS close to the LTC4240. See front page schematic.



*ADDITIONAL DETAILS OMITTED FOR CLARITY. DRAWING IS NOT TO SCALE!

Figure 18. Recommended Layout for Power MOSFET, Sense Resistor and GATE Components for the 5V Rail. Similar Layout for 3.3V Rail Not Shown

PCB Layout Considerations

For proper operation of the LTC4240's circuit breaker function, a 4-wire Kelvin connection to the sense resistors is highly recommended. A recommended PCB layout for the sense resistor, the power MOSFET, and the GATE drive components around the LTC4240 is illustrated in Figure 18. The drawing is not to scale and is only intended to show the low resistance, external high current path. In hot swap applications where load currents can reach 10A, narrow PCB tracks exhibit more resistance than wider tracks and operate at more elevated temperatures. Since the sheet resistance of 1 ounce copper is approximately 0.5mΩ/square, track resistances add up quickly in high-current applications. Thus, to keep PCB track resistance and temperature rise to a minimum, the suggested trace width in these applications for 1 ounce copper is 0.03" for each ampere of DC current.

In order to help dissipate the heat generated by the power MOSFET, the copper trace connected to the drain should be made as large as possible.

In the majority of applications, it will be necessary to use plated-through vias to make circuit connections from component layers to power and ground layers internal to the PC board. For 1 ounce copper plating, a general rule is 1A of DC current per via, making sure the via is properly dimensioned so that solder completely fills any void. For other plating thicknesses, check with your PCB fabrication facility.

Power MOSFET and Sense Resistor Selection

Table 7 lists some current MOSFET transistors that are available. Table 8 lists some current sense resistors that can be used with the LTC4240's circuit breakers. Table 9 lists supplier web site addresses for discrete components mentioned throughout the LTC4240 data sheet. High current applications should select a MOSFET with very low on-resistance and good transient thermal characteristics.

APPLICATIONS INFORMATION

Table 7. N-Channel Power MOSFET Selection Guide

CURRENT LEVEL (A)	PART NUMBER	DESCRIPTION	MANUFACTURER
0 to 2	MMDF3N02HD	Dual N-Channel SO-8 $R_{DS(ON)}$ = 0.1Ω	ON Semiconductor
2 to 5	MMSF5N02HD	Single N-Channel SO-8 $R_{DS(ON)}$ = 0.025Ω	ON Semiconductor
5 to 10	MTB50N06V	Single N-Channel DD-Pak $R_{DS(ON)}$ = 0.028Ω	ON Semiconductor
5 to 10	IRF7457	Single N-Channel SO-8 $R_{DS(ON)}$ = 0.007Ω	International Rectifier
5 to 10	Si7880DP	Single N-Channel PowerPAK™ $R_{DS(ON)}$ = 0.003Ω	Vishay-Siliconix

Table 8. Sense Resistor Selection Guide

CURRENT LIMIT VALUE	PART NUMBER	DESCRIPTION	MANUFACTURER
1A	LR120601R055F WSL1206R055	0.055Ω, 0.5W, 1% Resistor	IRC-TT Vishay-Dale
2A	LR120601R028F WSL1206R028	0.028Ω, 0.5W, 1% Resistor	IRC-TT Vishay-Dale
5A	LR120601R011F WSL2010R011	0.011Ω, 0.5W, 1% Resistor	IRC-TT Vishay-Dale
7.9A	WSL2512R007	0.007Ω, 1W, 1% Resistor	Vishay-Dale
11A	WSL2512R005	0.005Ω, 1W, 1% Resistor	Vishay-Dale

PowerPAK is a trademark of Vishay-Siliconix

Table 9. Manufacturers' Web Site

MANUFACTURER	WEB SITE
International Rectifier	www.irf.com
ON Semiconductor	www.onsemi.com
IRC-TT	www.irctt.com
Vishay-Dale	www.vishay.com
Vishay-Siliconix	www.vishay.com
Diodes, Inc.	www.diodes.com

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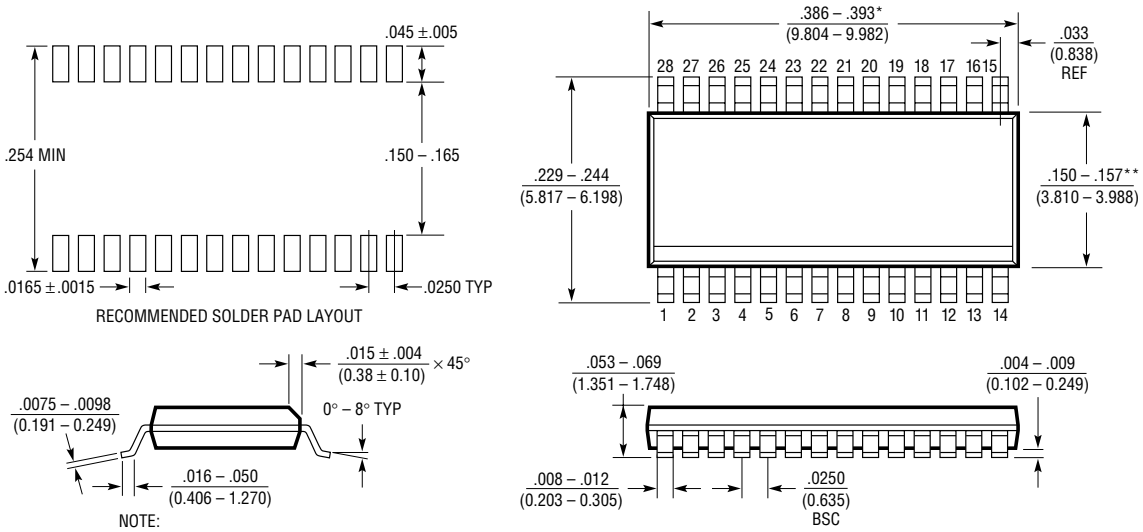
PACKAGE DESCRIPTION

GN Package
28-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1421	Hot Swap Controller	Dual Supplies for 3V to 12V, Additionally –12V
LTC1422	Hot Swap Controller in SO-8	Single Supply from 3V to 12V
LT1641-1/LT1641-2	Positive Voltage Hot Swap Controller in SO-8	Supplies from 9V to 80V, Latched Off/Auto Retry
LTC1642	Fault Protected Hot Swap Controller	3V to 15V, Overvoltage Protection Up to 33V
LTC1643AL/LTC1643AL-1/ LTC1643AH	PCI Bus Hot Swap Controllers	3.3V, 5V, 12V, –12V Supplies for PCI Bus
LTC1644	CompactPCI Hot Swap Controller	3.3V, 5V, ±12V, I/O Precharge and Local Reset Logic
LTC1645	2-Channel Hot Swap Controller	Operates from 1.2V to 12V, Power Sequencing
LTC1646	CompactPCI Hot Swap Controller for 3.3V and 5V	3.3V and 5V only, I/O Precharge and Local Reset Logic
LTC1647	Dual Hot Swap Controller	Dual ON Pins for Supplies from 3V to 15V
LTC4211	Single Hot Swap Controller with Multifunction Current Control	2.5V to 16.5V, Dual Level Circuit Breaker, No Gate Capacitor
LTC4230	Triple Hot Swap Controller with Multifunction Current Control	1.7V to 16.5V, Dual Level Circuit Breaker, No Gate Capacitor
LTC4241	PCI Hot Swap Controller with 3.3V Auxiliary	3.3V, 5V, ±12V and 3.3VAux Supplies for PCI Bus
LT4250L/LT4250H	–48 Hot Swap Controllers in SO-8	Active Current Limiting, Supplies from –20V to –80V
LTC4251	–48 Hot Swap Controller in SOT-23	Floating Topology, Active Current Limiting
LTC4252	–48 Hot Swap Controller in MSOP	Floating Topology, Active Current Limiting, $\overline{\text{PWRGD}}$ Output
LTC4350	Hot Swappable Load Share Controller	Eliminates ORing Diodes, Identifies and Localizes Faults

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