THE DATASHEET OF

LTC4216CDE#PBF

Ultralow Voltage Hot Swap Controller

FEATURES

- **Allows Safe Board Insertion and Removal from a Live Backplane**
- **Controls Load Voltages from 0V to 6V**
- **Fast Response Limits Peak Fault Current**
- **Adjustable Analog Current Limit**
- **Adjustable Soft-Start with Inrush Current Limiting**
- **Adjustable Response Time for Overcurrent Protection**
- Low Circuit Breaker Trip Threshold: 25mV
- No External Gate Capacitor Required
- Internal Charge Pump for N-Channel MOSFET
- Adjustable Output Power-Up Rate
- $\overline{\text{RESET}}$ and $\overline{\text{FAULT}}$ Output
- 10-Lead MSOP and 12-Lead (4mm × 3mm) DFN Packages

APPLICATIONS

- Electronic Circuit Breaker
- Live Board Insertion and Removal
- Industrial High Side Switch/Circuit Breaker
- Optical Networking

DESCRIPTION

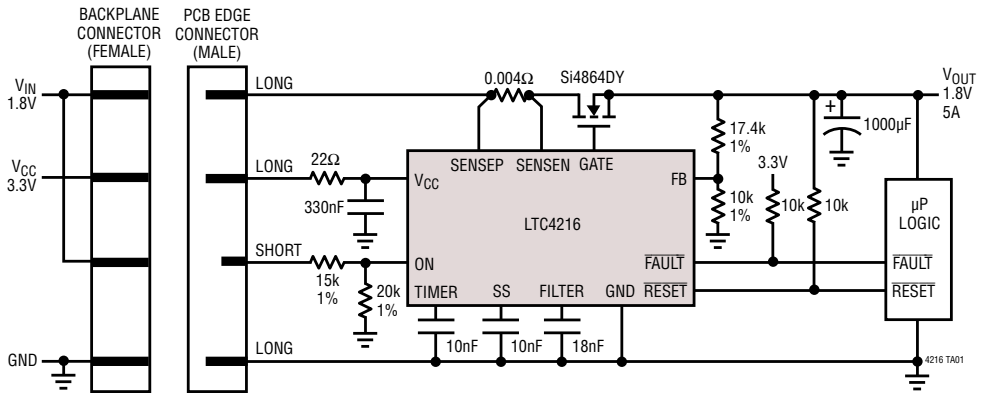
The LTC®4216 is a positive low voltage Hot Swap™ controller that allows a board to be safely inserted and removed from a live backplane. It controls load voltages ranging from 0V to 6V and isolates a severe fault with instantaneous analog current limiting.

An internal high side switch driver controls the gate of an external N-channel MOSFET. An adjustable soft-start limits the rate of change of the inrush current at start-up for a large load capacitor. Together with an analog current limit amplifier, an electronic circuit breaker with adjustable response time provides dual level overcurrent protection. No external gate capacitor is required for the analog current limit loop compensation.

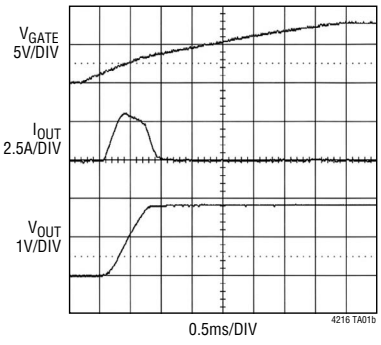
The FB pin monitors the output supply voltage and signals the $\overline{\text{RESET}}$ output pin. An ON pin provides on/off control and a $\overline{\text{FAULT}}$ pin indicates the fault status. The LTC4216 is available in the 10-lead MSOP and 12-lead (4mm × 3mm) DFN packages.

TYPICAL APPLICATION

Single Channel 1.8V Hot Swap Controller



Normal Power-Up with Soft-Start



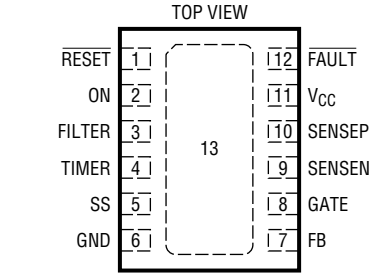
ABSOLUTE MAXIMUM RATINGS

(Note 1)

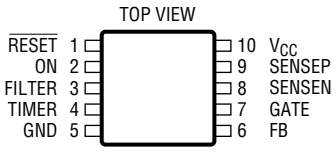
Bias Supply Voltage (V_{CC}).....– 0.3V to 9V
Input Voltages
FB, ON, SS, SENSEP, SENSEN .....– 0.3V to 9V
TIMER, FILTER.....–0.3V to V_{CC} + 0.3V
Output Voltages
$\overline{RESET}$, $\overline{FAULT}$ .....–0.3V to 9V
GATE.....–0.3V to 15V

Operating Temperature Range
LTC4216C ..... 0°C to 70°C
LTC4216I .....–40°C to 85°C
Storage Temperature Range
MS.....–65°C to 150°C
DE.....–65°C to 150°C
Lead Temperature (Soldering, 10sec)
MS Package.....300°C

PIN CONFIGURATION



DE PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 4.3°C/W
EXPOSED PAD (PIN 13) INTERNALLY CONNECTED TO GND
(PCB CONNECTION OPTIONAL)



MS PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 160°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4216CDE#PBF	LTC4216CDE#TRPBF	4216	12-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC4216IDE#PBF	LTC4216IDE#TRPBF	4216	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4216CMS#PBF	LTC4216CMS#TRPBF	LTBKV	10-Lead Plastic MSOP	0°C to 70°C
LTC4216IMS#PBF	LTC4216IMS#TRPBF	LTBKV	10-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Bias Supply Range		●	2.3		6	V
V_{SENSEP}	V_{SENSEP} Supply Range		●	0		6	V
I_{CC}	Bias Supply Current	V_{ON} = 2V, V_{FB} = 2V	●		1.6	3	mA
$V_{CC(UVL)}$	Bias Supply Undervoltage Lockout	V_{CC} Rising	●	1.97	2.12	2.23	V
$\Delta V_{CC(UVL,HYST)}$	Bias Supply Undervoltage Lockout Hysteresis		●	50	120	190	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\Delta V_{CB(TH)}$	Circuit Breaker Trip Voltage Threshold ($V_{SENSEP} - V_{SENSEN}$)	V_{SENSEP} = 0.4V, 3.3V	 ●	22.5 21.5	25 25	27.5 28.5	mV mV
$\Delta V_{ACL(TH)}$	Analog Current Limit Voltage Threshold ($V_{SENSEP} - V_{SENSEN}$)		●	32	40	48	mV
$I_{SENSEP(IN)}$	SENSEP Pin Input Current	$V_{SENSEP} = V_{SENSEN} = V_{CC}$ = 6V $V_{SENSEP} = V_{SENSEN}$ = 0V, V_{CC} = 6V	● ●	20	70 –7	250 –20	µA µA
$I_{SENSEN(IN)}$	SENSEN Pin Input Current	$V_{SENSEN} = V_{SENSEP} = V_{CC}$ = 6V $V_{SENSEN} = V_{SENSEP}$ = 0V, V_{CC} = 6V	● ●	 –5	10 –10	15 –15	µA µA
$I_{GATE(UP)}$	GATE Pull Up Current	Gate Drive On, V_{GATE} = 0V, V_{ON} = 2V	●	–16	–20	–26	µA
$I_{GATE(DN)}$	GATE Pull Down Current	Gate Drive Off, V_{GATE} = 5V, V_{ON} = 0.6V V_{SENSEP} - V_{SENSEN} = 55mV, V_{GATE} = 5V V_{SENSEP} - V_{SENSEN} = 100mV, V_{GATE} = 5V	● ● ●	100 1 15	600 5 50	1500 20 100	µA mA mA
ΔV_{GATE}	External N-Channel Gate Drive ($V_{GATE} - V_{SENSEN}$)	2.3V ≤ V_{CC} < 3V 3V ≤ V_{CC} ≤ 6V	● ●	4.0 4.5	5.0 6.2	7.9 7.9	V V
$V_{GATE(TH)}$	GATE Pin Threshold Voltage	V_{GATE} Falling	●	0.15	0.2	0.3	V
$V_{SS(CLP)}$	SS Pin Clamp Voltage	After End of SS Timing Cycle	●	1.3	1.65	2.0	V
$V_{SS(TH)}$	SS Pin Threshold Voltage	V_{SS} Falling	●	0.15	0.2	0.35	V
$I_{SS(UP)}$	SS Pull Up Current	V_{ON} = 2V, V_{SS} = 1.2V, V_{FB} = 2V V_{ON} = 2V, V_{FB} = 0V	● ●	–7 –0.3	–10 –1	–13 –2	µA µA
$I_{SS(DN)}$	SS Pull Down Current	V_{ON} = 0V, V_{SS} = 2V			8		mA
$V_{FB(TH)}$	FB Pin Threshold Voltage	V_{FB} Falling	●	0.593	0.602	0.611	V
$\Delta V_{FB(LINEREG)}$	FB Pin Threshold Line Regulation	2.3V ≤ V_{CC} ≤ 6V	●		0.2	3	mV
$\Delta V_{FB(HYST)}$	FB Pin Hysteresis				3		mV
$I_{FB(IN)}$	FB Pin Input Current	V_{FB} = 1.2V, V_{CC} = 6V	●		0	±1	µA
$V_{ON(TH)}$	ON Pin Threshold Voltage	V_{ON} Rising	●	0.77	0.8	0.83	V
$\Delta V_{ON(HYST)}$	ON Pin Hysteresis		●	40	80	130	mV
$V_{ON(FC)}$	ON Pin Fault Clear Threshold Voltage	V_{ON} Falling	●	0.36	0.4	0.44	V
$I_{ON(IN)}$	ON Pin Input Current	V_{ON} = 1.2V, V_{CC} = 6V	●		0	±1	µA
$V_{TMR(TH)}$	TIMER Pin Threshold Voltage	V_{TIMER} Rising V_{TIMER} Falling	● ●	1.216 0.15	1.253 0.2	1.291 0.35	V V
$I_{TMR(UP)}$	Timer Pull Up Current	Timer On, V_{ON} = 2V, V_{TIMER} = 1V	●	–1.5	–2	–2.5	µA
$I_{TMR(DN)}$	Timer Pull Down Current	Timer Off, V_{ON} = 0V, V_{TIMER} = 2V			8		mA
$V_{FILT(TH)}$	FILTER Pin Threshold Voltage	V_{FILTER} Rising V_{FILTER} Falling	● ●	1.216 0.15	1.253 0.2	1.291 0.35	V V
$I_{FILT(UP)}$	Filter Pull Up Current	V_{ON} = 2V, V_{FILTER} = 1V, In Fault Mode	●	–45	–60	–75	µA
$I_{FILT(DN)}$	Filter Pull Down Current	V_{ON} = 2V, V_{FILTER} = 1V, No Faults V_{ON} = 0V, V_{FILTER} = 2V, In Reset Mode	●	1.5	2.4 8	3.3	µA mA
$V_{\overline{FAULT}(TH)}$	$\overline{FAULT}$ Pin Threshold Voltage	$V_{\overline{FAULT}}$ Falling	●	1.216	1.253	1.291	V
$\Delta V_{\overline{FAULT}(HYST)}$	$\overline{FAULT}$ Pin Hysteresis				10		mV
$I_{\overline{FAULT}(UP)}$	$\overline{FAULT}$ Pin Current	V_{ON} = 0V, $V_{\overline{FAULT}}$ = 1.5V	●	–3	–5	–7	µA
V_{OL}	Output Low Voltage ($\overline{RESET}$, $\overline{FAULT}$)	$I_{\overline{RESET}} = I_{\overline{FAULT}}$ = 1.6mA	●		0.15	0.4	V
$I_{\overline{RESET}(LEAK)}$	$\overline{RESET}$ Pin Input Leakage Current	$V_{\overline{RESET}} = V_{CC}$ = 6V			0	±10	µA
$t_{CB(TRIP)}$	Circuit Breaker Trip to Gate Discharging	(V_{SENSEP} - V_{SENSEN}) = Step 0V to 150mV (V_{SENSEP} - V_{SENSEN}) = Step 0V to 30mV, $V_{SENSEP} = V_{CC}$, FILTER = 10nF to GND	● ●	 120	1 240	3 360	µs µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{\overline{FAULT}(EXT)}$	$\overline{FAULT}$ Low to Gate Discharging	$V_{\overline{FAULT}}$ = Step 2V to 0V	●		10	20	µs
t_{FILTER}	FILTER High to Gate Discharging	V_{FILTER} = Step 0V to 2V	●		20	40	µs
$t_{RST(ONLO)}$	Circuit Breaker Reset Delay Time, ON Low to $\overline{FAULT}$ High	V_{ON} = Step 2V to 0V	●		30	60	µs
$t_{RST(VCCLO)}$	Circuit Breaker Reset Delay Time, V_{CC} Low to $\overline{FAULT}$ High	V_{ON} = 2V, V_{CC} = Step 3.3V to 1.8V	●		50	100	µs
t_{OFF}	Turn-Off Time, ON Low to GATE Discharging	V_{ON} = Step 2V to 0.6V			15		µs

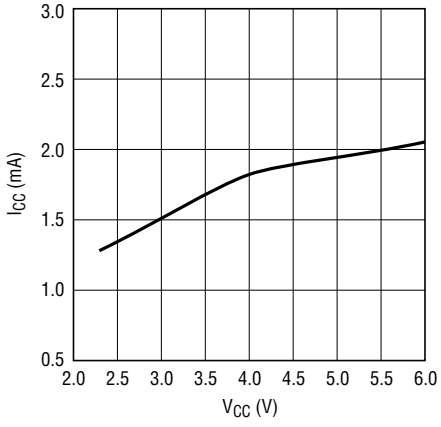
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of the device pins are negative; all voltages are referenced to GND unless otherwise specified.

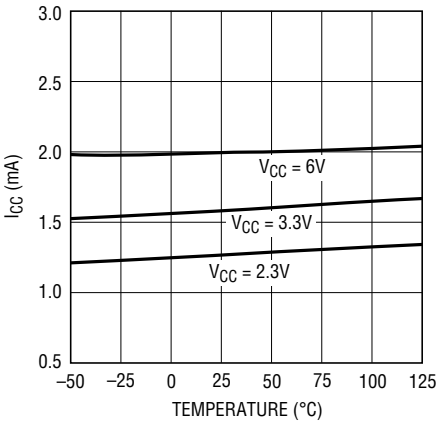
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C. V_{CC} = 3.3V, unless otherwise noted.

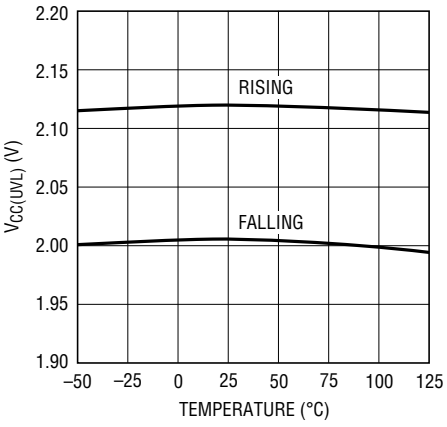
I_{CC} vs V_{CC}



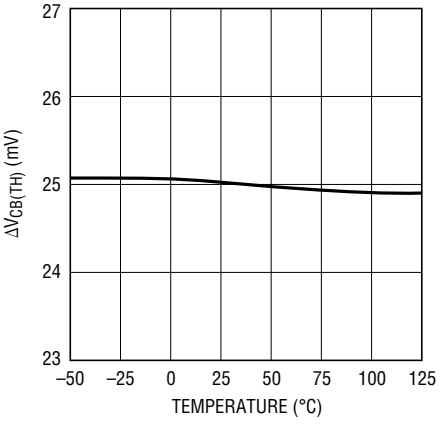
I_{CC} vs Temperature



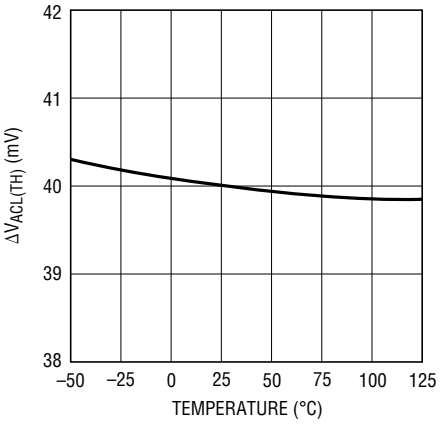
$V_{CC(UVL)}$ vs Temperature



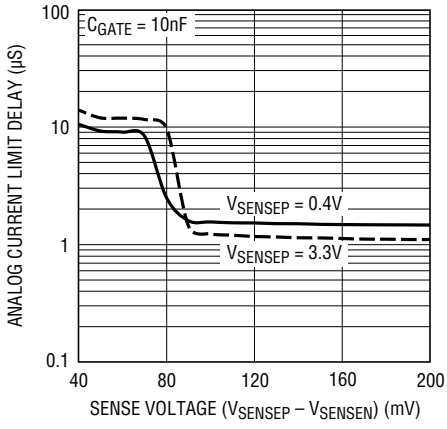
$\Delta V_{CB(TH)}$ vs Temperature



$\Delta V_{ACL(TH)}$ vs Temperature

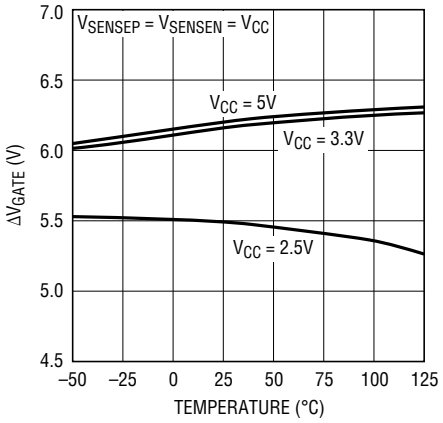


Analog Current Limit Delay vs Sense Voltage

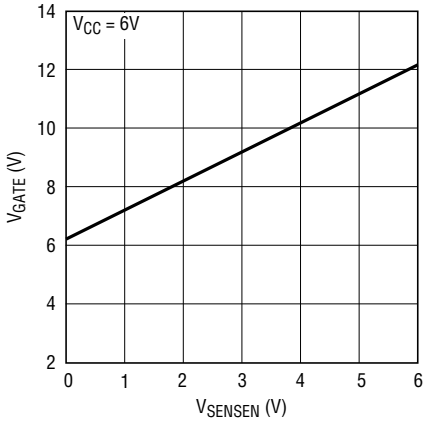


TYPICAL PERFORMANCE CHARACTERISTICS

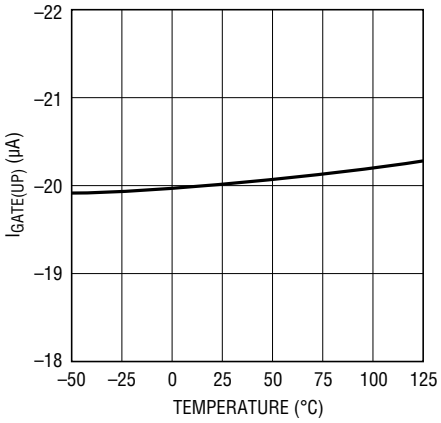
ΔV_{GATE} vs Temperature



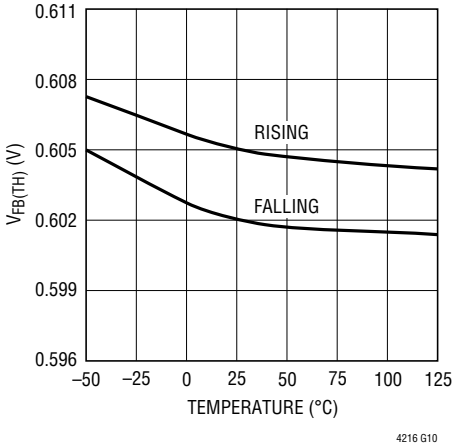
V_{GATE} vs V_{SENSEN}



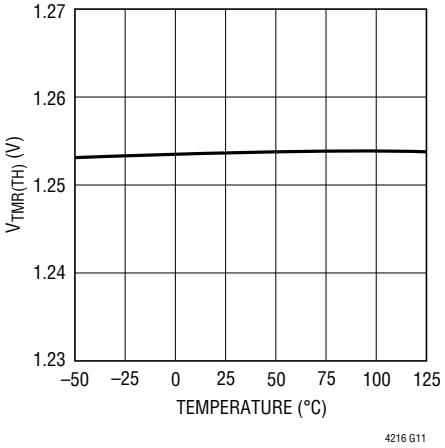
$I_{GATE(UP)}$ vs Temperature



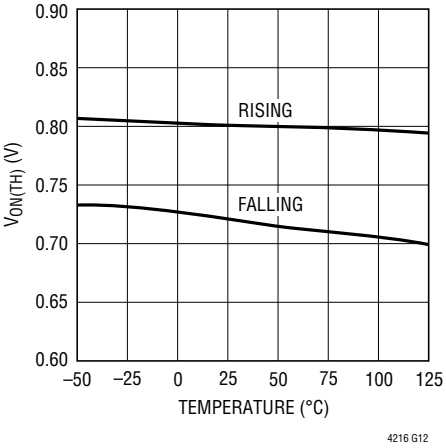
$V_{FB(TH)}$ vs Temperature



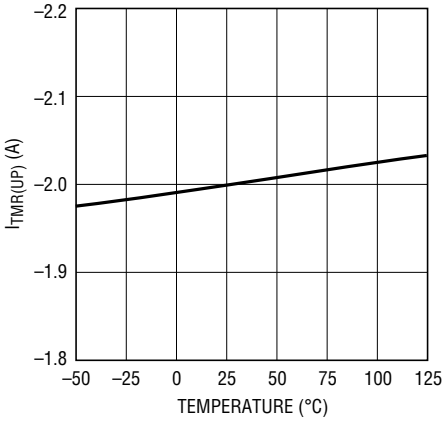
$V_{TMR(TH)}$ vs Temperature



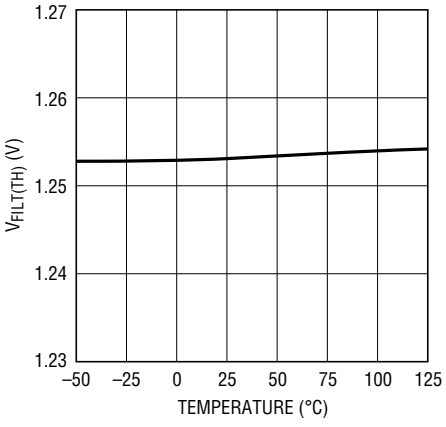
$V_{ON(TH)}$ vs Temperature



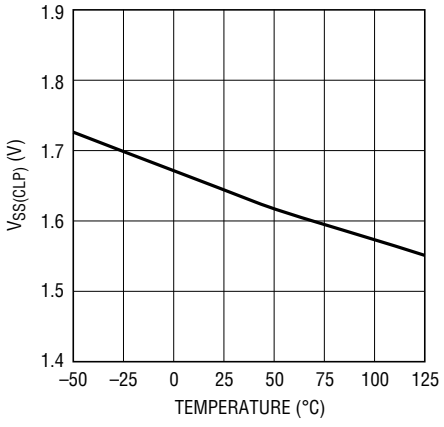
$I_{TMR(UP)}$ vs Temperature



$V_{FILT(TH)}$ vs Temperature

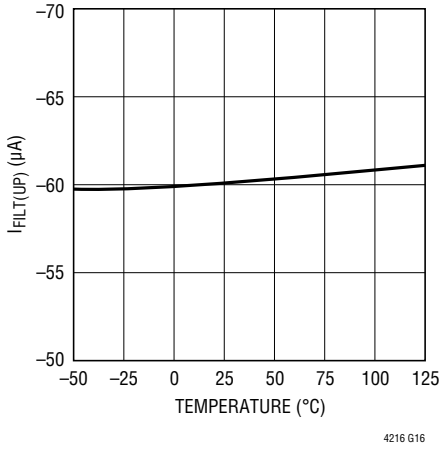


$V_{SS(CLP)}$ vs Temperature

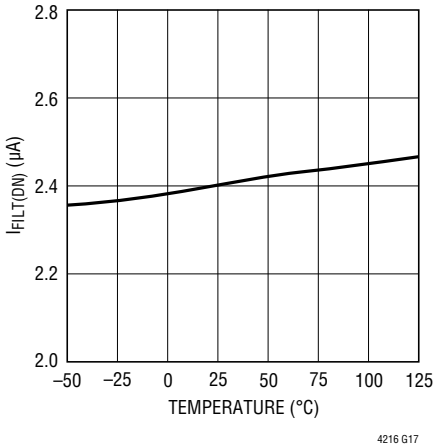


TYPICAL PERFORMANCE CHARACTERISTICS

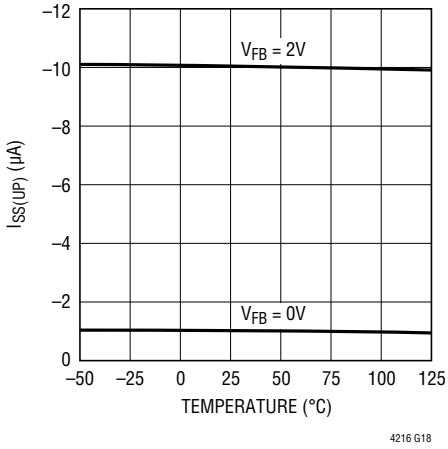
$I_{FILT(UP)}$ vs Temperature



$I_{FILT(DN)}$ vs Temperature



$I_{SS(UP)}$ vs Temperature



PIN FUNCTIONS (DE12/Package/MS Package)

$\overline{\text{RESET}}$ (Pin 1/Pin 1): Reset or Power-Good Output. Open drain output that pulls low if the FB pin voltage falls below its threshold (0.6V). During the start-up cycle, the $\overline{\text{RESET}}$ pin goes high impedance at the end of the second timing cycle after the FB pin goes above the FB threshold. This pin requires an external pull-up to a positive supply. If an undervoltage lockout condition occurs, the $\overline{\text{RESET}}$ pin pulls low and ignores the FB pin voltage.

ON (Pin 2/Pin 2): ON Control Input. A rising edge above the ON pin threshold (0.8V) initiates the start-up cycle and turns on the external N-channel MOSFET. A falling edge below 0.72V (80mV ON pin hysteresis) turns it off. If this pin is pulled below 0.4V, following a circuit breaker trip, it resets the electronic circuit breaker and fault latch.

FILTER (Pin 3/Pin 3): Fault Filter Input. Connect a capacitor between this pin and ground to set up the fault filter delay. This pin sources 60µA or sinks 2.4µA when the voltage across the sense resistor exceeds 25mV or drops below 25mV respectively. The filter comparator rising threshold is 1.253V.

TIMER (Pin 4/Pin 4): Timer Input. Connect a capacitor between this pin and ground to set up the start-up timing cycle duration. It also defines the $\overline{\text{RESET}}$ power-good delay from the instant the FB pin voltage exceeds 0.6V. This pin sources 2µA pull-up current during ramp up. The timer comparator rising threshold is 1.253V.

SS (Pin 5/Not Available): Soft-Start Control Input. Connect a capacitor between this pin and ground for soft-start during power-up. It controls the GATE ramp up, limiting the rate of change of the inrush current when the external MOSFET turns on. If soft-start function is not used, leave this pin unconnected.

GND (Pin 6/Pin 5): Device Ground.

FB (Pin 7/Pin 6): Output Monitor for Reset Output. A resistive divider from the external MOSFET's source terminal is tied to this pin. When the voltage at this pin drops below 0.6V, the $\overline{\text{RESET}}$ pin pulls low. The FB comparator falling threshold is 0.602V.

GATE (Pin 8/Pin 7): Gate Drive for External N-Channel MOSFET. An internal charge pump provides 20µA gate pull-up current and sufficient gate overdrive to the external MOSFET. An internal shunt regulator limits the GATE pin voltage to about 6.2V (typ) above the SENSEN pin voltage.

SENSEN (Pin 9/Pin 8): Circuit Breaker Negative Sense Input. Connect this pin to the sense resistor terminal wired to the drain of the external N-channel MOSFET. The sense

PIN FUNCTIONS (DE12/Package/MS Package)

resistor is placed in the power path between SENSEP and SENSEN pins to sense the output current. The electronic circuit breaker trips if the voltage across the sense resistor exceeds 25mV for more than a fault filter delay.

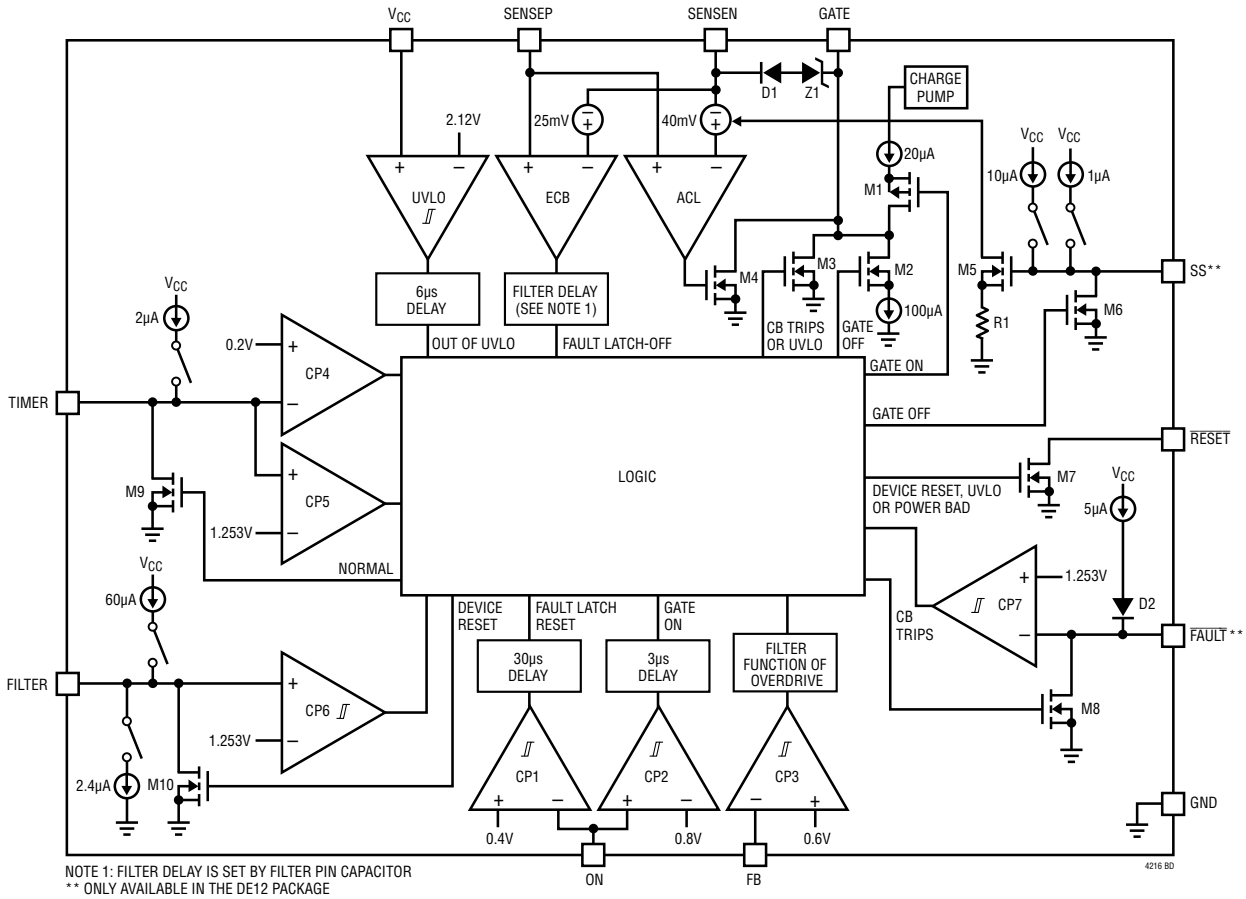
SENSEP (Pin 10/Pin 9): Circuit Breaker Positive Sense Input. Connect this pin to the sense resistor terminal wired to the positive supply input for the external output load. This positive supply range extends from 0V to 6V.

V_{CC} (Pin 11/Pin 10): Bias Supply Input. Operates from 2.3V to 6V. An internal undervoltage lockout circuit disables the device until the input supply voltage at V_{CC} exceeds 2.12V typically.

$\overline{FAULT}$ (Pin 12/Not Available): Fault Input and Output. As an input, driving this pin low (<1.253V) will latch-off the device to fault mode. As an output, it is either pulled high by an internal 5µA pull-up or an external pull-up resistor to positive supply under normal operating condition. It pulls low when the circuit breaker is tripped due to an overcurrent fault.

Exposed Pad (Pin 13/Not Available): Exposed pad may be left open or connected to device ground.

BLOCK DIAGRAM



OPERATION

The LTC4216 is a Hot Swap controller residing either on a removable circuit board or on the backplane. It monitors the current and protects the load with an external N-channel MOSFET and a current sensing resistor (see Figures 14 to 18). Both inrush current limiting and short-circuit protection are provided by the LTC4216. The device is powered via the bias supply input (V_{CC}) and it has a separate sense pin, SENSEP, to monitor the load supply (V_{IN}). The load supply can extend from 0V to 6V, with a minimum bias supply voltage of 2.3V.

When the ON pin is pulled from low to high, TIMER begins the first timing cycle by sourcing 2µA into C1 once these conditions are met: bias supply voltage out of undervoltage lockout (> 2.12V); TIMER, SS, FILTER and GATE pin voltages < 0.2V. When the C1 voltage rises above the TIMER pin threshold (1.253V), TIMER pulls low and releases both the SS and GATE pins. C2 starts to ramp up at the SS pin, controlling the rate of GATE ramp. This limits the rate of change of the inrush current flowing into the output load capacitance. $\overline{\text{RESET}}$ pin goes high after the second timing cycle when the FB pin voltage exceeds 0.6V and its hysteresis.

When the external MOSFET is fully turned on, the output will ramp to load supply voltage if the inrush into the load capacitance is low. However, if the inrush current exceeds the analog current limit of $\Delta V_{ACL(TH)}/R_{SENSE}$, the LTC4216 will ramp the output by sourcing the limited current into the load capacitance.

The LTC4216 provides protection against output short-circuits or current overload through an internal electronic circuit breaker with trip threshold of 25mV and an analog current limit circuit. The circuit breaker response time is set by C3 at the FILTER pin.

APPLICATIONS INFORMATION

Hot Circuit Insertion

When circuit boards are inserted into a live backplane, the supply bypass capacitors can draw huge transient current from the power bus as they charge. Potentially, the flow of current could damage the connector pins and glitch the power bus, causing other boards in the system to reset. The LTC4216 is designed to turn on or off a circuit board supply in a controlled manner, allowing insertion or removal without glitches or connector damage.

Overview of LTC4216 Features

1. Allows safe board insertion and removal from a live backplane.

2. Controls load voltages from 0V to 6V.

3. High side gate drive for external N-channel MOSFET.

4. Adjustable soft-start with inrush current limiting for large load capacitor during start-up.

5. Adjustable analog current limit (ACL) with circuit breaker fault time-out during an overcurrent fault condition. No external gate capacitor is required for the ACL loop compensation.

6. Electronic circuit breaker tripping at 25mV across the sense resistor. The response time is adjustable through an external capacitor at the FILTER pin.

7. Provides an ON pin to turn on and off the device. This can also be used to reset the device after a circuit breaker trip.

8. Provides output supply voltage monitoring through the FB pin and signals the $\overline{\text{RESET}}$ pin output.

9. Provides fault status output.

ON Control

The ON pin has two hysteretic comparators with different threshold levels (0.8V and 0.4V) and they serve two purposes:

1. Turn on the device if the ON pin voltage > 0.8V for more than 6µs and turn it off if the ON pin voltage < 0.72V for more than 15µs.

2. Reset the device if the ON pin voltage < 0.4V for more than 30µs after a circuit breaker trip.

There are various methods of setting the ON pin voltage:

1. Tie the ON pin to the load supply (V_{IN}) through a 10k pull-up resistor.

2. Drive the ON pin with an ON/OFF logic signal from the system controller.

3. Connect an external resistive divider at the ON pin. This divider can be used to set a higher value for the load supply undervoltage lockout voltage than the internal V_{CC} undervoltage lockout circuit.

For example, as shown in Figure 17, if both V_{CC} and SENSEP pins are connected to a 5V load supply, choosing the resistive divider values, R1 = 20k, R2 = 80.6k, turns on the device when the load supply voltage reaches around 80% of its final value.

V_{CC} Undervoltage Lockout

A hysteretic comparator, UVLO, monitors bias supply (V_{CC}) for undervoltage. The thresholds are defined by $V_{CC(UVL)}$ (2.12V) and its hysteresis, $\Delta V_{CC(UVL,HYST)}$ (120mV). When V_{CC} rises above $V_{CC(UVL)}$, the device is enabled. When V_{CC} falls below ($V_{CC(UVL)} - \Delta V_{CC(UVL,HYST)}$), the device is disabled and GATE is pulled low. If V_{CC} cycles below this threshold for more than 200µs, following a circuit breaker trip, it clears the fault latch. Any bias supply glitches that last less than 10µs will be rejected by the UVLO glitch filter.

Timer

An external capacitor, C1, is used at TIMER pin to provide two timing cycles for the LTC4216. The first timing cycle is the debounce cycle when the ON pin is first turned on, both the GATE and SS pins are held low and any short-circuit faults are ignored by the electronic circuit breaker. Second timing cycle is the power-good delay before the $\overline{\text{RESET}}$ pin goes high when the FB pin voltage exceeds 0.6V and its hysteresis.

The TIMER pin sources 2µA into C1 during the two timing cycles and is then pulled low by an internal N-channel

APPLICATIONS INFORMATION

switch when the TIMER pin voltage exceeds its threshold. The timer period for C1 to charge up to the TIMER pin threshold, $V_{TMR(TH)}$ (1.253V), is given by:

$$t_{TIMER} = \frac{1.253V \bullet C1}{2\mu A} \quad (1)$$

For example, if C1 = 10nF, t_{TIMER} = 6.2ms.

FB Glitch Filtering

The FB pin is used to monitor the output voltage of the external MOSFET through a resistive divider. Any transients on the FB pin due to the output low spikes will pull $\overline{RESET}$ low. To prevent $\overline{RESET}$ from generating an unwanted system reset, the FB comparator has a glitch filter to ride out these glitches. The filter time is 20µs for large transients (greater than 150mV) and up to 100µs for small transients. The relationship between glitch filter time and the FB pin transient voltage or FB overdrive is shown in Figure 1.

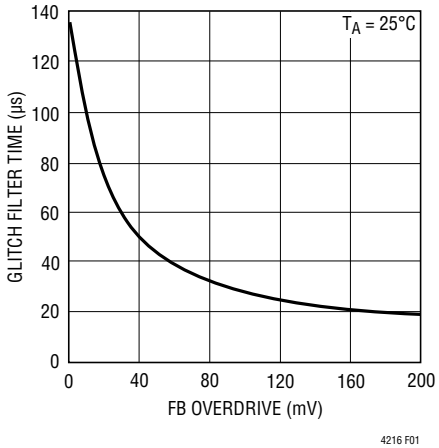


Figure 1. FB Comparator Glitch Filter Time vs FB Overdrive

Output Voltage Monitor

As shown in Figure 2, the output voltage is monitored through a resistive divider, R3 and R4, connected at the FB pin, and a FB comparator with 0.6V threshold.

The normal operation of the output voltage monitor after a start-up cycle is shown in Figure 3. At time point 1, when the FB pin voltage falls below 0.6V, the FB comparator output goes high. $\overline{RESET}$ is pulled low by an internal N-channel switch after a glitch filter delay at time point 2. When the FB pin voltage rises above 0.6V, the FB comparator output goes low and a new timing cycle starts. After a complete timing cycle at time point 6, $\overline{RESET}$ is pulled high by the external pull-up resistor, R5. The timer period given by Equation (1) sets the power-good delay for $\overline{RESET}$ going high. If the FB pin voltage stays above 0.6V for less than a timing cycle at time point 4, the $\overline{RESET}$ output remains low. Any overcurrent fault detected by the electronic circuit breaker or $\overline{FAULT}$ pin driven low externally during the timing cycle, will also pull the TIMER pin low and $\overline{RESET}$ output remains low.

When the device enters an undervoltage lockout condition or the ON pin voltage drops below 0.4V, $\overline{RESET}$ is pulled low, ignoring the FB pin voltage.

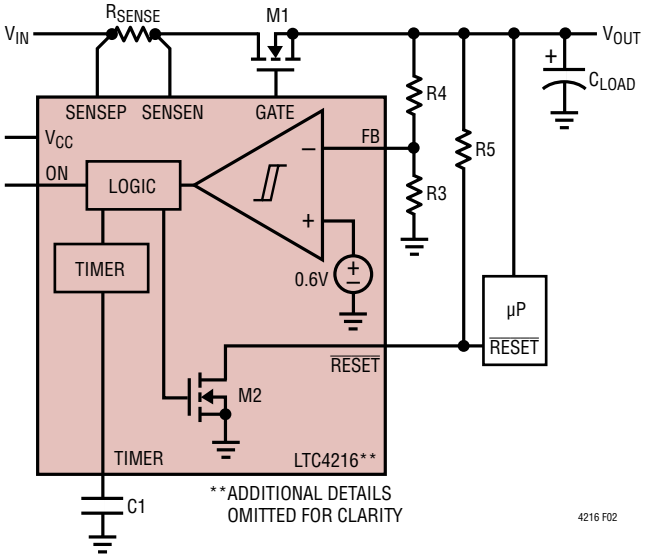


Figure 2. Output Voltage Monitor Block Diagram

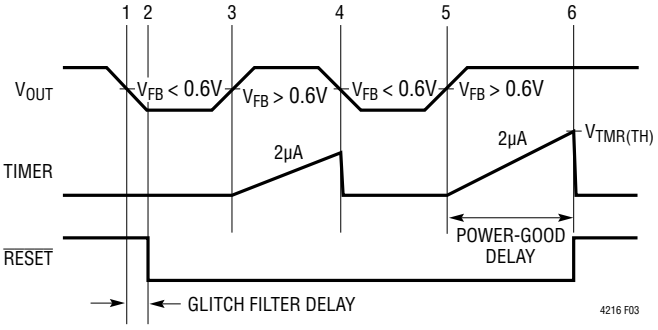


Figure 3. Output Voltage Monitor Waveforms in Normal Operation

APPLICATIONS INFORMATION

Electronic Circuit Breaker

The LTC4216 features an electronic circuit breaker function that protects the external MOSFET against short-circuits or excessive load current conditions on the supply. An external sense resistor connected between SENSEP and SENSEN pins is used to measure the load current. If the voltage across the sense resistor exceeds the circuit breaker trip threshold of 25mV for more than a fault filter delay, the gate of the MOSFET is pulled low, turning it off.

The fault filter delay is determined by a capacitor, C3, connected between the FILTER pin and ground as in Equation (2). The FILTER pin sources 60µA pull-up current when the sense voltage across the sense resistor exceeds 25mV. Otherwise, it pulls down with 2.4µA. When the FILTER pin voltage exceeds $V_{FILT(TH)}$ threshold (1.253V), there is an internal 20µs delay before the GATE pulls low and the $\overline{FAULT}$ pin will be pulled low. If no FILTER capacitor is used, the filter fault delay defaults to 20µs. The circuit breaker response time or fault filter delay with the FILTER capacitor, C3, is given by:

$$t_{CB(TRIP)} = \frac{1.253V \bullet C3}{60\mu A} + 20\mu s \quad (2)$$

The FILTER capacitor, C3, should be chosen so that the fault filter delay is not too short to trip the circuit breaker as the MOSFET current charges up a large output load capacitance in analog current limit during power-up. It also should not be too long to exceed the safe operating area (SOA) of the external MOSFET.

Intermittent overloads may exceed the current limit as in Figure 5, but if the duration is sufficiently short, the FILTER pin voltage may not reach the $V_{FILT(TH)}$ threshold and the device will not shut off. To handle this situation, the FILTER discharges with 2.4µA whenever voltage across the sense resistor is below 25mV. Any intermittent overload with an aggregate duty cycle of more than 4% will eventually trip the circuit breaker. Figure 6 shows the circuit breaker response time in seconds normalized to 1µF as given by Equation (3). The asymmetric charging and discharging of FILTER is a fair gauge of MOSFET heating.

$$\frac{t}{C3}(s/\mu F) = \frac{1.253}{(60 \bullet D) - 2.4} \quad (3)$$

Following a circuit breaker trip, the device is latched-off and $\overline{FAULT}$ is pulled low until the fault latch is cleared by pulling the ON pin low (< 0.4V) for at least 100µs. The FILTER pin is pulled low by an internal N-channel switch to discharge the capacitor quickly when the ON pin voltage falls below 0.4V and pulls down with 2.4µA when the ON pin voltage rises above 0.8V to initiate a new start-up cycle. The new timing cycle will not start until the FILTER pin voltage is below 0.2V. The electronic circuit breaker is disabled during the first timing cycle upon start-up and any short-circuit faults will be ignored.

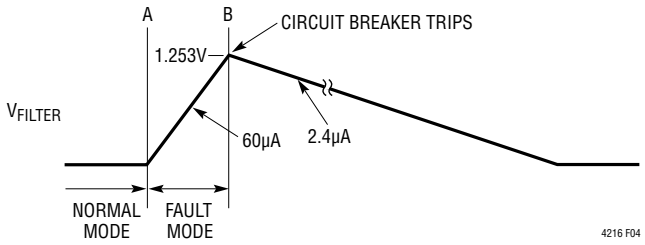


Figure 4. A Continuous Fault Timing

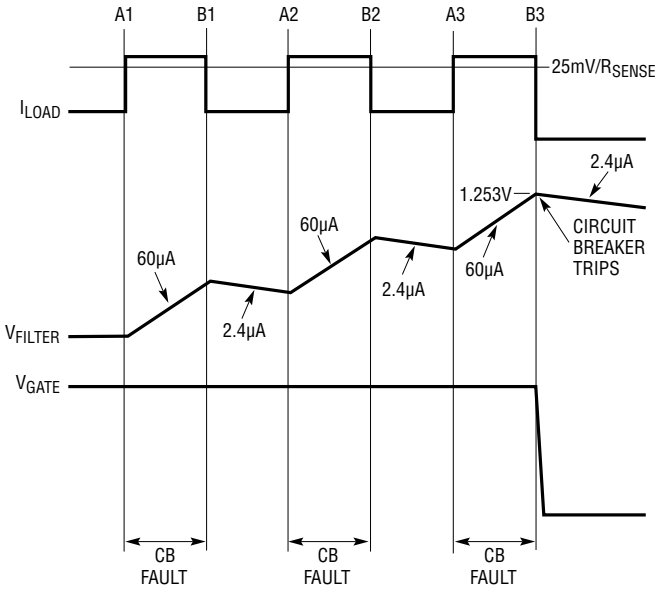


Figure 5. Multiple Intermittent Overcurrent Condition

APPLICATIONS INFORMATION

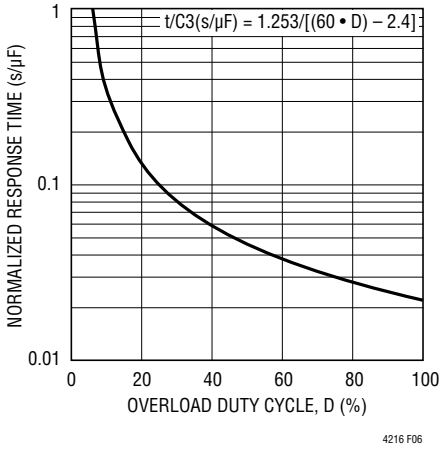


Figure 6. Circuit Breaker Filter Response for Intermittent Overload

Analog Current Limiting

In addition to an electronic circuit breaker, the LTC4216 has included a novel analog current limit (ACL) amplifier that does not require an external compensation capacitor at the GATE pin. The amplifier's stability is compensated by the large gate input capacitance (C_{ISS}) of the external MOSFET used. These MOSFETs usually have $C_{ISS} \geq 1nF$. However, if the MOSFET's gate input capacitance (C_{ISS}) is too small for loop stability, then connect an external capacitor between the GATE pin and ground to increase the total gate capacitance to ≥ 1nF. As given by Equation (4), the MOSFET current, I_{ACL}, is limited to the analog current limit voltage, $\Delta V_{ACL(TH)}$, 40mV typical, across the sense resistor, R_{SENSE}, connected between SENSEP and SENSEN pins.

$$I_{ACL} = \frac{\Delta V_{ACL(TH)}}{R_{SENSE}} \quad (4)$$

The $\Delta V_{ACL(TH)}$ threshold is 1.6 times higher than the $\Delta V_{CB(TH)}$ threshold (25mV typical) to provide dual level current sensing. When the ACL amplifier servos the MOSFET current at $\Delta V_{ACL(TH)}$ across the sense resistor, it exceeds $\Delta V_{CB(TH)}$ threshold causing the FILTER pin to charge C3 with 60μA pull-up. If the condition persists long enough for C3 to reach the $V_{FILT(TH)}$ threshold (1.253V), GATE is pulled low and $\overline{FAULT}$ latched low.

If the voltage across the sense resistor is greater than $\Delta V_{ACL(TH)}$ during an overload condition, the ACL amplifier will servo GATE downwards in an attempt to control the MOSFET current. Since the GATE pin voltage overdrives the MOSFET in normal operation, the ACL amplifier needs time to discharge the GATE to the threshold of the MOSFET for gate regulation. For mild overload, the ACL amplifier can control the MOSFET current, but in the event of a severe overload, the MOSFET current may overshoot as the MOSFET has large GATE overdrive initially. The GATE is quickly discharged to ground followed by the ACL amplifier taking control. For applications that require very fast analog current limit recovery from the GATE undershoot as it discharges, connect a series resistor, R_Z, with an external capacitor, C_Z, at the GATE pin as shown in Figure 17. The value of R_Z should be between 10Ω and 100Ω for optimum performance.

Soft-Start

The LTC4216 features a soft-start function that controls the di/dt of the inrush current during power-up. As large output load capacitors are commonly used in low voltage applications, the normal inrush can be large enough to glitch the load supply. With the soft-start function, the gate of the external MOSFET is allowed to turn on very gradually to control the inrush current flowing into the load capacitor without causing a supply glitch.

With an external capacitor, C2, connected between the SS pin and ground, the GATE is servoed by the ACL amplifier to track the rate of SS ramp-up during power-up. There are two slopes in the SS ramp-up profile: 10μA current source pull-up for a normal ramp rate; and 1μA current source pull-up for a slower ramp rate. Both the SS ramp rates are given as follows:

$$\text{Normal SS Ramp Rate: } \frac{dV_{SS(NOM)}}{dt} = \frac{10\mu A}{C2} \quad (5)$$

$$\text{Slower SS Ramp Rate: } \frac{dV_{SS(SLOW)}}{dt} = \frac{1\mu A}{C2} \quad (6)$$

APPLICATIONS INFORMATION

For example, if C2 = 10nF, $\frac{dV_{SS(NOM)}}{dt}$ = 1V/ms and $\frac{dV_{SS(SLOW)}}{dt}$ = 0.1V/ms.

After the initial timing cycle, the SS capacitor is charged by a 10µA current source pull-up and GATE is held low by the ACL amplifier. As SS ramps up, the ACL amplifier releases the GATE when it crosses its input offset voltage. At this instant, SS switches the pull-up current from 10µA to 1µA for a slower ramp rate. GATE continues to charge up with 20µA pull-up before the MOSFET reaches its turn-on threshold voltage. When the external MOSFET is first turned on, there is always a current step due to the high gain of the MOSFET. The slower SS ramp rate allows the gate of the external MOSFET to be turned on with a smaller inrush current step.

When the external MOSFET is turned on, load current starts to flow through the sense resistor, developing a voltage drop across it. This allows the ACL amplifier to servo the GATE to the voltage across the sense resistor, thus controlling the rate of change of the inrush current. At this instant, SS switches back from 1µA to 10µA current source pull-up for a normal ramp rate. GATE continues to ramp up as the ACL amplifier servos to track the SS ramp rate. At the end of SS ramp-up when SS reaches its final value, GATE is servoed to $\Delta V_{ACL(TH)}$ across the sense resistor. If the voltage across the sense resistor drops below $\Delta V_{ACL(TH)}$ due to a falling load current, the ACL amplifier shuts off and GATE ramps further by a 20µA pull-up.

SS is pulled low under any of the following conditions: in V_{CC} undervoltage lockout condition, during the first timing cycle or when the circuit breaker fault times out. If the soft-start function is not used, leave the SS pin unconnected.

Inrush Control with GATE Capacitor

For applications not requiring soft-start to control the di/dt of the inrush current during power-up, an alternative way to limit the inrush is to control the GATE pin voltage slew rate by connecting an external capacitor, C4, from the GATE pin to ground, as shown in Figure 7. An external resistor, R_G, of 10Ω prevents high frequency self-oscillations in the MOSFET. The GATE slew rate is given by:

$$\frac{dV_{GATE}}{dt} = \frac{20\mu A}{C4 + C_{GATE}} \quad (7)$$

where C_{GATE} is the associated parasitic GATE capacitance due to the external MOSFET's gate input capacitance, C_{ISS}.

The inrush current flowing into the load capacitor, C_{LOAD}, is limited to:

$$I_{INRUSH} = C_{LOAD} \bullet \frac{dV_{GATE}}{dt} = \frac{C_{LOAD}}{C4 + C_{GATE}} \bullet 20\mu A \quad (8)$$

For example, if C_{LOAD} = 4700µF, C4 = 33nF and C_{GATE} = 5nF, I_{INRUSH} = 2.5A.

If C_{LOAD} is very large and I_{INRUSH} exceeds the analog current limit, the GATE is servoed to control the inrush current to $\Delta V_{ACL(TH)}/R_{SENSE}$.

One limitation with this technique is that it slows down the system turn-on and turn-off time by adding a capacitor at the GATE pin. Should this technique be used, C4 ≤ 50nF is recommended. However, having an external gate capacitor helps to eliminate voltage spikes coupled through the MOSFET's drain-to-gate capacitance to the GATE pin when the supply power is first applied.

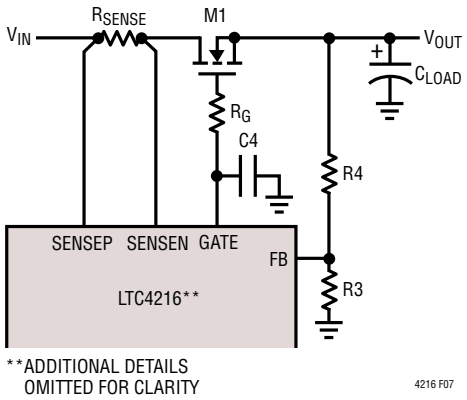


Figure 7. Inrush Control with External Gate Capacitor

APPLICATIONS INFORMATION

Normal Power-Up and Power-Down

Figure 8 illustrates the timing diagram for a normal power-up sequence in the case where a printed circuit board is inserted into a live backplane.

At time point 1, the bias supply (V_{CC}) ramps up and enables the device when the supply voltage rises above the undervoltage lockout threshold (2.12V). At time point 2, SENSEP supply, together with the ON pin, ramp up and start the first timing cycle when the ON pin voltage exceeds 0.8V. The TIMER capacitor is allowed to ramp up with 2µA pull-up once all these conditions are met: GATE < 0.2V, FILTER < 0.2V, TIMER < 0.2V, SS < 0.2V. At time point 3, TIMER reaches the $V_{TMR(TH)}$ threshold and the first timing cycle terminates. The electronic circuit breaker is enabled and TIMER capacitor is quickly discharged. At time point 4 checks are made for TIMER, GATE, FILTER and SS < 0.2V, ΔV_{SENSE} below 25mV and $\overline{FAULT}$ high before a GATE ramp-up cycle begins. GATE is held low by the analog current limit amplifier as SS capacitor ramps up with a 10µA current source. SS switches to 1µA pull-up for a slower ramp rate when it crosses the input offset voltage of the ACL amplifier. At this time point, the ACL amplifier releases the GATE and allows it to ramp up with a 20µA pull-up. At time point 6, when the GATE voltage reaches the turn-on threshold of the external MOSFET, current begins flowing into the load capacitor. The MOSFET current level at this time point is controlled by the ACL amplifier and the GATE ramp is slowed down. SS switches the pull-up current from 1µA to 10µA for a normal ramp rate. Between time points 6 and 7, the ACL amplifier servos the GATE voltage to track the SS ramp rate, limiting the slew rate of the load current. At time point 7, SS reaches its final value and GATE continue to ramp up with the 20µA pull-up if the load current is not in analog current limit. At time point 8, the FB pin voltage exceeds 0.6V and the second timing cycle is started. When the conditions of TIMER < 0.2V, ΔV_{SENSE} < 25mV and $\overline{FAULT}$ high are met, the TIMER capacitor is allowed to ramp up. When TIMER reaches the $V_{TMR(TH)}$ threshold at time point 9, $\overline{RESET}$ goes high, indicating to the system controller that power is good. After this, the TIMER is held low.

When the ON pin voltage falls below ($V_{ON(TH)} - \Delta V_{ON(HYST)}$) threshold (0.72V), it initiates a power-down sequence. At time point 11, GATE is discharged by both the ACL amplifier and a 100µA current source pull-down, causing the output voltage to fall gradually. When the FB pin voltage falls below 0.6V at time point 12, $\overline{RESET}$ goes low after a glitch filter delay (see the section on FB glitch filtering), indicating that power is bad. When the ON pin voltage falls below 0.4V, the device resets and GATE is pulled low by a strong pull-down device.

Soft-Start with Analog Current Limiting

When a very large output load capacitor is connected during soft-start, the GATE voltage is servoed to regulate the inrush current to $\Delta V_{ACL(TH)}/R_{SENSE}$. This is illustrated in the timing diagram of Figure 9. After the initial timing cycle, the GATE is allowed to ramp up, tracking the SS ramp rate between time points 5 and 8. At time point 7, when the load current builds up as the GATE pin voltage increases, the voltage across the sense resistor rises above $\Delta V_{CB(TH)}$ (25mV typical). The FILTER capacitor starts to charge up by a 60µA current source pull-up. At time point 8, SS reaches its final value at the end of SS ramp cycle. This allows the GATE to be regulated by the ACL amplifier at $\Delta V_{ACL(TH)}$ (40mV typical) across the sense resistor, R_{SENSE}, limiting the inrush to:

$$I_{LIMIT} = \frac{40mV}{R_{SENSE}} \quad (9)$$

The FILTER pin voltage continues to rise as the load capacitor charges up with the limited load current. At time point 9, the FB pin voltage exceeds 0.6V, but the second timing cycle is not allowed to start as the voltage across the sense resistor exceeds 25mV. At time point 10, the load current falls as the load capacitor is near full charge and the voltage across the sense resistor drops below 40mV. The analog current limit loop shuts off and the GATE ramps further till its final value. The FILTER capacitor discharges by a 2.4µA pull-down when the voltage across the sense resistor falls below 25mV at time point 11. The duration between time points 7 and 11 must be shorter than one circuit breaker delay, as given by Equation (2), to avoid a fault time-out during GATE ramp-up for very large load

APPLICATIONS INFORMATION

capacitors. A second timing cycle starts at time point 11 when the FB pin voltage exceeds 0.6V and the voltage across the sense resistor drops below 25mV.$\overline{\text{RESET}}$ goes high at the end of the second timing cycle (time point 12) when TIMER reaches the $V_{TMR(TH)}$ threshold.

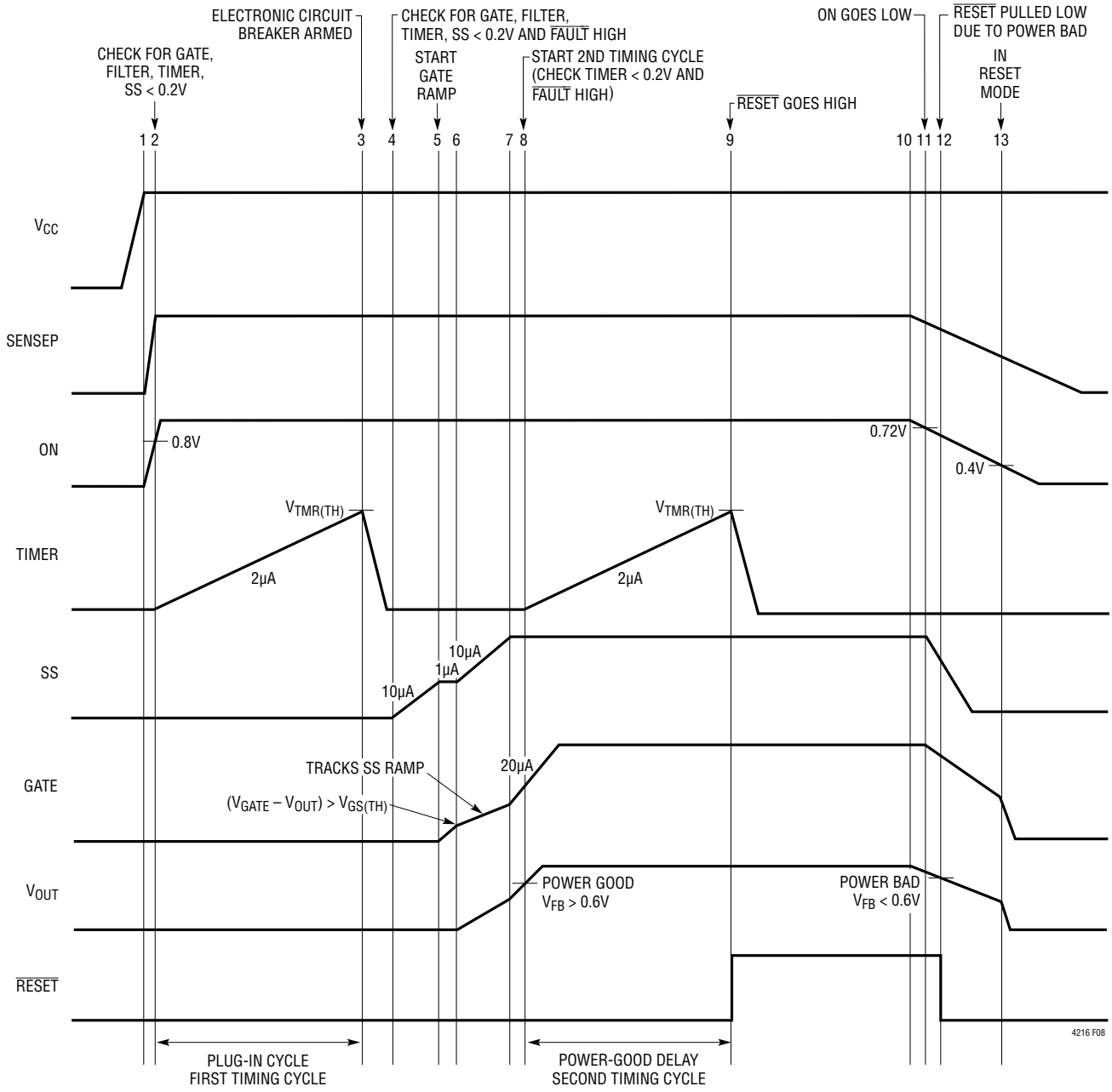


Figure 8. Normal Power-Up/Power-Down Sequence

APPLICATIONS INFORMATION

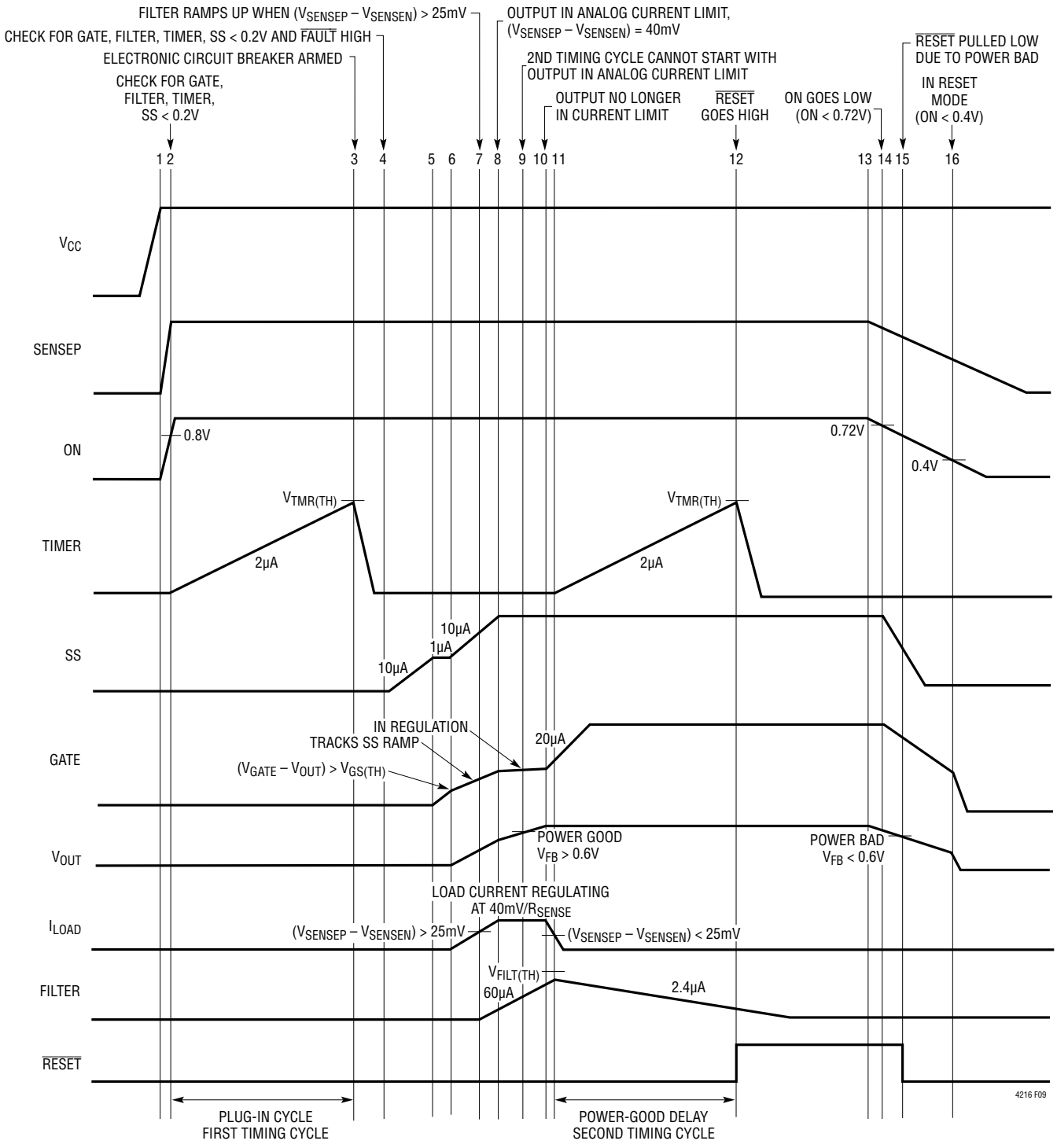


Figure 9. Normal Power-Up Sequence (with Analog Current Limiting)

APPLICATIONS INFORMATION

Power-Up into an Output-Short

Figure 10 shows the timing diagram in the case when the output is a dead short during power-up. As GATE ramps up at time point 6, the MOSFET current increases due to the output short causing the voltage drop across the sense resistor to rise above 25mV. FILTER sources 60µA, charging the external capacitor. At time point 7, GATE regulates to limit the output current to 40mV/R_{SENSE}. If the output continues to be in analog current limit when the FILTER pin voltage reaches its threshold (1.253V) at time point 8, the circuit breaker trips and GATE is pulled low. The device latches-off and $\overline{FAULT}$ is pulled low, indicating a fault condition. The FILTER capacitor discharges through a 2.4µA pull-down until the device resets.

Resetting the Electronic Circuit Breaker

When the LTC4216's electronic circuit breaker is tripped during a fault condition, $\overline{FAULT}$ is asserted low and the $\overline{RESET}$, SS and GATE pins are all pulled to ground. This is shown in the timing diagram of Figure 11. The LTC4216 remains latched-off until the external fault is cleared. To clear the internal fault latch and restart the device, pull the ON pin low (< 0.4V) at time point 4 for at least 100µs, after which the $\overline{FAULT}$ will go high at time point 5. Toggling the ON pin from low to high (> 0.8V) initiates a new start-up cycle.

Sense Resistor Considerations

The circuit breaker trip threshold of 25mV and the value of the sense resistor, R_{SENSE}, connected between the SENSEP and SENSEN pins, determine the trip current level as given by Equation (10). If the fault current level exceeds the analog current limit, the current is limited to a value given by Equation (11). Should the overload condition exist for more than one fault filter delay as given by Equation (2), the circuit breaker trips and the device is latched-off.

$$I_{TRIP(CB)} = \frac{\Delta V_{CB(TH)}}{R_{SENSE}} = \frac{25mV}{R_{SENSE}} \quad (10)$$

$$I_{ACL} = \frac{\Delta V_{ACL(TH)}}{R_{SENSE}} = \frac{40mV}{R_{SENSE}} \quad (11)$$

For a new circuit design, the sense resistor value is first calculated from the maximum operating load current under normal conditions and the minimum circuit breaker trip threshold. This is given by:

$$R_{SENSE} = \frac{\Delta V_{CB(TH,MIN)}}{I_{LOAD(MAX)}} = \frac{21.5mV}{I_{LOAD(MAX)}} \quad (12)$$

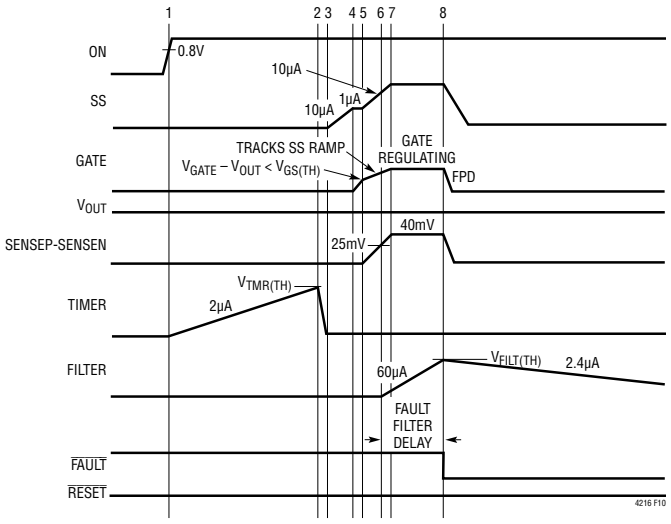


Figure 10. Power-Up into an Output-Short and Circuit Breaker Trips

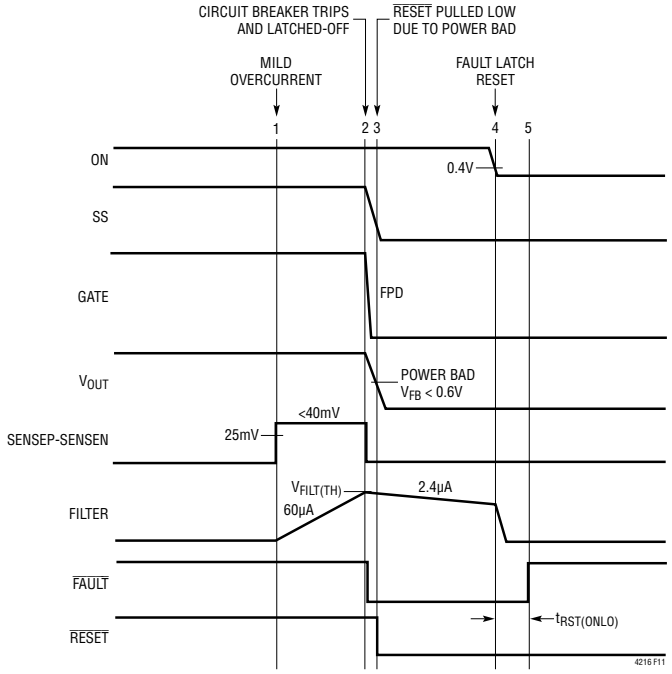


Figure 11. Mild Overcurrent Circuit Breaker Trips Followed by Device Reset

APPLICATIONS INFORMATION

For example, if $I_{LOAD(MAX)}$ = 5A, R_{SENSE} = 4.3mΩ. The nearest standard value is 4mΩ.

For proper circuit breaker operation, kelvin-sense PCB connections between the sense resistor and the LTC4216's SENSEP and SENSEN pins are strongly recommended. Figure 12 illustrates the correct way of making connections between the LTC4216 and the sense resistor. PCB layout should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistor should include good thermal management techniques for optimal sense resistor power dissipation.

The power rating of the sense resistor should accommodate the fault current level during analog current limit so that the component is not damaged before the circuit breaker trips.

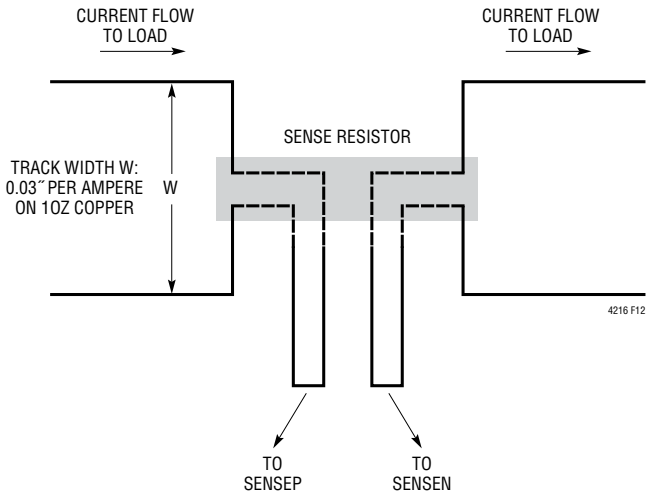


Figure 12. Making PCB Connections to the Sense Resistor

Circuit Breaker Trip Current Calculation

For a selected R_{SENSE} value, the typical load current that trips the circuit breaker is given by:

$$I_{TRIP(TYP)} = \frac{\Delta V_{CB(TH,TYP)}}{R_{SENSE(TYP)}} = \frac{25mV}{R_{SENSE(TYP)}} \quad (13)$$

The minimum load current that trips the circuit breaker is given by:

$$I_{TRIP(MIN)} = \frac{\Delta V_{CB(TH,MIN)}}{R_{SENSE(MAX)}} = \frac{21.5mV}{R_{SENSE(MAX)}} \quad (14)$$

where

$$R_{SENSE(MAX)} = R_{SENSE(TYP)} \bullet \left(1 + \frac{R_{TOL}}{100}\right)$$

The maximum load current that trips the circuit breaker is given by:

$$I_{TRIP(MAX)} = \frac{\Delta V_{CB(TH,MAX)}}{R_{SENSE(MIN)}} = \frac{28.5mV}{R_{SENSE(MIN)}}$$

where (15)

$$R_{SENSE(MIN)} = R_{SENSE(TYP)} \bullet \left(1 - \frac{R_{TOL}}{100}\right)$$

For example, if a sense resistor of 4mΩ ± 1% R_{TOL} is used for current sensing, the typical trip current, $I_{TRIP(TYP)}$ = 6.25A. From Equations (14) and (15), $I_{TRIP(MIN)}$ = 5.3A and $I_{TRIP(MAX)}$ = 7.2A respectively.

For proper operation and to avoid tripping the circuit breaker unnecessarily, the minimum trip current, $I_{TRIP(MIN)}$, must exceed the maximum operating load current of the circuit connected to the output of the MOSFET.

MOSFET Selection

The external MOSFET switch must have adequate safe operating area (SOA) to handle short-circuit conditions before the circuit breaker trips. These considerations take precedence over continuous drain current ratings. A MOSFET with adequate SOA for a given application can always handle the required drain current, but the opposite may not be true. Consult the manufacturer's MOSFET data sheet for safe operating area and effective transient thermal impedance curves.

MOSFET selection is a 3-step process by assuming the absence of a soft-start capacitor. First, R_{SENSE} is chosen and then the time required to charge the load capacitance is determined. This timing, along with the maximum short-circuit current and maximum load supply voltage, defines an operating point that is checked against the MOSFET's SOA curve.

In addition, consider three other key parameters:

APPLICATIONS INFORMATION

1. Maximum drain-to-source voltage, $V_{DS(MAX)}$

The $V_{DS(MAX)}$ rating must exceed the maximum load supply voltage including spikes and ringing.

2. Gate-to-source voltage, V_{GS}, overdrive

The absolute maximum rating for V_{GS} is typically ±8V for "logic level" and "sub-logic level" MOSFETs.

3. Drain-to-source resistance, $R_{DS(ON)}$

The $R_{DS(ON)}$ should be low for low voltage applications to allow its drain-to-source voltage, $V_{DS(ON)}$, to be a very small percentage of the supply voltage.

To begin a design, first specify the maximum operating load current and load capacitance. Calculate the R_{SENSE} value from Equation (12). The minimum trip current, $I_{TRIP(MIN)}$, given by Equation (14) should be set to accommodate the maximum operating load current.

During the start-up cycle, the LTC4216 may operate the MOSFET in analog current limit, forcing $\Delta V_{ACL(TH)}$ between 32mV to 48mV across R_{SENSE}. The minimum inrush current given by Equation (16) is calculated using the minimum $\Delta V_{ACL(TH)}$ and maximum R_{SENSE} value.

$$I_{INRUSH(MIN)} = \frac{\Delta V_{ACL(TH,MIN)}}{R_{SENSE(MAX)}} = \frac{32mV}{R_{SENSE(MAX)}} \quad (16)$$

The maximum short-circuit current given by Equation (17) is calculated using the maximum $\Delta V_{ACL(TH)}$ and minimum R_{SENSE} value.

$$I_{SHORT-CIRCUIT(MAX)} = \frac{\Delta V_{ACL(TH,MAX)}}{R_{SENSE(MIN)}} = \frac{48mV}{R_{SENSE(MIN)}} \quad (17)$$

Select the FILTER capacitor, C3, based on the slowest expected charging rate; otherwise, FILTER might time-out before the load capacitor is fully charged. A value for C3 is calculated based on the maximum time it takes the load capacitor, C_{LOAD}, to charge to its maximum value of load supply ($V_{IN(MAX)}$). That time is given by:

$$t_{CHARGE(LOAD)} = \frac{C_{LOAD} \bullet V_{IN(MAX)}}{I_{INRUSH(MIN)}} \quad (18)$$

Rearranging Equation (2) for the circuit breaker response time, the FILTER capacitor, C3, is given by:

$$C3 = \frac{(t_{CHARGE(LOAD)} - 20\mu s) \bullet 60\mu A}{1.253V} \quad (19)$$

Returning to Equation (2), the circuit breaker response time is calculated with a chosen C3 and used in conjunction with $V_{IN(MAX)}$ and $I_{SHORT-CIRCUIT(MAX)}$ to check the SOA curves of a prospective MOSFET.

As a numerical design example for the Typical Application, consider $V_{IN(MAX)}$ = 1.8V + 5%, maximum operating load current = 5A, C_{LOAD} = 1000µF. Equation (12) gives R_{SENSE} = 4.3mΩ. Choose R_{SENSE} = 4mΩ ± 1% tolerance. From Equations (14) and (16), $I_{TRIP(MIN)}$ = 5.3A (> $I_{LOAD(MAX)}$ = 5A) and $I_{INRUSH(MIN)}$ = 7.9A respectively. Equation (19) gives C3 = 10nF. To account for errors in C3, FILTER current (60µA) and FILTER threshold (1.253V), the calculated value should be multiplied by 1.5, giving the nearest standard value of C3 = 18nF.

If a short-circuit occurs, a current of up to $I_{SHORT-CIRCUIT(MAX)}$ = 12.1A will flow through the MOSFET for 400µs as dictated by C3 = 18nF in Equation (2). The MOSFET must be selected based on this criterion and checked against the SOA curve.

V_{CC} Supply RC Network

The LTC4216 has two separate pins, V_{CC} and SENSEP, for supply input and sensing:

1. V_{CC} pin for powering the internal circuitry.

2. SENSEP pin, together with the SENSEN pin, for sensing the current flowing from the load supply through the external sense resistor and N-channel MOSFET to the output load.

In most Hot Swap devices, V_{CC} and SENSEP are one common pin, providing the device's supply and external MOSFET's current sensing. However, supply dips due to output short can potentially trigger the device into an undervoltage lockout condition, causing the device to disable and its internal latches to reset.

As bypass capacitors are not allowed on the powered supply side of the external MOSFET switch residing on

APPLICATIONS INFORMATION

the plug-in boards, the LTC4216 provides two separate pins for bias supply input and load supply sensing. With this configuration, an RC network, R_Y and C_Y, shown in Figure 13, can be used with the V_{CC} pin to ride out supply glitches during output short or adjacent board short. The RC network shown has a time constant of 7µs and this is good enough for the supply to ride out most supply glitches, preventing the device from entering an undervoltage lockout condition unnecessarily. When V_{CC} and SENSEP pins are connected together, the R_Y value should be chosen such that V_{CC} pin voltage is lower than V_{SENSEP} – 70mV; otherwise, part of V_{CC} pin current will be diverted through SENSEP pin.

This unique scheme of separating the device's supply input and sensing also provides the flexibility of operating the load supply from ground to its supply rail with a minimum bias supply voltage of 2.3V. For proper operation, the load supply is required to be equal to or less than the bias supply voltage (maximum 6V).

Supply Transients Protection

There are two methods used in most applications to eliminate supply transients:

1. Transient voltage suppressor to clip the transient to a safe level.

2. Snubber (series RC) network.

For applications with load supply voltages of 3.3V or higher, the ringing and overshoot during hot-swapping or output short-circuit events can easily exceed the absolute maximum rating of the LTC4216. To minimize the risk, a transient voltage suppressor and snubber network are highly recommended at the SENSEP pin. For applications with load supply voltages of 2.5V or below, usually a snubber network is adequate to reduce the supply ringing.

Figure 13 shows the connections of the supply transient protection devices, Z1, R_X and C_X, around the LTC4216. The RC network, R_Y and C_Y, at the V_{CC} pin also serve as a snubber circuit for the load supply (V_{IN}). On the PCB layout, these transient protection devices should be mounted very close to the LTC4216's load supply rail using short lead lengths to minimize lead inductance.

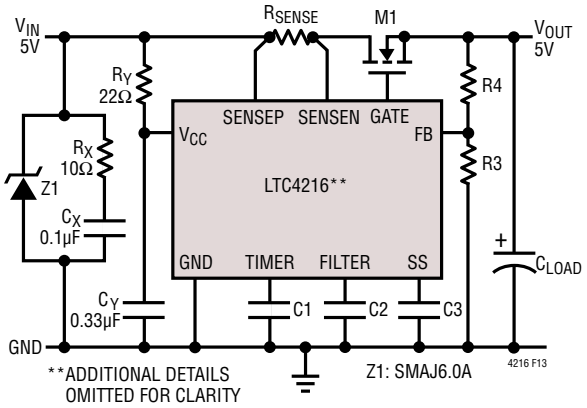


Figure 13. Connecting Transient Protection Devices to the LTC4216's Load Supply Rail

Staggered Pins Connections

The LTC4216 can be used on either the backplane side of the connector or a printed circuit board, and examples for both are shown in Figure 14 and 15. Printed circuit board edge connectors with staggered pins are recommended as the insertion and removal of circuit boards will sequence the pin connections. Supplies (V_{CC} and SENSEP) and ground connections on the printed circuit board should be wired to the long pins or blades of the edge connector. Control signal (ON) and status signals ($\overline{RESET}$ and $\overline{FAULT}$) passing through the edge connector should be wired to short pins or blades.

Backplane and PCB Connection Sensing

The LTC4216's ON pin can be used in various ways to detect whether the printed circuit board is seated properly in the backplane connector before the LTC4216 begins a start-up cycle.

An example is shown in Figure 14, in which the LTC4216 is mounted on the PCB and the R1/R2 resistive divider is connected to the ON pin. On the edge connector, R2 is wired to a short pin. Before the connectors are mated, the ON pin is held low by R1, keeping the LTC4216 in an off state. When the connectors are mated, the resistive divider is connected to the load supply (V_{IN}) and the ON pin voltage rises above 0.8V, turning the LTC4216 on.

APPLICATIONS INFORMATION

An example with LTC4216 mounted on the backplane is shown in Figure 15. In this case, the NPN transistor, Q1, and two resistors, R7 and R8, form the PCB connection sensing circuit with the ON pin. With the PCB out of the backplane connector, Q1 base is tied to load supply through R7, turning Q1 on and pulling the LTC4216's ON pin low. The base of Q1 is also wired to the backplane connector pin. When the PCB is inserted into the backplane, Q1 base is grounded through a short pin connection on the PCB. This turns off Q1 and the LTC4216's ON pin is allowed to pull high to the load supply through R8, turning it on.

In the previous examples, the PCB connection sensing circuits are not wired with interrupt capability from the system controller. As shown in Figure 16, adding logic-level discrete N-channel MOSFETs, M2 and M3, and a couple of resistors allow interrupt control to the sensing circuit. M2 is held on by its gate, pulling high through R8 to the load supply until the PCB is mated firmly to the backplane connector. A low logic-level for both the $\overline{ON}$/RST and $\overline{ON}$/OFF signals turns M2 and M3 off, allowing the ON pin to be pulled high and turning LTC4216 on. A high logic-level for the $\overline{ON}$/OFF signal turns off the device and pulls the GATE low. The device is reset by pulling the $\overline{ON}$/RST signal high.

5V Hot Swap Application

Figure 17 shows a Hot Swap application circuit with V_{CC} and SENSEP pins connected together to a 5V load supply (V_{IN}). The resistive divider, R1/R2, sets the undervoltage threshold for the load supply and allows the system to start up only after the supply voltage rises above 4V. The resistive divider, R3/R4, monitors V_{OUT} and signals

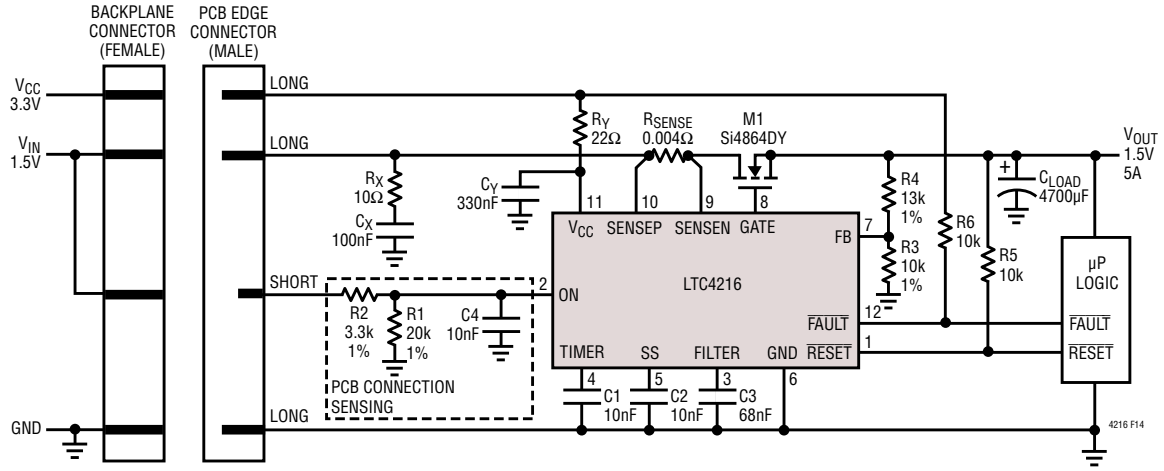


Figure 14. Single Channel 1.5V Hot Swap Controller

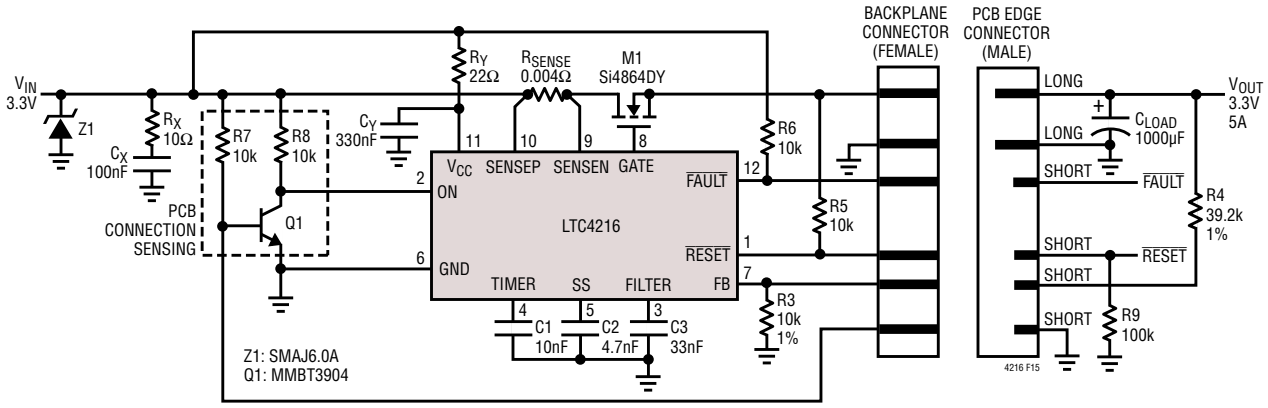


Figure 15. Hot Swap Controller on Backplane with Staggered Pin Connections

APPLICATIONS INFORMATION

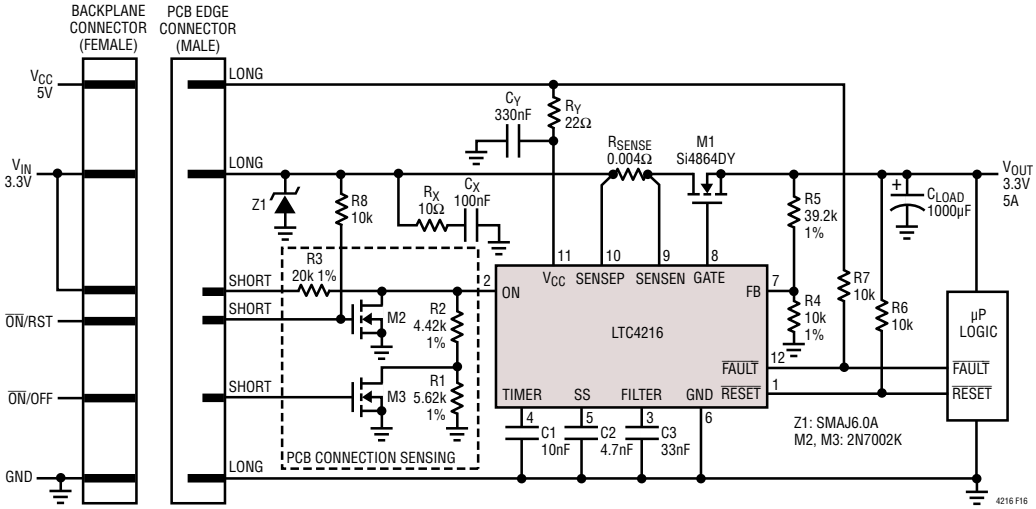


Figure 16. PCB Connection Sensing with ON/OFF Control

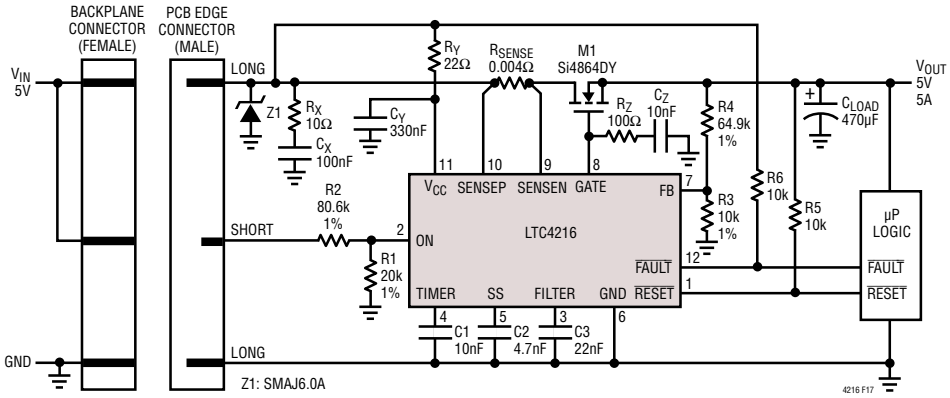


Figure 17. 5V Hot Swap Application

the $\overline{\text{RESET}}$ high when V_{OUT} rises above 4.5V. Transient voltage suppressor, Z1, and snubber network, R_X and C_X, connected at SENSEP pin are highly recommended to protect the 5V supply system from ringing and voltage spikes during a fault condition. The RC network, R_Y and C_Y, connected at the V_{CC} pin, allows the LTC4216 bias supply to ride out supply glitches during a fault condition or adjacent board short.

Auto-Retry after a Fault

As shown in Figure 18, the LTC4216 can be configured to automatically retry after a fault condition by connecting both the $\overline{\text{FAULT}}$ and ON pins together with an RC network. The network has a pull-up resistor, R_{AUTO}, tied to the load supply (V_{IN}) and an external capacitor, C_{AUTO}, connected to ground. The auto-retry circuit will attempt to restart the LTC4216 after a circuit breaker trip, as shown in the timing diagram of Figure 19. In addition to the cooling cycle provided by the TIMER period during auto-retry sequence, the RC time constant for the ON pin voltage to reach 0.8V provides additional turn-off time to prevent the external MOSFET from overheating. The auto-retry duty cycle is given by:

$$\text{Duty Cycle} \approx \frac{t_{SS} + t_{FILTER} \bullet 100\%}{t_{OFF} + t_{TIMER} + t_{SS} + t_{FILTER}} \qquad (20)$$

where

t_{TIMER} = TIMER period as given by Equation (1); t_{OFF} = time taken to charge the capacitor, C_{AUTO}, from

APPLICATIONS INFORMATION

$\overline{FAULT}$ V_{OL} to $V_{ON(TH)}$ threshold (0.8V). As there is an internal 5µA current source pull-up at the $\overline{FAULT}$ pin, it complicates the equation for t_{OFF}. This is approximately given by:

$$t_{OFF} \approx \frac{R_{AUTO} \bullet C_{AUTO} \bullet (V_{ON(TH)} - V_{OL})}{(V_{IN} - V_{ON(TH)}) + R_{AUTO} \bullet 5\mu A} \quad (21)$$

t_{FILTER} = circuit breaker response time as given by Equation (2); t_{SS} = approximated time taken to charge the soft-start capacitor, C2, from 0V to its final value (1.65V) by 10µA current source only.

For the component values shown, the external RC time constant is set at 0.2 second, t_{TIMER} = 62ms, t_{OFF} = 25ms at V_{IN} = 5V, t_{SS} = 1.6ms, t_{FILTER} = 480µs and the auto-retry duty cycle is 2.3%. The auto-retry duty cycle can be further reduced by increasing both the t_{TIMER} delay and the RC delay. As an example, increasing the TIMER capacitor, C1, value from 100nF to 330nF, and R_{AUTO} value from 200k to 470k reduces the duty cycle to 0.8%.

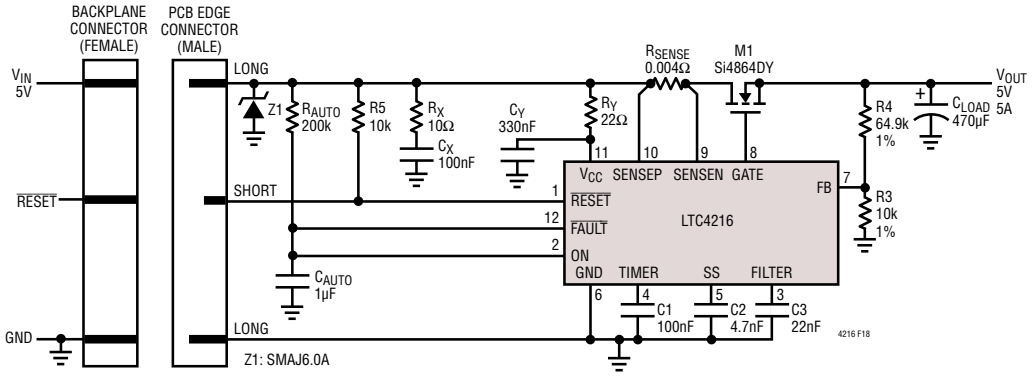


Figure 18. Auto-Retry Application

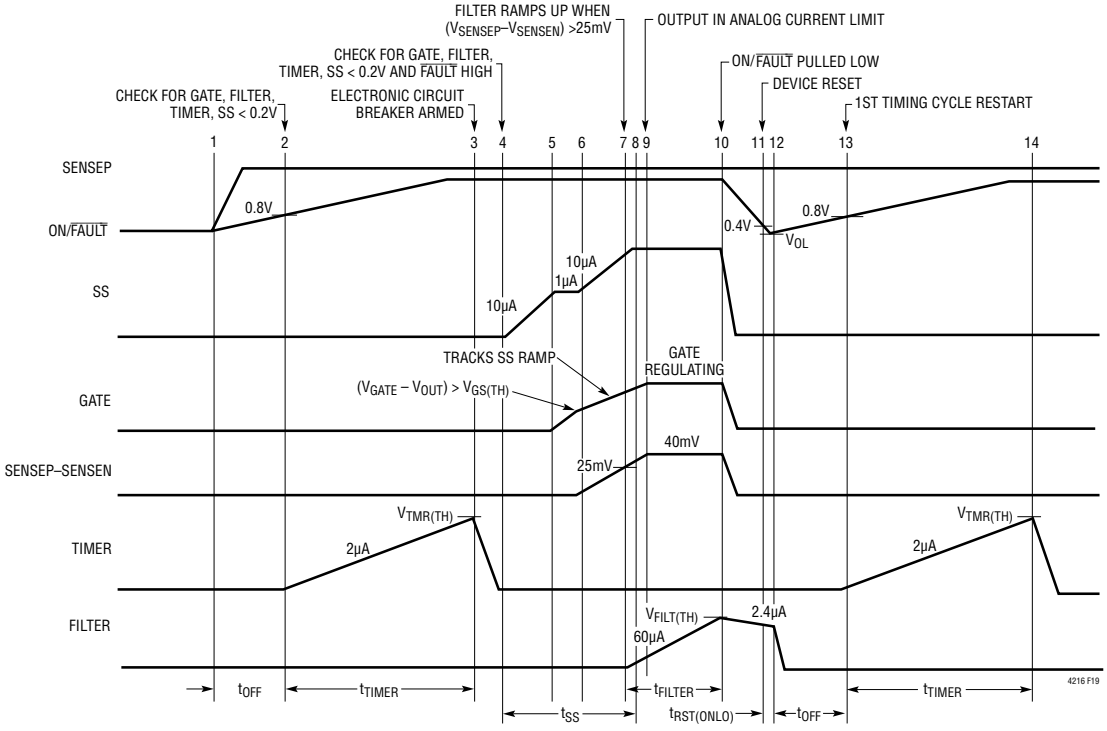
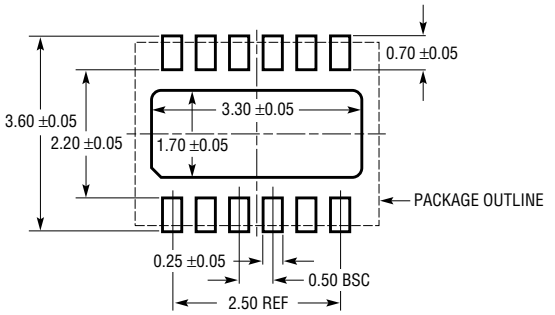


Figure 19. Auto-Retry Timing

PACKAGE DESCRIPTION

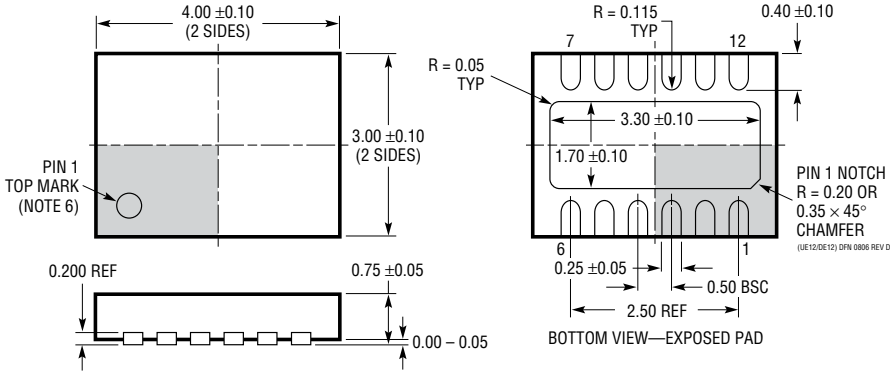
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DE/UE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1695 Rev D)

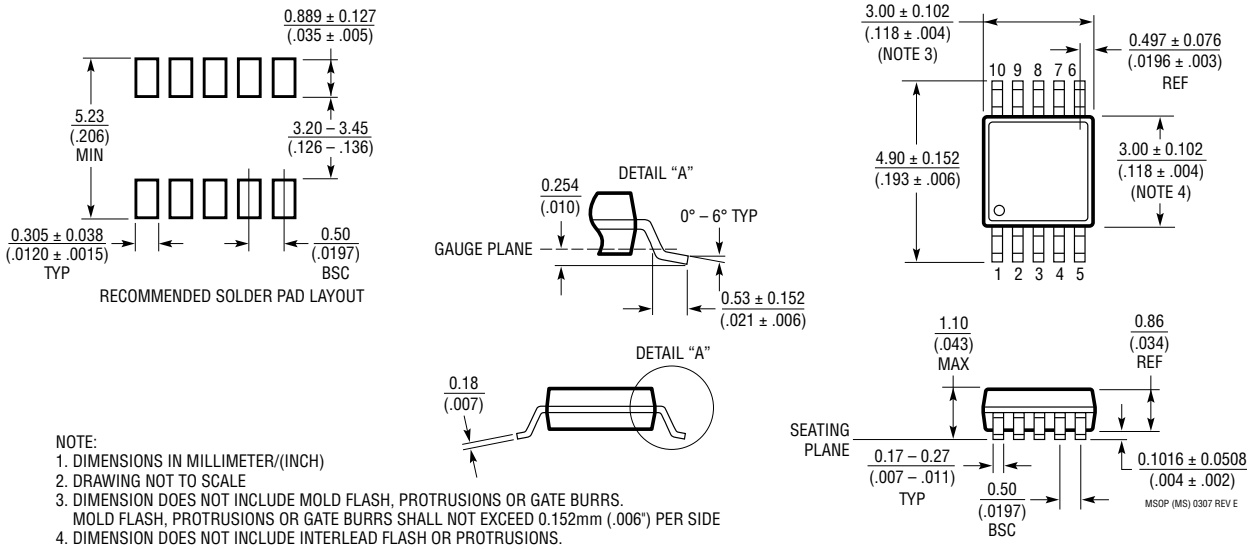


RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661 Rev E)



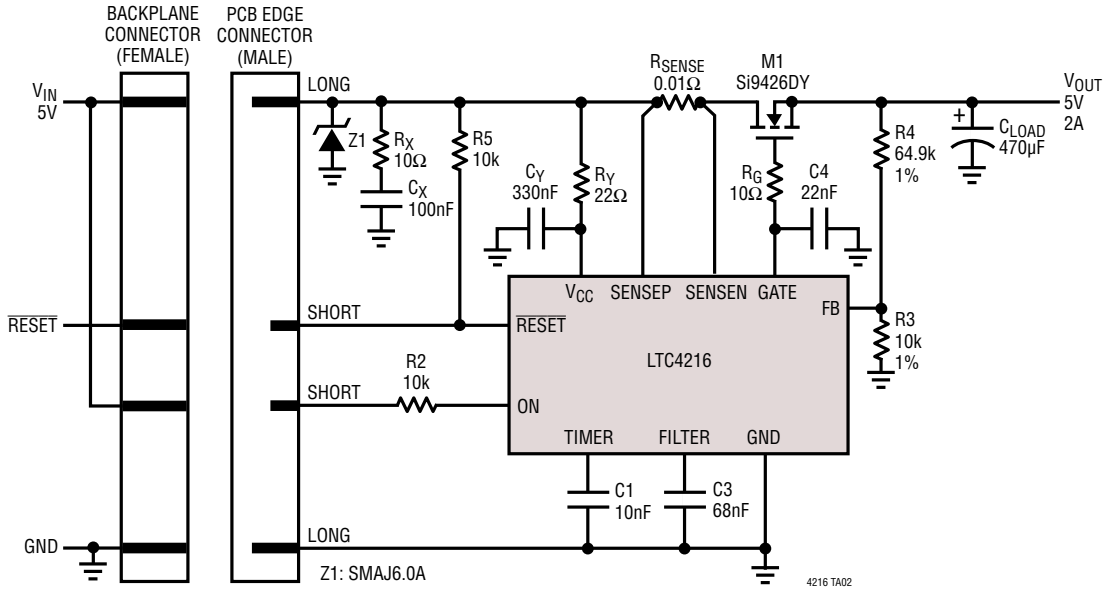
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	4/13	Corrected Supply Voltage to Output in the tenth feature	1
		Raised DE storage temperature limit to 150°C. Separated Order Information as per latest format	2
		Condition specified for $\Delta V_{CB(TH)}$. New specification for $t_{CB(TRIP)}$ without FILTER capacitor.	3
		Added new curve: Analog Current Limit Delay vs Sense Voltage	4
		Removed curve: $V_{\overline{FAULT}(TH)}$ vs Temperature	5
		Updated $\overline{RESET}$ pin description. Added threshold information to FILTER, TIMER and FB pin descriptions.	6
		Guidance given for the value of R_Z	12
		R_G added to Figure 7 and described before Equation 7	13

TYPICAL APPLICATION

LTC4216CMS with Gate Capacitor for Slew Rate Control



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1421	Dual Channels, Hot Swap Controller	Operates from 3V to 12V, Supports –12V, SSOP-24
LTC1422	Single Channel, Hot Swap Controller	Operates from 2.7V to 12V, SO-8
LTC1642	Single Channel, Hot Swap Controller	Operates from 3V to 16.5V, Overvoltage Protection up to 33V, SSOP-16
LTC1645	Dual Channel, Hot Swap Controller	Operates from 3V to 12V, Power Sequencing, SO-8 or SO-14
LTC1647-1/LTC1647-2/ LTC1647-3	Dual Channel, Hot Swap Controller	Operates from 2.7V to 16.5V, SO-8 or SSOP-16
LTC4210-1/LTC4210-2	Single Channel, Hot Swap Controller	Operates from 2.7V to 16.5V, Active Current Limiting, SOT23-6
LTC4211	Single Channel, Hot Swap Controller	Operates from 2.5V to 16.5V, Multifunction Current Control, MSOP-8 or MSOP-10
LTC4212	Single Channel, Hot Swap Controller	Operates from 2.5V to 16.5V, Power-Up Timeout, MSOP-10
LTC4214	Negative Voltage, Hot Swap Controller	Operates from –6V to –16V, MSOP-10
LT4220	Positive and Negative Voltage, Dual Channels, Hot Swap Controller	Operates from ±2.7V to ±16.5V, SSOP-16
LTC4221	Dual Hot Swap Controller/Sequencer	Operates from 1V to 13.5V, Multifunction Current Control, SSOP-16
LTC4230	Triple Channels, Hot Swap Controller	Operates from 1.7V to 16.5V, Multifunction Current Control, SSOP-20

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LTC4216
LT 0413 REV A • PRINTED IN USA

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View LTC4216CDE#PBF on WIN SOURCE
- Linear Technology Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management