# THE DATASHEET OF

# LTC4110EUHF#PBF

# Battery Backup System Manager

## FEATURES

- **Complete Backup Battery Manager for Li-Ion/ Polymer, Lead Acid, NiMH/NiCd Batteries and Super Capacitors**
- **Charge and Discharge Battery with Voltages Above and Below the Input Supply Voltage**
- **"No Heat" Battery Calibration Discharge Using System Load**
- **Automatic Battery Backup with Input Supply Removal Using PowerPath™ Control**
- **Standalone for Li-Ion/Polymer, SLA, and Supercaps**
- **Optional SMBus/I²C Support Allows Battery Capacity Calibration Operation with Host**
- **Over- and Under-Battery Voltage Protection**
- **Adjustable Battery Float Voltage**
- Precision Charge Voltage ±0.5%
- Programmable Charge/Calibration Current Up to 3A with ±3% Accuracy
- Optional Temperature Qualified Charging
- Wide Backup Battery Supply Range: 2.7V to 19V
- Wide Input Supply Range: 4.5V to 19V
- 38-Lead (5mm × 7mm) QFN Package

## APPLICATIONS

- Backup Battery Systems
- Server Memory Backup
- Medical Equipment
- High Reliability Systems

## DESCRIPTION

The LTC®4110 is a complete single chip, high efficiency, flyback battery charge and discharge manager with automatic switchover between the input supply and the backup battery or super capacitor. The IC provides four modes of operation: battery backup, battery charge, battery calibration and shutdown. Battery backup and battery charge are automatic standalone modes, while the optional calibration mode requires a CPU host to communicate over an SMBus. During calibration the flyback charger is used in reverse to discharge the battery with a programmable constant current into the system load eliminating heat generation. Three status outputs can be individually reconfigured over the SMBus to become GPIOs. User programmable overdischarge protection is provided. The SHDN pin isolates the battery to support shipping the product with a charged battery installed.

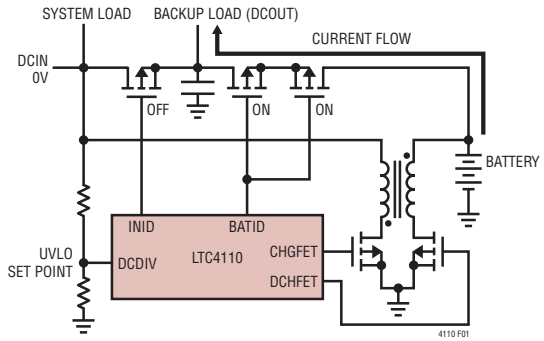
Multiple LTC4110s can be combined to form a redundant battery backup system or increase the number of battery packs to achieve longer backup run times.

The LTC4110 is available in a low profile (0.75mm), 38-pin 5mm × 7mm QFN package. The QFN features an exposed metal die mount pad for optimum thermal performance.

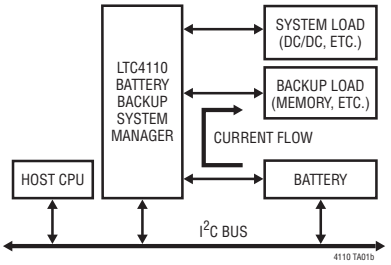
LT, LTC and LTM are registered trademarks of Linear Technology Corporation. PowerPath is a trademark of Linear Technology Corporation. All other trademarks are the property of their respective owners.

## TYPICAL APPLICATION

**Battery Backup System Manager**




**Server Backup System (In Backup Mode)**

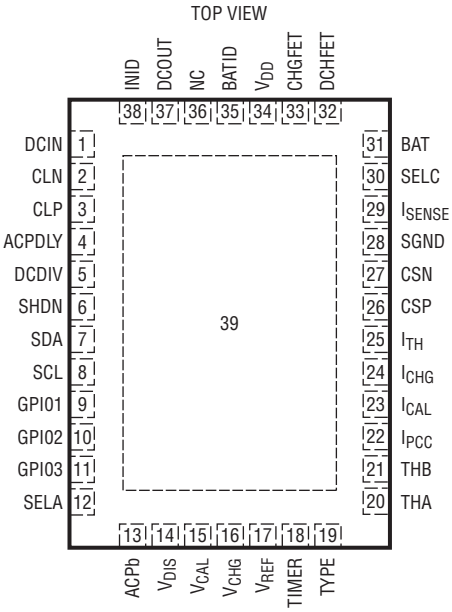


## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

DCIN, BAT, DCOUT, DCDIV, SHDN
to GND .....–0.3V to 20V
Input Voltage (CLP, CLN).....–0.3V to DCIN + 0.3V
Input Voltage (CSP, CSN) .....–0.3V to BAT + 0.3V
Input Voltage
(GPIO1, GPIO2, GPIO3, SELC, SELA, TYPE, $V_{CHG}$,
THA, THB, $I_{SENSE}$, ACPDLY, SDA, SCL) ....–0.3V to 7V
Input Voltage ($V_{CAL}$, $V_{DIS}$).....–0.3V to 1.35V
Output Voltage
(ACPb, GPIO1, GPIO2, GPIO3) .....–0.3V to 7V
CLP-CLN, CSP-CSN .....±1V
Operating Temperature Range (Note 2)....–40°C to 85°C
Junction Temperature (Note 3) ..... 105°C
Storage Temperature Range
QFN Package.....–65°C to 125°C

## PIN CONFIGURATION




UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN
$T_{JMAX}$ = 100°C, $\theta_{JA}$ = 34°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC4110EUHF#PBF | LTC4110EUHF#TRPBF | 4110 | 38-Lead (5mm × 7mm) Plastic QFN | –40°C to 85°C |
| **LEAD BASED FINISH** | **TAPE AND REEL** | **PART MARKING** | **PACKAGE DESCRIPTION** | **TEMPERATURE RANGE** |
| LTC4110EUHF | LTC4110EUHF#TR | 4110 | 38-Lead (5mm × 7mm) Plastic QFN | –40°C to 85°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. Unless otherwise specified, $V_{DCIN}$ = $V_{DCOUT}$ = $V_{DCDIV}$ = 12V, $V_{BAT}$ = 8.4V, GND = SGND = CLP = CLN = SHDN = 0V and $R_{VREF}$ = 49.9k. All currents into device pins are positive and all currents out of device pins are negative. All voltages are referenced to GND, unless otherwise specified.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Power Input** | | | | | | | |
| DCIN | Operating Voltage Range | Charge or Calibration Modes | ● | 4.5 | | 19 | V |
| DCOUT | Operating Voltage Range | Charge or Calibration Modes | ● | 4.5 | | 19 | V |
| | | Backup Mode | ● | 2.7 | | 19 | V |
| $V_{BAT}$ | Operating Voltage Range | Backup Mode | ● | 2.7 | | 19 | V |
| $I_{SPLY}$ | Supply Current ($I_{DCIN}$ + $I_{DCOUT}$) in Idle Mode (Note 4) | | | | 2 | 3 | mA |
| $I_{BIDL}$ | Battery Current in Idle Mode (Notes 4 and 5) | | | | 30 | 45 | µA |
| $I_{BBU}$ | Battery Current in Backup Mode (Note 5) | $V_{DCIN}$ = 0 | | | 2 | 3 | mA |
| $I_{BSD}$ | Battery Current in Shutdown (Note 5) | $V_{SHDN}$ = $V_{BAT}$, $V_{DCIN}$ = 0 | | | 20 | 45 | µA |
| $V_{UVI}$ | Undervoltage Lockout Exit Threshold | $V_{DCIN}$ Increasing | ● | 3.7 | 4 | 4.45 | V |
| $V_{UVD}$ | Undervoltage Lockout Entry Threshold | $V_{DCIN}$ Decreasing | ● | 3.4 | 3.7 | 4.1 | V |
| $V_{UVH}$ | Undervoltage Lockout Hysteresis | | | | 400 | | mV |
| **$V_{DD}$ Regulator** | | | | | | | |
| $V_{DD}$ | Output Voltage | No Load | ● | 4.5 | 4.75 | 5 | V |
| $V_{DD(MIN)}$ | Output Voltage | $I_{DD}$ = –10mA | ● | 4.25 | | | V |
| **Charging Performance** | | | | | | | |
| $V_{FTOL}$ | Charge Float Voltage Accuracy | 4.20V for Li-Ion. 2.35V for Lead Acid (Note 8)<br>$V_{CHG}$ = GND<br>–5°C < $T_A$ < 85°C (Note10)<br>–40°C < $T_A$ < 85°C | <br><br><br>● | –0.5<br><br>–0.8<br>–1 | | 0.5<br><br>0.8<br>1 | %<br><br>%<br>% |
| $V_{FATOL}$ | Charge Float Voltage Adjust Accuracy | 0.3V and –0.3V for Li-Ion Batteries, 0.15V and –0.15V for Lead Acid Batteries (Note 8) | ● | –2 | | 2 | % |
| $I_{BTOL}$ | Bulk Charge Current Accuracy (Note 7) | $V_{CSP}$ – $V_{CSN}$ =100mV<br>$V_{BAT}$ ≥ 3.1V<br>–40°C < $T_A$ < 85°C | <br><br>● | –3<br><br>–5 | | 3<br><br>5 | %<br><br>% |
| $I_{PTOL}$ | Preconditioning and Wake-Up Current Accuracy (Note 7) | $V_{BAT}$ ≥ 3.3V (Note 8), $V_{CSP}$ – $V_{CSN}$ = 10mV; Li-Ion and NiMH/NiCd Batteries Only | | –30 | | 30 | % |
| | | $V_{BAT}$ ≤ 3.3 (Note 8), $V_{CSP}$ – $V_{CSN}$ = 10mV; Li-Ion and NiMH/NiCd Batteries Only | | –40 | | 40 | % |
| $I_{SKVA}$ | Voltage Error Amplifier Sink Current at $I_{TH}$ Pin | $V_{ITH}$ = 2V | | | 96 | | µA |
| $I_{SRCA}$ | Current Error Amplifier Source Current at $I_{TH}$ Pin | $V_{ITH}$ = 2V | | | –24 | | µA |
| $I_{SKCA}$ | Current Error Amplifier Sink Current at $I_{TH}$ Pin | $V_{ITH}$ = 2V | | | 24 | | µA |
| $I_{VCHG}$ | $V_{CHG}$ Pin Bias Current | $V_{CHG}$ = 1.25V | | –100 | | 100 | nA |
| $V_{BC}$ | Bulk Charge Threshold Voltage; $V_{BAT}$ Increasing (Note 8) | Li-Ion, $V_{CHG}$ = GND<br>NiMH/NiCd | | 2.80<br>0.84 | 3.00<br>0.90 | 3.20<br>0.96 | V<br>V |
| $V_{BCH}$ | Bulk Charge Threshold Voltage Hysteresis; $V_{BAT}$ Decreasing (Note 8) | Li-Ion, $V_{CHG}$ = GND<br>NiMH/NiCd | | | 85<br>40 | | mV<br>mV |
| $V_{AR}$ | Auto Recharge Threshold Voltage; $V_{BAT}$ Decreasing | Standard Li-Ion Only; Specified as Percentage of Float Voltage | | 93 | 95 | 97 | % |
| $V_{ARH}$ | Auto Recharge Threshold Hysteresis Voltage; $V_{BAT}$ Increasing | Standard Li-Ion Only; Specified as Percentage of Float Voltage | | | 2 | | % |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. Unless otherwise specified, $V_{DCIN}$ = $V_{DCOUT}$ = $V_{DCDIV}$ = 12V, $V_{BAT}$ = 8.4V, GND = SGND = CLP = CLN = SHDN = 0V and $R_{VREF}$ = 49.9k. All currents into device pins are positive and all currents out of device pins are negative. All voltages are referenced to GND, unless otherwise specified.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{BOV}$ | Battery Overvoltage Threshold; $V_{BAT}$ Increasing | All Li-Ion, Lead Acid as Percentage of Float Voltage<br>NiMH/NiCd (Note 8) | | 105<br>1.80 | 107.5<br>1.85 | 110<br>1.90 | %<br>V |
| $V_{BOVH}$ | Battery Overvoltage Threshold Hysteresis; $V_{BAT}$ Increasing. | All Li-Ion, Lead Acid as Percentage of Float Voltage<br>NiMH/NiCd (Note 8) | | | 2<br>40 | | %<br>mV |
| $V_{REF}$ | Reference Pin Voltage Range | | ● | 1.208 | 1.220 | 1.232 | V |
| $F_{TMR}$ | Programmed Timer Accuracy | $C_{TIMER}$ = 47nF | ● | –15 | 0 | 15 | % |
| $t_{TIMEOUT}$ | Time Between Receiving Valid ChargingCurrent() and ChargingVoltage() Commands. Wake-Up Timer. | | ● | 140 | 175 | 210 | sec |
| **Calibration Performance** | | | | | | | |
| $V_{CTOL}$ | Calibration Cut-Off Default Voltage Accuracy; $V_{BAT}$ Decreasing | 2.75V for Li-Ion, 1.93V for Lead Acid, $V_{CAL}$ = GND (Note 8), 0.95V for NiMH/NiCd | <br>● | –1.1<br>–1.3 | | 1.1<br>1.3 | %<br>% |
| $V_{CTOLH}$ | Calibration Cut-Off Default Voltage Hysteresis; $V_{BAT}$ Increasing. (Note 8) | Li-Ion<br>Lead Acid<br>NiMH/NiCd | | | 85<br>50<br>40 | | mV<br>mV<br>mV |
| $V_{CATOL}$ | Calibration Cut-Off Voltage Adjust Accuracy | ±400mV for Li-Ion, ±300mV for Lead Acid, ±200mV for NiMH/NiCd (Note 8) | ● | –1.5 | | 1.5 | % |
| $I_{FTOL}$ | Calibration Current Accuracy (Note 7) | $V_{CSP} – V_{CSN}$ = –100mV | ● | –5 | | 5 | % |
| $I_{VCAL}$ | $V_{CAL}$ Pin Leakage Current | $V_{CAL}$ = 1.25V | | –100 | | 100 | nA |
| $I_{BDT}$ | Back-Drive Current Limit Threshold | $V_{CLP} – V_{CLN}$ Decreasing<br>$V_{CLN} = V_{DCIN}$ | ● | 7 | 10 | 13 | mV |
| $I_{BDH}$ | Back-Drive Current Limit Threshold Hysteresis | $V_{CLP} – V_{CLN}$ Increasing<br>$V_{CLN} = V_{DCIN}$ | | | 1 | | mV |
| $V_{OVP}$ | Calibration Mode Input Overvoltage Comparator DCDIV Pin Threshold | $V_{DCDIV}$ Rising | ● | 1.4 | 1.5 | 1.6 | V |
| $V_{OVPH}$ | Calibration Mode Input Overvoltage Comparator DCDIV Pin Hysteresis | $V_{DCDIV}$ Falling | | | 100 | | mV |
| **AC Present and Discharge Cut-Off Comparators** | | | | | | | |
| $V_{AC}$ | AC Present Comparator DCDIV Pin Threshold | $V_{DCDIV}$ Falling | ● | 1.196 | 1.22 | 1.244 | V |
| $V_{ACH}$ | AC Present Comparator DCDIV Pin Hysteresis | $V_{DCDIV}$ Rising | | | 50 | | mV |
| $I_{AC}$ | AC Present Comparator DCDIV Pin Input Bias Current | $V_{DCDIV}$ = 1.25V | | | | 100 | nA |
| $t_{AC}$ | ACPb Pin Externally Programmed Falling Delay | $C_{ACPDLY}$ = 100nF, $R_{VREF}$ = 49.9k,<br>$V_{DCDIV}$ Stepped From 1.17V to 1.30V | | 8 | 10 | 12 | ms |
| $V_{DTOL}$ | Discharge Cut-Off Default Voltage Accuracy; $V_{BAT}$ Decreasing | 2.75V for Li-Ion, 1.93V for Lead Acid, $V_{DIS}$ = GND, 0.95V for NiMH/NiCd | ● | –1.5 | | 1.5 | % |
| $V_{DTOLH}$ | Discharge Cut-Off Default Voltage Hysteresis; $V_{BAT}$ Increasing (Note 8) | Li-Ion<br>Lead acid<br>NiMH/NiCd | | | 85<br>50<br>40 | | mV<br>mV<br>mV |
| $V_{DATOL}$ | Discharge Cut-Off Voltage Adjust Accuracy | ±400mV for Li-Ion, ±300mV for Lead Acid, ±200mV for NiMH/NiCd | ● | 2 | | 2 | % |
| $I_{VDIS}$ | $V_{DIS}$ Pin Bias Current | $V_{DIS}$ = 1.25V | | –100 | | 100 | nA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. Unless otherwise specified, $V_{DCIN}$ = $V_{DCOUT}$ = $V_{DCDIV}$ = 12V, $V_{BAT}$ = 8.4V, GND = SGND = CLP = CLN = SHDN = 0V and $R_{VREF}$ = 49.9k. All currents into device pins are positive and all currents out of device pins are negative. All voltages are referenced to GND, unless otherwise specified.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Input and Battery Ideal Diodes and Switches** | | | | | | | |
| $V_{FR}$ | Forward Regulation Voltage ($V_{DCIN}$-$V_{DCOUT}$, $V_{BAT}$-$V_{DCOUT}$) | 2.7V ≤ $V_{DCIN}$ ≤ 19V | ● | 10 | 20 | 32 | mV |
| $V_{REV}$ | Reverse Voltage Turn-Off Voltage ($V_{DCIN}$-$V_{DCOUT}$, $V_{BAT}$-$V_{DCOUT}$) | 2.7V ≤ $V_{DCIN}$ ≤ 19V | ● | –30 | –18 | –8 | mV |
| $V_{GON}$ | "ON" Gate Clamping Voltage ($V_{DCIN}$-$V_{INID}$, $V_{BAT}$-$V_{BATID}$) | $I_{INID}$, $I_{BATID}$ = 1µA | | 7 | 8.3 | 9.7 | V |
| $V_{GOFF}$ | "OFF" Gate Voltage ($V_{DCIN}$-$V_{INID}$, $V_{BAT}$-$V_{BATID}$) | $I_{INID}$, $I_{BATID}$ = –10µA<br>$V_{SHDN}$ = 0V and $V_{DCIN}$ (Shutdown) | | | | 0.25 | V |
| $V_{FO}$ | BATID Fast-On Voltage Comparator Threshold | $I_{BATID}$ > 500µA | | 45 | | 100 | mV |
| | INID Pin Delay Times | $C_{INID}$ = 10nF<br>DCIN is Switched Between 12.2V and 11.8V | | | | | |
| $t_{IIDON}$<br>$t_{IIDOFF}$ | Turn "ON"<br>Turn "OFF" | From DCOUT – $V_{GOFF}$ to DCOUT –6V<br>From DCOUT – $V_{GON}$ to DCOUT –1.5V | | | 450<br>8 | 700<br>20 | µs<br>µs |
| | BATID Pin Delay Times | $C_{BATID}$ = 2.5nF<br>BAT is Switched Between 12.2V and 11.8V | | | | | |
| $t_{BIDON}$<br>$t_{BIDOFF}$ | Turn "ON"<br>Turn "OFF" | From DCOUT – $V_{GOFF}$ to DCOUT –6V<br>From DCOUT – $V_{GON}$ to DCOUT –1.5V | | | 15<br>8 | 60<br>20 | µs<br>µs |
| **PWM Flyback Converter** | | | | | | | |
| $V_{OHF}$ | CHGFET, DCHFET High | $I_{CHGFET}$, $I_{DCHFET}$ = –1mA | | 4.5 | 4.75 | 5.25 | V |
| $V_{OLF}$ | CHGFET, DCHFET Low | $I_{CHGFET}$, $I_{DCHFET}$ = 1mA | | | | 50 | mV |
| $V_{OLFX}$ | CHGFET, DCHFET in Shutdown and Backup Modes | $V_{DCIN}$ = $V_{DCDIV}$ = $V_{DCOUT}$ = 0V (Shutdown Mode), $V_{DCIN}$ = $V_{DCDIV}$ = 0V (Backup Mode)<br>$I_{CHGFET}$, $I_{DCHFET}$ = 1µA | | | | 100 | mV |
| | CHGFET, DCHFET Transition Times | | | | | | |
| $t_R$<br>$t_F$ | Rise Time<br>Fall Time | $C_{LOAD}$ = 1.6nF, 20% to 80%<br>$C_{LOAD}$ = 1.6nF, 20% to 80% | | | 35<br>15 | 65<br>65 | ns<br>ns |
| $F_{PWM}$ | PWM Oscillator Switching Frequency | | ● | 255 | 300 | 340 | kHz |
| **SafetySignal Decoder and Thermistor Interface** | | | | | | | |
| $SS_{OR}$ | SafetySignal Decoder SafetySignal Trip (RES_COLD/RES_OR) | $R_{THA}$ = 1130Ω ±1%, $C_{TH}$ = 1nF (Note 6) $R_{THB}$ = 54.9k ±1%.<br>Smart Batteries and Li-Ion Only | ● | 95 | 100 | 105 | k |
| $SS_{CLD}$ | SafetySignal Decoder SafetySignal Trip (RES_IDEAL/RES_COLD) | $R_{THA}$ = 1130Ω ±1%, $C_{TH}$ = 1nF (Note 6) $R_{THB}$ = 54.9k ±1%<br>Smart Batteries and Li-Ion Only | ● | 28.5 | 30 | 31.5 | k |
| $SS_{IDL}$ | SafetySignal Decoder SafetySignal Trip (RES_HOT/RES_IDEAL) | $R_{THA}$ = 1130Ω ±1%, $C_{TH}$ = 1nF (Note 6) $R_{THB}$ = 54.9k ±1%<br>Smart Batteries and Li-Ion Only | ● | 2.85 | 3 | 3.15 | k |
| $SS_{HOT}$ | SafetySignal Decoder SafetySignal Trip (RES_UR/RES_HOT) | $R_{THA}$ = 1130Ω ±1%, $C_{TH}$ = 1nF (Note 6) $R_{THB}$ = 54.9k ±1%<br>Smart Batteries and Li-Ion Only | ● | 425 | 500 | 575 | Ω |
| $V_{HOT}$ | THB Pin Hot Threshold Voltage | $V_{THB}$ Decreasing; Lead Acid Only | ● | 0.28 • $V_{THA}$ | 0.30 • $V_{THA}$ | 0.36 • $V_{THA}$ | V |
| $V_{HOTH}$ | THB Pin Hot Threshold Hysteresis Voltage | $V_{THB}$ Increasing; Lead Acid Only | | | 50 | | mV |
| $V_{REM}$ | THB Pin Battery Removal Threshold Voltage | $V_{THB}$ Increasing; Lead Acid Only | ● | 0.90 • $V_{THA}$ | 0.94 • $V_{THA}$ | 0.96 • $V_{THA}$ | V |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. Unless otherwise specified, $V_{DCIN}$ = $V_{DCOUT}$ = $V_{DCDIV}$ = 12V, $V_{BAT}$ = 8.4V, GND = SGND = CLP = CLN = SHDN = 0V and $R_{VREF}$ = 49.9k. All currents into device pins are positive and all currents out of device pins are negative. All voltages are referenced to GND, unless otherwise specified.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{REMH}$ | THB Pin Battery Removal Threshold Hysteresis Voltage | $V_{THB}$ Decreasing; Lead Acid Only | | | 25 | | mV |
| **Logic and Status Output Levels** | | | | | | | |
| $V_{ILS}$ | SCL/SDA Input Pins Low Voltage | | ● | | | 0.8 | V |
| $V_{IHS}$ | SCL/SDA Input Pins High Voltage | | ● | 2.1 | | | V |
| $V_{OLS}$ | SDA Output Pin Low Voltage | $I_{PULL-UP}$ = 350µA | ● | | | 0.4 | V |
| $V_{OLG}$ | ACPb, GPIO1,2,3 Output Pins Low Voltage | $I_{ACPb}$, $I_{GPIO1}$, $I_{GPIO2}$, $I_{GPIO3}$ = 10mA | | | | 1 | V |
| $I_{OHG}$ | ACPb, GPIO1,2,3 Output Pins Open Leakage Current | Outputs Open, $V_{ACPb}$, $V_{GPIO1,2,3}$ = 5V | | –2 | | 2 | µA |
| $V_{ILG}$ | GPIO Input Low Voltage | | ● | | | 1 | V |
| $V_{IHG}$ | GPIO Input High Voltage | | ● | 1.5 | | | V |
| $V_{ILSD}$ | SHDN Input Pin Low Voltage | | | | | 0.5 | V |
| $V_{IHSD}$ | SHDN Input Pin High Voltage | | | 2.4 | | | V |
| $I_{ISD}$ | SHDN Input Pin Pull-Up Current | $V_{SHDN}$ = 2.4V | | –3.5 | –2 | –1 | µA |
| $T_{LR}$ | Logic Reset Duration After Power-Up From Zero | $V_{DCIN}$ Transition From 0V to 5V in <1ms; $V_{BAT}$ = 0 | | | | 1 | s |
| **SMBus Timing (Note 9)** | | | | | | | |
| $t_{HIGH}$ | SCL Serial Clock High Period | $I_{PULL-UP}$ = 350µA, $C_{LOAD}$ = 250pF, $R_{PU}$ = 9.31k | ● | 4 | | | µs |
| $t_{LOW}$ | SCL Serial Clock Low Period | $I_{PULL-UP}$ = 350µA, $C_{LOAD}$ = 250pF, $R_{PU}$ = 9.31k | ● | 4.7 | | | µs |
| $t_{TO}$ | Timeout Period | | ● | 25 | | | ms |
| $t_F$ | SDA/SCL Fall Time | $C_{LOAD}$ = 250pF, $R_{PU}$ = 9.31k | ● | | | 300 | ns |
| $t_{SU-STA}$ | Start Condition Set-Up Time | | ● | 4.7 | | | µs |
| $t_{HD-STA}$ | Start Condition Hold Time | | ● | 4 | | | µs |
| $t_{HD-DAT}$ | SDA to SCL Falling-Edge Hold Time, Slave Clocking in Data | | ● | 300 | | | ns |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. Specific functionality or parametric performance of the device beyond the limits expressly given in the Electrical Characteristics table is not implied by these maximum ratings.

**Note 2:** The LTC4110E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

**Note 3:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Overtemperature protection will become active at a junction temperature greater than the maximum operating junction temperature. Continuous operation above the specified maximum operation temperature may result in device degradation or failure. Operating junction temperature $T_J$ (in °C) is calculated from the ambient temperature $T_A$ and the average power dissipation $P_D$ (in watts) by the formula $T_J = T_A + \theta_{JA} \bullet P_D$.

**Note 4:** The LTC4110 is idle with no application load. It is not charging or calibrating the battery and is not in backup or shutdown mode. The internal clock is running and the SMBus is functional.

**Note 5:** Combined current of CSP, CSN and BAT pins set to $V_{BAT}$ with no application load.

**Note 6:** $C_{TH}$ is defined as the sum of capacitance on THA, THB SafetySignal.

**Note 7:** Does not include tolerance of current sense or current programming resistors.

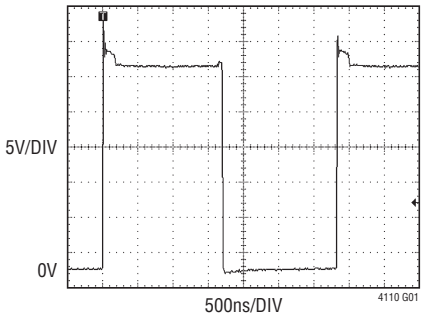
**Note 8:** Given as a per cell voltage referred to the BAT pin ($V_{BAT}$/number of series cells).

**Note 9:** Refer to System Management Bus Specification, Revision 1.1, section 2.1 for Timing Diagrams and section 8.1, for $t_{LOW}$ and $t_{TIMEOUT}$ requirements.

**Note 10:** Specifications over the –5°C to 85°C operating ambient temperature range are assured by design, characterization and correlation with statistical process controls.

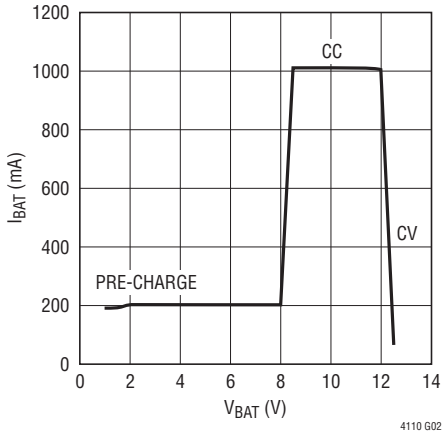
# TYPICAL PERFORMANCE CHARACTERISTICS

### Typical CHGFET and DCHFET Waveforms

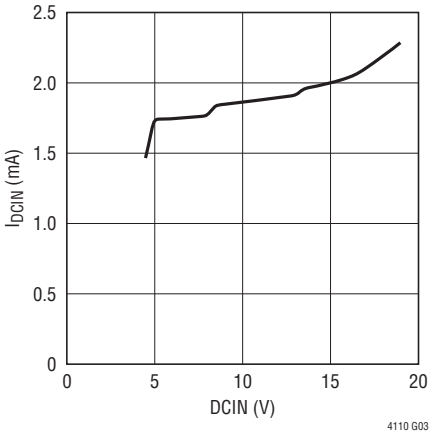



$V_{IN}$ = 12V
$V_{BAT}$ = 12V (NiMH)

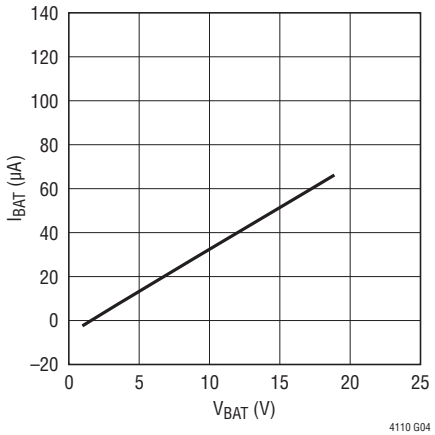
### Output Charging Characteristics Showing Constant Current and Constant Voltage Operation



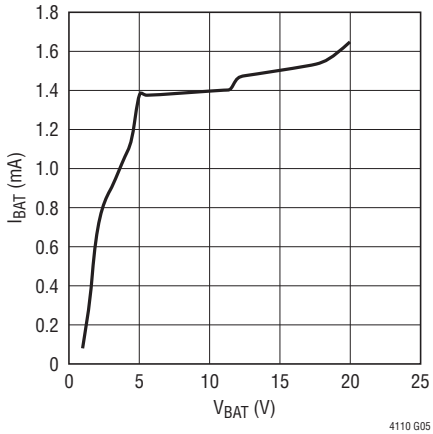

### Supply Current vs DCIN Voltage in Idle Mode



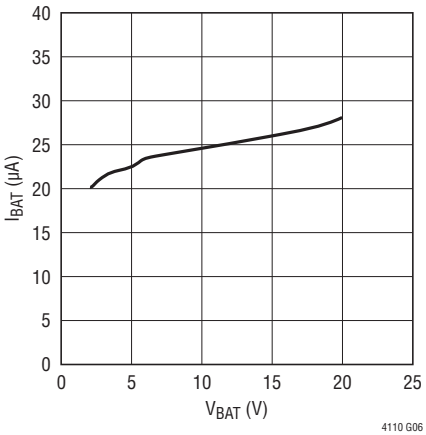

### Battery Leakage in Idle Mode – IBIDL



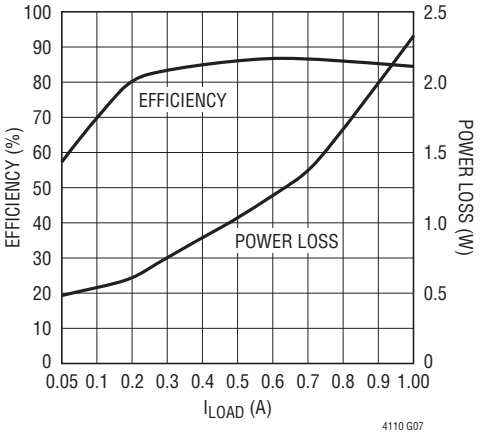

### Battery Current in Backup Mode – IBBU



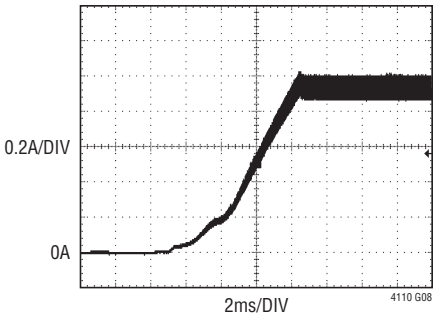

### Battery Leakage in Shutdown Mode vs Battery Voltage



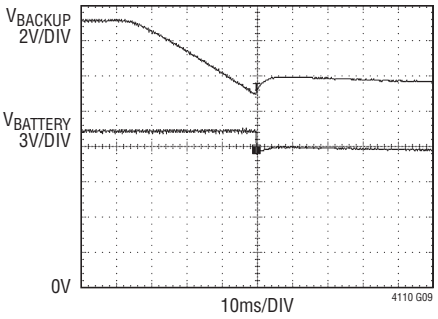

### Charging Efficiency/Power Loss, $12V_{IN}$ and $12.6V_{OUT}$ (Xfmr = BH 510-1019)




### Soft-Start Waveform




### Backup Mode On and Off Waveform




NiMH BATTERY (12V)
$I_{LOAD}$ = 3A
$V_{IN}$ = 15V FALLING

## PIN FUNCTIONS

**DCIN (Pin 1):** External DC Power Sense Input. Provides a control input and supply for the main supply ideal diode function.

**CLN (Pin 2):** Current Limit Sense Negative Input. See CLP pin.

**CLP (Pin 3):** Current Limit Sense Positive Input. This pin and the CLN pin form a differential input that senses voltage on an external resistor for reverse current entering the power source while in low loss calibration mode. Should the current approach reversal, this function will terminate calibration. An RC filter may be required to filter out system load noise. Connect both CLP and CLN pins to GND to disable this function. A differential voltage of >1V between the CLP and CLN pins may damage the device.

**ACPDLY (Pin 4):** ACPb Delay Control Pin. A capacitor connected from ACPDLY to GND and a resistor from $V_{REF}$ to GND programs delay in the ACPb pin high-to-low transition. Open if minimum delay is desired.

**DCDIV (Pin 5):** AC Present Detection Input. Backup operation is invoked when the system power voltage, divided by an external resistor divider, falls below the threshold of this pin.

**SHDN (Pin 6):** Active High Shutdown/Reset Control Logic Input. Forces micropower shutdown mode if high when DCIN supply is removed. Forces all registers to reset if high when DCIN supply is present. Normally tied to ground. Internal pin pull-up current.

**SDA (Pin 7):** SMBus Bidirectional Data Signal. Connect to $V_{DD}$ when not in use.

**SCL (Pin 8):** SMBus Clock Signal Input From SMBus Host. Connect to $V_{DD}$ when not in use.

**GPIO1 (Pin 9):** General Purpose I/O or Charge Status Pin. A logic-level I/O bit port that is configurable as a host-driven input/output port or as a battery charge status output (CHGb) with an open-drain N-MOSFET that is asserted low when any smart battery or Li-Ion battery is in any phase of charging or when lead acid battery charge current is >C/x where:

$$x = \frac{C}{I_{CHG}} \bullet 5$$

(See C/x Charge Termination section for more details). If the No SMBus option is selected with the SELA pin, the GPIO1 pin defaults as battery charge status. Refer to Table 5a.

**GPIO2 (Pin 10):** General Purpose I/O Pin. A logic-level I/O bit port that is configurable as a host-driven input/output port or as a battery undervoltage status output (BKUP_FLTb) with an open-drain N-MOSFET that is asserted low only while in backup mode if the battery's average cell voltage drops below voltage programmed by the $V_{DIS}$ pin. If the No SMBus option is selected with the SELA pin, then the GPIO2 pin defaults as battery undervoltage status. Refer to Table 5c.

**GPIO3 (Pin 11):** General Purpose I/O Pin. A logic-level I/O bit port that is configurable as a host-driven input/output port or as a calibration complete status output (CAL_COMPLETEb) with an open-drain N-MOSFET that is asserted low when calibration has been completed. If the SELA pin is programmed for no SMBus use then the status output is charge fault (CHGFLTb) instead of calibration complete. Refer to Table 5e.

**SELA (Pin 12):** SMBus Address Selection Input. Selects the LTC4110 SMBus address to facilitate redundant backup systems when standard batteries are used. Connect to GND for 12h, $V_{DD}$ for 28h and the $V_{REF}$ pin for 20h. When a smart battery is selected by the TYPE pin, the SELA pin must be connected to GND to select address 12h. If the SMBus is not used or to force all GPIOs to status mode upon power-up, connect pin to a typically 0.5 • $V_{REF}$ voltage from $V_{REF}$ pin resistor divider. The SMBus address, if used, will be 12h.

## PIN FUNCTIONS

**ACPb (Pin 13):** AC Present Status Digital Output. Open-Drain N-MOSFET output is asserted low when the main supply is present as detected by the DCDIV pin and internal DCIN UVLO.

**$V_{DIS}$ (Pin 14):** Battery Discharge Voltage Limit During Backup Program Input. Battery threshold voltage at which backup mode will terminate by turning off the isolation P-MOSFET with the BATID pin. Adjustable from external resistor string biased from $V_{REF}$ pin. For default threshold connect to GND pin.

**$V_{CAL}$ (Pin 15):** Battery Voltage Limit During Calibration Program Input. Battery threshold voltage at which calibration will terminate. Adjustable from external resistor string biased from $V_{REF}$ pin. For default threshold connect to GND pin.

**$V_{CHG}$ (Pin 16):** Battery Float Voltage Program Input. Trims the float voltage during charging. Programmed from external resistor string biased from $V_{REF}$ pin. Connect to GND for default float voltage.

**$V_{REF}$ (Pin 17):** Voltage Reference Output and Timing Programming Input. Provides a typical virtual reference of 1.220V ($V_{REF}$) for an external resistor divider tied between this pin and GND that programs the $V_{CHG}$, $V_{CAL}$ and $V_{DIS}$ pin functions. Total resistance from $V_{REF}$ to GND, along with the capacitor on the timer pin, programs the charge time. Voltage reference output remains active in all modes except shutdown. Load current must be between 10µA and 25µA.

**TIMER (Pin 18):** Charge Timing Input. A capacitor connected between TIMER and GND along with the resistance connected from $V_{REF}$ to GND programs the charge time intervals.

**TYPE (Pin 19):** Refer to Table 8.

**THA (Pin 20):** SafetySignal Force/Sense Pin to Smart Battery and Force Pin to Lead Acid Battery Thermistor. See description of operation for more detail. The maximum allowed combined capacitance on THA, THB and SafetySignal is 1nF. For lead acid battery applications the maximum capacitance on the THA pin is 50pF.

**THB (Pin 21):** SafetySignal Force/Sense Pin to Smart Battery and Sense Pin to Lead Acid Battery Thermistor. See description of operation for more detail. The maximum allowed combined capacitance on THA, THB and SafetySignal is 1nF.

**$I_{PCC}$ (Pin 22):** Battery Preconditioning Charge Current Program Input. Programs the battery current during preconditioning or wakeup charging. Programmed from external resistor to GND.

**$I_{CAL}$ (Pin 23):** Battery Discharge Current During Calibration Program Input. Programs the constant discharge current at the battery during calibration. Programmed from external resistor to GND.

**$I_{CHG}$ (Pin 24):** Battery Current During Charge Program Input. Programs the battery current while constant-current bulk charging. Programmed from external resistor to GND.

**$I_{TH}$ (Pin 25):** Control Signal of the Current Mode PWM. AC compensates control loop. Higher $I_{TH}$ voltage corresponds to higher charging current.

**CSP (Pin 26):** Current Sense Positive Input. This pin and the CSN pin measure voltage across the external current sense resistor to control battery current during charging and calibration.

**CSN (Pin 27):** Current Sense Negative Input. This pin and the CSP pin measure voltage across the external current sense resistor to control battery current during charging and calibration.

**SGND (Pin 28):** Signal Ground Reference Input. This pin should be Kelvin connected to the flyback current sense resistor and to the battery return.

**$I_{SENSE}$ (Pin 29):** Current Sense Input. Senses current in the flyback transformer by monitoring voltage across the external current sense resistor. This pin should be Kelvin-connected to the resistor.

**SELC (Pin 30):** Refer to Table 8.

## PIN FUNCTIONS

**BAT (Pin 31):** Battery Voltage Sense Input. This pin is used to monitor the battery and control charging voltage through an internal resistor divider connected to this pin that is disconnected in shutdown mode. Also provides a control input for battery ideal diode functions. Pin should be Kelvin-connected to battery to avoid voltage drop errors.

**DCHFET (Pin 32):** Drives the Gate of an External N-MOSFET. Used to drive energy into the battery side of the high efficiency switch mode converter during low loss calibration discharge of the battery. Provides synchronous rectification during battery charging.

**CHGFET (Pin 33):** Drives the Gate of an External N-MOSFET. Used to drive energy into the supply side of the high efficiency switch mode converter during battery charging. Provides synchronous rectification during low loss calibration mode.

**$V_{DD}$ (Pin 34):** Bypass Capacitor Connection for Internal $V_{DD}$ Regulator. Bypass at pin with 100nF low ESR capacitor to GND.

**BATID (Pin 35):** Drives the Gate of the Battery P-MOSFET Ideal Diode. Controls low loss ideal diode between the battery and backup load when in backup mode. When not in backup mode, the P-MOSFET is turned off to prevent battery power from back driving into main power.

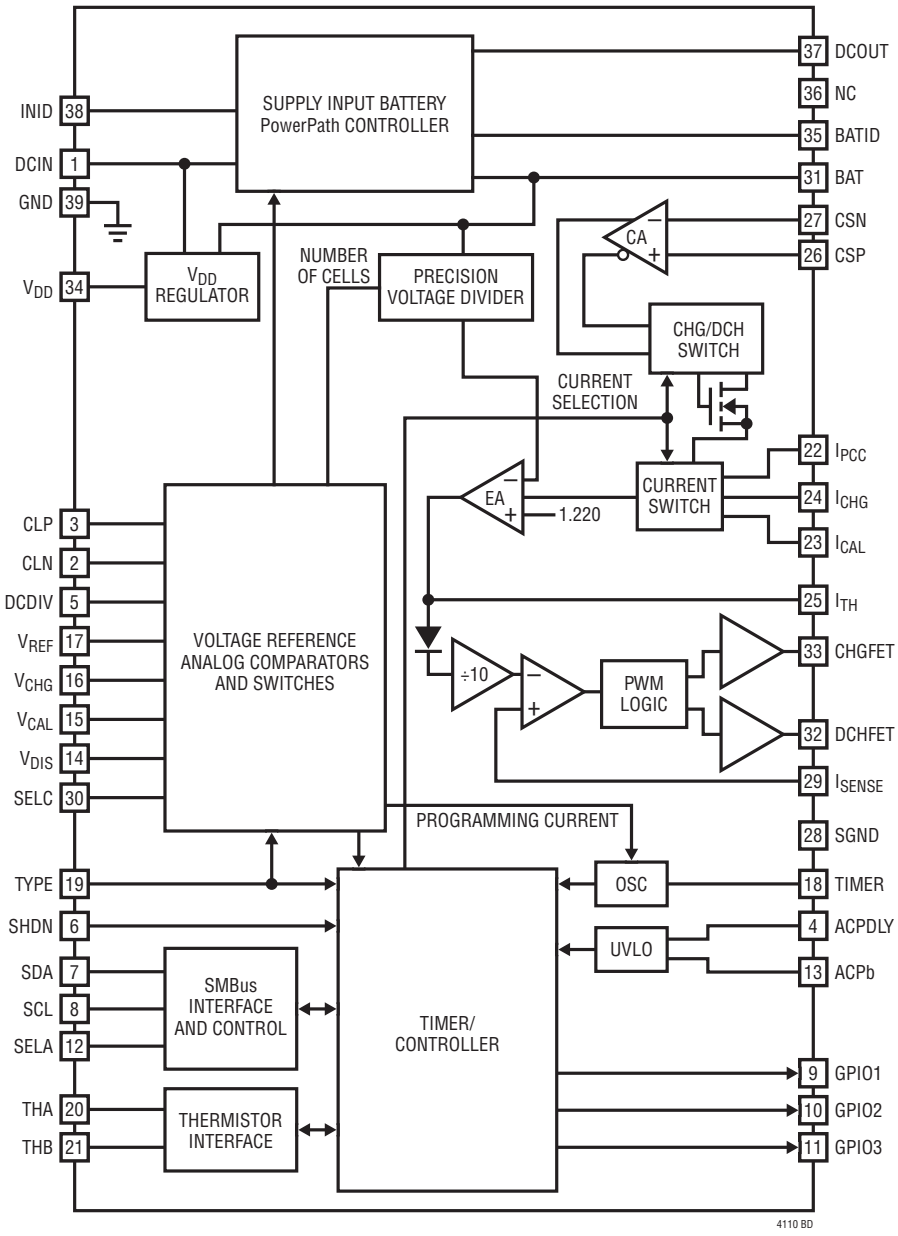
**NC (Pin 36):** No Connect.

**DCOUT (Pin 37):** System Power Output Voltage Monitor Input. Provides a control input for supply input ideal diode and battery ideal diode functions. Also supplies power to the IC. Bypass at pin with 100nF low ESR capacitor to GND.

**INID (Pin 38):** Drives the Gate of the Supply Input P-MOSFET Ideal Diode. Controls low loss ideal diode between the supply input and backup load when not in backup mode.

**Exposed Pad (Pin 39):** Ground. The Exposed Pad must be soldered to the PCB.

## BLOCK DIAGRAM



## OPERATION

### OVERVIEW

In the typical application, the LTC4110 is placed in series with main power supply that powers all or part of the system, which must include the device(s) or system that needs battery backup.

The LTC4110 has four modes of operation:

- Battery Backup Mode
- Battery Charge Mode
- Battery Calibration Mode
- Shutdown Mode

The LTC4110 provides complete PowerPath control for the battery backed up load switching automatically from the main power supply to the battery when battery backup mode is required. Low loss ideal diode FET switches are used to connect the main supply or the battery to the backup load which permit multiple LTC4110's to work together in a scalable fashion to permit longer backup times, redundancy and/or higher load currents. In battery charge mode, power is drawn from the main supply by a high efficiency synchronous flyback charger. The LTC4110 maintains the state of charge (SOC) of the battery at all times so the battery is ready at all times. Use of a flyback converter permits charging of batteries who's termination voltage can be greater than the main supply voltage, while at the same time providing high DC isolation to minimize parasitic drain on the battery. Testing, maintenance support and capacity verification of the battery is supported through the LTC4110's calibration mode. In calibration mode, the same synchronous flyback used to charge the battery is also used in reverse to allow safe controlled discharge of the battery back into the main supply eliminating wasted heat and energy. The product will not need to provide any additional thermal management to support this mode. Shutdown mode disconnects the battery from the load to preserve capacity and permits shipping the product with an energized battery installed at the factory, eliminating battery installation at the site. The LTC4110 supports optional control and monitoring of all activities by a host including faults over the industry standard SMBus, which is a variation of the $I^2C$ bus. However no host is required as the LTC4110 is fully functional in a standalone mode. Combining all these functions into a single IC reduces circuit area compared to presently available solutions.

The LTC4110 is designed to work with both standard battery and smart battery configurations. Smart batteries are standard batteries with industry standard gas gauge electronics built in offering accurate SOC information for the host. Furthermore, being intimate with all aspects of the battery, it also has the ability to control the charge process. Smart batteries use the SMBus as the communication bus for data exchange and charge control. For more information about smart batteries, see www.sbs-forum.org for specifications or contact Linear Technology Applications.

It is important to know that the LTC4110 uses the TYPE pin to learn what type of battery it will be working with. The TYPE pin setting globally affects all of the operating modes, options including GPIO and control ranges. Table 1 and Table 2 give you a complete breakdown of all the battery types supported relative to the TYPE pin settings

**Table 1. LTC4110 Battery Pack Charge Mode Capabilities**

| BATTERY TYPE | CHEMISTRY | | | MAXIMUM CHARGE TIME (SLA EXCLUDED) |
|---|---|---|---|---|
| | Li-Ion/Polymer | Nickel | SLA/Lead Acid | |
| Standard Battery | Yes | No | Yes | Adj. Up to 12 Hours |
| Smart Battery | Yes | Yes | Yes | Unlimited |

**Table 2. LTC4110 Battery Pack Charge Voltage Capabilities**

| CHEMISTRY | $V_{CELL}$ FULL CHARGE | $V_{CELL}$ ADJ. RANGE | SERIES CELL COUNT | NOMINAL STACK VOLTAGE (V) |
|---|---|---|---|---|
| Lead Acid | 2.35V | ±0.15V | 2, 3, 5 and 6 | 4, 6, 10 and 12 |
| Li-Ion/Polymer | 4.2V | ±0.3V | 1, 2, 3 and 4 | 3.6, 7.2, 10.8 and 14.4 |
| NiMH/NiCd | N/A | N/A | 4, 6, 9 and 10 | 4.8, 7.2, 10.8 and 12 |
| Super Caps | 2.5V, 2.7V or 3V | Yes | 2 to 7 | 5 to 18 |

## OPERATION

and ranges. It should be noted that even if the LTC4110 TYPE pin is not set to a smart battery mode, any SMBus commands sent by a host or a smart battery are still acted upon. For SuperCap support, see the Applications Information section.

### BATTERY BACKUP MODE

Figure 1 shows the LTC4110 in backup mode and the corresponding PowerPath enabled. The LTC4110 use the DCDIV pin to typically monitor the DCIN voltage through an external resistor divider. The DCDIV pin sets the backup mode threshold voltage and senses the need to enter backup mode. DCDIV can alternately be driven with other signals such as logic. When the DCDIV pin voltage drops below the AC present threshold voltage (see $V_{AC}$) backup mode is entered. Backup mode is also entered whenever the internal undervoltage lockout, UVLO, senses that DCIN ($V_{UVD}$) or DCOUT has fallen to excessively low voltages. In backup mode the battery P-MOSFET ideal diode is enabled to backup the load from the battery. The supply input P-MOSFET ideal diode isolates the main supply input from the load and the flyback switcher N-MOSFETs are inhibited from turning on. Also, after the threshold is passed, hysteresis ($V_{ACH}$) is switched in. When the supply is returning and the AC present threshold voltage plus the hysteresis voltage is reached on the DCDIV pin, both of the battery P-MOSFETs are rapidly switched off ($t_{dDOFF}$) and the supply input P-MOSFET ideal diode provides the load current. When forward biased, the ideal diodes regulate their forward voltage drop to 20mV typical ($V_{FR}$) when the MOSFET is sufficiently sized. If the voltage input falls and results in a forward voltage below 20mV, then the ideal diode will begin turning off at a slow rate. Should the ideal diode see a –18mV typical ($V_{REV}$) or lower reverse voltage, the ideal diode will turn off quickly ($t_{dDOFF}$).

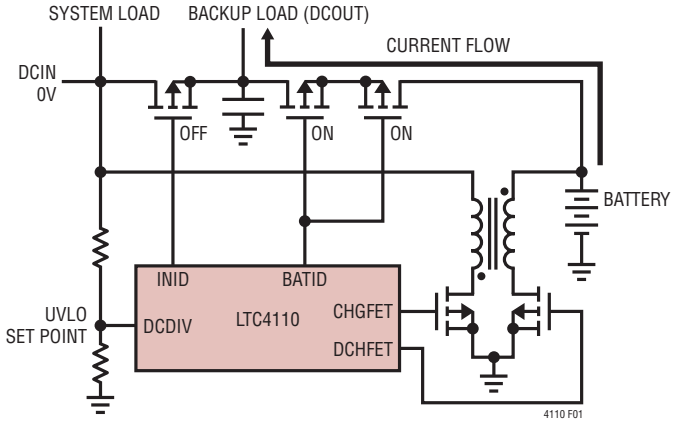



**Figure 1. Backup Mode Operation**

While in backup, the battery's average cell voltage is monitored to protect the battery from excessive discharge. If the cell voltage drops below the value programmed by the $V_{DIS}$ pin (Li-Ion default = 2.75V/cell, NiMH/NiCd default = 0.95V/cell, lead acid default = 1.93V/cell), the battery P-MOSFETs are rapidly turned off and the battery is disconnected from the load. If DCIN is above UVLO, the load and the LTC4110 will be powered from the supply input. If DCIN is below UVLO, the LTC4110 enters the micropower shutdown mode (see the Shutdown Mode section for more details). Also, the SMBus accessible BKUP_FLT fault bit is set and maintained as long as sufficient battery voltage is present ($V_{BAT} \geq 2.7V$). This fault bit can be read after DCIN returns to a voltage level exceeding the internal UVLO threshold (see $V_{UVI}$) and DCOUT has regained sufficient voltage (see DCOUT) to provide internal power. If the GPIO2 port is programmed as the BKUP_FLTb status output after DCIN returns, it will be forced low to represent an inverted BKUP_FLT bit. When DCIN returns, as sensed by the UVLO, the shutdown mode is automatically cancelled and normal operation can resume, however, the BKUP_FLT bit remains set until either the SHDN pin is set high (all registers reset) or register bits POR_RESET or BUFLT_RST are set. See the Shutdown Mode section for details. During backup, the external thermistor network is monitored for battery presence.

### BATTERY CHARGE MODE

Figure 2 shows the charge path to charge a battery. Current is pulled from the supply input to charge the battery. At the same time, the input supply provides power to both the system load and the backup load. The battery is isolated from the load at all times so it cannot affect charger terminations algorithms.

If we ignore battery chemistry for a moment, as far as the LTC4110 charger is concerned, there are only two basic charge modes. When the TYPE pin selects a standard battery mode, charge termination is controlled by the LTC4110

## OPERATION

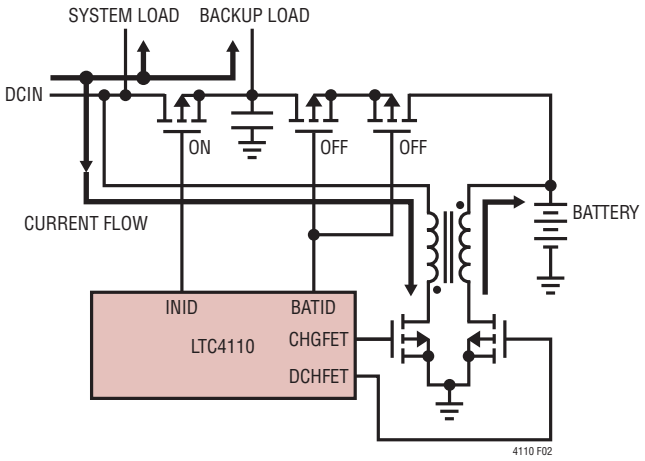



**Figure 2. Charge Mode Operation**

for the battery chemistry selected. Specifically the TIMER pin becomes active and used to detect faults conditions or terminate the charge cycle itself as needed. Smart battery SMBus charge control commands are still honored if any are sent at any time. A smart battery can safely function in a standard battery mode if identical in chemistry and voltage configuration as the standard battery. When the TYPE pin selects a smart battery mode, this simply disables the TIMER pin and its function in charge termination. The smart battery is able to restart or terminate a charge cycle at any time using charge commands over the SMBus. This mode also enables smart battery wake-up and watchdog functions based on $t_{TIMEOUT}$ per the smart battery standards. However it is not recommended to use a standard battery with a LTC4110 configured for smart battery mode operation. You can shorten battery life, damage or destroy the battery. In the extreme case this can cause an explosion since no charge termination mechanisms are active.

The following sections explain detailed operation for each charge mode as selected by the TYPE pin.

### STANDARD LI-ION/POLYMER BATTERY CHARGE MODE

The charger is programmed for standard Li-Ion batteries by connecting the TYPE pin to GND. During Li-Ion charging, the LTC4110 operates as a high efficiency, synchronous, PWM flyback battery charger with constant-current and constant float voltage regions of operation. The constant-charge current is programmed by the combination of a resistor ($R_{CHG}$) from the $I_{CHG}$ pin to ground, a battery current sense resistor ($R_{SNS(BAT)}$) and CSP/CSN pin resistors. The constant voltage (float voltage) is programmed to one of four values (4.2V, 8.4V, 12.6V, 16.8V) depending on the number of series cells using the SELC pin and can be adjusted ±0.3V/cell with the $V_{CHG}$ pin. If adjusted, the auto recharge threshold and overvoltage threshold will track proportionally.

The charge cycle begins when the supply input is present as sensed by the DCDIV pin and DCIN above UVLO, the battery cell voltage is below the auto recharge threshold (95% of the programmed float voltage; see $V_{AR}$), thermistor temperature is within ideal limits, COLD, under range (see SafetySignal Decoder section) or is optioned out and the register bit CHARGE_INHIBIT is cleared (see Tables 6 and 7 for register details).

Soft-start ramps the charge current at a rate set by the capacitor on the $I_{TH}$ pin. When charging begins, the programmable timer initiates timing and the CHGb (GPIO1 pin) status output is pulled LOW. An external capacitor on the TIMER pin, along with the current set by the total series resistance connected to the $V_{REF}$ pin, sets the total charge time.

If the battery voltage is less than the 3.0V/cell bulk charge threshold ($V_{BC}$), the charger will begin with a preconditioning trickle charge current. The trickle current is programmed by the resistor ($R_{PCC}$) from the $I_{PCC}$ pin to ground. During preconditioning trickle charging, if the battery voltage stays below the bulk charge threshold ($V_{BC}$) 25% of the programmed bulk charge time, the battery may be defective and the charge sequence will be terminated immediately. To indicate this fault, the CHGb (GPIO1 pin) becomes high impedance, the CHG_STATE_0 and CHG_STATE_1 register bits will be set low and CHG_FLT register bit will be set high. Charge is terminated and the timer reset until the fault is cleared by the RESET_TO_ZERO or POR_RESET SMBus write commands, SHDN pin toggle or the battery removed and replaced. Removing the supply input will not clear the fault if the battery is present.

If the battery voltage exceeds 107.5% ($V_{BOV}$) of the programmed float voltage during any stage of charge, the charger pauses until the voltage drops below the hysteresis ($V_{BOVH}$). The timer is not stopped and no fault is indicated.

## OPERATION

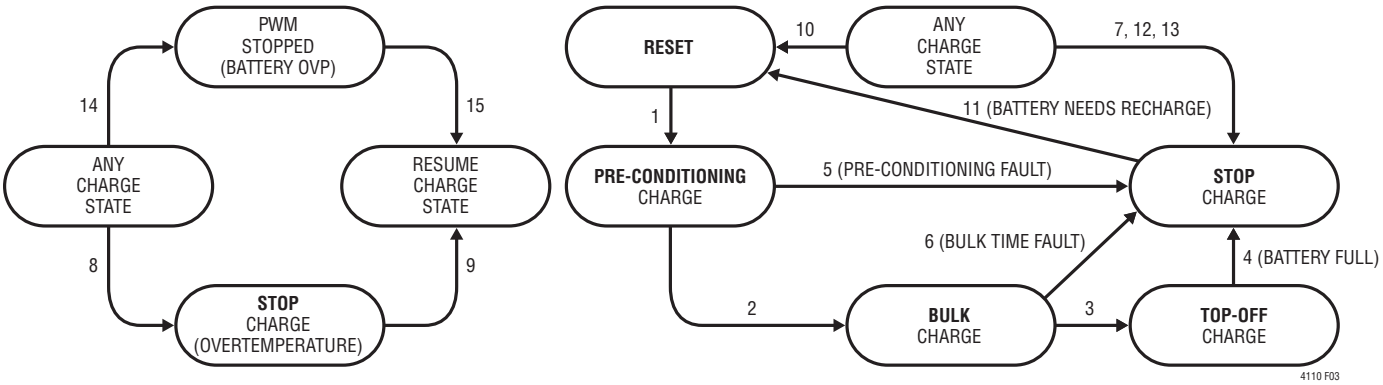



**Figure 3. Standard Li-Ion Charge State Diagram (Does Not Include Calibration)**

| # | Logic | Event (T = True, F = False) [Notes] | Notes and/or Actions (T = True, F = False) |
|---|---|---|---|
| 1 | | RES_OR = F & DCDIV pin = T & SHDN pin = F & CHARGE_INHIBITED = F & CHG_FLT = F & $V_{BAT} < V_{BC}$ | $I_{PPC}$ & Timer/4(PreCond) = Started & CHG = T & ALARM_INHIBITED = F |
| | Or | RES_OR = F & DCDIV pin = T & SHDN pin = F & CHARGE_INHIBITED = F & CHG_FLT=F & ChargingVoltage() ≠ 0 & ChargingCurrent() ≠ 0 | (RES_OR = F = Bat Inserted -> See ChargeStatus() )<br>(POR_RESET -> See ChargeMode() |
| 2 | | $V_{BAT} > V_{BC}$ | $I_{PPC}$ = Off & $I_{CHG}$ = On & Timer/4(PreCond) = Stopped & Timer(Bulk) = Started. |
| 3 | | C/5 = T | Timer(Bulk) = Stopped & Timer/4(Top Off) = Started |
| 4 | | Timer/4(Top Off = done [Battery is full] | $I_{CHG}$ = Off & CHG = F (Typical Full State) |
| 5 | | Timer/4(PreCond) = done before $V_{BAT} > V_{BC}$ | $I_{PPC}$ = Off & CHG_FLT = T & CHG = F |
| 6 | | Timer(Bulk) = done before C/5 = T | $I_{CHG}$ = Off & CHG_FLT = T & CHG = F |
| 7 | | RESET_TO_ZERO = T [See ChargeMode()] | $I_{CHG}$ or IPPC = Off & All Timers = Reset & CHG_FLT = F & CHG = F |
| | Or | CHARGE_INHIBIT=T [See ChargeMode()] | |
| 8 | | RES_HOT = T & RES_UR = F [See ChargeStatus()] | $I_{CHG}$ or $I_{PPC}$ = Off & CHG_FLT = T, Timers paused. |
| 9 | | RES_HOT = F [See ChargeStatus()] | $I_{CHG}$ or $I_{PPC}$ = On & CHG_FLT = F, Timers resume. |
| 10 | | DCDIV pin = F | $I_{CHG}$ or $I_{PPC}$ = Off & All Timers = Reset & ALARM_INHIBITED = F & CHG_FLT = F & CHG = F & CHARGE_INHIBITED = F |
| | Or | RES_OR = T [Bat Removed, See ChargeStatus()] | |
| | Or | SHDN pin = T | |
| | Or | $V_{UVD}$ = T | |
| | Or | POR_RESET = T [See ChargeMode()] | |
| 11 | | $V_{AR}$ = T [AutoRestart] | (The battery needs another charge cycle or Smart Battery has requested to start another cycle.) |
| | Or | ChargingVoltage() & ChargingCurrent() ≠ 0 | |
| 12 | | AlarmWarning() command is sent by Smart Battery over SMBus with any of the following bits set to True: | $I_{CHG}$ or $I_{PPC}$ = Off & All Timers = Reset & CHG = F & ALARM_INHIBITED = T |
| | | OVER_CHARGED_ALARM | |
| | Or | TERMINATE_CHARGE_ALARM | (ALARM_INHIBITED bit is found in ChargeStatus()) |
| | Or | Reserved ALARM | |
| | Or | OVER_TEMPERATURE_ALARM | |
| 13 | | ChargingVoltage() or ChargingCurrent() = 0 sent | $I_{CHG}$ or $I_{PPC}$ = Off & CHG = F |
| 14 | | $V_{BOV}$ = T [Battery Overvoltage] | PWM stopped. Timers remain running. |
| 15 | | $V_{BOV}$ = F | PWM restarted. |

Note: For all charge states, $V_{CHG}$ is always active.

## OPERATION

When the battery voltage exceeds the bulk charge threshold ($V_{BC}$), the charger begins the bulk charge portion of the charge cycle. As the battery accepts charge, the voltage increases. Constant-current charge continues until the battery approaches the constant voltage. At this time, the charge current will begin to drop, signaling the beginning of the constant-voltage portion of the charge cycle.

The charger will maintain the constant voltage across the battery until either C/x is reached or 100% of the programmed bulk charge time has elapsed during bulk charge. When the current drops to approximately 20% of the full-scale charge current, an internal C/x comparator will initiate the start of the top-off stage. The top-off stage charges for 25% of the total programmed bulk charge time. When the time elapses, charge is terminated and CHGb (GPIO1 pin) is forced to a high impedance state and CHG_STATE_0 and CHG_STATE_1 register bits will be set low. Should the total bulk charge time elapse before C/x is reached, charge is terminated and a CHG_FLT fault is indicated until cleared by the RESET_TO_ZERO or POR_RESET SMBus write commands, SHDN pin toggle or the battery removed and replaced. Fault conditions are not cleared when the supply input is removed if the battery has sufficient voltage.

An optional external thermistor network is sampled at regular intervals to monitor battery temperature and to detect battery presence. If the thermistor temperature is hot (see the SafetySignal Decoder section), the charge timer is paused, charge current is halted, CHG_FLTb (GPIO3 pin) is forced low and the CHG_FLT bit will be set high. CHGb (GPIO1 pin) , CHG_STATE_0 and CHG_STATE_1 register bits will not be affected. When the thermistor value returns to an acceptable value, charging resumes, CHG_FLTb (GPIO3 pin) returns to high impedance and the CHG_FLT bit will be reset low. An open thermistor indicates absence of a battery. To defeat the temperature monitoring function, replace the thermistor with a resistor to indicate ideal battery temperature. When a thermistor is not used, the resistor circuit must be routed through the battery connector if battery presence detection is required.

After a charge cycle has ended without fault, the charge cycle is automatically restarted if the average battery cell voltage falls below the auto recharge threshold. At any time charging can be forced to stop by pulling the SHDN pin high or setting the CHARGE_INHIBIT bit high through the SMBus.

### SMART BATTERY CHARGE MODE

This section explains operation for smart batteries with a SMBus interface. Smart Li-Ion is selected by connecting the TYPE pin to the $V_{DD}$ pin and smart Nickel (NiMH/NiCd) is selected by connecting the TYPE pin to the $V_{REF}$ pin. The LTC4110 only implements a subset of smart battery charger commands; the actual charging algorithm is determined by LTC4110 through external resistors even if the battery is “smart.”

The LTC4110 operates as a high efficiency, synchronous, PWM flyback battery charger with constant current and constant float voltage regions of operation. The constant-charge current is programmed by the combination of a resistor ($R_{CHG}$) from the $I_{CHG}$ pin to ground, a battery current sense resistor ($R_{SNS(BAT)}$) and CSP/CSN pin resistors. For Li-Ion the constant voltage (float voltage) is programmed to one of four values (4.2V, 8.4V, 12.6V, 16.8V) depending on the number of series cells using the SELC pin and can be adjusted ±0.3V/cell with the $V_{CHG}$ pin. For nickel batteries the constant-voltage function is not used, however, a non-zero value is still required to be written to the ChargingVoltage() register. The internal auto recharge function is inhibited for smart batteries.

If the battery voltage exceeds 107.5% ($V_{BOV}$) of the programmed float voltage during any stage of charge, the charger pauses until the voltage drops below the hysteresis ($V_{BOVH}$). The timer is not stopped and no fault is indicated. This function is disabled when nickel based smart batteries are used.

There are four states associated with smart battery charge mode, namely:

- SMBus Wake-Up Charge State
- SMBus Preconditioning Charge State
- SMBus Bulk Charge State
- SMBus OFF State

These states are explained in the following four sections.

## OPERATION

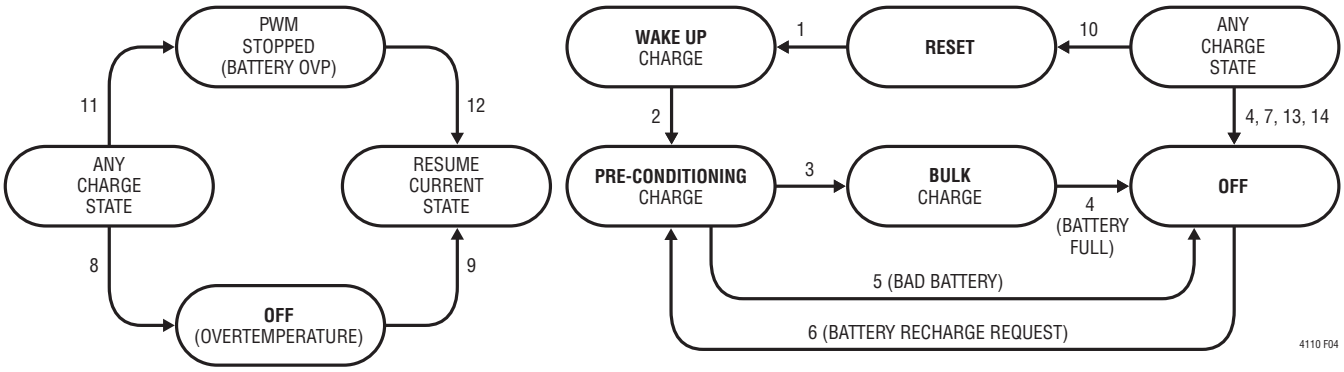



**Figure 4. Smart Battery Charge State Diagram (Does Not Include Calibration)**

| # | Logic | Event (T = True, F = False) [Notes] | Notes and/or Actions (T = True, F = False) |
|---|---|---|---|
| 1 | <br><br>Or | RES_OR = F & DCDIV pin = T & SHDN pin = F & CHARGE_INHIBITED = F & CHG_FLT = F & RES_HOT = F<br><br>RES_OR = F & DCDIV pin = T & SHDN pin = F & CHARGE_INHIBITED = F & CHG_FLT = F & RES_HOT = T & RES_UR = T | $I_{PPC}$ = On (Constant Current only) & TTIMEOUT = Started & CHG = T |
| 2 | | ChargingVoltage() & ChargingCurrent() ≠ 0 sent | Timer/4(Pre-Charge) = Started & TTIMEOUT disabled & ALARM_INHIBITED = F |
| 3 | | $V_{BAT} > V_{BC}$ | $I_{PPC}$ = Off, $I_{CHG}$ = On, Timer/4(Pre-Charge) = Stopped & Timer(SMBus) = Started |
| 4 | | ChargingVoltage() or ChargingCurrent() = 0 sent | $I_{CHG}$ = Off & All Timers = Reset & CHG = F |
| 5 | | Timer/4(Pre-Charge) = Done before $V_{BAT} > V_{BC}$ | $I_{PPC}$ = Off & All Timers = Reset & CHG = F |
| 6 | | ChargingVoltage() & ChargingCurrent() ≠ 0 sent & RES_OR = F & DCDIV pin = T & SHDN pin = F & CHARGE_INHIBITED = F & CHG_FLT = F | $I_{PPC}$ = On & Timer/4(Pre-Charge) = Started & CHG = T & ALARM_INHIBITED = F |
| 7 | | TTIMEOUT = Done (Dead Battery or Loss of SMBus) | $I_{CHG}$ = Off & All Timers Reset & CHG = F |
| 8 | | RES_HOT = T & RES_UR = F [See ChargeStatus()] | $I_{CHG}$ or $I_{PPC}$ = Off & CHG_FLT = T, Timer = Paused. |
| 9 | | RES_HOT = F [See ChargeStatus()] | $I_{CHG}$ or $I_{PPC}$ = On & CHG_FLT = F, Timer = Resume. |
| 10 | <br>Or<br>Or<br>Or<br>Or | DCDIV pin = F<br>RES_OR = T [Bat Removed, See ChargeStatus()]<br>SHDN pin = T<br>$V_{UVD}$ = T<br>POR_RESET = T [See ChargeMode()] | $I_{CHG}$ or $I_{PPC}$ = Off & All Timers = Reset & CHG_FLT = F & CHG = F & ALARM_INHIBITED = F & CHARGE_INHIBITED = F |
| 11 | | $V_{BOV}$ = T [Battery Overvoltage] | PWM stopped. Timers remain running. |
| 12 | | $V_{BOV}$ = F | PWM restarted. |
| 13 | <br>Or | RESET_TO_ZERO = T [See ChargeMode()]<br>CHARGE_INHIBIT = T [See ChargeMode()] | $I_{CHG}$ or $I_{PPC}$ = Off & All Timers = Reset & CHG_FLT = F & CHG = F |
| 14 | <br><br>Or<br>Or<br>Or | AlarmWarning() command is sent by Smart Battery over SMBus with any of the following bits set to True:<br>OVER_CHARGED_ALARM<br>TERMINATE_CHARGE_ALARM<br>Reserved ALARM<br>OVER_TEMPERATURE_ALARM | $I_{CHG}$ or $I_{PPC}$ = Off. & All Timers = Reset & CHG = F & ALARM_INHIBITED = T<br><br>(ALARM_INHIBITED bit is found in ChargeStatus()) |

Note: $V_{CHG}$ is active in all charge states except for nickel batteries which operate in constant current mode.

## OPERATION

### SMBUS WAKE-UP CHARGE STATE

The battery will be charged with a fixed "wake-up" current regardless of previous ChargingCurrent() and ChargingVoltage() register values during wake-up charging. The current is identical to the preconditioning charge current which is programmed with an external resistor through the $I_{PCC}$ pin. The wake-up timer has the same period as $t_{TIMEOUT}$, typically 175sec (see $t_{TIMEOUT}$).

The following conditions must be met to allow wake-up charge of the battery:

- The SafetySignal must be RES_COLD, RES_IDEAL, or RES_UR.
- AC must be present. This is qualified by DCDIV > $V_{AC}$ + $V_{ACH}$ and DCIN above UVLO.
- Wake-up charge initiates if a battery does not write non-zero values to ChargingCurrent() and ChargingVoltage() registers when AC power is applied and a battery is present or when AC is present and a battery is subsequently connected.

The following conditions will terminate the wake-up charge state and end charge attempts, unless otherwise noted.

- The $t_{TIMEOUT}$ period is reached (see $t_{TIMEOUT}$) when the SafetySignal is RES_COLD or RES_UR. The state machine will go to the SMBus OFF state. The CHG_FLT bit is not set.
- The SafetySignal is registering RES_HOT. The state machine will go to the SMBus OFF state.
- The SafetySignal is registering RES_OR. The state machine will go to the reset state.
- The LTC4110 will leave the wake-up charge state and go into the SMBus preconditioning charge state if the ChargingCurrent() AND ChargingVoltage() registers have been written to non-zero values.
- The AC power is no longer present (DCDIV < $V_{AC}$ or DCIN below UVLO). The state machine will go to the reset state.
- The ALARM_INHIBITED becomes set in the ChargerStatus() register. The state machine will go to the SMBus OFF state.
- CHARGE_INHIBIT is set in the BBuControl() register. Charge is stopped, however, the wake-up timer is not paused. Clearing CHARGE_INHIBIT will enable the LTC4110 to resume charging.
- There is insufficient DCIN voltage to charge the battery as determined by the internal UVLO. This causes the state machine to enter the reset state and stop all charge activity. The LTC4110 will resume wake-up charging when there is sufficient DCIN voltage to charge the battery.
- The CAL_START bit in the BBuControl() register is set. Charge is stopped and the LTC4110 enters the calibration state.
- Writing a zero value to either the ChargingVoltage() or ChargingCurrent() register. The state machine will go to the SMBus OFF state.
- RESET_TO_ZERO is set in the BBuControl() register. Charge is stopped; the SMBus OFF State is entered.

### SMBUS PRECONDITIONING CHARGE STATE

During the SMBus preconditioning charge state, the charger will be operating in the preconditioning charge current limit. The following conditions must be met in order to allow SMBus preconditioning charge to start:

- The ChargingVoltage() AND ChargingCurrent() registers must be written to non-zero values. The LTC4110 will not directly report the status of these registers. The battery needs only write one pair of ChargingVoltage() and ChargingCurrent() registers to stay in this state. The $t_{TIMEOUT}$ timer is not operational in SMBus preconditioning charge state.
- The SafetySignal must be RES_COLD, RES_IDEAL, or RES_UR.
- AC must be present and sufficient. This is qualified by DCDIV > $V_{AC}$ + $V_{ACH}$ and DCIN > UVLO.

The following conditions will affect the SMBus preconditioning charge state as specified below:

- The SafetySignal is registering RES_HOT. Charge is stopped; the SMBus OFF state is entered.

## OPERATION

- The SafetySignal is registering RES_OR. Charge is stopped. The LTC4110 enters the reset state.
- The AC power is no longer present (DCDIV < $V_{AC}$ or DCIN < UVLO). The LTC4110 enters the reset state.
- ALARM_INHIBITED is set in the ChargerStatus() register. Charge is stopped. The LTC4110 enters the SMBus OFF state.
- CHARGE_INHIBIT is set in the BBuControl() register. Charge is stopped, however, the T/4 timer is not paused. Clearing CHARGE_INHIBIT will enable the LTC4110 to resume charge.
- RESET_TO_ZERO is set in the BBuControl() register. Charge is stopped. The LTC4110 enters the SMBus OFF state.
- Writing a zero value to ChargeVoltage() or ChargeCurrent() register. Charge is stopped. The LTC4110 enters the SMBus OFF state.
- If the battery voltage exceeds the bulk charge threshold, the LTC4110 will enter the SMBus bulk charge state.
- If the T/4 timeout occurs, charge is stopped and the LTC4110 enters the SMBus OFF state.
- The CAL_START bit in the BBuControl() register is set. Charge is stopped and the LTC4110 enters the calibration mode.

### SMBus BULK CHARGE STATE

The charger will be operating in the bulk charge current limit during the SMBus bulk charge state. The following conditions must be met in order to allow SMBus bulk charge to start:

- The ChargeVoltage() AND ChargeCurrent() registers must be written to non-zero values. The LTC4110 will not directly report the status of these registers.
- The SafetySignal must be RES_COLD, RES_IDEAL, or RES_UR.
- AC must be present and sufficient. This is qualified by DCDIV > $V_{AC}$ + $V_{ACH}$ and DCIN > UVLO.

The following conditions will affect the SMBus bulk charge state as specified below:

- The ChargeCurrent() AND ChargeVoltage() registers have not been written for $t_{TIMEOUT}$. Charge is stopped and the LTC4110 enters the SMBus OFF state.
- The SafetySignal is registering RES_OR. Charge is stopped and the LTC4110 enters the reset state.
- The SafetySignal is registering RES_HOT. Charge is stopped and the LTC4110 enters the SMBus OFF state.
- The AC power is no longer present (DCDIV < $V_{AC}$ or DCIN < UVLO). Charge is stopped and the LTC4110 enters the reset state.
- ALARM_INHIBITED is set in the ChargerStatus() register. Charge is stopped and the LTC4110 enters the SMBus OFF state.
- CHARGE_INHIBIT is set in the BBuControl() register. Charge is stopped. Clearing CHARGE_INHIBIT will enable the LTC4110 to resume charge. The $t_{TIMEOUT}$ timer does not pause when CHARGE_INHIBIT is set.
- RESET_TO_ZERO is set in the BBuControl() register. The LTC4110 enters the SMBus OFF state.
- Writing a zero value to the ChargeVoltage() or to the ChargeCurrent() register. Charge is stopped and the LTC4110 enters the SMBus OFF state.
- The CAL_START bit in the BBuControl() register is set. Charge is stopped and the LTC4110 enters the calibration mode.

### SMBus OFF STATE

This state is different from the reset state in that all charge is disallowed regardless of the value of the thermistor. The following conditions will affect the SMBus OFF state as specified below:

- The ChargeCurrent() AND ChargeVoltage() registers have both been written to non-zero values, the battery thermistor is registering RES_COLD, RES_IDEAL or RES_UR and CHARGE_INHIBT is clear. The LTC4110 enters the SMBus preconditioning charge state.

## OPERATION

- The CAL_START bit in the BBuControl() register is set. The LTC4110 enters the calibration state.
- The battery thermistor is registering RES_OR. The LTC4110 enters the reset state.

### LEAD ACID BATTERY CHARGE MODE

The charger is programmed for lead acid batteries by connecting the TYPE pin to a voltage derived from the $V_{REF}$ pin resistor divider of nominally 0.5 • $V_{REF}$. During charge, the LTC4110 operates as a high efficiency, synchronous, PWM flyback battery charger with constant current and constant float voltage regions of operation. The constant-charge current is programmed by the combination of a resistor ($R_{CHG}$) from the $I_{CHG}$ pin to ground, a battery current sense resistor ($R_{SNS}$) and CSP/CSN pin resistors. The float voltage is programmed to one of four values (4.7V, 7.05V, 11.75V, 14.1V) depending on the number of series cells (2, 3, 5 or 6) using the SELC pin and can be adjusted ±0.15V/cell with the $V_{CHG}$ pin.

A new charge cycle begins with the charger in the bulk charge current limited state. In this state, the charger is a current source providing a constant charge rate and the CHGb (GPIO1 pin) is forced low. No time limits are placed upon lead acid battery charge. The charger monitors the battery voltage and as it reaches the float voltage the charger begins its float charge. While in float, the charge current diminishes as the battery accepts charge. Float voltage temperature compensation and temperature fault monitoring, if desired, are accomplished with an external thermistor network.

Charge is active when the supply input is present as sensed by the DCDIV pin and DCIN above UVLO, thermistor temperature is ideal according to the thermistor monitor circuit (see SafetySignal Decoder) and the charge register bit CHARGE_INHIBIT is cleared. Soft-start ramps the charge current at a rate set by the capacitor on the $I_{TH}$ pin. When charge begins, the CHGb (GPIO1 pin) status output is forced to GND. At any time charge can be forced to stop by pulling the SHDN pin high or setting the CHARGE_INHIBIT bit high through the SMBus.

If the battery voltage exceeds 107.5% ($V_{BOV}$) of the programmed float voltage during any stage of charge, the charger pauses until the voltage drops below the hysteresis ($V_{BOVH}$). No fault is indicated.

An optional external NTC thermistor network can be used to provide an adjustable negative TC for the float voltage, monitor battery temperature and to detect battery presence. If the thermistor value indicates a hot temperature, voltage falling to $V_{HOT}$ on THB pin, charge current is halted, CHG_FLTb (GPIO3 pin) is forced low and the CHG_FLT bit will be set high. CHGb (GPIO1 pin) and CHG_STATE_0 and CHG_STATE_1 register bits will not be affected. When the thermistor value returns to ideal when the voltage exceeds $V_{HOT}$ +$V_{HOTH}$ on THB pin, charge resumes CHG_FLTb (GPIO3 pin) returns to high impedance and the CHG_FLT bit will be reset low. An open thermistor indicates an over-range which is considered absence of a battery. Low temperature is not monitored. However, since battery removal detection looks at the thermistor for a high resistance ($V_{REM}$ on THB pin), extremely cold temperatures may result in an indication of battery absence. To defeat the temperature monitoring register, replace the thermistor with a resistor to indicate normal battery temperature. When a thermistor is not used the resistor circuit must be routed through the battery connector if battery presence detection is required.

### BATTERY CALIBRATION MODE

Figure 6 shows the LTC4110 in battery calibration mode and the corresponding PowerPath enabled. During calibration, the host CPU can calibrate a gas gauge or verify the battery's ability to support a load by use of a low heat producing method. Calibration requires a host to communicate over a SMBus. In the low heat method, a synchronous PWM flyback charger is used in reverse to discharge the battery with a programmable constant-current into the system load thereby saving space and eliminating heat generation compared with resistive loads. Protection circuits prevent accidental overdrive back into the power source if the system load is insufficient. The constant-charge current is programmed by the combination of a resistor ($R_{CAL}$) from the $I_{CAL}$ pin to ground, a battery current sense resistor ($R_{SNS(BAT)}$) and CSP/CSN pin resistors. Calibration is initiated by setting the CAL_START bit in the BBuControl() register. The CAL_ON bit in the BBuStatus() register will

## OPERATION

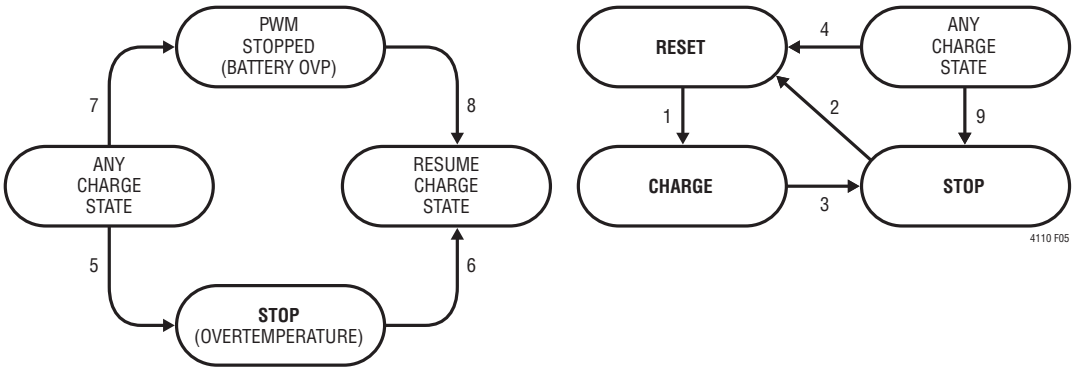



**Figure 5. SLA Charge State Diagram (Does Not Include Calibration)**

| # | Logic | Event (T = True, F = False) [Notes] | Notes and/or Actions (T = True, F = False) |
|---|---|---|---|
| 1 | | RES_OR = F & DCDIV pin = T & SHDN pin = F & CHARGE_INHIBITED = F & CHG_FLT = F | $I_{CHG}$ = On & CHG = T |
| 2 | Or | $V_{AR}$ = T [AutoRestart]<br>ChargingVoltage() & ChargingCurrent() ≠ 0 sent | ALARM_INHIBITED = F |
| 3 | Or<br>Or | ChargingVoltage() or ChargingCurrent() = 0 sent<br>RESET_TO_ZERO = T [See ChargeMode()]<br>CHARGE_INHIBIT = T [See ChargeMode()] | $I_{CHG}$ = Off & CHG = F |
| 4 | Or<br>Or<br>Or<br>Or | DCDIV pin = F<br>RES_OR = T [Bat Removed, See ChargeStatus()]<br>SHDN pin = T<br>$V_{UVD}$ = T<br>POR_RESET = T [See ChargeMode()] | $I_{CHG}$ = Off & CHG = F & CHARGE_INHIBITED = F & ALARM_INHIBITED = F |
| 5 | | RES_HOT = T & RES_UR = F [See ChargeStatus()] | $I_{CHG}$ = Off & CHG_FLT = T |
| 6 | | RES_HOT = F [See ChargeStatus()] | $I_{CHG}$ = On & CHG_FLT = F |
| 7 | | $V_{BOV}$ = T | PWM stopped. Timers remain running. |
| 8 | | $V_{BOV}$ = F | PWM restarted. |
| 9 | Or<br>Or<br>Or | AlarmWarning() command is sent by Smart Battery over SMBus with any of the following bits set to True:<br>OVER_CHARGED_ALARM<br>TERMINATE_CHARGE_ALARM<br>Reserved ALARM<br>OVER_TEMPERATURE_ALARM | $I_{CHG}$ = Off & CHG = F & ALARM_INHIBITED = T<br><br>(ALARM_INHIBITED bit is found in ChargeStatus()) |

Note: For all charge states, $V_{CHG}$ is always active

be set to indicate calibration in progress. Soft-start ramps the discharge current at a rate set by the capacitor on the $I_{TH}$ pin (typically 10ms with 0.1µF capacitor). A limit to how far the battery cell voltage will be discharged during calibration can be programmed with the $V_{CAL}$ pin (Li-Ion default = 2.75V/cell, lead acid default = 1.93V/cell, Smart NiMH/NiCd default = 0.95V/cell). When the limit is reached calibration is terminated, the CAL_COMPLETE bit in the BBuStatus() register is set, the CAL_ON bit in the BBuStatus() register will be cleared and the charge mode is automatically entered to begin recharging the battery. If the GPIO3 is configured as a calibration complete status output (CAL_COMPLETEb), it will be forced low until reset by the CAL_RESET write bit. Calibration is inhibited during backup or shutdown modes. Calibration is also inhibited when a thermistor is sensed absent.

During calibration, user-programmable supply back-drive protections are provided. These protections prevent a reversal of current into the main supply and/or possibly raising the supply voltage to unsafe levels should the

## OPERATION

system load not be adequate to absorb the current. The primary protection is accomplished with an external current sense resistor ($R_{CL}$), connected between the CLP and CLN pins, through which the system load current flows. When the voltage across the resistor reaches 10mV ($I_{BDT}$) or less, representing a low forward current, calibration mode is terminated. The current protection can be completely disabled by connecting both CLP and CLN pins to GND. As an alternative where $R_{CL}$ sensing is not an option for the application, a secondary method is accomplished by monitoring the supply voltage through the DCDIV pin. Once the DCDIV pin voltage goes above $V_{OVP}$, calibration mode is terminated. In either case, the CAL_FLT register is set high and the charge mode is automatically entered to begin recharging the battery. Both of these protections are automatically disabled when not in calibration. However, in calibration, *one or the other* of these two protective methods *should* be used. You can optionally do both. Failure to implement any form of protection can result in destructive voltages being generated in the application.

If the calibration cycle fails due to loss of the main power source a fault condition results that sets the CAL_FLT register bit and backup mode is entered.

An optional external thermistor network is sampled at regular intervals to monitor battery temperature and to detect battery presence. If the thermistor value indicates a temperature outside of ideal limits (hot or over-range) the calibration current is halted and the CAL_FLT bit will be set high. When the thermistor value returns to an acceptable value (under-range, cold or ideal), charge mode is automatically entered to begin recharging the battery. Calibration can be restarted by clearing the CAL_FLT bit and sending another CAL_START command.

An open thermistor (over-range) indicates absence of a battery. To defeat the temperature monitoring function, replace the thermistor with a resistor to indicate ideal battery temperature. When a thermistor is not used, the resistor circuit must be routed through the battery connector if battery presence detection is required. If the battery should be removed during calibration, calibration will terminate and the CAL_FLT read bit will be set high.

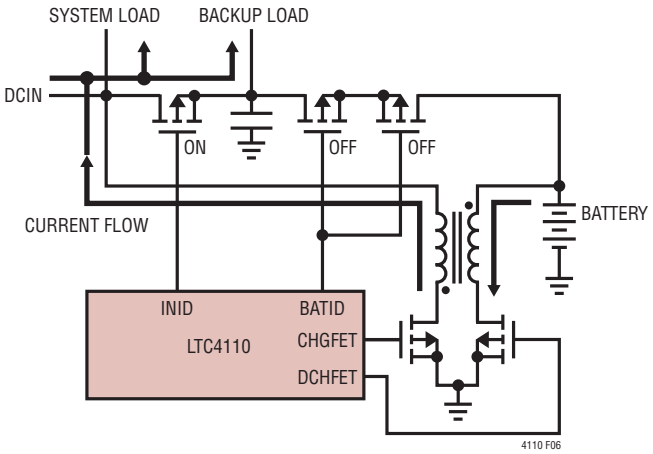



**Figure 6. Calibration Mode Operation**

The CAL_FLT bit can be cleared by writing a one to the CAL_RESET or POR_RESET registers, or by forcing the SHDN pin high. The CAL_FLT bit is not cleared by removing and reapplying the supply input if the battery has maintained sufficient voltage ($V_{BAT} \geq 2.7V$).

Calibration can start only if the CAL_FLT bit in the BBuStatus() register is clear. Once the LTC4110 is in calibration state, the following events will stop calibration:

- BKDRV is sensed. The CAL_FLT bit is set.
- A HOT thermistor is sensed. The CAL_FLT bit is set.
- Loss of battery presence is sensed. The CAL_FLT bit is set.
- The calibration cutoff threshold has been reached. The CAL_COMPLETE bit is set. The LTC4110 will start charging based upon the TYPE and SELA pins.
- An OVER_TEMP_ALARM, RESERVED_ALARM, or TERMINATE_DISCHARGE_ALARM bit in the AlarmWarning() register is set. The CAL_FLT bit is set. The LTC4110 will start charging.
- Loss of AC presence. The CAL_FLT bit is set.

### SHUTDOWN MODE

The LTC4110 can be forced into either a micropower shutdown state or an all logic register reset state with the SHDN pin.

## OPERATION

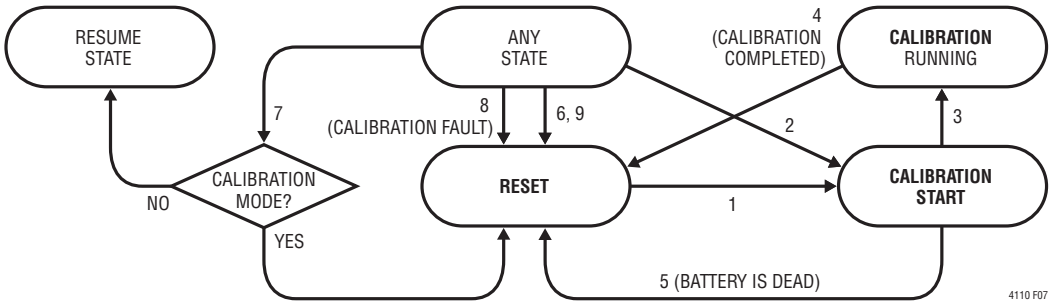



**Figure 7. Calibration State Diagram**

| # | Logic | Event (T = True, F = False) [Notes] | Notes and/or Actions (T = True, F = False) |
|---|---|---|---|
| 1 | | RES_OR = F & DCDIV pin = T & SHDN pin = F & CAL_FLT = F & CAL_START = T | CAL_COMPLETE = F<br>(Calibration started while in Reset {Idle or Cold Power-Up}) |
| 2 | | RES_OR = F & DCDIV pin = T & SHDN pin = F & CAL_FLT = F & CAL_START = T | $I_{CHG}$ or IPPC = Off & All Timers = Reset & CAL_COMPLETE = F<br>(Calibration was initiated while in any mode other than Reset.) |
| 3 | | [Calibration Automatically Started] | $I_{CAL}$ = ON & CAL_ON = T |
| 4 | | $V_{BAT} < V_{CAL}$ [Battery has reached Discharge] | $I_{CAL}$ = Off & CAL_ON = F & CAL_COMPLETE = T<br>(Normal Calibration Cycle) |
| 5 | | $V_{BAT} < V_{CAL}$ [Battery is Discharged] | CAL_COMPLETE = T<br>(Battery is already discharged. Cancel Calibration.) |
| 6 | | AlarmWarning() command is sent by Smart Battery over SMBus with any of the following bits set to True:<br>OVER_TEMP_ALARM or Reserved ALARM or TERMINATED_DISCHARGE_ALARM] | $I_{CAL}$ = Off & CAL_ON = F & ALARM_INHIBITED = T<br><br>(ALARM_INHIBITED bit is found in ChargeStatus()) |
| 7 | | CAL_RESET = T | $I_{CAL}$ = Off & CAL_ON = F & CAL_COMPLETE = F & CAL_FLT = F |
| 8 | <br>Or<br>Or<br>Or | RES_HOT = T & RES_UR = F [See ChargeStatus()]<br>RES_OR = T [Bat Removed, See ChargeStatus()]<br>$V_{OVP}$ = T [Output Over-Voltage condition sensed)]<br>$I_{BDT}$ = T [Output Back Drive Current condition sensed)] | $I_{CAL}$ = Off & CAL_ON = F & CAL_FLT = T |
| 9 | <br>Or<br>Or<br>Or | DCDIV pin = F<br>SHDN pin = T<br>$V_{UVD}$ = T<br>POR_RESET = T [See ChargeMode()] | $I_{CAL}$ = Off & CAL_ON = F & ALARM_INHIBITED = F & CHARGE_INHIBITED = F |

### REGISTER RESET STATE

The SHDN pin will reset all logic registers when taken high, but only if DCIN is present as determined by DCDIV > $V_{AC}$ + $V_{ACH}$ and DCIN above UVLO. Micropower shutdown state will not be entered, but the LTC4110 will be idle and not able to enter charge or calibration modes. If SHDN is switched low then normal operation will resume.

While in register reset state, charge and calibration modes are inhibited, and all registers including the backup fault bit register are set to their default states and the internal timer is reset. The status pin ACPb is active, but GPIO1, GPIO2 and GPIO3 are reset to their default states. The SMBus is enabled, however, it is not able to communicate with the LTC4110. The DCIN to DCOUT PowerPath controller is functional and the $V_{DD}$ and $V_{REF}$ pin voltages remain.

### MICROPOWER SHUTDOWN STATE

If the SHDN pin remains high when DCIN is removed as detected by the undervoltage lockout UVLO (see $V_{UVD}$), micropower shutdown is entered, battery backup mode is inhibited and all registers are reset. During this condition, the level of the SHDN pin is ignored and has no effect.

## OPERATION

The micropower shutdown state will be maintained if the DCIN supply is removed and sufficient battery voltage is present ($V_{BAT} \geq 2.7V$). When DCIN is reapplied as detected by the UVLO (see $V_{UVI}$), regardless of the level of the SHDN pin, the shutdown state is automatically cancelled. Register reset state is cancelled until DCIN is reapplied as determined by the DCDIV pin.

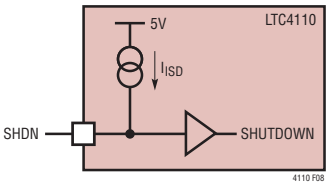



**Figure 8. Shutdown Control Input**

In shutdown; charge, calibration and backup modes are inhibited, all registers are set to their default states (with exception of the backup fault bit register), the internal timer is reset and oscillator disabled, the status pins; ACPb, GPIO1, GPIO2 and GPIO3 are a high impedance and the LTC4110 is put into a micropower state. While in shutdown the SMBus is disabled and the SDA and SCL pins are high impedance. In addition, the shutdown state will disconnect loads from the battery to prevent its discharge as follows:

- The BATID pin is forced to the battery voltage to turn off the battery P-MOSFETs for isolation of the load from the battery
- The CHGFET and DCHFET pins are forced to GND to turn off the flyback switcher N-MOSFETs
- Current into the BAT pin is minimized. Also the $V_{DD}$ and $V_{REF}$ pin voltages will fall to zero.

While in shutdown, the LTC4110 will draw a small current from battery ($I_{BSD}$) if the DCIN supply is absent. If the SHDN pin is open an internal weak pull-up current ($I_{ISD}$) pulls the pin voltage up thereby entering the shutdown state.

### PWM OPERATION

A conceptual diagram of the LTC4110 PWM engine is shown in Figure 9.

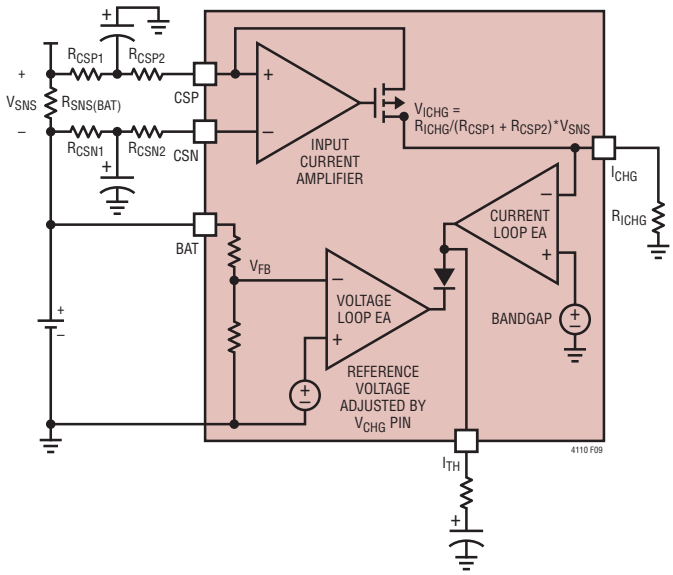



**Figure 9. LTC4110 PWM Engine**

The voltage across the external current programming resistor $R_{SNS(BAT)}$ is averaged by the RC network connected to the CSP and CSN pins and then amplified by a ratio of $R_{ICHG}/(R_{CSP1} + R_{CSP2})$. This amplified voltage is compared with the bandgap reference through the current loop error amplifier to adjust the $I_{TH}$ pin which sets the current comparator threshold to maintain a constant charging current. Once the battery voltage rises to close to the programmed float voltage, the voltage loop error amplifier gradually pulls the $I_{TH}$ pin low, reduces the charging current and maintain a constant voltage charging.

### C/x CHARGE TERMINATION

LTC4110 monitors the charging current through the voltage on the $I_{CHG}$ pin, once the current drops below 20% of the bulk charging current, an internal C/x comparator is tripped, and the LTC4110 will enter top-off charge stage if standard Li-Ion battery mode is selected or release the GPIO1 pin if no-host SLA battery mode is selected. The actual x value depends on the programmed charging current and the C rate of the battery.

$$x = \frac{C}{I_{CHG}} \bullet 5$$

## OPERATION

Where:

C = C rate of the battery

$I_{CHG}$ = Programmed charging current

For Example, if we charge a 3Ah battery with 1A current, then x = 15.

### SAFETYSIGNAL DECODER

**Table 3. SafetySignal State Ranges (Except SLA)**

| SafetySignal CHARGE RESISTANCE | CHARGE STATUS BITS | DESCRIPTION |
|---|---|---|
| 0Ω to 500Ω | RES_UR, RES_HOT, BATTERY_PRESENT | Under range |
| 500Ω to 3k | RES_HOT, BATTERY_PRESENT | Hot |
| 3kΩ to 30k | BATTERY_PRESENT | Ideal |
| 30k to 100k | RES_COLD, BATTERY_PRESENT | Cold |
| Above 100k | RES_OR, RES_COLD | Overrange |

Note: The under range detection scheme is a very important feature of the LTC4110. The $R_{THA}/R_{SafetySignal}$ divider trip point of 0.307 • 4.75V = 1.46V is well above the 0.047 • $V_{DD}$ = 140mV threshold of a system using a 10k pull-up. A system using a 10k pull-up would not be able to resolve the important under range to a hot transition point with a modest 100mV of ground offset between battery and SafetySignal detection circuitry. Such offsets are anticipated when charging at normal current levels.

**Table 4. SafetySignal for SLA (7.256k Between THA and THB)**

| SafetySignal CHARGE RESISTANCE | CHARGE STATUS BITS | DESCRIPTION |
|---|---|---|
| 0Ω to 3.1k | RES_HOT, BATTERY_PRESENT | Hot |
| 3.1k to 114k | BATTERY_PRESENT | Ideal |
| 114k | RES_COLD, RES_OR | Battery Removal |

This decoder measures the resistance of the SafetySignal and features high noise immunity at critical trip points. The SafetySignal decoder is shown in Figure 10.

The value of $R_{THA}$ is 1.13k and $R_{THB}$ is 54.9k. SafetySignal sensing is accomplished by a state machine that reconfigures the switches of Figure 10 using THA_SELB and THB_SELB, a selectable reference generator, and two comparators. The state machine successively samples the SafetySignal value starting with the RES_OR ≥ RES_COLD threshold,

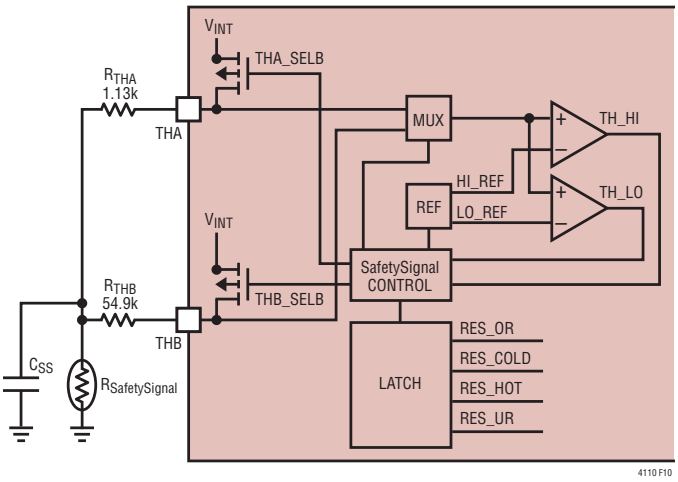



**Figure 10. Battery Safety Decoder (Except SLA)**

then RES_COLD ≥ RES_IDEAL threshold, RES_IDEAL ≥ RES_HOT threshold, and finally the RES_HOT ≥ RES_UR threshold. Once the SafetySignal range is determined, the lower value thresholds are not sampled. The SafetySignal decoder block uses the previously determined SafetySignal value to provide the appropriate adjustment in threshold to add hysteresis. The $R_{THB}$ resistor value is used to measure the RES_OR ≥ RES_COLD and RES_COLD ≥ RES_IDEAL thresholds by connecting the THB pin to an internal voltage and measuring the voltage resultant on the THA pin. The $R_{THA}$ resistor value is used to measure the RES_IDEAL ≥ RES_HOT and RES_HOT ≥ RES_UR thresholds by connecting the THA pin to the internal voltage and measuring the resultant voltage on the THB pin. The SafetySignal impedance is interpreted according to Table 3.

When the DCIN supply is present, a full sampling of the SafetySignal is performed every 27ms. When the supply is absent, a low power limited sampling of the SafetySignal is performed every 218ms. A full sampling of the thermistor state is performed only if a change of battery presence is detected when the supply is not present.

### GPIO AND STATUS FUNCTIONS

All of the GPIO pins are open drain with N-MOSFET drivers capable of sinking current sufficient to drive an LED (see $V_{OL}$). The pins are not capable of sourcing any current and instead enter a Hi-Z mode when the output is not low. An external pull-up will be required to create any high output logic state.

## OPERATION

The three I/O outputs, GPIO1, GPIO2 and GPIO3 are digital I/O pins with two modes of operation.

1) General Purpose I/O

2) Status Reporting

A host can set the mode of each I/O pin with each I/O pin's setting independent of the others such that any combination of status reporting or bit I/O can be implemented. Only a UVLO or a SHDN event will change the GPIO_n_EN bits back to default values. If you enable a GPIO pin to report status output, it overrides the GPIO_n_OUT setting. In addition, the LTC4110 supports a special power up mode of status reporting on all 3 IO pins for standalone applications where it is assumed "no host" exists. This power up status mode is enabled if the SELA pin is set to 0.5 • $V_{REF}$ voltage as developed from $V_{REF}$ pin resistor divider. This mode does not actually disable the SMBus in any way and if a host does exist in this power up mode, the host can reprogram the I/O settings at any time.

All GPIO pins operate as digital inputs at all times regardless of the pin settings with pin state reported on the GPIO_n_IN bits in the BBuStatus() register. However to actually read digital input data from an external device, you must disable the GPIO_n_EN bit. Otherwise the input will simply reflect the output state assuming external powered pull-ups exist.

There are a total of 5 status signals possible. CHGb, C/xb, BKUP-FLTb, CHG_FLTb, and CAL_COMPLETEb. Each of these signals is asserted low on the output when they are true. CHGb is an asserted low signal when either CHG_STATE_0 or CHG_STATE_1 is set to one. C/xb is asserted low signal when C/x state in the charge cycle is reached. This status signal is only available if the TYPE pin is set to SLA mode and replaces the CHGb status output. BKUP_FLTb is asserted low when the BKUP_FLT bit is set to one in the BBuStatus() register. BKUP_FLT is a sticky bit that is designed to be cleared primarily through the setting of the BUFLT_RST bit in the BBuControl() register. The value of this bit does not inhibit charging or calibration functions. CHG_FLTb is asserted low when the CHG_FLT bit is set to one in the BBuStatus() register. CAL_COMPLETEb bit is asserted low when the conditions of successful calibration cycle are met. CAL_COMPLETEb status output can be used as an interrupt to a host for the purpose of help implementing a simple gas gauge function or capacity verification function with a standard battery. However, if the LTC4110 is set up in no host mode, CAL_COMPLETEb as a status signal is not considered usable since it is assumed there is no host to enable calibration mode. Therefore the CHG_FLTb signal is substituted for CAL_COMPLETEb as the status output signal. Table 5 describes the specific modes and status signal options of each GPIO pin.

**Table 5a. GPIO1 Modes**

| HOST PROGRAMMED BIT SETTINGS | | | GPIO_1 MODE | DATA | NOTE |
|---|---|---|---|---|---|
| GPIO_1_EN | GPIO_1_OUT | GPIO_1_CHG | | | |
| 0 | 0 | 0 | Digital Input | Input Data | GPIO_1_IN |
| 1 | X | 1 | Status Output | CHGb | With Pull-Up |
| 1 | 0 | 0 | Digital Output | 0 | With Pull-Up |
| 1 | 1 | 0 | Digital Output | 1 | With Pull-Up |

**Table 5b. GPIO1 Power Up Mode (SELA = 0.5 • $V_{REF}$)**

| FORCED BIT SETTINGS | | | TYPE = SLA | GPIO_1 MODE | DATA | NOTE |
|---|---|---|---|---|---|---|
| GPIO_1_EN | GPIO_1_OUT | GPIO_1_CHG | | | | |
| 1 | X | 1 | 0 | Status Output | CHGb | With Pull-Up |
| 1 | X | 1 | 1 | Status Output | C/xb | With Pull-Up |

## OPERATION

**Table 5c. GPIO2 Modes**

| HOST PROGRAMMED BIT SETTINGS | | | GPIO_2 MODE | DATA | NOTE |
|---|---|---|---|---|---|
| GPIO_2_EN | GPIO_2_OUT | GPIO_2_BUFLT | | | |
| 0 | 0 | 0 | Digital Input | Input Data | GPIO_2_IN |
| 1 | X | 1 | Status Output | BKUP_FLTb | With Pull-Up |
| 1 | 0 | 0 | Digital Output | 0 | With Pull-Up |
| 1 | 1 | 0 | Digital Output | 1 | With Pull-Up |

**Table 5d. GPIO2 Power Up Mode (SELA = 0.5 • $V_{REF}$)**

| FORCED BIT SETTINGS | | | GPIO_2 MODE | DATA | NOTE |
|---|---|---|---|---|---|
| GPIO_2_EN | GPIO_2_OUT | GPIO_2_ BUFLT | | | |
| 1 | X | 1 | Status Output | BKUP_FLTb | With Pull-Up |

**Table 5e. GPIO3 Modes**

| HOST PROGRAMMED BIT SETTINGS | | | GPIO_3 MODE | DATA | NOTE |
|---|---|---|---|---|---|
| GPIO_3_EN | GPIO_3_OUT | GPIO_3_CAL | | | |
| 0 | 0 | 0 | Digital Input | Input Data | GPIO_3_IN |
| 1 | X | 1 | Status Output | CAL_COMPLETEb | With Pull-Up |
| 1 | 0 | 0 | Digital Output | 0 | With Pull-Up |
| 1 | 1 | 0 | Digital Output | 1 | With Pull-Up |

**Table 5f. GPIO3 Power Up Mode (SELA = 0.5 • $V_{REF}$)**

| FORCED BIT SETTINGS | | | GPIO_3 MODE | DATA | NOTE |
|---|---|---|---|---|---|
| GPIO_3_EN | GPIO_3_OUT | GPIO_3_ CAL | | | |
| 1 | X | 1 | Status Output | CHG_FLTb | With Pull-Up |

### SMBUS INTERFACE

All communications over the SMBus are interpreted by the SMBus interface block. The SMBus interface is a SMBus slave device. All internal LTC4110 registers may be updated and accessed through the SMBus interface as required. The SMBus protocol is a derivative of the $I^2C$-Bus™. (For a complete description of the bus protocol requirements, reference "The $I^2C$-Bus and How to Use It, V1.0" by Philips®, and "System Management Bus Specification, Version 1.1," from the SMBus organization). See Table 6: Register Command Set Description and Table 7: Summary of Supported SMBus Functions, for complete details.

All data is clocked into the shift register on the rising edge of SCL. All data is clocked out of the shift register on the falling edge of SCL. Detection of an SMBus Stop condition, or power-on reset will reset the SMBus interface to an initial state at any time. The LTC4110 command set is interpreted by the SMBus interface and passed onto the charger controller block as control signals or updates to internal registers. Smart battery charge commands are

## OPERATION

processed to allow compliance with smart battery charge and discharge termination and protection control. However, there is no actual value processing of the voltage or current charge commands. IC will acknowledge all smart battery write commands, but process only a subset of them. Full SMBus error and reset handling is supported. The SMBus remains functional during backup mode, but not in SHDN mode.

The LTC4110 SMBus address can be changed when standard batteries are used to facilitate redundant backup systems. Connect SELA pin to GND for 12h, $V_{DD}$ for 28h and $V_{REF}$ for 20h. When a smart battery is selected by the TYPE pin the SELA pin must be connected to GND to select address 12h. Note: Although there are only 7 address bits for SMBus, the above addresses shown follow the smart battery convention of including the Read/Write bit as part of the address value. The Read/Write bit becomes the LSB of the SMBus address with the Read/Write bit value assumed to be a 0 value.

If multiple LTC4110s with smart batteries are to be used, each LTC4110 must be SMBus isolated from all other LTC4110s so the main bus or host bus can only see one LTC4110 and its corresponding smart battery at a time. Failure to do so will cause multiple LTC4110s and smart batteries responding to a single host query resulting in errors. There are multiple channel SMBus multiplexer ICs such as the LTC4305 and LTC4306 to help implement the required isolation. Furthermore, if a given SMBus is high in SMBus device count or long in length, you may want to consider using SMBus accelerators. The above ICs listed support that option.

If the SMBus is not used or to force all GPIOs to status mode upon power-up, connect SELA to a typically 0.5 • $V_{REF}$ voltage from $V_{REF}$ pin resistor divider. The SMBus address then, if used, will be 12h.

Pull-ups are required on the SDA and SCL pin such that when they are not being used, they are in a default high state that means no bus activity. The pull-up voltage need only be high enough to satisfy the logic high threshold. Tying the pins low is a valid state on the SMBus that means anything but the bus is free. This state will force the LTC4110's internal SMBus state machine to reset itself because it thinks the SMBus is hung.

The LTC4110 does not support or respond to the following SMBus V1.1 timing specifications:

a) $T_{TIMEOUT}$ (This is not to be confused with the LTC4110's $t_{TIMEOUT}$ specification.)

b) $T_{LOW:SEXT}$

c) $T_{LOW:MEXT}$

The above specifications have to do with detecting bus hangs or SMBus devices that are taking too long to reply using clock stretching and slowing down the SMBus bandwidth. The LTC4110 is a slave only device that does not do any clock stretching and works all the way up to maximum 100kHz bus speed. It will not hang the bus. The design will always reset its SMBus interface upon receiving an SMBus Start Bit or a Stop Bit regardless of the prior state of the bus.

## OPERATION

**Table 6. Register Command Set Descriptions (XxxxXxxx() – Register Byte, XXXXXXXX – Status Bit)**

| LABEL | DESCRIPTION |
|---|---|
| ChargerStatus() – Read Only. The SMBus host uses this command to read the LTC4110's charge status bits. | |
| AC_PRESENT | Set to 1 when sufficient input voltage (DCDIV > $V_{AC}$ + $V_{ACH}$ and DCIN above UVLO) available and switches load from battery to main supply. Zero indicates backup mode engaged. |
| BATTERY_PRESENT | BATTERY_PRESENT is set if a battery is present, otherwise it is cleared. The LTC4110 uses the SafetySignal to determine battery presence. If the LTC4110 detects a RES_OR condition, the BATTERY_PRESENT bit is cleared immediately. The LTC4110 will not set the BATTERY_PRESENT bit until it successfully samples the SafetySignal twice and does not detect a RES_OR condition on either sampling. If AC is not present (DCDIV < $V_{AC}$ or DCIN below UVLO), this bit may not be set for up to one-half second after the battery is connected to the SafetySignal. The ChargingCurrent() and ChargingVoltage() register values are immediately cleared whenever this bit is cleared. Charging will never be allowed if this bit is cleared. |
| ALARM_INHIBITED | ALARM_INHIBITED bit is set if a valid AlarmWarning() message has been received and charging is inhibited as a result. This bit is cleared if POR_RESET is set, both ChargingVoltage() and ChargingCurrent() are rewritten to the LTC4110, the power is removed (DCDIV < $V_{AC}$ or DCIN below UVLO), the SHDN pin is set high, or if a battery is removed. |
| RES_UR | Set to 1 when NTC pin is below 500Ω typical. This bit is never set when TYPE pin selects SLA battery.. |
| RES_HOT | The RES_HOT bit is set only when the SafetySignal resistance is less than 3kΩ (3.1kΩ for SLA) typical, which indicates a hot battery. The RES_HOT bit will be set whenever the RES_UR bit is set. |
| RES_COLD | The RES_COLD bit is set only when the SafetySignal resistance value is greater than 30kΩ typical. The SafetySignal indicates a cold battery. The RES_COLD bit will be set whenever the RES_OR bit is set. This bit is the same as RES_OR for SLA. |
| RES_OR | The RES_OR bit is set when the SafetySignal resistance value is above 100kΩ (114kΩ for SLA) typical. The SafetySiganl indicates an open circuit. |
| LEVEL:3/LEVEL:2 | The LTC4110 always reports itself as a Level 2 Smart Battery Charger. |
| CHARGE_INHIBITED | Indicates charge inhibited is enabled when set to a one. This is a duplicate of the CHARGE_INHIBIT bit in the BBuStatus() register. |
| ChargingCurrent() – Write Only. The battery, system host or other master device sends the desired charging current to the LTC4110. | |
| ChargingCurrent() | LTC4110 only monitors for zero or non-zero values. A value of zero will stop the charger. A non-zero value here, and for ChargingVoltage(), will restart the charger. |
| ChargingVoltage() – Write Only. The Battery, System Host or other master device sends the desired charging voltage to the LTC4110. | |
| ChargingVoltage() | LTC4110 only monitors for zero or non-zero values. A value of zero will stop the charger. A non-zero value here, and for ChargingCurrent(), will restart the charger. |
| AlarmWarning() – Write Only. The Smart Battery, acting as a bus master device, sends the AlarmWarning() message to the LTC4110 to notify it that one or more alarm conditions exist. Alarm indications are encoded as bit fields in the battery's status register, which is then sent to the LTC4110 by this function. Only the OVER_CHARGED_ALARM, TERMINATE_CHARGE_ALARM,RESERVED_ALARM, OVER_TEMP_ALARM and TERMINATE_DISCHARGE_ALARM bits are supported by the LTC4110. The ALARM_INHIBITED bit in the ChargerStatus() register indicates whether a charging process or a calibration process was halted by a write to this register. | |
| OVER_CHARGED_ALARM | Set to one indicates battery has been overcharged and stops charge. Setting this bit will only stop a charging process (default = zero). |
| TERMINATE_CHARGE_ALARM | Set to one indicates battery requesting charge termination. Setting this bit will only stop a charging process (default = zero). |
| RESERVED_ALARM | Set to one for reserved alarm condition. Setting this bit will stop both a calibration process and a charging process (default = zero). |

## OPERATION

| LABEL | DESCRIPTION |
|---|---|
| OVER_TEMP_ALARM | Set to one indicates battery is temperature is out of range. Setting this bit will stop both a calibration process and a charging process (default = zero). |
| TERMINATE_DISCHARGE_ALARM | Set to one indicates battery requesting discharge termination. Smart battery only. Setting this bit will only stop a calibration process (default = zero). |
| BBuStatus() – Read Only. The SMBus host uses this command to read the LTC4110's status bits. | |
| CAL_ON | Set to one indicates calibration in progress to discharge the battery. |
| CAL_COMPLETE | Set to one indicates calibration process is complete. Can be used as a battery capacity indicator. Bit is cleared by CAL_RESET. This bit is available as a status signal output on the GPIO3 pin. |
| BKUP_ON | Set to one verifies backup mode is active |
| GPIO_1_IN | Shows logic state of general purpose I/O Pin #1. This is always enabled. |
| GPIO_2_IN | Shows logic state of general purpose I/O Pin #2. This is always enabled. |
| GPIO_3_IN | Shows logic state of general purpose I/O Pin #3. This is always enabled. |
| CHG_FLT | Set to one indicates battery charge fault. |
| BKUP_FLT | Set to one indicates battery cell voltage < $V_{DIS}$. This bit state is retained as long as sufficient $V_{BAT}$ is applied. This bit is available as a status signal output on the GPIO2 port. This bit remains until either the SHDN pin is cycled or register bits POR_RESET or BUFLT_RST are set when DCOUT returns. |
| CAL_FLT | Set to one indicates a calibration fault. Calibration terminated early. |
| CHG_STATE_0 | Combined with CHG_STATE_1 indicates phase of charging. 00 = Off, 01 = precharge, 10 = bulk charge, 11 = top off charge |
| CHG_STATE_1 | See CHG_STATE_0 |
| CHARGE_INHIBITED | Indicates charge inhibited is enabled when set to a one. This as a duplicate of CHARGE_INHIBIT bit in the ChargerStatus() register. |
| BBuControl() – Write Only. The SMBus host uses this command to control the LTC4110. | |
| CAL_START | Set to one starts a discharge based calibration of battery (default = self cleared to zero-off) |
| CAL_RESET | Set to one clears the CAL_FLT as well as the CAL COMPLETE and CAL_ON status bits. If calibration is in progress, it will also stop the calibration process (default = self cleared to zero-off) |
| GPIO_1_EN | Set to one enables GPIO1 pin as an output (default = set to one if programming SMBus not used by connecting SELA pin to $0.5V_{REF}$, otherwise default = set to zero/GPIO1 high-Z ) |
| GPIO_2_EN | Set to one enables GPIO2 pin as an output (default = set to one if programming SMBus not used by connecting SELA pin to $0.5V_{REF}$, otherwise default = set to zero/ GPIO2 high-Z) |
| GPIO_3_EN | Set to one enables GPIO3 pin as an output (default = set to one if programming SMBus not used by connecting SELA pin to $0.5V_{REF}$, otherwise default = set to zero/ GPIO3 high-Z) |
| GPIO_1_OUT | Programmable logic bit whose state will be reflected on the GPIO1 pin if the GPIO_1_CHG bit is cleared (default = set to zero/GPIO1 pulled low) |
| GPIO_2_OUT | Programmable logic bit whose state will be reflected on the GPIO2 pin if the GPIO_2_BUFLT bit is cleared (default = set to zero/GPIO2 pulled low). |
| GPIO_3_OUT | Programmable logic bit whose state will be reflected on the GPIO3 pin if the GPIO_3_CALCOM bit is cleared (default = set to zero/GPIO3 pulled low) |

## OPERATION

| LABEL | DESCRIPTION |
|---|---|
| GPIO_1_CHG | Set to one sends an inverted CHG_ON (internal register, set to 1 when either CHG_STATE_0 or CHG_STATE_1 is set to 1) status signal out to the GPIO1 pin. If this bit is set, the value of CHG_ON overrides the value of the GPIO_1_OUT bit state. Pin must be output enabled with GPIO_1_EN bit (default = set to zero/off) |
| GPIO_2_BUFLT | Set to one sends an inverted BKUP_FLT status signal out to the GPIO2 pin. If this bit is set, the value of BKUP_FLT overrides the value of the GPIO_2_OUT bit state. Pin must be output enabled with GPIO_2_EN bit (default = set to zero/off) |
| GPIO_3_CALCOM | Set to one sends an inverted CAL_COMPLETE signal out to the GPIO3 pin. If this bit is set, the value of CAL_COMPLETE overrides the value of the GPIO_3_OUT bit state. Pin must be output enabled with GPIO_3_EN bit (default = set to zero/off) |
| RESET_TO_ZERO | Set to one resets all faults and timers in charge and forces the ChargingCurrent() and ChargingVoltage() to zero values. Clears Alarm_Warning() register. Does not affect BBuControl() register. Bit clears to zero automatically after the command is executed (default = cleared to zero-no reset) |
| POR_RESET | Resets LTC4110 to power-on default values. Setting the bit to a one will activate POR_RESET. POR_RESET performs a total chip wide reset like the SHDN pin function without the chip actually shutting down. This includes clearing any bits in registers. The bit clears itself automatically after the command is executed (default = cleared/no reset) |
| BUFLT_RST | Resets the BKUP_FLT bit. The bit clears itself automatically after the command is executed (default = cleared). |
| CHARGE_INHIBIT | Disables charging of battery. Set to one halts charge current while holding the charger state and pausing all battery charge timers without changing the ChargingCurrent() and ChargingVoltage() values. Charge may be enabled by clearing this bit. This bit is automatically cleared when power is reapplied or when a battery is re-inserted (default = cleared to zero-off) |

## OPERATION

**Table 7. Summary of Supported SMBus Functions**

| Function | Access | SMBus Address | Command Code | Data Type | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ChargerStatus() | | 7'b0001_001 | 8'h13 | Status | AC_PRESENT | BATTERY_PRESENT | POWER_FAIL | ALARM_INHIBITED | RES_UR | RES_HOT | RES_COLD | RES_OR | VOLTAGE_OR | CURRENT_OR | LEVEL:3/LEVEL:2 | | CURRENT_NOTREG | VOLTAGE_NOTRES | POLLING_ENABLED | CHARGE_INHIBITED |
| | Read | | | Return Value | 1/0 | 1/0 | 0 | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1/0 |
| Charging-Current() | | 7'b0001_001 | 8'h14 | Value | Note 1 | | | | | | | | | | | | | | | |
| | Write | | | Permitted Values | Unsigned Integer Representing Current in mA | | | | | | | | | | | | | | | |
| Charging-Voltage() | | 7'b0001_001 | 8'h15 | Value | Note 2 | | | | | | | | | | | | | | | |
| | Write | | | Permitted Values | Unsigned Integer Representing Voltage in mV | | | | | | | | | | | | | | | |
| Alarm-Warning() | | 7'b0001_001 | 8'h16 | Control | OVER_CHARGED_ALARM | TERMINATE_CHARGE_ALARM | RESERVED_ALARM | OVER_TEMP_ALARM | TERMINATE_DISCHARGE_ALARM | RESERVED | REMAINING_CAPACITY_ALARM | REMAINING_TIME_ALRAM | INITIALIZED | DISCHARGING | FULLY_CHARGED | FULLY_DISCHARGED | ERROR | | | |
| | Write | | | Permitted Values | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BBuStatus() | | 7'b0001_001 | 8'h3D | Status | CAL__ON | CAL_COMPLETE | BKUP_ON | Reserved | Reserved | GPIO_1_IN | GPIO_2_IN | GPIO_3_IN | Reserved | CHG_FLT | BKUP_FLT | CAL_FLT | CHG_STATE_0 | CHG_STATE_1 | Reserved | CHARGE_INHIBITED |
| | Read | | | Return Values | 1/0 | 1/0 | 1/0 | 0 | 0 | 1/0 | 1/0 | 1/0 | 1 | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 | 0 | 1/0 |
| BBuControl() [Charger-Mode()] | | 7'b0001_001 | 8'h12 | Control | CAL_START | CAL_RESET | GPIO_1_EN | GPIO_2_EN | GPIO_3_EN | GPIO_1_OUT | GPIO_2_OUT | GPIO_3_OUT | Reserved | GPIO_1_CHG | GPIO_2_BUFLT | GPIO_3_CALCOM | RESET_TO_ZERO | POR_RESET | BUFLT_RST | CHARGE_INHIBIT |
| | Write | | | Permitted Values | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 | 0 | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 |

Note 1: IC only looks for a zero (off) or a non-zero (on) value. Actual charge current is set by the $I_{CHG}$ pin.

Note 2: IC only looks for a zero (off)or a non-zero (on) value. Actual charge voltage is set by the $V_{CHG}$ pin.

## APPLICATIONS INFORMATION

The first configuration option to set for the LTC4110 is the type and cell count of the battery you wish to use. Pins TYPE and SELC are use to set this configuration. Please note NiMH and NiCd batteries are only supported in the smart battery configuration. The three state input pins SELA, SELC and TYPE should NOT be changed while power is applied to the IC unless in shutdown mode. Such action will result in unpredictable behavior from the LTC4110.

### SUPERCAPS

Table 8 shows all of the options with the exception of SuperCaps. SuperCaps are supported by using standard Li-ion or SLA modes in combination with the adjusting the charge voltage with the $V_{CHG}$ pin. As far as the LTC4110 is concerned, it is still working with a Li-ion or SLA battery and will follow all the charge states as required for that chemistry. Table 9 shows the required configuration based on the desired cap voltage and series cell count. Other per cell voltages can be obtained by adjusting the $V_{CHG}$ pin as required.

When the LTC4110 is configured to charge a super cap, if TYPE pin is tied to $0.5V_{REF}$, use the bulk charge current equation (see the Programming Charging/Calibration Current section for details) to set the charging current. If TYPE pin is tied to GND, then the charging current will equal to preconditioning charge current when the cap voltage is below the bulk charge threshold (as listed in Table 9) and bulk charge current when the voltage is above the threshold. Simply tie the $I_{PCC}$ pin to $I_{CHG}$ pin if these two currents need to be the same. If the capacitor is too small (<10mF), the voltage might rise too fast to be regulated by the loop. In that case, the capacitor will be charged to over voltage pretection threshold (typically 107.5% of the float voltage. See $V_{BOV}$)

**Table 8. Battery Type and Number of Series Cell Selection for Batteries**

| | STANDARD Li-Ion (TYPE = GND) | SLA (TYPE = $0.5V_{REF}$) | SMART NiMH/NiCd (TYPE = $V_{REF}$) | SMART Li-Ion (TYPE = $V_{DD}$) |
|---|---|---|---|---|
| SELC = GND | 1 | 2 | 4 | 1 |
| SELC = $0.5V_{REF}$ | 2 | 3 | 6 | 2 |
| SELC = $V_{REF}$ | 3 | 5 | 9 | 3 |
| SELC = $V_{DD}$ | 4 | 6 | 10 | 4 |

Note: When smart battery is selected by the TYPE pin, SELA pin must be connected to GND to select address 12h.

**Table 9. Battery Type and Number of Series Cell Selection for Super Caps**

| CAP VOLTAGE (V) | SERIES CAP COUNT | STACK CAP VOLTAGE (V) | TYPE | SELC | $V_{CHG}$ | BULK CHARGE THRESHOLD (V/CELL) |
|---|---|---|---|---|---|---|
| 2.5 | 2 | 5 | $0.5V_{REF}$ | GND | $0.625V_{REF}$ | N/A |
| 2.5 | 3 | 7.5 | $0.5V_{REF}$ | $0.5V_{REF}$ | $0.625V_{REF}$ | N/A |
| 2.5 | 5 | 12.5 | $0.5V_{REF}$ | $V_{REF}$ | $0.625V_{REF}$ | N/A |
| 2.5 | 6 | 15 | $0.5V_{REF}$ | $V_{DD}$ | $0.625V_{REF}$ | N/A |
| 2.5 | 7 | 17.5 | GND | $V_{DD}$ | $0.646V_{REF}$ | 1.71 |
| 2.7 | 3 | 8.1 | GND | $0.5V_{REF}$ | $0.375V_{REF}$ | 2 |
| 2.7 | 5 | 13.5 | GND | $V_{REF}$ | $0.750V_{REF}$ | 1.8 |
| 2.7 | 6 | 16.2 | GND | $V_{DD}$ | $0.375V_{REF}$ | 2 |
| 3 | 3 | 9 | GND | $0.5V_{REF}$ | $0.750V_{REF}$ | 2 |
| 3 | 4 | 12 | GND | $V_{REF}$ | $0.333V_{REF}$ | 2.25 |
| 3 | 5 | 15 | $0.5V_{REF}$ | $V_{DD}$ | $0.625V_{REF}$ | N/A |
| 3 | 6 | 18 | GND | $V_{DD}$ | $0.750V_{REF}$ | 2 |

## APPLICATIONS INFORMATION

### SOFT-START

The LTC4110 is soft-started with the 0.1µF capacitor on the $I_{TH}$ pin. On start-up, the $I_{TH}$ pin voltage will rise quickly to 0.1V, then ramp up at a rate set by the internal 24µA pull-up current and the external capacitor. Battery charging current starts ramping up when $I_{TH}$ voltage reaches 0.7V and full current is achieved with $I_{TH}$ at about 2V. With a 0.1µF capacitor, time to reach full charge current is about 8ms and it is assumed that input voltage to the charger will reach full value in less than 8ms. The capacitor can be increased up to 1µF if longer input start-up times are needed.

In any switching regulator, conventional timer-based soft-starting can be defeated if the input voltage rises much slower than the timeout period. This happens because the switching regulators in the battery charger and the computer power supply are typically supplying a fixed amount of power to the load. If input voltage comes up slowly compared to the soft-start time, the regulators will try to deliver full power to the load when the input voltage is still well below its final value. If the adapter is current limited, it cannot deliver full power at reduced output voltages and the possibility exists for a quasi "latch" state where the adapter output stays in a current limited state at reduced output voltage. For instance, if maximum charger plus computer load power is 30W, a 15V adapter might be current limited at 2.5A. If adapter voltage is less than (30W/2.5A = 12V) when full power is drawn, the adapter voltage will be pulled down by the constant 30W load until it reaches a lower stable state where the switching regulators can no longer supply full load. This situation can be prevented by utilizing the DCDIV resistor divider, set higher than the minimum adapter voltage where full power can be achieved.

### CALIBRATION MODE BACK-DRIVE CURRENT PROTECTION

A resistor between CLP and CLN programs the minimum supply forward current, this feature prevent the LTC4110 from back-driving the supply in calibration mode and pulling the voltage higher when the system load is low. The resistor value is given by

$$R_{CL} = \frac{I_{BDT}}{I_{FR(MIN)}}$$

where

$I_{BDT}$ = back-drive current limit threshold, 10mV typical

$I_{FR(MIN)}$ = minimum forward current in calibration mode

An RC filter may be required to filter out system load noise as shown in Figure 11.

### BATTERY AND CHARGER CURRENT SENSE

The LTC4110 uses two sense resistors to monitor and control all charge and calibration currents: $R_{SNS(BAT)}$ and $R_{SNS(FET)}$.

#### $R_{SNS(BAT)}$

$R_{SNS(BAT)}$ is used to monitor the DC current going into the battery for charge, and the current going out of the battery for calibration. Before any current programming can be done, the value of $R_{SNS(BAT)}$ must be determined first. Highest accuracy is achieved when full-scale current, $I_{MAX}$ is set to develop a 100mV drop across the resistor. Although values greater than 100mV can be used to improve accuracy, this requires larger sense resistors to handle the extra heat and lower efficiency. $I_{MAX}$ must be set to

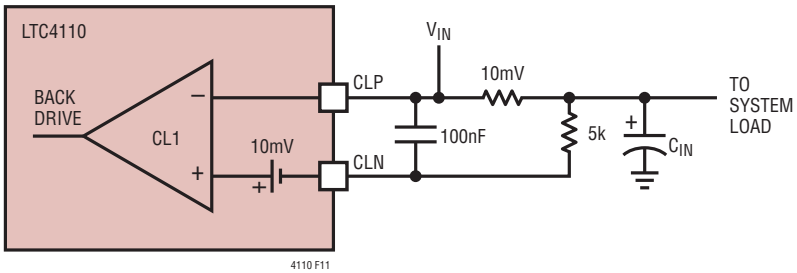



**Figure 11. Back-Drive Protection**

## APPLICATIONS INFORMATION

the highest current flow between charge and calibration modes, whichever is greater.

$$R_{SNS(BAT)} = \frac{100mV}{I_{MAX}}$$

See Table 10 for example values.

$R_{SNS(BAT)}$ accuracy is intentionally made very high to permit development of an accurate host software based capacity measurements of standard batteries. Use resistors with 1% accuracy or better or use a 4-terminal Kelvin sensing resistor. See the PCB Layout section for a reasonable no cost Kelvin sensing layout that permits the use of less expensive standard two terminal sense resistors. For more electrical information relating to $R_{SNS(BAT)}$ itself, see the Component Selection section.

As designed, any significant AC ripple voltage seen by CSP and CSN pins can lead to current sensing errors for both current programming and capacity measurements. To prevent the Flyback's AC ripple voltage from interfering with DC accuracy, $R_{SNS(BAT)}$ must have a RC filter network installed between the $R_{SNS(BAT)}$ and CSP and CSN pins.

The CSP and CSN pins have an input bias current of ±10nA typically. A very large $R_{CSP1} + R_{CSP2}$ value will cause a large current mismatch error. The current flowing into the CSP and CSN pins equals $V_{SNS}/(R_{CSP1} + R_{CSP2}) = 100mV/(R_{CSP1} + R_{CSP2})$, a very small $R_{CSP1} + R_{CSP2}$ value will result in a large current. Typically a value between 3k and 30k gives the best performance.

Recommended starting values for the filter is:

$R_{CSP1} = R_{CSN1}$ between 1K and 2K

$R_{CSP1} + R_{CSP2} = R_{CSN1} + R_{CSN2}$ = about 3K

$C_{CSP} = C_{CSN}$ = about 3 • $C_{ITH}$.

Figure 12 shows typical values for $C_{ITH}$ = 0.1µF

### $R_{SNS(FET)}$

The LTC4110's Flyback converter operates in current mode with $R_{SNS(FET)}$ monitoring cycle-by-cycle transformer current in both Charge and Calibration modes. The LTC4110's $I_{SENSE}$ pin serves two functions. First is to regulate the primary current as required by the feedback loop. Second is to monitor the secondary current and check for short circuits. The traditional Flyback primary and secondary currents look like the following:

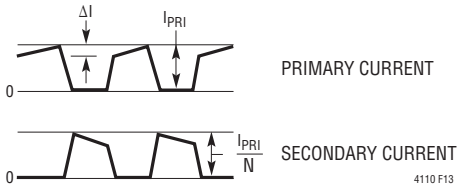



**Figure 13. Flyback Primary and Secondary Current**

The waveforms in Figure 13 each assume a view of positive current flow into the load. The value N represents the ratio of the secondary to the primary with the primary set to a value of 1. Unlike a traditional Flyback topology, the LTC4110 Flyback is bi-directional, so the meaning of "primary" is a function of the operating mode. In order

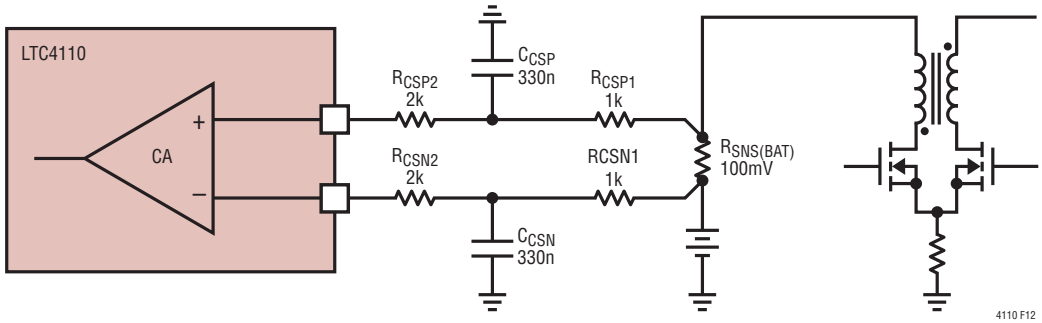



**Figure 12. CSP, CSN RC Filter**

## APPLICATIONS INFORMATION

to monitor the primary current in both sides with a single $R_{SNS(FET)}$ resistor, both transformer windings must be connected prior to $R_{SNS(FET)}$. Since the secondary phase is always 180 degrees out of phase with the primary, the following current waveform in Figure 14 is the result.

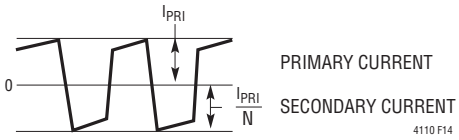



**Figure 14. $R_{SNS(FET)}$ Current Waveform**

In terms of current sensing, the primary current portion of the above waveform is monitored for peak current (DC + AC) at any time in any mode. It does not monitor the batteries' DC current. The LTC4110 uses leading edge blanking to mask out noise to make the application of this part simple to use. The secondary portion of the above waveform is monitored for negative peak current to sense for short circuit.

The value of ripple current, $\Delta I$, is a direct function of the transformer inductance. See transformer section for more information about transformer ripple current.

You must calculate the $I_{PRI}$ for both charge current mode and calibration current mode. The equation for calculating the $I_{PRI}$ for charge mode is as follows:

$$I_{PRI(CHG)} = \frac{I_{CHG}}{E} \bullet \left(\frac{V_{BAT}}{V_{DCIN}} + N\right) + \frac{V_{BAT} \bullet V_{DCIN}}{2 \bullet f \bullet L_{PRI} \bullet \left(V_{BAT} + N \bullet V_{DCIN}\right)} \quad (1)$$

$I_{PRI}$ for the Calibration mode is as follows:

$$I_{PRI(CAL)} = I_{CAL} \bullet \left(\frac{V_{BAT}}{N \bullet V_{DCIN}} + 1\right) + \frac{V_{BAT} \bullet V_{DCIN}}{2 \bullet f \bullet (N^2 \bullet L_{PRI}) \bullet \left(V_{DCIN} + \frac{V_{BAT}}{N}\right)} \quad (2)$$

The value of E is the flyback efficiency. Use 80% (0.8) as the value since the flyback uses synchronous rectification. E is not used for the calibration equation because in calibration mode input current is regulated, not the output current.

The LTC4110's $I_{SENSE}$ pin has a limited usable positive voltage range for $V_{SNS(FET)}$. The range must be between 30mV and 150mV peak in both charge and calibration modes when operating at full current. The negative portion of the waveform is also monitored but has a dynamic trip level that tracks the actual primary current. The trip level has a gain factor of –3. If the secondary current trips the negative level, the flyback goes into current limit.

These limits have the following implications:

- The ratio of peak current between $I_{PRI(CHG)}$ and $I_{PRI(CAL)}$ cannot be greater than 5-to-1 as seen by $R_{SNS(FET)}$.
- The transformer turns ratio will approximately reduce the maximum available DC current ratio between $I_{CHG}$ to $I_{CAL}$ by a factor of 1/N. The additional variables being ripple current and efficiency.
- You cannot use a transformer with a turns ratio greater than 3.
- Because efficiency is always less than 100%, you never have to worry about peak secondary current causing a false short circuit trip within the turns ratio limit of 3 or less.

As a design starting point, use the lowest value between $I_{PRI(CHG)}$ and $I_{PRI(CAL)}$ for $I_{PRI}$, let $V_{SNS(FET)}$ be set to 50mV for good efficiency and solve for $R_{SNS(FET)}$.

$$R_{SNS(FET)} = \frac{V_{SNS(FET)}}{I_{PRI}}$$

With an initial value of $R_{SNS(FET)}$ identified, solve for $V_{SNS(FET)}$ using the highest value between $I_{PRI(CHG)}$ or $I_{PRI(CAL)}$ and see if the calculated value of $V_{SNS(FET)}$ falls below the upper limits. If it is too high, you may have to drop the value of $R_{SNS(FET)}$. If you cannot meet the $V_{SNS(FET)}$ upper or lower limits and/or ratio limits, you may have to back off on one of the $I_{CHG}$ and $I_{CAL}$ DC current parameters to compensate.

Once within all the limits, optimize $R_{SNS(FET)}$ for maximum efficiency by using very low value of $R_{SNS(FET)}$ and/or find a popular $R_{SNS(FET)}$ value. The tradeoff of using lower values of $R_{SNS(FET)}$ is increased waveform jitter due to higher switching noise sensitivity issues.

# APPLICATIONS INFORMATION

## PROGRAMMING CHARGE VOLTAGE

Depending on the battery chemistry chosen by the TYPE pin, a charge termination voltage or a float voltage will be required. The difference between the two is time. A float voltage is applied to a battery forever. The $V_{CHG}$ pin is used to set any of these voltages and the equations remain the same. For this document, we will use the term float voltage generically. If nickel chemistry is chosen, the $V_{CHG}$ pin is disabled placing the charger in constant current mode. If you are using a smart battery, wake-up charge is subject to the $V_{CHG}$ pin setting when active.

Connecting the $V_{CHG}$ pin to GND will set the default per cell float voltage (4.2V for Li-ion, 2.35V for SLA). If a different float voltage is needed, tie the $V_{CHG}$ pin to a voltage between 0.25 $V_{BGR}$ and 0.75 $V_{BGR}$ using a resistor divider on the $V_{REF}$ pin. Unlike $V_{REF}$, $V_{BGR}$ is an internal reference voltage of the same voltage as $V_{REF}$ but with a much tighter (±0.5%) tolerance than $V_{REF}$.

$$\Delta V_{FLOAT} = \left(2 \bullet \frac{V_{CHG}}{V_{BGR}} - 1\right) \bullet 0.6$$

where

$\Delta V_{FLOAT}$ = Adjusted Float Voltage – Default Float Voltage

$V_{CHG}$ = $V_{CHG}$ Pin Voltage,

$V_{BGR}$ = 1.220V

The resistor divider connected to $V_{REF}$ pin will affect timer (see the Programming Charge Time with TIMER and $V_{REF}$ Pins section for more details).

## THERMISTOR FOR LEAD ACID BATTERIES

When the TYPE pin is programmed for Lead Acid, THA pin will be force to $V_{BGR}$, THB will be used to sense the NTC resistance. The value of R1 is given by:

$$R1 = R0 \bullet \frac{\beta - 2 \bullet T0}{\beta + 2 \bullet T0}$$

where:

R0 = thermistor resistance (Ω) at T0

T0 = thermistor reference temperature (°K)

β = exponential temperature coefficient of resistance

The LTC4110 is designed to work best with a 5% 10k NTC thermistor with a β near 3750, such as the Siemens/EPCOS B57620C103J062. In this case, R1 = 7256Ω.

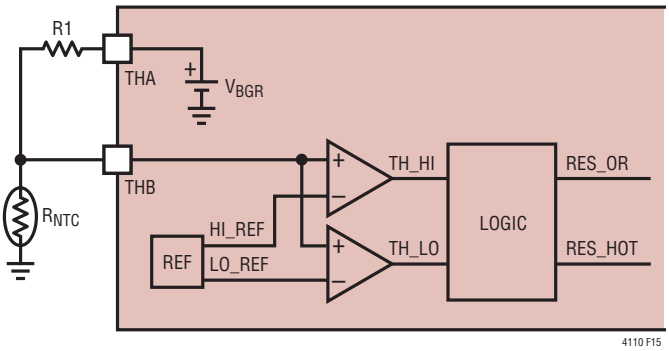



**Figure 15. Lead Acid Thermistor**

## LEAD ACID BATTERY TEMPERATURE COMPENSATION

To program the temperature compensation for SLA charging, an external circuit is needed as shown in Figure 16.

The values are given by:

$$R1 = R0 \bullet \frac{\beta - 2 \bullet T0}{\beta + 2 \bullet T0}$$

$$k1 = \frac{R0}{R0 + R1}$$

$$TCk1 = -\frac{\beta \bullet R1 \bullet R0}{(R1 + R0)^2 \bullet T0^2}$$

$$k2 = \frac{TCV_{FLOAT}}{1.2 \bullet TCk1}$$

$$k3 = \frac{0.5 + \Delta V_{FLOAT} / 1.2 - k1 \bullet k2}{1 - k2}$$

where:

$TCV_{FLOAT}$ = temperature coefficient of the float voltage (Range: –2mV/°C – –6mV/°C)

$\Delta V_{FLOAT}$ = float voltage at 25°C – default float voltage 2.35V (Range: –0.15V – 0.15V)

For example, if a 10k NTC with β = 3750 is used, desired

## APPLICATIONS INFORMATION

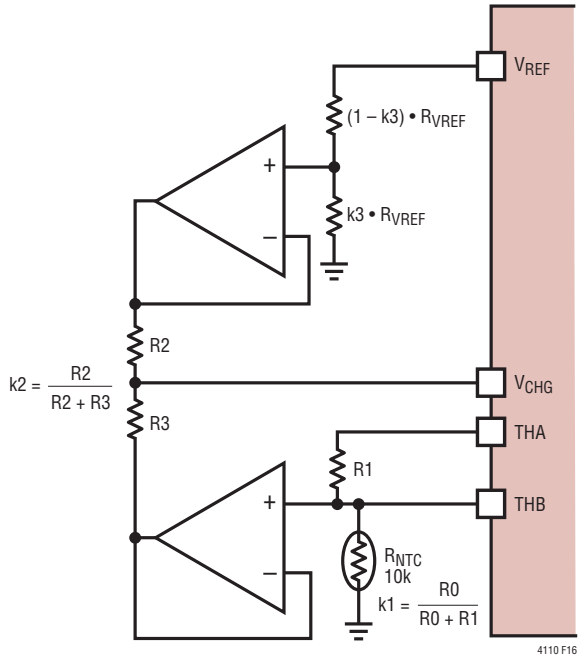



**Figure 16. Lead Acid Temperature Compensation**

float voltage = 2.5V at 25°C with a temperature coefficient of –2mV/°C, then R1 = 7256, k1 = 0.580, TCk1 = –10.3m/°C, $\Delta V_{FLOAT}$ = 2.5 – 2.35 = 0.15V, k2 = 0.162, k3 = 0.634.

### PROGRAMMING CURRENT

Charge/calibration currents are programmed using the following equations:

$$I_{CHG} = \frac{V_{BGR}}{R_{SNS(BAT)}} \bullet \frac{R_{CSP}}{R_{ICHG}}$$

$$I_{PCC} = \frac{V_{BGR}}{R_{SNS(BAT)}} \bullet \frac{R_{CSP}}{R_{IPCC}}$$

$$I_{CAL} = \frac{V_{BGR}}{R_{SNS(BAT)}} \bullet \frac{R_{CSN}}{R_{ICAL}}$$

where:

$I_{CHG}$ = bulk charge current

$I_{PCC}$ = preconditioning charge current

$I_{CAL}$ = calibration current

$V_{BGR}$ = 1.220V

$R_{SNS(BAT)}$ = resistor between flyback transformer and battery

$R_{CSP} = R_{CSP1} + R_{CSP2}$

$R_{CSN} = R_{CSN1} + R_{CSN2}$

$R_{ICHG}$ = resistor connected between $I_{CHG}$ pin and GND

$R_{IPCC}$ = resistor connected between $I_{PCC}$ pin and GND

$R_{ICAL}$ = resistor connected between $I_{CAL}$ pin and GND.

If any programming resistor value on any of the three pins exceeds 100k, see Flyback Compensation section for more information.

Pins can be tied together to save components if any of the currents have the same value. If two pins share a common programming resistor greater than 100k, only one compensation circuit is required.

If the TYPE pin is set for SLA/LEAD ACID, then the $I_{PCC}$ pin is not used. You can leave the $I_{PCC}$ pin open.

### PROGRAMMING BACKUP MODE ENTRY THRESHOLD AND CALIBRATION MODE BACK-DRIVE VOLTAGE DETECTION THRESHOLD

A resistor divider connected to supply input sets both the backup mode entry threshold and the calibration mode back-drive voltage detection threshold.

$$V_{BACKUP} = \left(\frac{R2}{R1} + 1\right) \bullet V_{BGR}$$

$$V_{BACKDRIVE} = \left(\frac{V_{OVP}}{V_{BGR}}\right) \bullet V_{BACKUP}$$

$$\frac{R2}{R1} = \frac{V_{BACKUP}}{V_{BGR}} - 1$$

where:

$V_{BACKUP}$ = supply voltage when backup starts, it should not be programmed to less than 4.5V

$V_{BACKDRIVE}$ = supply voltage when calibration is terminated, it should not be programmed to more than 20V

$V_{OVP}$ = DCDIV pin back-drive detect threshold in calibration mode, typically 1.5V (see $V_{OVP}$)

## APPLICATIONS INFORMATION

R1 = resistor connected between DCDIV and GND

R2 = resistor connected between supply input and DCDIV

$V_{BGR}$ = reference voltage 1.220V

For example, if supply input = 12V and backup starts when it drops to 11V, then $V_{BACKUP}$ = 11V, $V_{BACKDRIVE}$ = 13.5V, R2/R1 = 8.02, choose R1 = 10k, then R2 = 80.6k.

If a higher ratio than $V_{OVP}/V_{BGR}$ = 1.23 is desired between $V_{BACKDRIVE}$ and $V_{BACKUP}$, a third resistor can be used as shown in Figure 17.

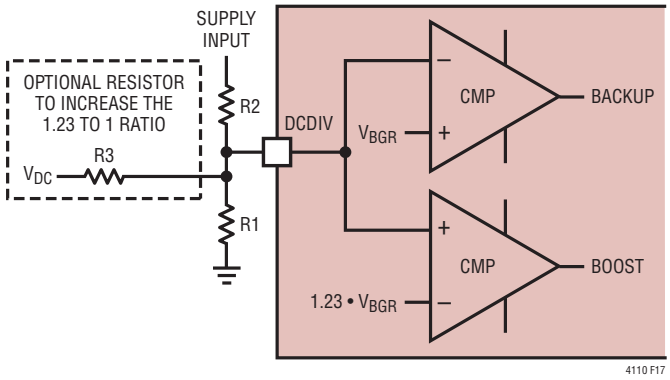



**Figure 17. Backup and Boost Detect Comparators**

$$\frac{R2}{R1} = \frac{V_{BACKDRIVE} - V_{BACKUP}}{0.23 \bullet V_{BGR}} - \frac{V_{BACKDRIVE} - 1.23 \bullet V_{BACKUP}}{0.23 \bullet V_{DC}} - 1$$

$$\frac{R3}{R1} = \frac{V_{DC}}{V_{BGR}} \bullet \frac{V_{BACKDRIVE} - V_{BACKUP}}{V_{BACKDRIVE} - 1.23 \bullet V_{BACKUP}} - \frac{0.23 \bullet V_{DC}}{V_{BACKDRIVE} - 1.23 \bullet V_{BACKUP}} - 1$$

where:

$V_{DC}$ = Any regulated DC voltage available in the system such as SMBus pull up, LED supply or LTC4110's $V_{DD}$ voltage, must be higher than 1.7V. R3 = resistor connected between $V_{DC}$ and DCDIV.

For example, if supply input = 12V and backup starts when it drops to 8V, calibration terminates when it rises to 16V, and $V_{DC} = V_{DD}$ = 4.75V, then R2/R1 = 21.87, R3/R1 = 3.88, choose R1 = 10k then R2 = 221k and R3 = 39.2k.

If the noise on supply input is a problem, a capacitor can be connected between DCDIV and GND.

### PROGRAMMING CALIBRATION/BACKUP CUT-OFF THRESHOLD

The pins $V_{CAL}$ and $V_{DIS}$ are used to calculate custom discharge cut-off voltages for their respective operating modes. The equations shown below are generic for both. There is no implied relationship between $V_{CAL}$ and $V_{DIS}$ for they are independent of each other.

The equations are most helpful if you pick the $V_{CUTOFF}$ voltage you want, within the range limits offered, and then solve for $V_{CAL}$ or $V_{DIS}$. With the voltage value of $V_{CAL}$ or $V_{DIS}$ calculated, determine the necessary voltage divider network from $V_{REF}$ required to get the calculated voltage on these pins respectively. It is recommended that one single series resistor divider network from $V_{REF}$ to ground be used to obtain all of the pin voltages you need. It should be noted that custom values of $V_{CHG}$ would also affect the divider network complexity. See Programming Charge Voltage section for more information.

Connect the $V_{CAL}$ or $V_{DIS}$ pin to GND will set the default calibration/backup cut-off threshold (2.75V for Li-Ion, 1.93V for SLA, 0.95V for NiMH/NiCd). These threshold voltages can be adjusted (±400mV for Li-Ion, ±300mV for SLA, ±200mV for NiMH/NiCd) by tying the pin to appropriate voltage on the $V_{REF}$ pin resistor divider according to the following equations:

$$V_{CUTOFF} = \frac{V_{CAL} \text{ or } V_{DIS}}{V_{BGR}} \bullet 4.2 \quad (Li-Ion)$$

$$V_{CUTOFF} = \frac{V_{CAL} \text{ or } V_{DIS}}{V_{BGR}} \bullet 2.35 \quad (SLA)$$

$$V_{CUTOFF} = \frac{V_{CAL} \text{ or } V_{DIS}}{V_{BGR}} \bullet 2 \quad (NiMH / NiCD)$$

## APPLICATIONS INFORMATION

where

$V_{CUTOFF}$ = adjusted cutoff threshold voltage

$V_{CAL}/V_{DIS}$ = voltage on $V_{CAL}$ or $V_{DIS}$ pin

$V_{BGR}$ =1.220V

The resistor divider connected to $V_{REF}$ pin will affect timer. See the Programming Charge Time with TIMER and $V_{REF}$ Pins section for more details.

### PROGRAMMING CHARGE TIME WITH TIMER AND $V_{REF}$ PINS

Charge time limits for Li-Ion batteries can be programmed by selection of capacitance on the TIMER pin, but is dependent upon resistance on the $V_{REF}$ pin. Typical programmed bulk charge times range from 2 to 12 hours and is set as follows:

$$C_{TIMER}(F) = \frac{T(Hrs)}{(944 \bullet R_{VREF}(\Omega))}$$

As an example if $R_{VREF}$ = 113k and the desired bulk charge time limit is five hours then $C_{TIMER}$ = 47nF. See $F_{TMR}$ which directly affects the 944 constant in the Electrical Characteristics Table for the tolerance.

Avoid capacitors with high leakage currents. The $V_{REF}$ pin load resistor range is 49k to 125k or 10µA to 25µA of load current. At 125k the maximum capacitance on $V_{REF}$ is limited to a maximum of 50pF to maintain sufficient AC stability for the internal amplifier. At 49k the maximum is 125pF. The maximum capacitance is inversely proportional to the resistance.

The voltage ($V_{REF}$) on the $V_{REF}$ pin can be used as a precision voltage for other uses with some limitations. The total $V_{REF}$ pin current must not exceed 25µA and the capacitance must be limited as discussed above. Load current fluctuations will modulate the programmed charge time. In shutdown mode $V_{REF}$ will drop to 0V.

In some applications a divided down $V_{REF}$ voltage is needed to program the SELA, SELC, TYPE, $V_{CHG}$, $V_{CAL}$ and $V_{DIS}$ pins. This is easily implemented by use of a resistor divider connected from $V_{REF}$ to GND that sets the $V_{REF}$ pin current instead of a single resistor.

If the TYPE pin is set for SLA/LEAD ACID or any nickel based smart battery, the TIMER pin is not used. You can ground the TIMER pin. Furthermore, if there is no need of any timer function and there is no need of any voltage divider from $V_{REF}$ to ground, you must still keep a load on the $V_{REF}$ pin between 10µA and 25µA. It is recommended you place a 49.9k load resistor from $V_{REF}$ to ground.

### CHARGING BATTERIES OVER 12 HOURS

In situations where required bulk charge time cycle will exceed the 12 hour time limit imposed by the charge TIMER pin, you have two options. You can have an SMBus host clear the CHG_FLT bit and force start another charge cycle or you can switch to a smart version of the same battery. If you chose the former, reduce the TIMER pin time to about 2/3 of the actual time required. This will result in faster termination in the second cycle and with autorestart cycles when $V_{AR}$ is tripped. If you choose the smart battery option, the smart battery itself safely controls charge termination. Bulk charge can last as long as necessary to charge the battery to 100%. No host is required to do anything, as the battery will maintain its full charge state using its SMBus charge commands.

### PROGRAMMING AC PRESENT INDICATION DELAY TIME WITH ACPDLY AND $V_{REF}$ PINS

When the main supply, DCIN, returns after a power failure the ACPb pin is driven low to indicate presence of main power. This transition can be delayed to allow time for the system to stabilize before actions are taken by the system based on this pin status. The high to low transition only delay on the ACPb pin can be programmed by selection of capacitance on the ACPDLY pin, but is dependent upon resistance on the $V_{REF}$ pin. Typical programmed delay times range from 10ms to 200ms and is set as follows:

$$C_{ACPDLY}(F) = \frac{T(s)}{2 \bullet R_{VREF}(\Omega)}$$

As an example if $R_{VREF}$ = 113k and the desired delay time is 105ms then $C_{TIMER}$ = 470nF. See $t_{AC}$ in the Electrical Characteristics Table for the tolerance.

## APPLICATIONS INFORMATION

Avoid capacitors with high leakage currents. See the Programming Charge Time with TIMER and $V_{REF}$ Pins section for details concerning the $V_{REF}$ pin. For minimum delay open the ACPDLY pin.

### BAT PIN CURRENT IN IDLE MODE

When LTC4110 is in IDLE mode (i.e., not in charge, calibration or backup mode), there will be a typical 30µA current pulled from the battery through the BAT pin, if this current is of concern, a diode in series with a resistor can be connected between DCIN and battery to compensate it.

### SHOW BATTERY FULL WITH ACPB AND CHGB

Tie the source of an N-MOSFET to ACPb, gate to CHGb and drain in series with R to an LED to show battery full. In that case if CHG or ACP status LED is not needed, replace it with a short but keep the pull-up resistor.

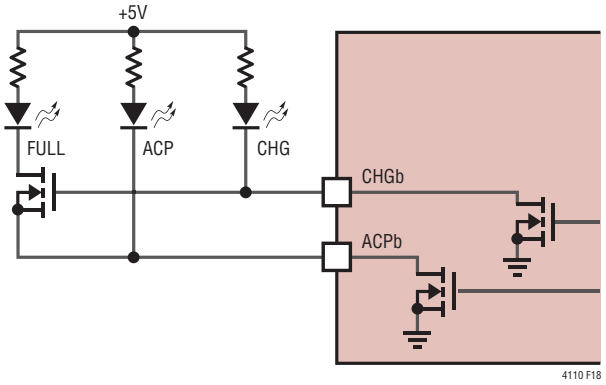



**Figure 18. Display Battery Full**

### FLYBACK COMPENSATION

The values given for the $I_{TH}$ pin in the application schematics have been found to compensate both the voltage loop and current loop quite well. However, if the resistor connected to $I_{CHG}$, $I_{CAL}$ or $I_{PCC}$ is larger than 100k, a 37k resistor in series with a 100nF capacitor should also be connected between that pin and GND to compensate the loop.

### SLOPE COMPENSATION

The LTC4110 injects a ramping current through its $I_{SENSE}$ pin into an external slope compensation resistor ($R_{SL}$). This current ramp starts at zero right after the primary side MOSFET (CHGFET in charge mode, DCHFET in calibration mode) is turned on. The current rises linearly towards a peak of $V_{SEC}$/400k (where $V_{SEC}$ = BAT in charge mode, $V_{SEC}$ = DCIN in calibration mode), shutting off once the primary side MOSFET is turned off. A series resistor ($R_{SL}$) connecting the $I_{SENSE}$ pin to the current sense resistor ($R_{SNS(FET)}$) thus develops a ramping voltage drop. From the perspective of the $I_{SENSE}$ pin, this ramping voltage adds to the voltage across the sense resistor, effectively reducing the current comparator threshold in proportion to duty cycle. This stabilizes the control loop against subharmonic oscillation. The amount of reduction in the current comparator threshold ($\Delta V_{ISENSE}$) can be calculated using the following equation:

$$\Delta V_{ISENSE} = DUTY\ CYCLE \bullet \frac{V_{SEC}}{400k} \bullet R_{SL}$$

To program m = m2,

$$R_{SL} = \frac{1}{N} \bullet \frac{400k \bullet R_{SNS,FET}}{F \bullet Lm}$$

where

N = transformer turns ratio $N_{BAT}/N_{DCIN}$

$R_{SNS(FET)}$ = sense resistor connected between MOSFET and GND

f = switching frequency

Lm = magnetizing inductance of the transformer

Designs not needing slope compensation may replace $R_{SL}$ with a short.

### CALCULATING IC POWER DISSIPATION

The power dissipation of the LTC4110 is dependent upon the gate charge of the two MOSFETs ($Q_{G1}$ and $Q_{G2}$). The gate charge is determined from the manufacturer's data sheet and is dependent upon both the gate voltage swing and the drain voltage swing of the MOSFET. Use 5V for the gate voltage swing and $V_{DCIN}$ for the drain voltage swing.

$$P_D = V_{DCIN} \bullet (f_{OSC} (Q_{G1} + Q_{G2}) + I_Q)$$

## APPLICATIONS INFORMATION

Example:

$V_{DCIN}$ = 12V, $f_{OSC}$ = 300kHz, $Q_{G1}$ = $Q_{G2}$ = 15nC, $I_Q$ = 3mA

$P_D$ = 144mW

### SNUBBER DESIGN

The values given in the applications schematics have been found to work quite well for this 12V-1A application. Care should be taken in selecting other values for your application since efficiency may be impacted by a poor choice. For a detailed look at snubber design, Application Note 19 is very helpful.

### COMPONENT SELECTION

#### Current Sense Resistors

The LTC4110 uses up to three sense resistors—one of them optional. In general, current sense resistors should have a low temperature coefficient and sufficient power dissipation capability to avoid self-heating. Tolerance depends on system accuracy requirements.

**$R_{SNS(FET)}$:** The power rating of $R_{SNS(FET)}$ is defined by the highest value between $I_{CHG}$ or $I_{CAL}$ and the transformer turns ratio. Use one the following equations to calculate $I_{RSNS(FET)}$ depending on which value, $I_{CHG}$ or $I_{CAL}$ whichever is higher.

$$I_{R(SNSFETCHG)} = I_{CHG} \bullet \sqrt{\left(1+\frac{V_{BAT}}{N \bullet V_{DCIN}}\right)\left(\frac{N \bullet V_{BAT}}{E^2 \bullet V_{DCIN}}+1\right)}$$

$$I_{R(SNSFETCAL)} = I_{CAL} \bullet \sqrt{\left(1+\frac{V_{BAT}}{N \bullet V_{DCIN}}\right)\left(\frac{N \bullet E^2 \bullet V_{BAT}}{V_{DCIN}}+1\right)}$$

Plug in the higher value of the above two results as $I_{R(SNSFET)}$ and solve for power:

$$P_{R(SNSFET)} = I_{R(SNSFET)}^2 \bullet R_{SNS(FET)}$$

**$R_{CL}$:** $R_{CL}$ power rating is a function of the maximum forward current the system load draws. See Figure 11.

$$P_{R(CL)} = I_{MAX}^2 \bullet R_{CL}$$

Find a sense resistor who's power rating is greater than $P_{R(CL)}$

**$R_{SNS(BAT)}$:** $R_{SNS(BAT)}$ power rating is a function of the highest current value between $I_{CHG}$ or $I_{CAL}$ with which the battery will work. Plug in the higher of the two into $I_{BAT(MAX)}$ and solve:

$$P_{R(SNSBAT)} = I_{MAX}^2 \bullet R_{SNS(BAT)}$$

Use a sense resistor with a power rating greater than $P_{SNS(BAT)}$

### FLYBACK MOSFET SELECTION

The LTC4110 uses two low side N-channel switching MOSFETs in its flyback converter. These MOSFETs have dual roles. An any given time, only one MOSFET is the primary switch while the other acts as a synchronous rectifier on the secondary to improve efficiency. The individual MOSFETs' roles depend on whether the battery is being charged or calibrated. Each MOSFET specification must account for both roles.

The MOSFET voltage ratings in a flyback design must deal with other factors beyond $V_{IN}$. During switch "on" time, a current is established in the primary leakage inductance ($L_L$) equal to peak primary current ($I_{PRI}$). When the switch turns off, the energy stored in $L_L$, (Energy = $I_{PRI}^2 \bullet L_L/2$) causes the switch voltage to fly up, starting from the input voltage on up to the breakdown of the MOSFET if the voltage is not clamped. Thus, the snubber design is critical in dealing with this voltage spike and can influence the MOSFET voltage selection value. From a MOSFET point of view, the minimum voltage must be greater than the snubber clamp voltage $V_{SNUB}$. If $V_{SNUB}$ itself is too low, zener clamp dissipation rises rapidly thus encouraging higher MOSFET voltages. The maximum DC voltage that the N-channel MOSFETs sees is:

$$V_{CHG(FET)} = V_{DCIN} + \frac{V_{BAT}}{N}$$

$$V_{CAL(FET)} = V_{BAT} + N \bullet V_{DCIN}$$

## APPLICATIONS INFORMATION

The $V_{DS}$ ratings of the MOSFETs need to be higher than these values.

The MOSFET current ratings for the primary side must be higher than $I_{PRI}$, which is $I_{PRI(CHG)}$ or $I_{PRI(CAL)}$ for charge and Calibration mode respectively. See Equations 1 and 2. MOSFET current ratings for the secondary side must be higher than $I_{PRI}/N$. Since both MOSFETs must perform both roles, the minimum current rating of the MOSFETs should be greater than the higher of these values.

MOSFET power dissipation is a function of the RMS current flowing through the MOSFET.

Charge Mode:

$$I_{PRI(FETCHG)} = \frac{I_{CHG}}{E} \bullet \frac{\sqrt{V_{BAT} \bullet (V_{BAT} + N \bullet V_{DCIN})}}{V_{DCIN}}$$

$$I_{SEC(FETCHG)} = I_{CHG} \bullet \sqrt{\frac{V_{BAT} + N \bullet V_{DCIN}}{N \bullet V_{DCIN}}}$$

Calibration Mode:

$$I_{PRI(FETCAL)} = I_{CAL} \bullet \sqrt{\frac{V_{BAT} + N \bullet V_{DCIN}}{N \bullet V_{DCIN}}}$$

$$I_{SEC(FETCAL)} = I_{CAL} \bullet E \bullet \frac{\sqrt{V_{BAT} \bullet (V_{BAT} + N \bullet V_{DCIN})}}{V_{DCIN}}$$

Where $I_{PRI(FETCHG)}$ is the same FET as $I_{SEC(FETCAL)}$ and $I_{PRI(FETCAL)}$ is the same FET as $I_{SEC(FETCHG)}$.

Using the equation below, plug in the higher current from above into $I_{FET}$ to find each FET's power dissipation for the given mode.

$$P_{FET} = I_{FET}^2 \bullet R_{DS(ON)}$$

The $R_{DS(ON)}$ value of the MOSFET depends on $V_{GS}$. Conservatively you can use the $R_{DS(ON)}$ value with a $V_{GS}$ rating of 4.5V. If you are using a dual-MOSFET package, determine whether charge mode or calibration mode results is the highest overall power dissipation and use that as the rating for the dual MOSFET.

The MOSFET should be specified for fast or PWM switching. The MOSFET that meets all the above specifications but has the lowest $Q_G$ and/or $Q_{GD}$ is often the best choice.

### PowerPath MOSFET SELECTION

Important parameters for the selection of PowerPath MOSFETS are the maximum drain-source voltage $V_{DS(MAX)}$, threshold voltage $V_{GS(VT)}$, on-resistance $R_{DS(ON)}$ and $Q_{GATE}$.

The maximum allowable drain-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the maximum drain-source voltage seen in the application.

The gates of these MOSFETs are driven by the INID (Input Ideal Diode) and BATID (Battery Ideal Diode) pins. The gate turn-on voltage, $V_{GS}$, is set by the smaller of the PowerPath supply voltage or the internal clamping voltage $V_{GON}$. For the MOSFET driven from the INID pin its PowerPath supply voltage is the higher of the DCIN pin or DCOUT pin voltage. For the MOSFETs driven from the BATID pin, their PowerPath supply voltage is the higher of the DCOUT pin or BAT pin voltage. Logic-level $V_{GS(VT)}$ MOSFET is commonly used, but if a low supply voltage limits the gate voltage a sub-logic-level threshold MOSFET should be considered.

As a general rule, select a MOSFET with a low enough $R_{DS(ON)}$ to obtain the desired $V_{DS}$ while operating at full current load and an achievable $V_{GS}$. The MOSFET normally operates in the linear region and acts like a voltage controlled resistor. If the MOSFET is grossly undersized then it can enter the saturation region and a large $V_{DS}$ may result. However, the drain-source diode of the MOSFET, if forward biased will limit $V_{DS}$. A large $V_{DS}$ combined with the load current could result in excessively high MOSFET power dissipation. Keep in mind that the LTC4110 will regulate the forward voltage drop across the MOSFETs at 20mV ($V_{FR}$) if $R_{DS(ON)}$ is low enough. The required $R_{DS(ON)}$ can be calculated by dividing 0.02V by the load current in amps. Achieving forward regulation will minimize power loss and heat dissipation, but it is not a necessity. If a forward voltage drop of more than 20mV is acceptable then a smaller MOSFET can be used, but must be sized compatible with the higher power dissipation. Care should be taken to ensure

## APPLICATIONS INFORMATION

that the power dissipated is never allowed to rise above the manufacturer's recommended maximum level.

Switching transition time is another consideration. When the LTC4110 senses a need to switch any PowerPath MOSFETs on or off time delays are encountered. MOSFETs with higher $Q_{GATE}$ will require more bulk capacitance on DCOUT to hold up all the system's power supply function during the transition. The transition time of a MOSFET to an on or off state is directly proportional to the MOSFET gate charge. Switching times are given in the Electrical Characteristics Table (see $t_{dDON}$, $t_{dDOFF}$).

### TRANSFORMER

There are two ways to design a transformer.

1. Design it yourself.
2. Work with a transformer vendor to identify an off-the-shelf transformer.

Even if you choose to design it yourself, you still have to find a transformer manufacturer to make it for you.

We recommend contacting a transformer manufacturer directly since they often have online tools that can help you quickly find and select the right transformer. There are many off the shelf transformers that can be successfully be used with the LTC4110. Table 10 shows some suggested off the shelf transformers.

If you want to design a custom transformer optimized for your design, Application Note 19 has an example of how to design a Flyback transformer in the "Transformer" section.

Regardless of which way you go, we offer the following thoughts.

Turns ratio affects the duty factor of the power converter which impacts current and voltage stress on the power MOSFETs, input and output capacitor RMS currents and transformer utilization (size vs power). Using a 50% duty factor under nominal operating conditions usually gives reasonable results. For a 50% duty factor, the turns ratio is:

$$N = \frac{V_{BAT}}{V_{DCIN}}$$

$V_{BAT}$ is the nominal battery voltage. N should be calculated for the design operating in charging mode and in calibration mode. The final turns ratio should be chosen so that it is approximately equal to the average of the two calculated values for N. In addition, choose a turns ratio which can be made from the ratio of small integers. This allows bifilar windings to be used in the transformer, which can reduce the leakage inductance and the need for aggressive snubber design, thus improving efficiency.

Avoid transformer saturation under all operating conditions and combinations (usually the biggest problems occur at high output currents and extreme duty cycles). Choose the magnetizing inductance so that the current ripple is about 20% of DC current.

Finally, in low voltage applications, select a transformer with low winding resistance. This will improve efficiency at heavier loads.

**Table 10. Recommended Components Values for 12V Input Supply Li-Ion Battery Backup System Manager**

| Cell | MAX ($I_{CHG}$, $I_{CAL}$) (A) | $R_{SNS(BAT)}$(mΩ) | $R_{SNS(FET)}$(mΩ) | TRANSFORMER INDUCTANCE (µH) | TRANSFORMER VENDOR AND PART NUMBER |
|---|---|---|---|---|---|
| 3 | 1 | 100 | 50 | 24 | BH 510-1019 TDK PCA14.5/6ER-U03S002 |
| 3 | 2 | 50 | 25 | 12 | COILTRONICS VP4-0140-R |
| 3 | 3 | 33 | 15 | 9 | TDK PCA20EFD-U04S002 |
| 4 | 1 | 100 | 50 | 24 | COILTRONICS VPH4-0140-R |
| 4 | 2 | 50 | 25 | 12 | COILTRONICS VPH4-0075-R |
| 4 | 3 | 33 | 15 | 9 | COILTRONICS VP5-0155-R |

Note: 1:1 turns ratio for all the transformers listed in the table..

# APPLICATIONS INFORMATION

## INPUT AND OUTPUT CAPACITORS

The LTC4110 uses a synchronous flyback regulator to provide high battery charging current. A chip ceramic capacitor is recommended for both the input and output capacitors because it provides low ESR and ESL and can handle the high RMS ripple currents. However, some Hi-Q capacitors may produce high transients due to self resonance under some start-up conditions, such as connecting the charger input to a hot power source. For more information, refer to Application Note 88.

For charge mode, the ripple current can be calculated as follows:

$$I_{RMSDCINCAP} = \frac{I_{CHG}}{E} \bullet \sqrt{\frac{N \bullet V_{BAT}}{V_{DCIN}}}$$

and

$$I_{RMSBATCAP} = I_{CHG} \bullet \sqrt{\frac{V_{BAT}}{N \bullet V_{DCIN}}}$$

For calibration mode, the ripple current can be calculated as follows:

$$I_{RMSDCINCAP} = I_{CAL} \bullet E \bullet \sqrt{\frac{N \bullet V_{BAT}}{V_{DCIN}}}$$

and

$$I_{RMSBATCAP} = I_{CAL} \bullet \sqrt{\frac{V_{BAT}}{N \bullet V_{DCIN}}}$$

EMI considerations usually make it desirable to minimize ripple current in the battery leads, and beads or inductors may be added to increase battery impedance at the 300kHz switching frequency. Switching ripple current splits between the battery and the output capacitor depending on the ESR of the output capacitor and the battery impedance. If the ESR of the output capacitor is 0.1Ω and the battery impedance is raised to 2v with a bead or inductor, only 5% of the ripple current will flow in the battery. Similar techniques may also be applied to minimize EMI from the input leads.

### Diodes

Schottky diodes should be placed in parallel with the drain and source of the Flyback MOSFETs. This prevents body diode turn-on and improves efficiency by eliminating loss from reverse recovery in these diodes. It also reduces conduction loss during the dead time of the MOSFETs.

## PROTECTING SMBUS PINS

The SMBus inputs, SCL and SDA, are exposed to uncontrolled transient signals whenever a battery is connected to the system. If the battery contains a static charge, the SMBus inputs are subjected to transients that can cause damage after repeated exposure. Also, if the battery's positive terminal makes contact to the connector before the negative terminal, the SMBus inputs can be forced below ground with the full battery potential, causing a potential for latch-up in any of the devices connected to the SMBus inputs. Therefore, it is good design practice to protect the SMBus inputs as shown in Figure 19.

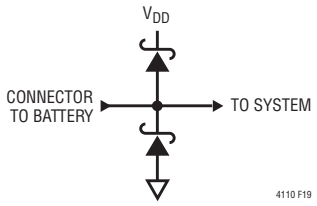



**Figure 19. SMBus Protection**

## START-UP DELAYS

When exiting shutdown mode, internal supplies must ramp up and settle. 500µs-1ms should be adequate after shutdown is exited or when power is quickly (<100µs) first applied to the IC. For slow power ramp-up (>1ms) internal supplies will be in regulation after power input reaches 4.5V. Until internal supplies settle, status outputs may be invalid.

## APPLICATIONS INFORMATION

### OPERATION WITH DUAL BACKUP SYSTEMS

If a dual backup system consisting of two LTC4110s each with its own backup battery is needed and a SMBus is used, each LTC4110 should be programmed by the SELA pin to have different addresses. If smart batteries with SMBus are used, a SMBus mux may be required to selectively address each battery. This mux may also be used to address the LTC4110. See SMBus Interface section for more information.

### BACKUP OPERATION WITH EXTERNAL BACKUP SUPPLY REGULATOR

If a dedicated DC regulator with enable inputs is used in place of an actual battery to supply backup power, the PowerPath MOSFETs connected to the BATID pin may not be required. It depends on the regulator's ability to accept being back driven by a voltage on the DCOUT pin coming from some other power source such as DCIN. The ACPb pin can control the regulator such that it is turned on when DCIN goes away. However for fastest transient response, keeping the regulator on may prove to work better. The output voltage of the regulator should be less than DCOUT under normal operating conditions so that DCIN is providing the power to the load. The voltage provided by the regulator must not be allowed to go below the lower limit of the DCOUT pin or erratic operation may result.

### BACKUP OPERATION WITH A DOWNSTREAM REGULATOR

Since the backup voltage supplied to the load is not regulated, often some form of a regulator is needed between the LTC4110 and the actual load. The characteristics of this regulator should offer high efficiency when running from the battery in backup mode to maximize backup time. Some regulators may need advance warning when to enter into this mode, which can be accomplished by using the LTC4110's ACPb pin.

### DCIN TO BATTERY TRANSITION CHATTER REMOVAL

The LTC4110 is designed to automatically switch the battery to the output load when DCIN is lost. Under certain conditions, a rapid loss of DCIN can cause the input and battery ideal diode circuits to chatter. The result is the transition time between the DCIN FET turning fully off and the battery FET turning fully on can last in excess of 200ms with each switching on and off multiple times.

This problem is likely to occur under the following conditions:

1. Large system load causing the INID pin to be more than 3V below DCIN.
2. The DCIN and battery voltages are approximately the same.
3. The DCIN pin goes high impedance very rapidly (less than 10µs)

Q1 and R1 shown in Figure 20 increase the effective hysteresis of the DCDIV pin by using the ACPb pin to drive Q1. The threshold of Q1 must be less than the $V_{SUPPLY}$ to assure the drain of Q1 pulls down to ground when ACPb is high. R1 sets the amount of increase in negative hysteresis you need relative to the values chosen for the DCDIV resistor divider. A 100k is suggested as a starting point. You will also need to place a capacitor $C_{ACPDLY}$ on the ACPDLY pin. This capacitor in conjunction with resistor $R_{VREF}$ should be set for a delay of 10ms, which is more than sufficient to eliminate all the chatter.

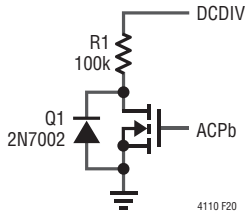



**Figure 20.**

# APPLICATIONS INFORMATION

## PCB LAYOUT CONSIDERATIONS

For maximum efficiency, the switch node rise and fall times should be minimized. To prevent magnetic and electrical field (EMI) radiation and high frequency resonant problems, proper layout of the components connected to the IC is essential.

### Flyback Layout

Lowest EMI and maximum efficiency are obtained when the high frequency switching current loop area is minimized. It is best to make direct connections, avoiding the use of other circuit board copper planes, i.e. no vias, in making the following connections for this prevents current based noise injection into the copper planes below.

1. Input/output capacitors positive terminals need to be placed as close as possible between the flyback transformer "top" or positive supply rail connections and $R_{SNS(FET)}$ ground connection.
2. Place flyback MOSFETs drain connections right next to the flyback transformers "bottom" connections.
3. Place the $R_{SNS(FET)}$ current sense resistor right next to the N-MOSFET source connections completing the connection back to the input/output capacitors' negative terminals.
4. Place the snubber connections as close as possible to the circuit after the above layout connections are completed as required. Again, avoid using vias.
5. The layer below the flyback layout should be ground.

### Other Recommendations

6. Optionally use vias to connect power supply sources positive and negative (ground) connections from other copper layers to the flyback layout. Place multiple vias in a tight cluster such that they act as one large via. Recommended 1 via for each 0.5A of current
7. The current sense feedback traces must be routed together as a single pair on the same layer at any given time with smallest trace spacing possible. Locate any filter component on these traces next to the IC and not at the sense resistor location.
8. The control IC must be close to the switching FET's gate terminals. Keep the gate drive signals short for a clean FET drive. This includes IC supply pins that connect to the switching FET source pins. The IC can be placed on the opposite side of the PCB relative to flyback layout above.
9. Figure 21 shows an inexpensive way to achieve Kelvin like sensing using standard current sense resistors.

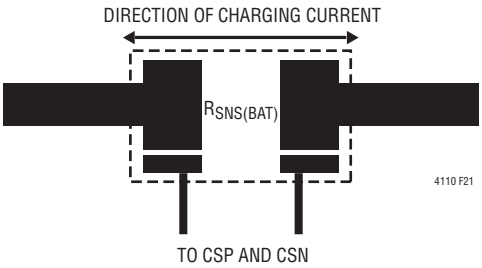
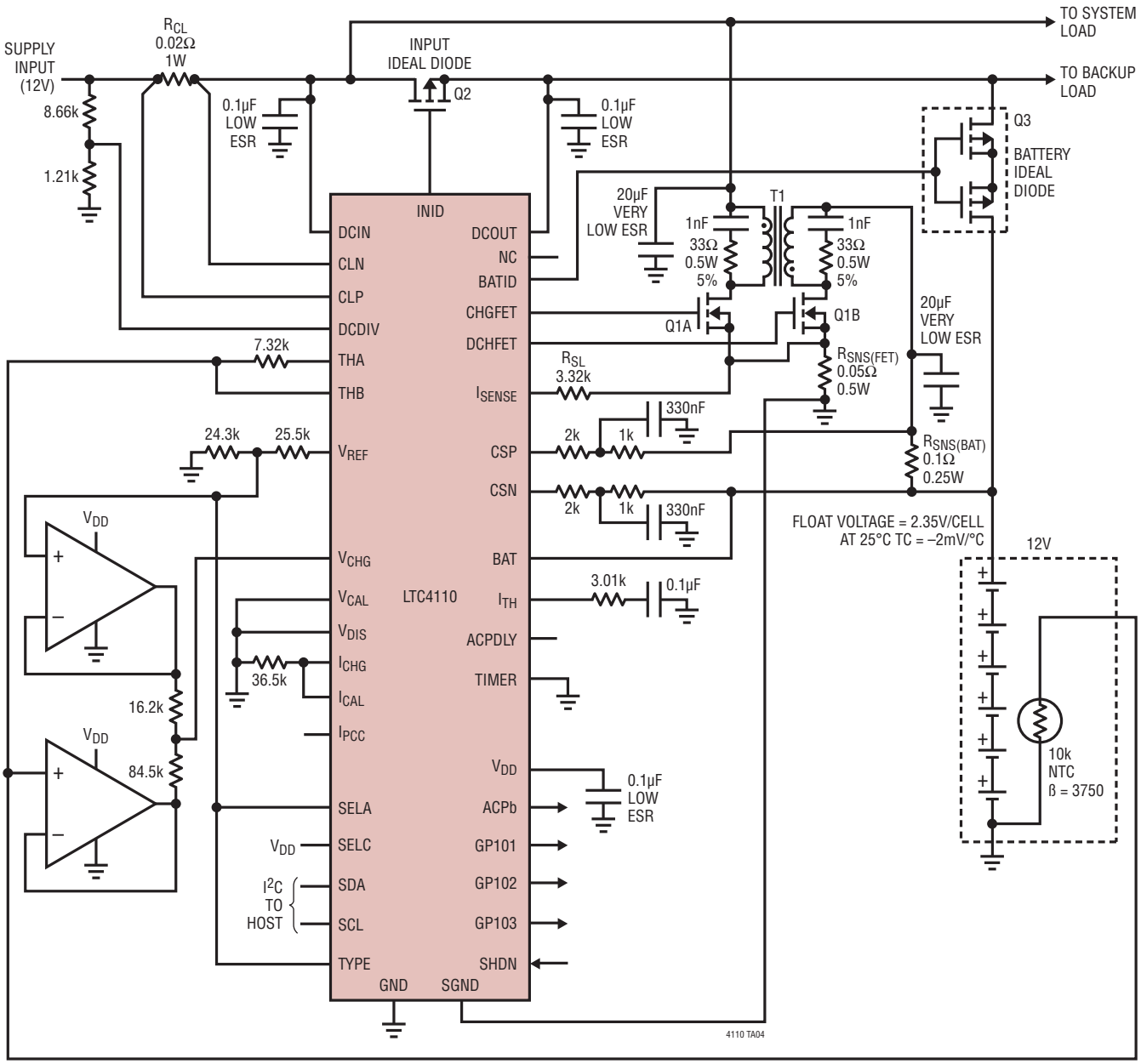



**Figure 21. Kelvin Sensing of Battery Current**

## TYPICAL APPLICATIONS

**Battery Backup System Manager Controlling a Six-Series Cell SLA Battery with Temperature Compensation**

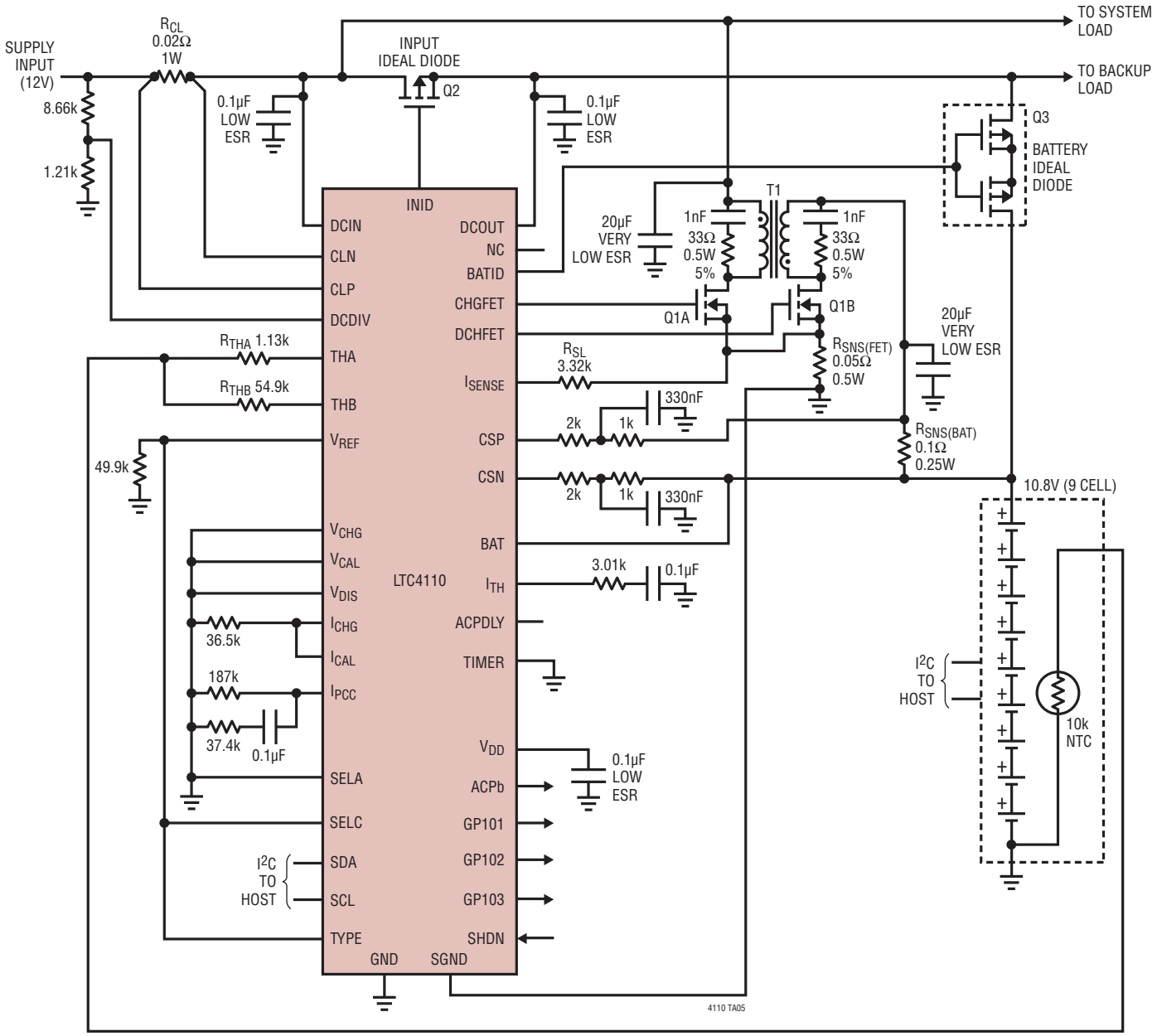



NO TIMER
HIGH CURRENT BACKUP LOAD DESIGN
0.5A BACKDRIVE CURRENT CUTOFF (CALIBRATION)
1A CHARGE AND CALIBRATION CURRENT
ALL RESISTORS ARE 1% UNLESS NOTED OTHERWISE

Q1: Si7216DN
Q2: Si7445DP
Q3: Si7983DP
T1: BH510-1019

# TYPICAL APPLICATIONS

**Battery Backup System Manager Controlling a Nine-Series Cell NiMH Battery with Calibration Managed by Host Processor**

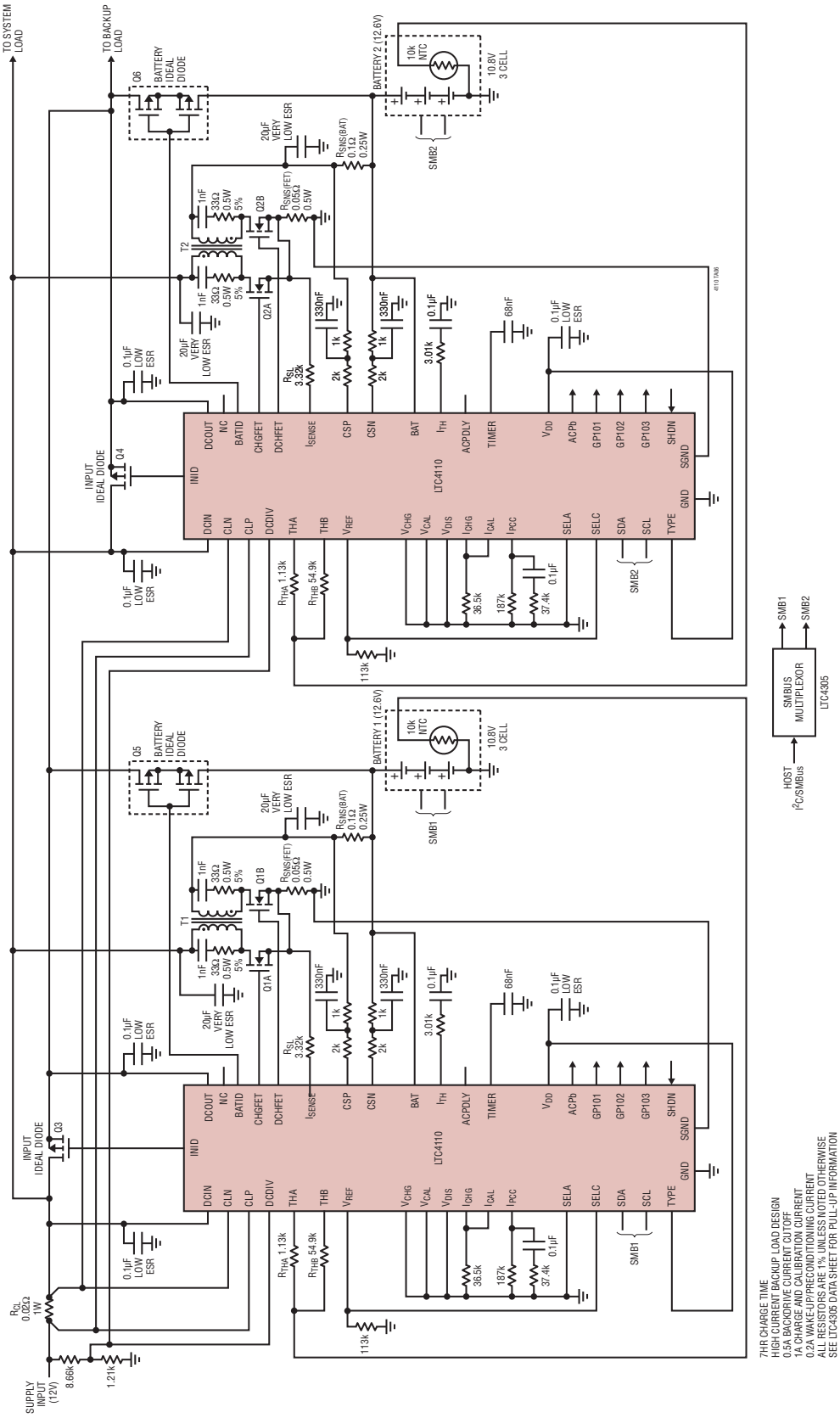



NO TIMER
HIGH CURRENT BACKUP LOAD DESIGN
0.5A BACKDRIVE CURRENT CUTOFF (CALIBRATION)
1A CHARGE AND CALIBRATION CURRENT
0.2A WAKE-UP/PRECONDITIONING CURRENT
HOST PROVIDES SMBus PULL-UP RESISTORS
ALL RESISTORS ARE 1% UNLESS NOTED OTHERWISE

Q1: Si7216DN
Q2: Si7445DN
Q3: Si7983DP
T1: BH510-1019

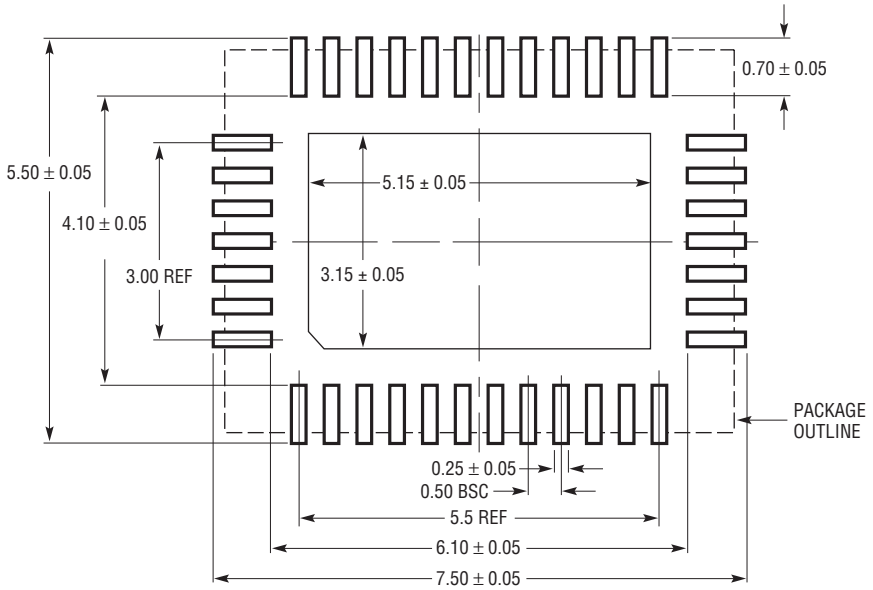
## TYPICAL APPLICATIONS

**Dual Battery Backup System Managers Controlling a Two Three-Series Cell Li-Ion, Gas Gauge Smart Batteries with Calibration Managed by Host Processor and SMBus Multiplexer**

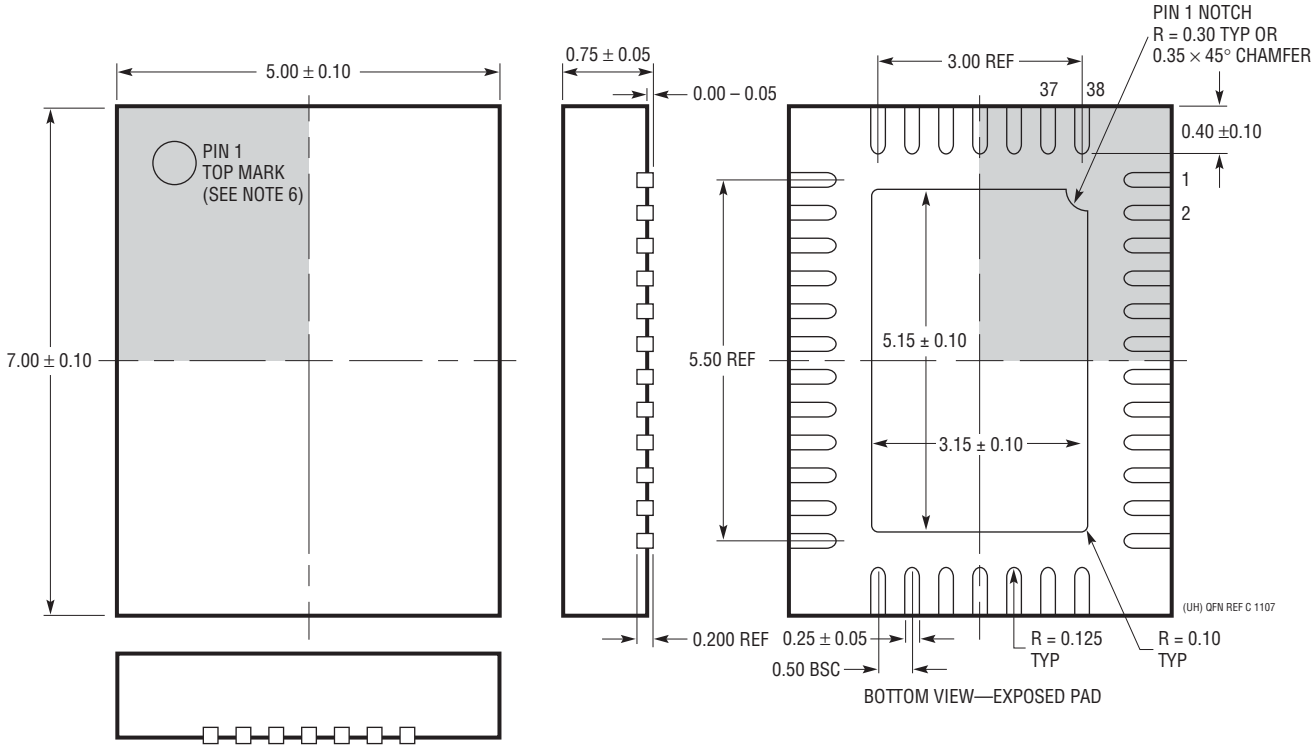


# PACKAGE DESCRIPTION

**UHF Package**
**38-Lead Plastic QFN (5mm × 7mm)**
(Reference LTC DWG # 05-08-1701)




RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED




BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



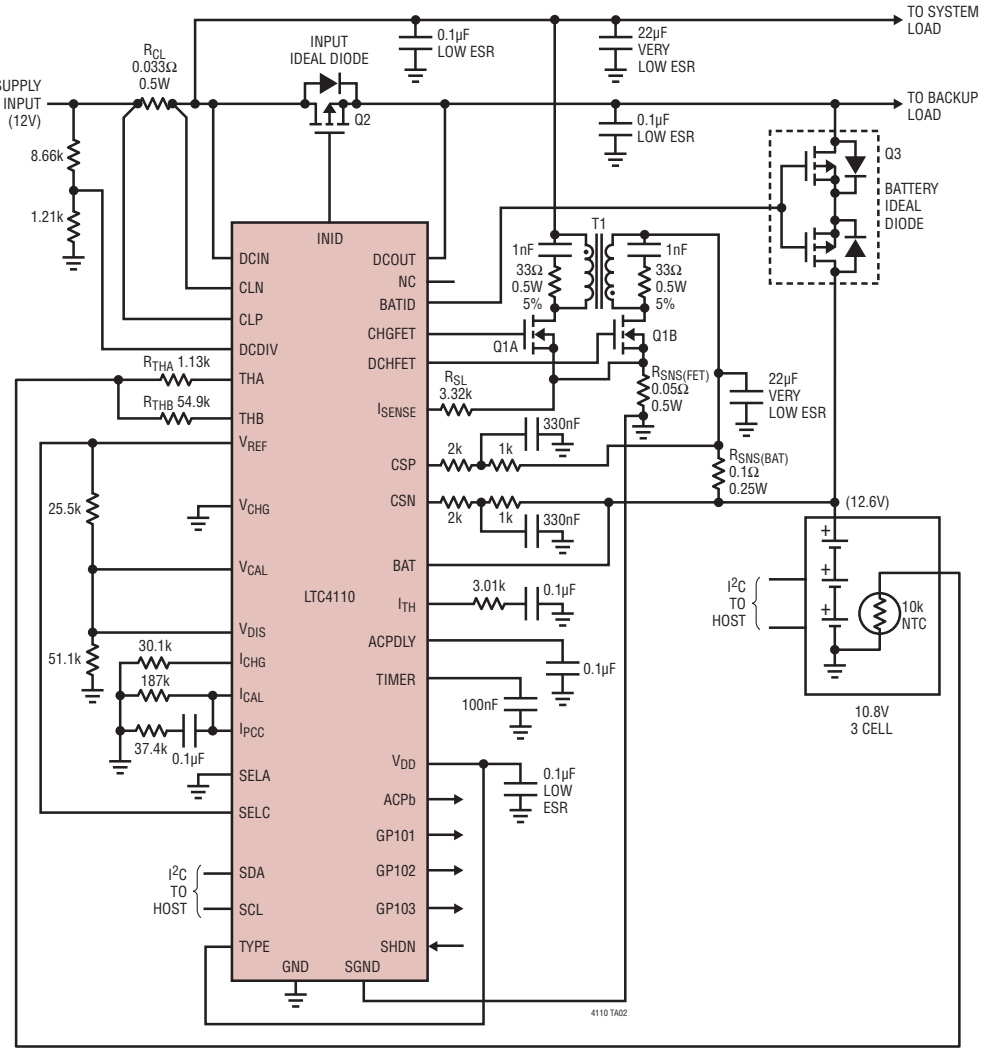
Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

## TYPICAL APPLICATION

**Battery Backup System Manager Controlling a Three-Series Cell Li-Ion, Gas Gauge Smart Battery with Calibration Managed by Host Processor**

15ms ACPDLY
7HR TIMER
LOW CURRENT BACKUP DESIGN
2.8V CUTOFF VOLTAGE FOR $V_{CAL}$ AND $V_{DIS}$
1A CHARGE CURRENT
0.2A CALIBRATION AND PRECONDITIONING CURRENT
0.3A BACKDRIVE CURRENT CUTOFF
HOST PROVIDES SMBus PULL-UP RESISTORS
ALL RESISTORS ARE 1% UNLESS NOTED OTHERWISE

Q1: Si7216DN
Q2: Si7445DP
Q3: SiA911DJ
T1: BH510-1019




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1760 | Smart Battery System Manager | Autonomous Power Management and Battery Charging for Two Smart Batteries, SMBus Rev 1.1 Compliant |
| LTC1960 | Dual Battery Charger/Selector with SPI Interface | Simultaneous Charge or Discharge of Two Batteries, DAC Programmable Current and Voltage, Input Current Limiting Maximizes Charge Current |
| LTC4412/ LTC4412HV | PowerPath Controllers in ThinSOT™ | More Efficient than Diode ORing, Automatic Switching Between DC Sources, Simplified Load Sharing, $3V \le V_{IN} \le 28V$, ($3V \le V_{IN} \le 36V$ for HV) ThinSOT Package |
| LTC4414 | 36V, Low Loss PowerPath Controller for Large PFETs | Drives Large $Q_G$ PFETs, Very Low Loss Replacement for Power Supply ORing Diodes, 3.5V to 36V AC/DC Adapter Voltage Range, MSOP-8 Package |
| LTC4416/ LTC4416-1 | Dual, Low Loss PowerPath Controllers | Drives Large PFETs, Low Loss Replacement for Power Supply ORing Diodes, Operation to 36V, Programmable Autonomous Switching |

ThinSot is a Trademark of Linear Technology Corporation.




Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT 0409 REV B • PRINTED IN USA

© LINEAR TECHNOLOGY CORPORATION 2008

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View LTC4110EUHF#PBF on WIN SOURCE
- Linear Technology Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management