THE DATASHEET OF

LTC2926IGN#PBF

MOSFET-Controlled Power Supply Tracker

FEATURES

- **Flexible Power Supply Tracking and Sequencing**
- **Adjustable Ramp Rates, Offsets and Time Delays**
- **Controls Three Supplies with Series MOSFETs**
- **Integrated Remote Sense Switching**
- FAULT Input/Output
- STATUS Output/Power Good Input
- Available in 20-Lead Narrow SSOP and 20-Lead QFN (4mm × 5mm) Packages

APPLICATIONS

- V_{CORE} and $V_{I/O}$ Supply Tracking
- Microprocessor, DSP and FPGA Supplies
- Servers
- Communications Systems

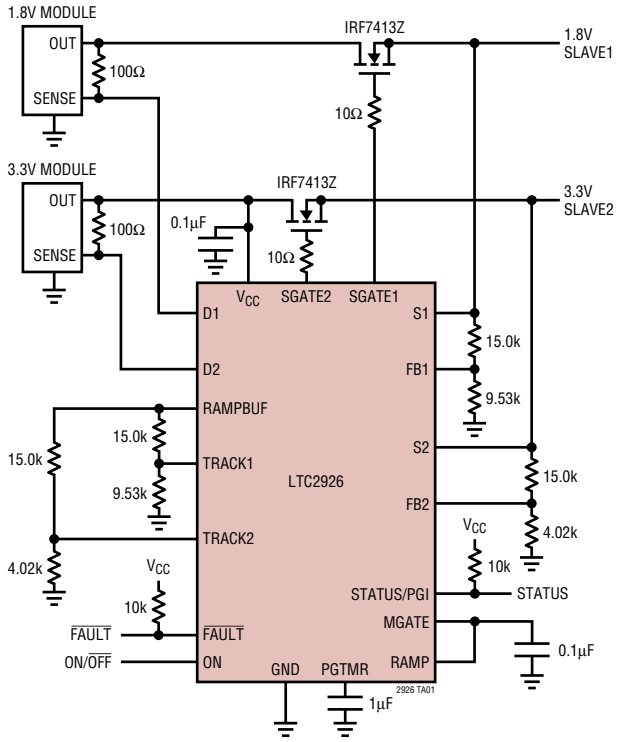
DESCRIPTION

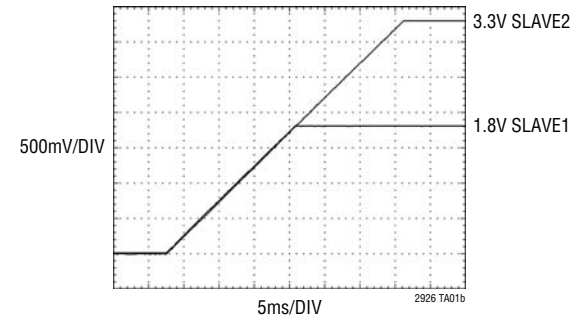
The LTC2926 provides a simple solution for tracking and sequencing up to three power supply rails. An N-channel MOSFET and a few resistors per channel configure the load voltages to ramp up and down together, with voltage offsets, with time delays or with different ramp rates.

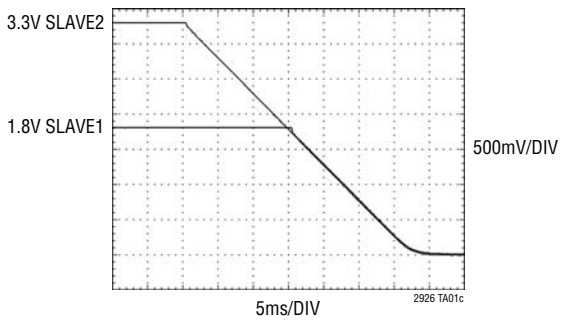
Automatic remote sense switching compensates for voltage drops across the MOSFETs. The LTC2926 provides two integrated switches as well as a signal to control optional additional external N-channel MOSFET sense switches.

The LTC2926 includes I/O signals for communication with other devices. The status output asserts after tracking and sequencing have completed. A low voltage on the power good input after an adjustable timeout period causes load disconnect. A low voltage on the fault I/O causes immediate load disconnect. Until it is reset, a fault latch prevents tracking and keeps the loads disconnected.

TYPICAL APPLICATION





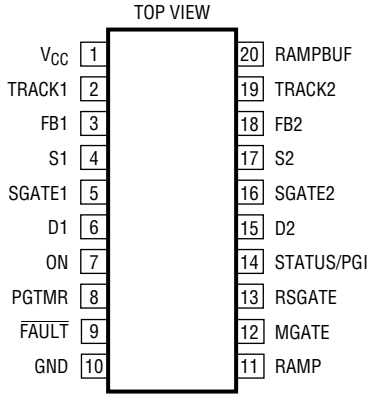


ABSOLUTE MAXIMUM RATINGS

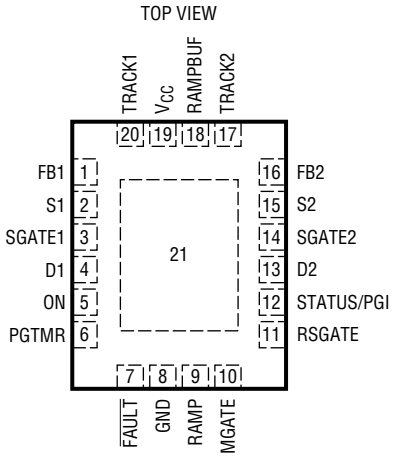
(Notes 1, 2)

Supply Voltage (V_{CC}) ..... –0.3V to 10V
Input Voltages
ON ..... –0.3V to 10V
RAMP .....–0.3V to V_{CC} + 1V
TRACK1, TRACK2 .....–0.3V to V_{CC} + 0.3V
PGTMR .....–0.3V to V_{CC} + 0.3V
Input/Output Voltages
$\overline{FAULT}$ ..... –0.3V to 10V
STATUS/PGI (Note 3)..... –0.3V to 11.5V
Output Voltages
RAMPBUF.....–0.3V to V_{CC} + 0.3V
FB1, FB2, D1, S1, D2, S2 ..... –0.3V to 10V
MGATE, RSGATE (Note 3)..... –0.3V to 11.5V
SGATE1, SGATE2 (Note 3) ..... –0.3V to 11.5V
RMS Currents
TRACK1, TRACK2 .....5mA
FB1, FB2 .....5mA
D1, S1, D2, S2 .....30mA
Operating Temperature
LTC2926C ..... 0°C to 70°C
LTC2926I ..... –40°C to 85°C
Storage Temperature Range
GN Package ..... –65°C to 150°C
UFD Package..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
GN Package ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
20-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 85°C/W



UFD PACKAGE
20-LEAD (4mm × 5mm) PLASTIC QFN
EXPOSED PAD (PIN 21) IS GND
PCB CONNECTION OPTIONAL
T_{JMAX} = 125°C, θ_{JA} = 43°C/W

ORDER PART NUMBER	ORDER PART NUMBER	UFD PART MARKING*
LTC2926CGN LTC2926IGN	LTC2926CUFD LTC2926IUFD	2926 2926

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.*The temperature grade is identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage							
V_{CC}	Input Supply Voltage	Operating Range	●	2.9	3.3	5.5	V
I_{CC}	Input Supply Current	I_{TRACKn} = 0mA, I_{FBn} = 0mA, $I_{RAMPBUF}$ = 0mA	●	1.5	2.5	3.5	mA
		I_{TRACKn} = –1mA, I_{FBn} = –1mA, $I_{RAMPBUF}$ = –3mA	●	8.5	9.5	10.5	mA
$V_{CC(UVLO)}$	Input Supply Undervoltage Lockout	V_{CC} Rising	●	2.2	2.4	2.6	V
$\Delta V_{CC(UVLO)}$	Input Supply Undervoltage Lockout Hysteresis		●	15	50	75	mV
Control and I/O							
$V_{ON(TH)}$	ON Pin Threshold Voltage	V_{ON} Rising	●	1.20	1.23	1.26	V
$\Delta V_{ON(TH)}$	ON Pin Threshold Voltage Hysteresis		●	40	75	110	mV
I_{ON}	ON Pin Input Current	V_{ON} = 1.2V, V_{CC} = 5.5V	●		0	±100	nA
$V_{ON(CLR)}$	ON Pin Fault Clear Threshold Voltage	V_{ON} Falling	●	0.465	0.500	0.535	V
t_{CLR}	Fault Clear Delay	V_{ON} Falling	●	1	3	10	µs
$V_{ON(ARM)}$	ON Pin Fault Arm Threshold Voltage	V_{ON} Rising	●	0.565	0.600	0.635	V
t_{ARM}	Fault Arm Delay	V_{ON} Rising	●	1	4.5	10	µs
$V_{\overline{FAULT}(TH)}$	$\overline{FAULT}$ Pin Input Threshold Voltage	$V_{\overline{FAULT}}$ Falling	●	0.465	0.500	0.535	V
$I_{\overline{FAULT}(UP)}$	$\overline{FAULT}$ Pin Pull-up Current	Fault Latch Clear, $V_{\overline{FAULT}}$ = 1.5V	●	–3.0	–8.5	–13	µA
$V_{\overline{FAULT}(OL)}$	$\overline{FAULT}$ Pin Output Low Voltage	Fault Latch Set, $I_{\overline{FAULT}}$ = 5mA, V_{CC} = 2.7V	●		100	400	mV
$V_{\overline{FAULT}(OH)}$	$\overline{FAULT}$ Pin Output High Voltage ($V_{CC} - V_{\overline{FAULT}}$)	Fault Latch Clear, $I_{\overline{FAULT}}$ = –1µA	●	300	550	900	mV
$V_{PGI(TH)}$	STATUS/PGI Pin Input Threshold Voltage	$V_{STATUS/PGI}$ Rising	●	1.10	1.23	1.36	V
$\Delta V_{PGI(TH)}$	STATUS/PGI Pin Input Threshold Voltage Hysteresis		●	30	75	150	mV
$I_{PGI(UP)}$	STATUS/PGI Pin Pull-Up Current	STATUS/PGI On, $V_{STATUS/PGI}$ = 1.5V	●	–7	–10	–13	µA
$V_{STATUS(OL)}$	STATUS/PGI Pin Output Low Voltage	V_{ON} Low, $I_{STATUS/PGI}$ = 5mA, V_{CC} = 2.7V	●		200	400	mV
$V_{STATUS(OH)}$	STATUS/PGI Pin Output High Voltage ($V_{STATUS/PGI} - V_{CC}$)	$I_{STATUS/PGI}$ = –1µA	●	5.0	5.5	6.0	V
$V_{PGTMR(TH)}$	PGTMR Pin Threshold Voltage	V_{PGTMR} Rising	●	1.10	1.23	1.36	V
$I_{PGTMR(UP)}$	PGTMR Pin Pull-Up Current	ON High, V_{PGTMR} = 1V	●	–8	–10	–12	µA
$I_{PGTMR(DN)}$	PGTMR Pin Pull-Down Current	ON Low, V_{PGTMR} = 0.1V, V_{CC} = 2.7V	●	0.5	4	10	mA
$V_{PGTMR(CLR)}$	PGTMR Pin Clear Threshold Voltage	V_{PGTMR} Falling	●	50	100	150	mV
Ramp Buffer							
$I_{RAMP(IN)}$	RAMP Pin Input Current	0V < V_{RAMP} < 5.5V, V_{CC} = 5.5V	●		0	±1	µA
$V_{RAMPBUF(OS)}$	Ramp Buffer Offset Voltage	V_{RAMP} = 1/2 V_{CC}, $I_{RAMPBUF}$ = 0mA	●		0	±10	mV
$V_{RAMPBUF(OL)}$	RAMPBUF Pin Output Low Voltage	$I_{RAMPBUF}$ = 3mA	●		32	60	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{RAMPBUF(OH)}$	RAMPBUF Pin Output High Voltage (V_{CC} – $V_{RAMPBUF}$)	$I_{RAMPBUF}$ = –3mA	●		60	80	mV
Tracking Channels							
$I_{ERROR(\%)}$	I_{FBn} to I_{TRACKn} Current Mismatch (I_{FBn} – I_{TRACKn})/I_{TRACKn} • 100%	I_{TRACKn} = –10µA I_{TRACKn} = –1mA	● ●		0 0	±3 ±3	% %
V_{TRACK}	TRACK Pins Voltage	I_{TRACKn} = –10µA I_{TRACKn} = –1mA	● ●	0.776 0.776	0.800 0.800	0.824 0.824	V V
$V_{FB(REF)}$	FB Pins Internal Reference Voltage	V_{TRACKn} = V_{CC}, I_{FBn} = 0mA	●	0.784	0.800	0.816	V
$I_{FB(LEAK)}$	FB Pins Leakage Current	V_{FBn} = 0.8V, V_{CC} = 5.5V	●		0	±10	nA
$V_{FB(CLAMP)}$	FB Pins Clamp Voltage	–1mA < I_{FBn} < –1µA	●	1.7	2.0	2.4	V
Master Ramp and Supply							
ΔV_{MGATE}	MGATE Pin External N-Channel Gate Drive (V_{MGATE} – V_{CC})	I_{MGATE} = –1µA	●	5.0	5.5	6.0	V
$I_{MGATE(UP)}$	MGATE Pin Pull-Up Current	Fault Latch Clear, V_{ON} High, V_{MGATE} = 3.3V	●	–7	–10	–13	µA
$I_{MGATE(DN)}$	MGATE Pin Pull-Down Current	Fault Latch Clear, V_{ON} Low, V_{MGATE} = 3.3V	●	7	10	13	µA
$I_{MGATE(FAULT)}$	MGATE Pin Fault Pull-Down Current	Fault Latch Set, V_{ON} High, V_{MGATE} = 5.5V, V_{CC} = 5.5V	●	5	20	50	mA
Slave Supplies							
ΔV_{SGATE}	SGATE Pins External N-Channel Gate Drive (V_{SGATEn} – V_{CC})	I_{SGATEn} = –1µA, V_{FBn} = 0.75V	●	5.0	5.5	6.0	V
$I_{SGATE(UP)}$	SGATE Pins Pull-Up Current	Fault Latch Clear, V_{FBn} = $V_{FB(REF)}$ – 10mV, V_{SGATEn} = 3.3V	●	–6	–10	–13	µA
$I_{SGATE(DN)}$	SGATE Pins Pull-Down Current	Fault Latch Clear, V_{FBn} = $V_{FB(REF)}$ + 10mV, V_{SGATEn} = 3.3V	●	6	10	13	µA
$I_{SGATE(UPFST)}$	SGATE Pins Fast Pull-Up Current	Fault Latch Clear, V_{FBn} = 0V, V_{SGATEn} = 3.3V	●	–21	–30	–39	µA
$I_{SGATE(DNFST)}$	SGATE Pins Fast Pull-Down Current	Fault Latch Clear, V_{FBn} = 1V, V_{SGATEn} = 3.3V	●	21	30	39	µA
$I_{SGATE(FAULT)}$	SGATE Pins Fault Pull-Down Current	Fault Latch Set, V_{ON} High, V_{SGATEn} = 5.5V, V_{CC} = 5.5V	●	5	20	50	mA
Remote Sense Switches							
ΔV_{RSGATE}	RSGATE Pin External N-Channel Gate Drive (V_{RSGATE} – V_{CC})	I_{RSGATE} = –1µA	●	5.0	5.5	6.0	V
$I_{RSGATE(UP)}$	RSGATE Pin Pull-Up Current	Fault Latch Clear, Switches On, V_{RSGATE} = 0V	●	–7	–10	–13	µA
$I_{RSGATE(DN)}$	RSGATE Pin Pull-Down Current	Fault Latch Clear, Switches Off, V_{RSGATE} = 3.3V	●	7	10	13	µA
$I_{RSGATE(FAULT)}$	RSGATE Pin Fault Pull-Down Current	Fault Latch Set, Switches Off, V_{RSGATE} = 5.5V, V_{CC} = 5.5V	●	5	20	50	mA
$V_{RSGATE(TH)}$	RSGATE Pin Threshold Voltage	Ramping Completed on Pin Low, RSGATE Falling	●	1.10	1.23	1.36	V
$R_{SW(ON)}$	Remote Sense Switch On-Resistance	Switches On, V_{Dn} = V_{CC} + 0.3V, I_{Sn} = –10mA	●		2	10	Ω

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

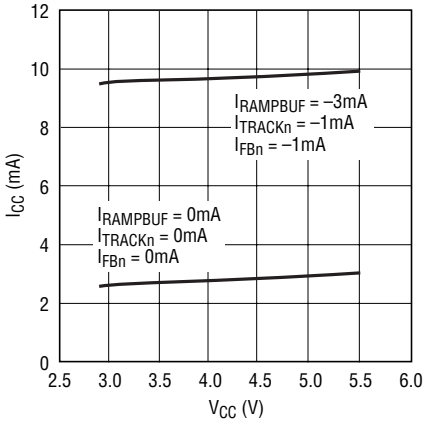
Note 2: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 3: The MGATE, SGATE1, SGATE2, RSGATE and STATUS/PGI pins are internally limited to a minimum of 11.5V. Driving these pins to voltages beyond the clamp level may damage the part.

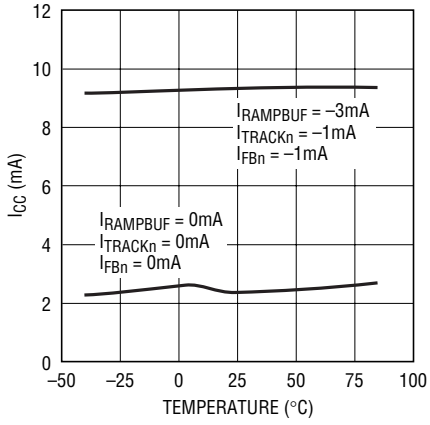
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C, V_{CC} = 3.3V unless otherwise specified.

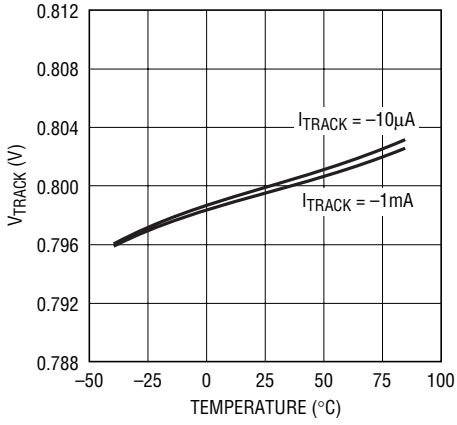
Supply Current vs Supply Voltage



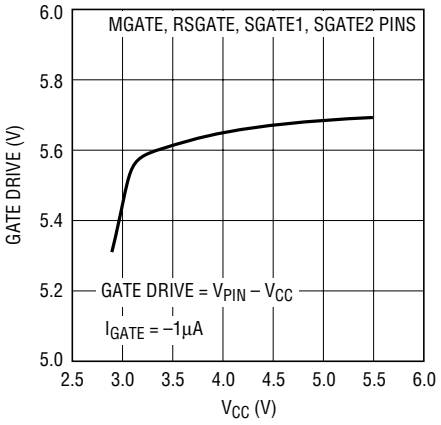
Supply Current vs Temperature



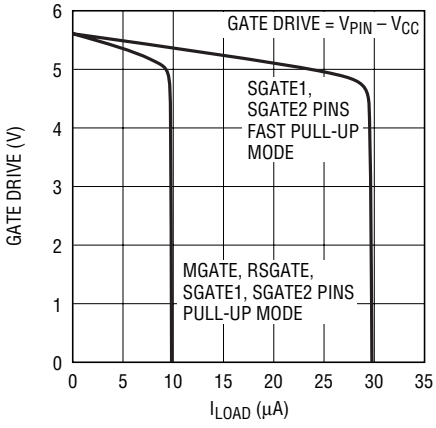
Track Pin Voltage vs Temperature



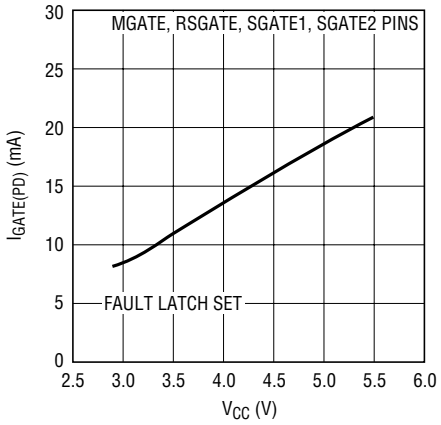
Gate Drive Voltages vs Supply Voltage



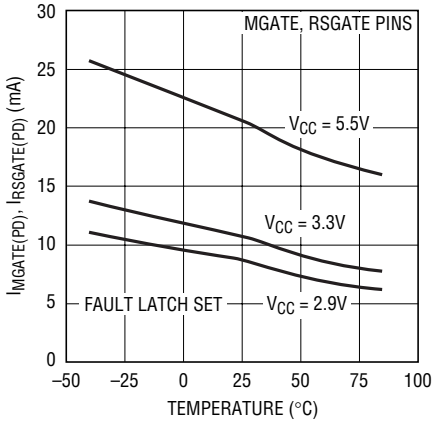
Gate Drive Voltages vs Load Current



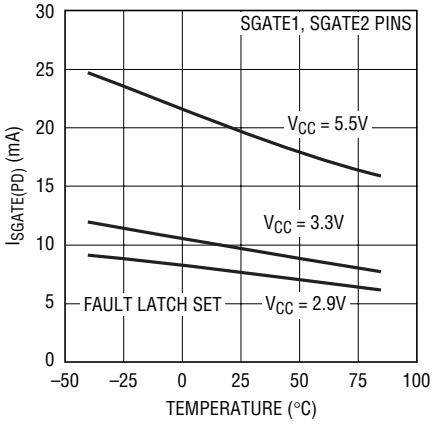
Gate Fault Pull-Down Currents vs Supply Voltage



MGATE, RSGATE Fault Pull-Down Currents vs Temperature



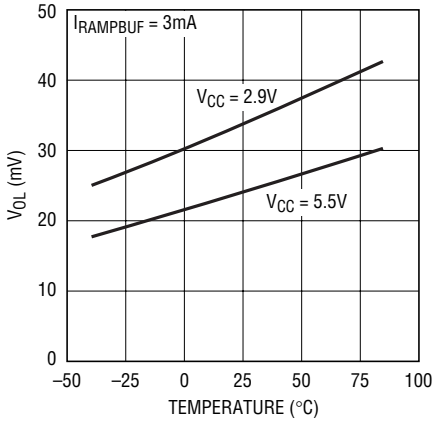
SGATE Fault Pull-Down Current vs Temperature



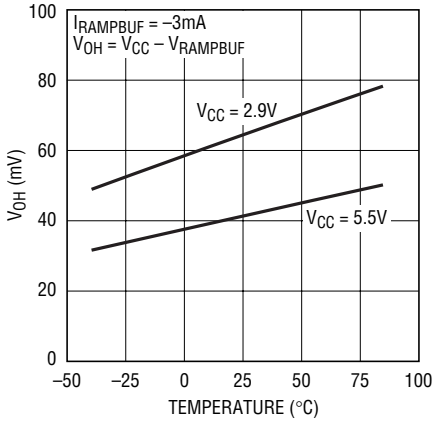
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C, V_{CC} = 3.3V unless otherwise specified.

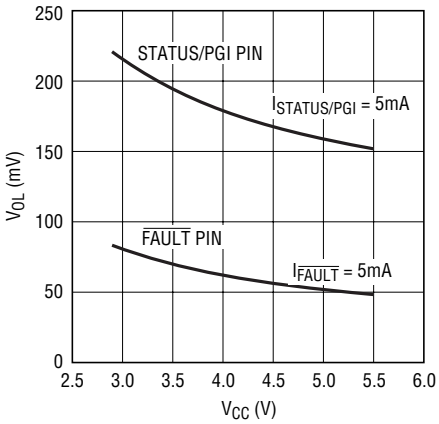
RAMPBUF Output Low Voltage vs Temperature



RAMPBUF Output High Voltage vs Temperature



Logic Output Low Voltages vs Supply Voltage



PIN FUNCTIONS GN/UFD Packages

D1, S1, D2, S2 (Pins 6, 4, 15, 17/Pins 4, 2, 13, 15): Remote Sense Switches #1 and #2. A 10Ω (max) switch connects each pair of pins (D1/S1 and D2/S2) after MGATE, SGATE1 and SGATE2 are all fully enhanced (MGATE > RAMP + 4.9V or RAMP > V_{CC}, and SGATE1, SGATE2 > V_{CC} + 4.9V). The switch can be used to compensate for the voltage drop across the external MOSFET that controls a slave or the master supply. Connect the switch between the load and the supply's sense node. Before the external MOSFET is fully enhanced, a resistor between the supply's output and sense nodes provides local feedback. When the ON pin voltage is low, the switch will open before the MGATE, SGATE1 and SGATE2 pins will ramp down. Leave unused switch terminal pairs unconnected.

Exposed Pad (Pin 21, UFD Package Only): Exposed pad may be left open or connected to device GND.

$\overline{\text{FAULT}}$ (Pin 9/Pin 7): Negative-Logic Fault Input/Output. Under normal conditions the internal fault latch is not set and an 8.5µA current pulls up $\overline{\text{FAULT}}$ to a diode drop below V_{CC}. When the voltage at $\overline{\text{FAULT}}$ is pulled below 0.5V, a fault condition is latched and an internal N-channel MOSFET pulls $\overline{\text{FAULT}}$ to GND until the latch is reset. The fault condition also pulls STATUS/PGI low, opens the remote sense switches, and pulls MGATE, SGATE1 and SGATE2 to GND to disconnect the master and slave supplies from their loads. Pulling STATUS/PGI below 1V after the power good time-out delay also latches a fault. The fault latch is reset when the ON pin voltage is below 0.5V, or when V_{CC} is undervoltage. The fault latch is armed when the ON pin voltage exceeds 0.6V. To auto-retry after a fault, connect $\overline{\text{FAULT}}$ to the ON pin. Leave the $\overline{\text{FAULT}}$ pin unconnected if it is unused.

FB1, FB2 (Pins 3, 18/Pins 1, 16): Feedback Control Input/Outputs. Each FB pin connects to the feedback node of a slave supply. Connect an FB pin to the tap point of a resistive voltage divider between the source (load side) of the external MOSFET and GND. For a slave supply with an accessible feedback path, no external MOSFET may be necessary. In that case, connect an FB pin to the tap point of a resistive voltage divider between the supply generator's feedback node and GND. To prevent damage to the slave supply, the FB pins will not force the slave's feedback node above 2.4V. In addition, it will not actively sink current even when the LTC2926 is not powered. Tie unused FB pins to GND.

GND (Pin 10/Pin 8): Device Ground.

MGATE (Pin 12/Pin 10): Master Gate Drive for External N-Channel MOSFET/Master Ramp. When the ON pin is high, an internal 10µA current charges the gate of an external N-channel MOSFET. A capacitor from MGATE to GND sets the master ramp rate. Add a 10Ω resistor between the capacitor and the MOSFET's gate to prevent high frequency oscillations. An internal charge pump guarantees that the MGATE pin voltage will pull up to 5.5V above V_{CC}, which ensures that logic-level N-channel MOSFETs are fully enhanced. When the ON pin is pulled low, the MGATE pin is pulled to GND by a 10µA current source. Upon a fault condition, the MGATE pin is pulled low immediately with 20mA. To create a master ramp signal without an external MOSFET, tie the MGATE pin to the RAMP pin. A weak internal clamp on the RAMP pin limits MGATE to V_{CC} + 1V in this case. Leave the MGATE pin unconnected if it is unused.

ON (Pin 7/Pin 5): On Control Input. The ON pin has a threshold of 1.23V with 75mV of hysteresis. A high causes 10µA to flow out of the MGATE pin, ramping up the supplies. A low causes 10µA to flow into the MGATE pin, ramping down the supplies. Pull the ON pin below 0.5V to reset the fault latch. Pull the ON pin above 0.6V after a fault latch reset to arm the fault latch.

PGTMR (Pin 8/Pin 6): Power Good Timer. Connect an external capacitor between PGTMR and GND to set the Power Good Time-Out Delay. When the ON pin is above 1.23V, a 10µA current pulls up PGTMR to V_{CC}, otherwise an internal N-channel MOSFET pulls PGTMR to GND. If the voltage on PGTMR exceeds 1.23V and the voltage on STATUS/PGI is not above 1.23V, a fault condition is latched, the remote sense switches are opened, and $\overline{\text{FAULT}}$, STATUS/PGI, MGATE, SGATE1, SGATE2 and RSGATE will be immediately pulled to GND. To disable the Power Good Timer tie PGTMR to GND.

PIN FUNCTIONS GN/UFD Packages

RAMP (Pin 11/ Pin 9): Ramp Buffer Input. Connect the RAMP pin to the master ramp signal to force the slave supplies to track it. When the RAMP pin is connected to the source of an external N-channel MOSFET, the slave supplies track the MOSFET's source, the master supply voltage, as it ramps up and down. When a master supply is not required, the RAMP pin can be tied directly to the MGATE pin to form a master ramp voltage. In this configuration, the supplies track the capacitor on the MGATE pin as it is charged and discharged by the 10µA current source that is controlled by the ON pin. The RAMP pin is weakly clamped to V_{CC} + 1V. Do not drive RAMP above V_{CC} with a low impedance source to avoid sinking large currents into the pin. Ground the RAMP pin if it is unused.

RAMPBUF (Pin 20/Pin 18): Ramp Buffer Output. The RAMPBUF pin provides a low impedance buffered version of the signal on the RAMP pin. This buffered output drives the resistive voltage dividers that connect to the TRACK pins. Limit the capacitance at the RAMPBUF pin to less than 100pF.

RSGATE (Pin 13/Pin 11): Gate Drive for Internal and External N-Channel MOSFET Remote Sense Switches. A remote sense path between a load and the sense input of its supply generator automatically compensates for voltage drops across the tracking MOSFET. After the series MOSFETs are fully enhanced, a 10µA current pulls up RSGATE. An internal charge pump guarantees that RSGATE will pull up to 5.5V above V_{CC}, which ensures that logic-level N-channel MOSFETs are fully enhanced. When the voltage at RSGATE exceeds V_{CC} + 4.9V, the STATUS/PGI pull-down is released. When the ON pin is low, a 10µA current source pulls RSGATE to GND. Supplies will not track down until the RSGATE pin voltage falls below 1.23V, which ensures that the remote sense switches open before the loads are disconnected. Connect RSGATE to the gates of additional external N-channel MOSFETs to create more remote sense switches. Upon a fault condition, the RSGATE pin is pulled low immediately with 20mA. Optionally connect a capacitor between RSGATE and GND to set the switch-on rate or to add delay between switch closure and STATUS/PGI assertion. Leave RSGATE unconnected if it is unused.

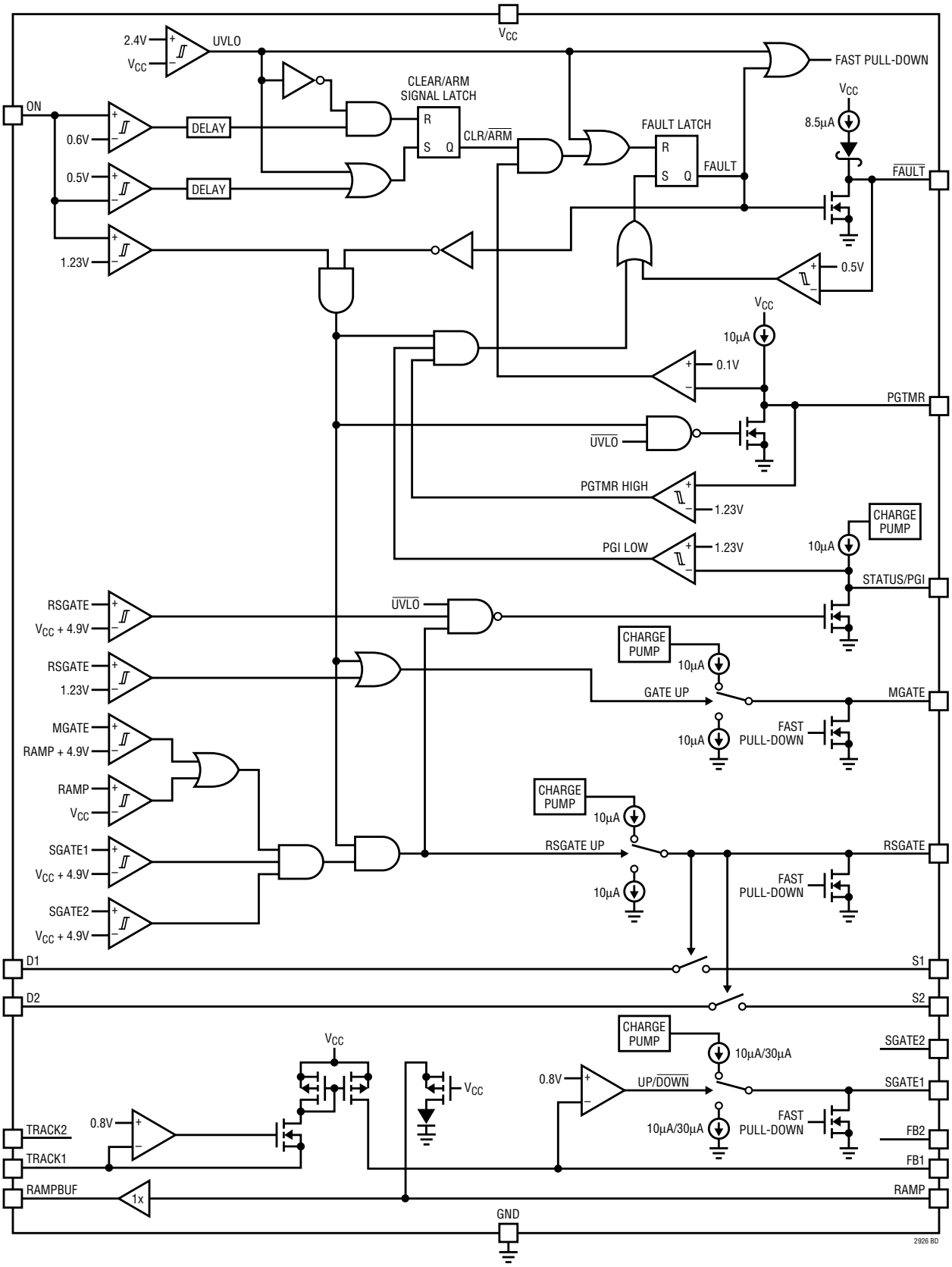
SGATE1, SGATE2 (Pins 5, 16/Pins 3, 14): Slave Gate Controllers for External N-Channel MOSFETs. Each SGATE pin ramps a slave supply by controlling the gate of an external N-channel MOSFET so that its source terminal follows the tracking profile set by external resistors and the master ramp. It is a good practice to add a 10Ω resistor between this pin and the MOSFET's gate to prevent high frequency oscillations. An internal charge pump guarantees that the SGATE pin voltage will pull up to 5.5V above V_{CC}, which ensures that logic-level N-channel MOSFETs are fully enhanced. Leave unused SGATE pins unconnected.

STATUS/PGI (Pin 14/Pin 12): Status Output/Power Good Input. A 10µA current pulls up STATUS/PGI when MGATE, SGATE1 and SGATE2 are fully enhanced, and the remote sense switches are closed, otherwise an internal N-channel MOSFET pulls down STATUS/PGI. If the STATUS/PGI pin is pulled below 1V after the power-good time-out delay (see PGTMR pin description), the fault latch is set, and MGATE, SGATE1, SGATE2 and RSGATE are all pulled low immediately. An internal charge pump guarantees that the STATUS/PGI pin voltage will pull up to 5.5V above V_{CC}. An external pull-up resistor may be added to limit the STATUS/PGI voltage to logic levels. Leave the STATUS/PGI pin unconnected if it is unused.

TRACK1, TRACK2 (Pins 2, 19/Pins 20, 17): Tracking Control Inputs. A resistive voltage divider between RAMPBUF and each TRACK pin determines the tracking profile of each supply channel. Each TRACK pin pulls up to 0.8V, and the current supplied at TRACK is mirrored at FB. The TRACK pins are capable of supplying at least 1mA when V_{CC} = 2.9V. They may be capable of supplying up to 10mA when the supply is at 5.5V, so care should be taken not to short this pin for extended periods. Limit the capacitance at the TRACK pins to less than 25pF. Leave unused TRACK pins unconnected.

V_{CC} (Pin 1/Pin 19): Positive Voltage Supply. Operating range is from 2.9V to 5.5V. An undervoltage lockout resets the part when the supply is below 2.4V. V_{CC} should be bypassed to GND with a 0.1µF capacitor.

FUNCTIONAL BLOCK DIAGRAM



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Power Supply Tracking and Sequencing

The LTC2926 handles a variety of power-up profiles to satisfy the requirements of digital logic circuits including FPGAs, PLDs, DSPs and microprocessors. These requirements fall into one of the four general categories illustrated in Figures 1 to 4.

Some applications require that the potential difference between two power supplies must never exceed a specified voltage. This requirement applies during power-up and power-down as well as during steady-state operation, often to prevent destructive latch-up in a dual supply IC. Typically, this is achieved by ramping the supplies up and down together (Figure 1). In other applications it is desirable to have the supplies ramp up and down ratiometrically (Figure 2) or with fixed voltage offsets between them (Figure 3).

Certain applications require one supply to come up after another. For example, a system clock may need to start before a block of logic. In this case, the supplies are sequenced as in Figure 4, where the 1.8V supply ramps up completely followed by the 2.5V supply.

Operation

The LTC2926 provides a simple solution to allow all of the power supply tracking and sequencing profiles shown in Figures 1 to 4. A single LTC2926 controls up to three supplies: two "slave" supplies that track a "master" signal. With just four resistors and an external N-channel MOSFET, each slave supply is configured to ramp up and down as a function of the master signal. This master signal can be a third supply that is ramped up through an external MOSFET, whose ramp rate is set with a single capacitor, or it can be a signal generated by tying the MGATE and RAMP pins together to an external capacitor.

Tracking Cell and Gate Controller Cell

The LTC2926's operation is based on the combination of a tracking cell and a gate controller cell that is shown in Figure 5. The tracking cell servos the TRACK pin at 0.8V, and the current supplied by the TRACK pin is mirrored at the FB pin. The gate controller cell servos the FB pin at 0.8V by driving the gate of the external N-channel MOSFET (Q_{EXT}), and establishes the slave output voltage at the source of the MOSFET based on the TRACK pin current and resistors

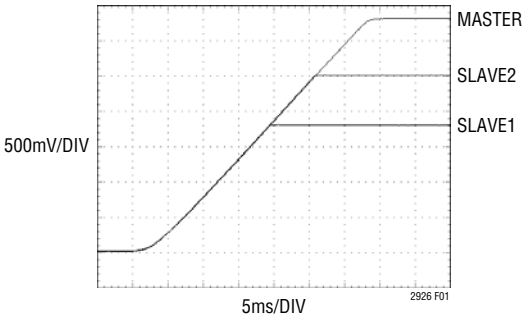

Figure 1. Coincident Tracking

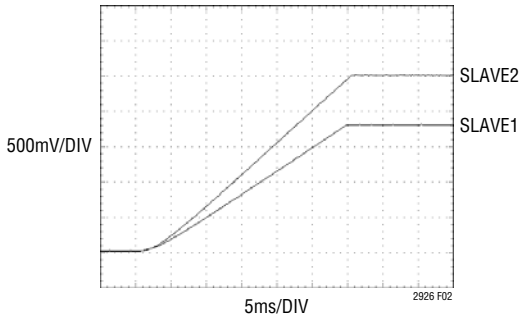

Figure 2. Ratiometric Tracking

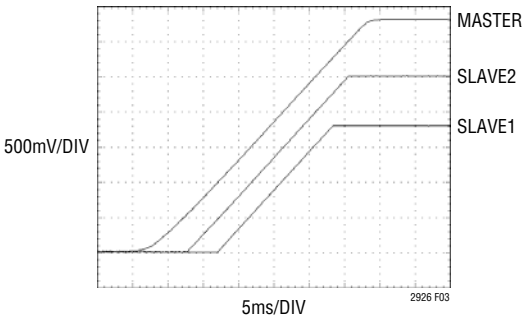

Figure 3. Offset Tracking

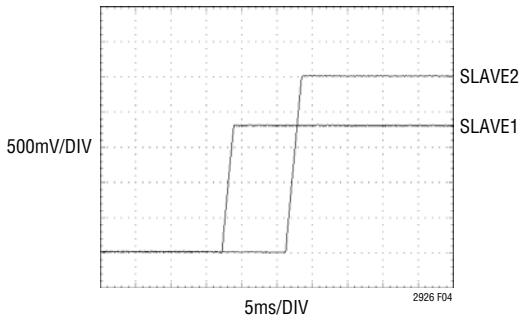

Figure 4. Supply Sequencing

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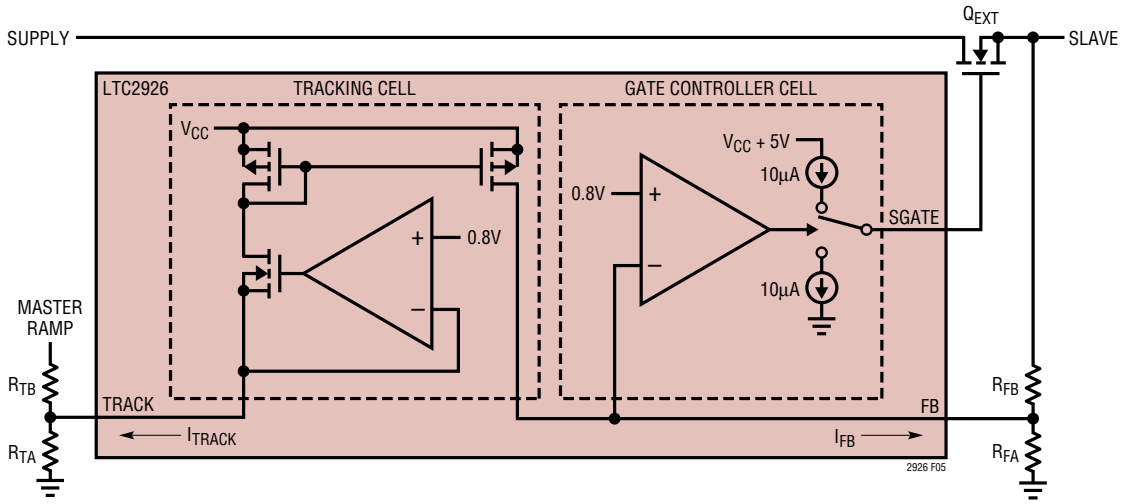

Figure 5. Simplified Tracking Cell and Gate Controller Cell Combination

R_{FA} and R_{FB}. The slave output voltage varies as a function of the master signal with terms set by R_{TA} and R_{TB}. By selecting appropriate values of R_{TA} and R_{TB}, it is possible to generate any of the profiles in Figures 1 to 4.

Controlling the Ramp-Up and Ramp-Down Behavior

The operation of the LTC2926 is most easily understood by referring to the simplified functional diagram in Figure 6. When the ON pin is low, the remote sense switch is opened and the MGATE pin is pulled to ground causing the master signal to remain low. Since the current through R_{TB1} is at its maximum when the master signal is low, the current sourced by FB1 is also at its maximum. The current forces the FB1 pin voltage above 0.8V, which pulls the SGATE1 pin low and disconnects the slave's supply generator. The minimum voltage across the slave load is a function of the maximum FB1 current, the feedback divider resistors, and the load resistance (see Load Requirements).

When the ON pin rises above 1.23V, the master signal ramps up, and the slave supply tracks the master signal. The master ramp rate is set by an external capacitor driven by a 10µA current source from an internal charge pump. If no external MOSFET is used for the master signal, the ramp rate is set by tying the MGATE and RAMP pins together at one terminal of the external capacitor (see Ratiometric Tracking Example or Supply Sequencing Example). The MGATE pin voltage will be limited to V_{CC} + 1V (max) by the weak internal clamp on the RAMP pin.

The rising master signal decreases the tracking current mirrored out of the FB1 pin. The gate controller circuitry maintains 0.8V at FB1 by driving the SGATE1 voltage and, via the external MOSFET source-follower, the slave supply output. When the slave supply output reaches the slave supply module voltage, the FB1 pin will fall below 0.8V and the gate controller will drive the SGATE1 pin above V_{CC} to fully enhance the MOSFET.

After the MGATE, SGATE1 and SGATE2 pins reach their maximum voltages, the RSGATE pin is pulled up by a 10µA current source from an internal charge pump, which closes the integrated remote sense switches. The integrated remote sense switch allows the slave supply generator to compensate for voltage drop across the slave's MOSFET (Q1).

When the ON pin falls below $V_{ON(TH)} – \Delta V_{ON(TH)}$, typically 1.16V, the remote sense switch opens and the MGATE pin pulls down with 10µA. The master signal and the slave supplies will fall at the same rate as they rose previously, following the tracking or sequencing profile in reverse.

The ON pin can be controlled by a digital I/O pin or it can be used to monitor an input supply. By connecting a resistive voltage divider from an input supply to the ON pin, the supplies will ramp up only after the monitored supply reaches a preset voltage.

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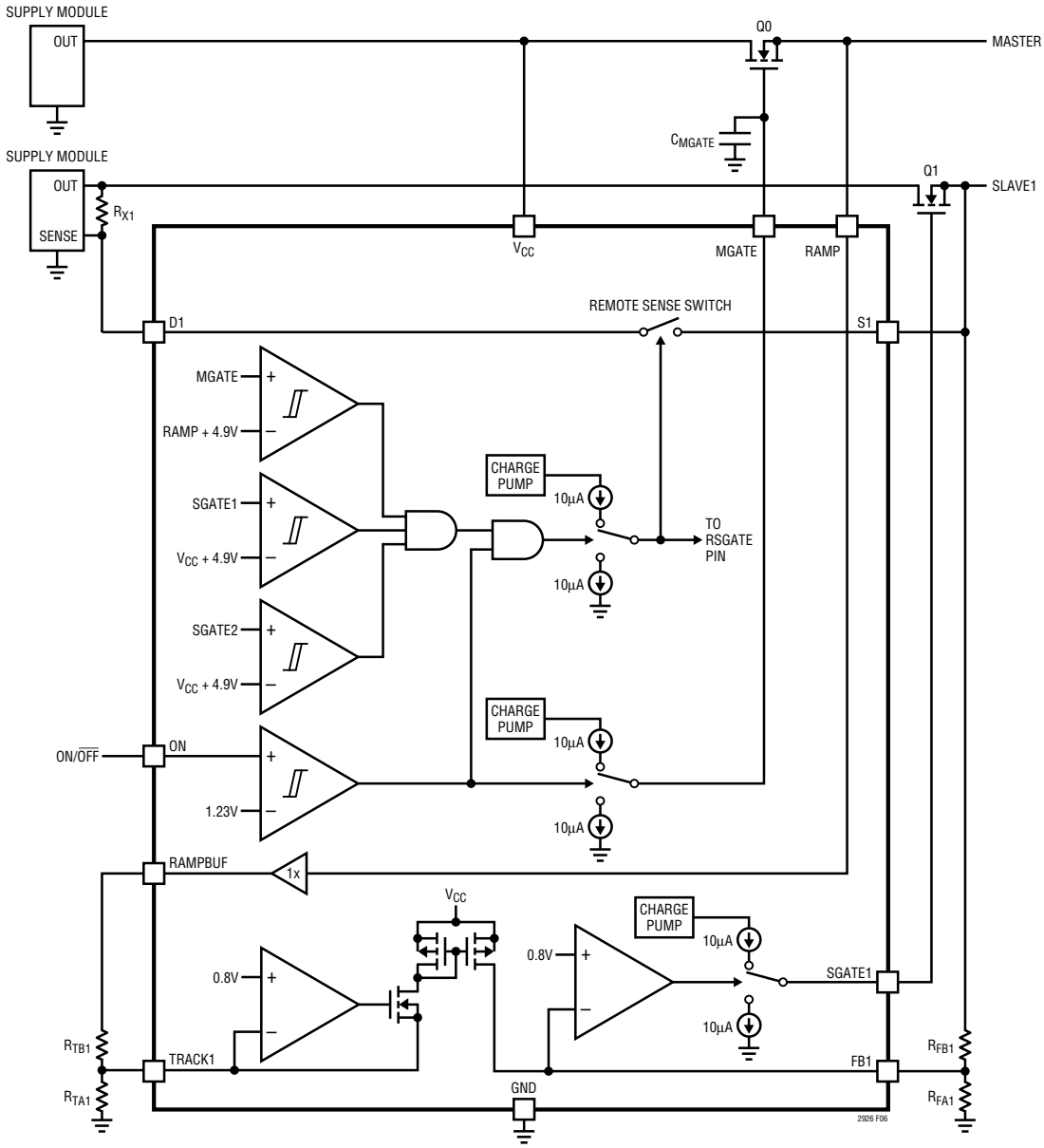

Figure 6. Simplified Functional Block Diagram

Optional Master Supply MOSFET

Figure 7 illustrates how an optional external N-channel MOSFET (device Q0) can ramp up a supply that doubles as the master signal. The MOSFET's gate is tied to the MGATE pin and its source is tied to the RAMP pin. The MGATE pin sources or sinks 10µA to ramp the MOSFET's gate up or down at a rate set by the external capacitor connected to the MGATE pin. The series MOSFET controls any supply with an output voltage between 0V and V_{CC}.

To compensate for voltage drop across the master supply MOSFET, add an optional external remote sense switch (device Q3 in Figure 7) connected between RAMP and the sense input of the master voltage supply module. Tie the gate of the external switch MOSFET to the RSGATE pin for automatic remote sense switching.

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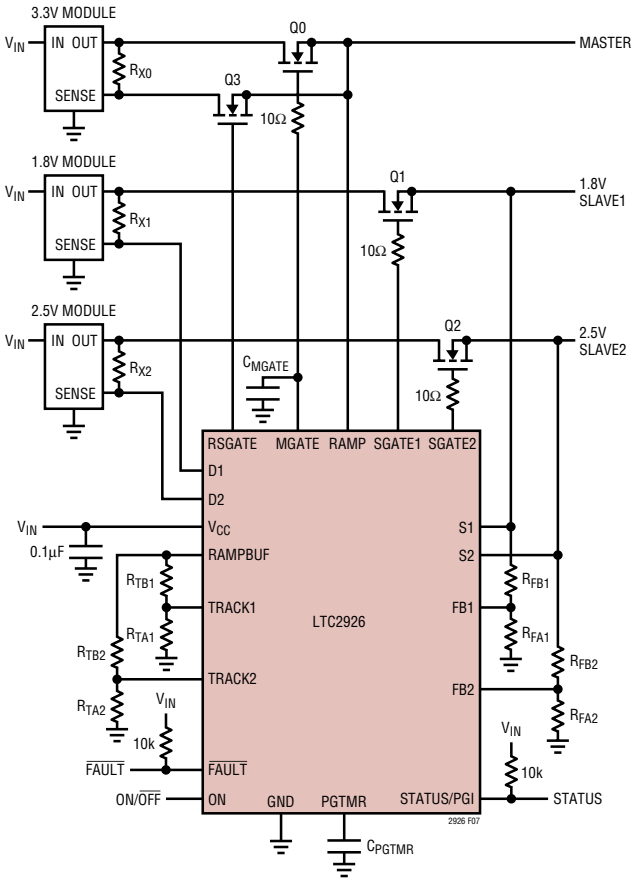

Figure 7. Typical Application with Master Supply

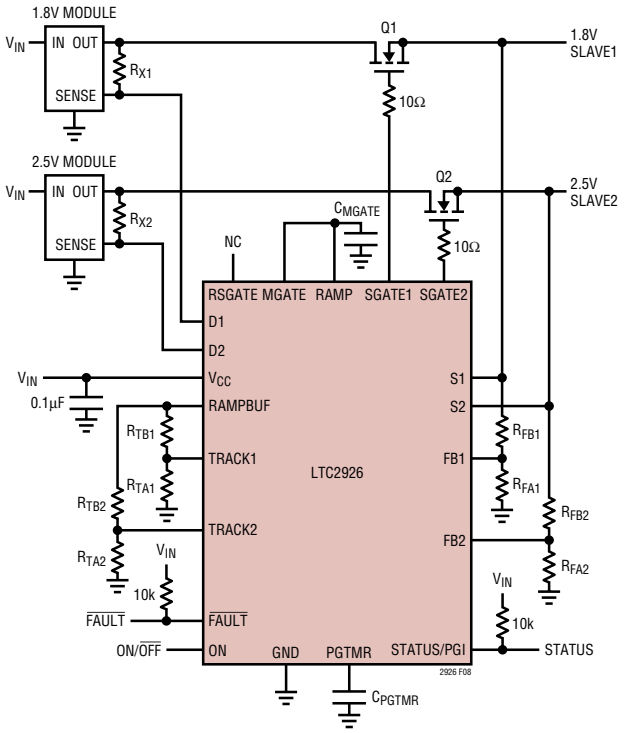

Figure 8. Typical Application Without Master Supply

Ramp Buffer

The RAMPBUF pin provides a buffered version of the RAMP pin voltage that drives the resistive dividers on the TRACK pins. When there is no external MOSFET, it sources or sinks up to 3mA to drive the track resistors even though the MGATE pin only supplies 10µA (Figure 8). The RAMPBUF pin also proves useful in systems with an external MOSFET. If R_{TBn} were directly connected to the MOSFET's source (the master output), the servo mechanism of the tracking cell could potentially drive the master output towards 0.8V when the MOSFET is off. The ramp buffer prevents this by eliminating that path for current.

Fault Input/Output

The $\overline{FAULT}$ pin allows external upstream monitoring circuits to control and to communicate with the LTC2926. The pin is driven internally by an N-channel MOSFET pull-down to GND, and by an 8.5µA pull-up to V_{CC} through a series diode. Under normal conditions, the MOSFET is off and the current pulls the $\overline{FAULT}$ pin voltage high. When an upstream monitor signal pulls $\overline{FAULT}$ below 0.5V, the LTC2926's internal fault latch is set, which immediately opens the remote sense switches and cuts off the master and slave supplies by pulling MGATE, SGATE1 and SGATE2 to GND. A fault also activates the internal MOSFET pull-down on the STATUS/PGI pin, which indicates to external downstream monitoring circuits that the supplies are no longer valid (see Status Output). Until the fault latch is reset, the supplies stay disconnected and an internal pull-down keeps the $\overline{FAULT}$ pin low as a signal to upstream monitors.

Fault latch reset is initiated by bringing the ON pin voltage below 0.5V, and completed when PGTMR is <0.1V. Reducing the V_{CC} pin voltage below $V_{CC(UVLO)} - \Delta V_{CC(UVLO)}$, typically 2.35V, also resets the fault latch. After it is cleared, the fault latch is armed by bringing the ON pin voltage above 0.6V. No faults can be latched until after the latch is armed.

The $\overline{FAULT}$ pin is pulled up by 8.5µA to V_{CC} through a Schottky diode, which allows the pin to be pulled safely above the LTC2926's supply if required. Leave the $\overline{FAULT}$ pin unconnected if it is unused.

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Status Output

The output aspect of the STATUS/PGI pin allows the LTC2926 to control and communicate with external downstream circuits. The pin is driven internally by an N-channel MOSFET pull-down to GND and a 10µA pull-up to an internal charge pump. The pull-down keeps the STATUS/PGI pin low until MGATE, SGATE1 and SGATE2 are fully enhanced, and the remote sense switches are closed. The pull-down then shuts off, and STATUS/PGI pin rises, indicating to downstream monitors that the supplies are fully ramped up. The STATUS/PGI pin pulls low when the MGATE, SGATE1, SGATE2 or RSGATE pin is low, either because a fault has been latched, or because the ON pin is low.

An internal charge pump rail at V_{CC} + 5.5V sources the STATUS/PGI pull-up current. An external resistor may be added to create logic level voltages, or the pin may be used to enhance the gates of external N-channel MOSFET switches, if desired.

Power Good Timeout

The input aspect of the STATUS/PGI pin allows external downstream monitoring circuits to control the LTC2926 as shown in Figure 9. The power good timeout circuit disconnects the supply generators if for any reason the voltage level of the STATUS/PGI pin is not high after the timeout period. During a ramp-up, the timeout circuit will trip if the internal pull-down on STATUS/PGI fails to release, which indicates that supply ramping was not completed in the time allotted. If supply ramping completes, any downstream circuits that pull down the STATUS/PGI pin after the timer duration also will trip the timeout circuit. A fault caused by a power good timeout has the same effect as a fault triggered by the $\overline{FAULT}$ pin: supplies are disconnected and the fault latch is set. The fault latch may be cleared as described in the Fault Input/Output section above.

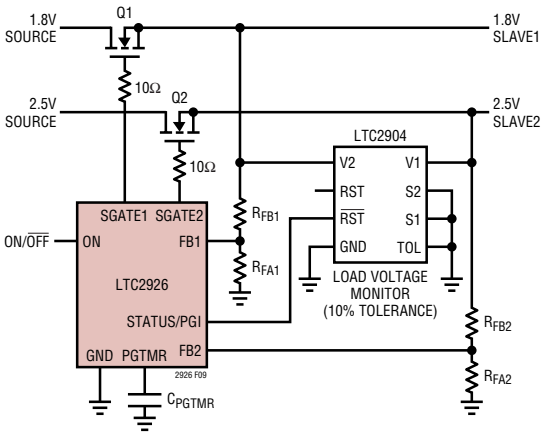

Figure 9. External Load Monitor Controlling LTC2926 via Power Good Input

The power good timer duration is configured by a capacitor tied between PGTMR and GND. The pin's 10µA current source ramps up the capacitor voltage when the ON pin is high, otherwise 4mA pulls PGTMR to GND. The capacitor, C_{PGTMR}, required to configure the power good timeout duration, t_{PGTMR}, is determined from:

$$C_{PGTMR} = \frac{10\mu A \bullet t_{PGTMR}}{1.23V}$$

If the power good timeout feature is not used, tie PGTMR to GND.

Retry on Fault

The LTC2926 continuously attempts to ramp up the supplies after a fault if the $\overline{FAULT}$ pin is tied to the ON pin. When the $\overline{FAULT}$ and ON pins go low together, the internal fault latch is set by the falling $\overline{FAULT}$ pin, and the fault latch is reset by the falling ON pin. A short internal delay of several microseconds guarantees triggering of fast pull-down circuits on the RSGATE, MGATE, SGATE1 and SGATE2 pins, which opens the remote sense switches and disconnects the master and slave supplies before the fault latch is reset. If no external signal pulls down the $\overline{FAULT}$ pin, the internal 8.5µA pull-up current or an external pull-up resistor increases the ON (and $\overline{FAULT}$) pin voltage above 0.6V, which arms the fault latch. A ramp-up begins when ON is above 1.23V.

In applications where the LTC2926 is configured for fault retry, some details of the retry behavior are determined by the source and duration of the fault signal. When a fault is triggered by an external pull-down signal on the $\overline{FAULT}$ (and ON) pin, supply ramping will not restart until the low input ceases. When a power good fault is triggered by an external pull-down signal on the STATUS/PGI pin, supply ramping restarts immediately. If the low signal persists

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through the power good timeout period, a fault and retry will subsequently occur.

To ensure a consistent power good timeout period, the LTC2926 requires the PGTMR pin voltage to fall below 0.1V for the fault latch reset to complete. The ON pin needs to be held low for only 10µs to initiate fault reset; it is allowed to go high while the timing capacitor on PGTMR discharges to 0.1V (see Functional Block Diagram).

When a resistive voltage divider drives the ON and $\overline{FAULT}$ pins together, include the contribution of $I_{\overline{FAULT}(UP)}$ when choosing the resistor values (Figure 10a). When a logic output drives both pins, up to 30kΩ of series resistance may be added to limit the output current while the fault pull-down is active (Figure 10b).

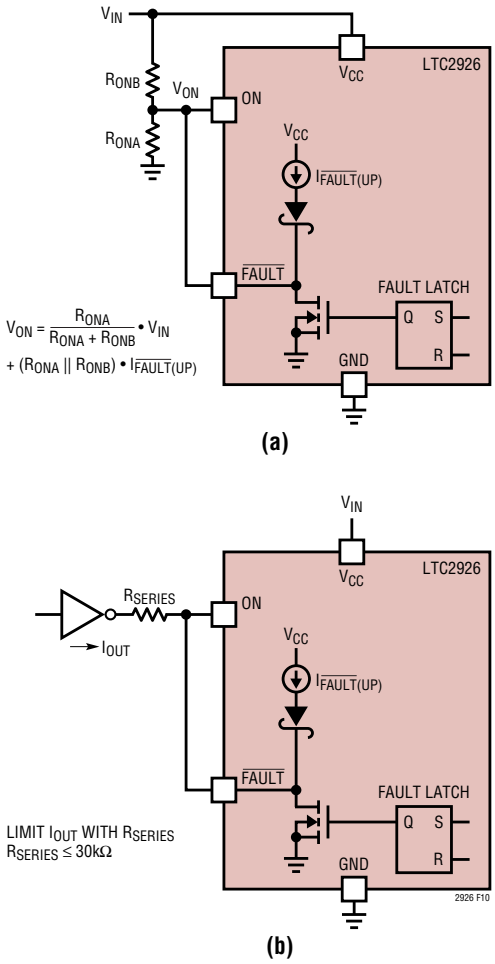

Figure 10. Fault Retry Configurations, (a) Resistive Voltage Divider and (b) Logic Driven

Automatic Remote Sense Switching

The LTC2926 provides integrated remote sense switches that solve the problem of voltage drops in the external series MOSFETs that control supply ramping. A switch creates a feedback path from a slave supply output to the slave supply generator sense input that allows the generator to compensate for the I • R drop across the controlling MOSFET (see, for example, Figure 6). After the supply ramping is complete, but before the internal pull-down releases the STATUS/PGI pin, the two integrated remote sense switches are closed.

For applications that require more than two remote sense switches, connect the RSGATE pin to the gates of additional external N-channel MOSFETs. An internal charge pump guarantees that RSGATE will reach V_{CC} + 5.5V, which allows full enhancement of logic-level MOSFETs with source or drain voltages up to V_{CC}.

The switches are open when supply ramping has not completed to avoid creating a power path between the supply generator and the load. When the remote sense switches are open, the supply generator's sense input must be connected locally to its output through a resistor that is much larger than the remote sense switch resistance of 10Ω (max); a 100Ω resistor is adequate for most applications as in Figure 7.

Some supply modules have built-in resistors of 10Ω or less between their out and sense pins, which may require a lower switch resistance. Choose an external N-channel MOSFET with an $R_{DS(on)}$ that is at most 1/10 the module out-to-sense resistance, but that is still much larger than the $R_{DS(on)}$ of the power path MOSFET.

If neither external remote sense switches nor a status activation delay is required, leave the RSGATE pin unconnected.

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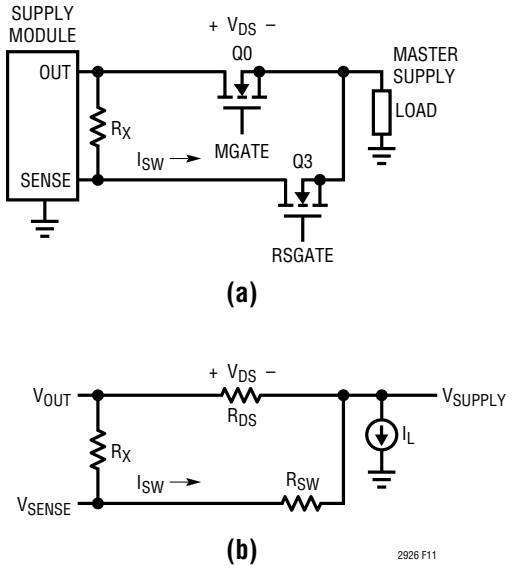

Figure 11. Supply and Sense Path Detail, (a) Functional Diagram and (b) Equivalent Circuit When Remote Sense Switch Is Closed

Considerations when Using Remote Sense Switches

Consider the supply and sense path detail functional diagram and equivalent circuit in Figure 11. For proper compensation of the I • R drop across the external control MOSFET Q0 by the supply module, the voltage at its sense pin input must be equal to the supply voltage at the load. Solving for V_{SENSE} in the equivalent circuit yields:

$$V_{SENSE} = \left(\frac{R_X}{R_X + R_{SW}}\right) \bullet V_{SUPPLY} + \left(\frac{R_{SW}}{R_X + R_{SW}}\right) \bullet V_{OUT}$$

For the best compensation, i.e., $V_{SENSE} \approx V_{SUPPLY}$, choose $R_X >> R_{SW}$.

The remote sense switch is intended to be a low-current voltage feedback path. The control MOSFET (Q0 in Figure 11a) should carry all but a tiny fraction of the entire load current. The remote sense switch current is:

$$I_{SW} = I_{LOAD} \bullet \left(\frac{R_{DS}}{R_X + R_{SW} + R_{DS}}\right)$$

To minimize switch current, choose $R_X >> R_{DS}$. In applications that use the LTC2926's integrated remote sense switches, I_{SW} must not exceed the Absolute Maximum Ratings for switch pin currents.

It is recommended design practice to satisfy both resistance value conditions.

SGATE Voltage at Ramp Start/End

When the master ramp is 0V (before ramp up or after ramp down), the control MOSFET ideally conducts no current. If the tracking profile has no delay or offset, the gate control loops may force the SGATE pins either to ground or to just below the MOSFET threshold voltage, depending on reference offsets, resistor mismatches and the load resistance. In both cases the slave load will be at about 0V, but if a known state of SGATE is desired, include an offset in the tracking profile.

To guarantee grounding of the SGATE pins at RAMP = 0V, include a positive offset, V_{OS}, based on the maximum slave supply voltage, $V_{SLAVE}(max)$, and the tracking/feedback resistor tolerance. Note that at the start of ramp up, the gate capacitance of the MOSFET must be charged to the threshold voltage before the source begins ramping. The SGATE pins do provide extra current to speed the initial charging.

Calculate the required V_{OS} from:

$$V_{OS} \geq k \bullet V_{SLAVE}(max)$$

For 1% resistors k = 1/8, for 5% resistors k = 1/4, for 10% resistors k = 2/5.

To guarantee the SGATE pins sit at the MOSFET threshold voltages at RAMP = 0V, include a negative offset. Note that when the master ramp goes to 0V, the slave supplies will remain above ground by the magnitude of the offset.

Calculate the required V_{OS} from:

$$V_{OS} \leq -k \bullet V_{SLAVE}(max)$$

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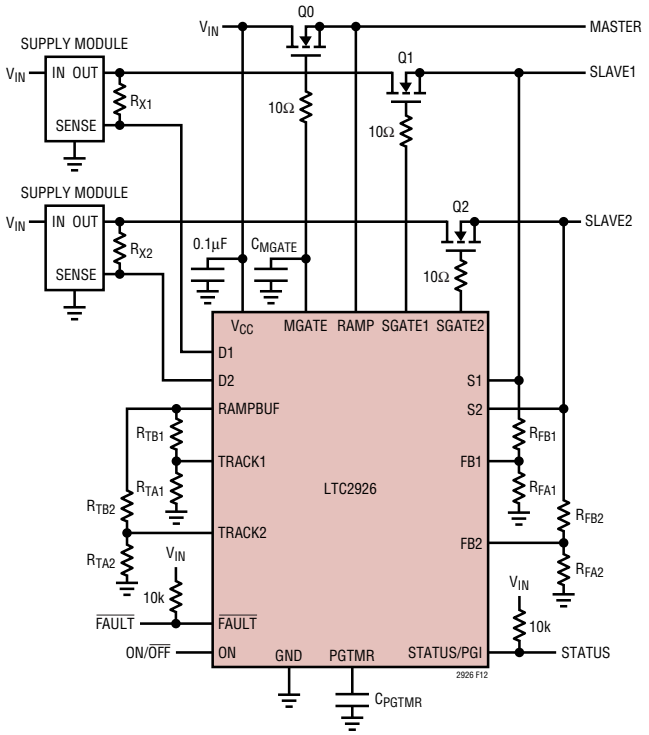

Figure 12. Three-Supply Application

Three-Step Design Procedure

The following three-step design procedure allows one to choose the FBn resistors, R_{FAn} and R_{FBn}, the TRACKn resistors, R_{TAn} and R_{TBn}, and the master ramp capacitor, C_{MGATE}, that give any of the tracking or sequencing profiles shown in Figures 1 to 4. A three-supply application circuit is shown in Figure 12.

1. Set the ramp rate of the master signal.

Solve for the value of C_{MGATE}, the capacitor on the MGATE pin, based on the desired ramp rate (volts per second) of the master ramp signal, S_M, and the MGATE pull-up current I_{MGATE}, which is nominally 10µA.

$$C_{MGATE} = \frac{I_{MGATE}}{S_M} \quad (1)$$

If the master ramp signal is a master supply, consider the gate capacitance of the required external N-channel MOSFET. If the gate capacitance is comparable to C_{MGATE}, reduce the external capacitor's value to compensate for the gate capacitance of the MOSFET.

If the master ramp signal is not a master supply, tie the RAMP pin to the MGATE pin.

2. Choose the feedback resistors based on the slave supply voltage and slave load.

It is important that the feedback resistors are significantly larger than the load resistance, especially as the slave voltage nears ground (see Load Requirements).

First determine the effective slave load resistance, R_L (not shown), at low slave voltage levels, and select the value of the top feedback resistor, R_{FB}, to satisfy:

$$R_{FB} \geq 100 \bullet R_L \text{ (recommended)},$$
$$R_{FB} \geq 23 \bullet R_L \text{ (required)} \quad (2)$$

Second, determine a value for the lower feedback resistor, R_{FA}, that will ensure that the LTC2926 fully enhances the gate of the slave control MOSFET at the end of ramping. Select R_{FA} based on R_{FB}, the resistor tolerance, TOL_R, and the maximum slave supply voltage, $V_{SLAVE}(max)$:

$$R_{FA} < R_{FB} \bullet \left(\frac{1-TOL_R}{1+TOL_R}\right) \Big/ \left(\frac{V_{SLAVE}(max)}{0.784V} - 1\right) \quad (3)$$

Note: Choose the value of $V_{SLAVE}(max)$ to cover all slave supply voltage tolerances by a good margin. Exceeding the $V_{SLAVE}(max)$ voltage used for this calculation can result in triggering a Power Good Fault unintentionally.

If the slave generator has an accessible resistive divider and a ground-based voltage reference, it may be able to be controlled without a series MOSFET. In that case, let the generator's design set R_{FA} and R_{FB}, substitute the generator's reference voltage for $V_{FB(REF)}$ in step 3, and see the subsection Slave Control Without MOSFETs.

3. Solve for the tracking resistors that set the desired ramp rate and voltage offset or time delay of the slave supply.

Choose a ramp rate for the slave supply, S_S. If the slave supply tracks coincidently with the master supply or with only a fixed offset or delay, then the slave ramp rate equals the master ramp rate. Be sure that the slave ramp rate and its offset or delay allows the slave voltage to finish ramping

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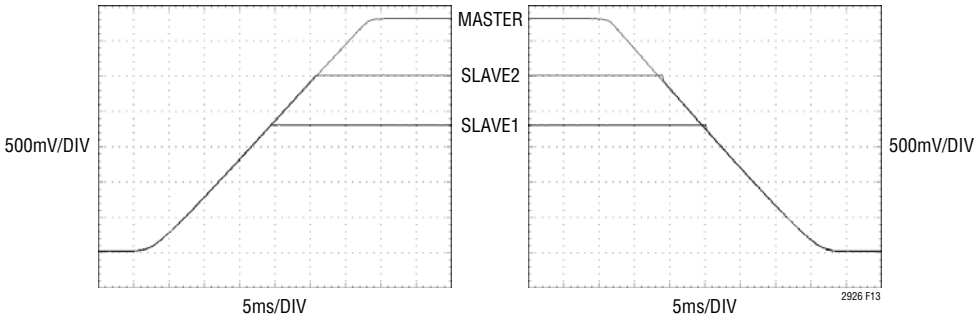


Figure 13. Coincident Tracking Waveforms from Figure 14 Circuit

before the master ramp reaches its final value; otherwise, the slave supply voltage will be held below its intended level. Calculate the upper track resistor, R_{TB}, from:

$$R_{TB} = R_{FB} \bullet \left(\frac{S_M}{S_S} \right) \quad (4)$$

Choose a voltage difference between the master and slave ramps, ΔV, if offset tracking is desired. If a time delay is desired for supply sequencing, calculate an effective voltage difference based on the master ramp rate. If neither voltage offset nor time delay is required, set ΔV = 0V.

ΔV = a voltage difference (offset tracking), or (5a)

$\Delta V = S_M \bullet t_{DLY}$ (supply sequencing), or (5b)

ΔV = 0V (coincident/ratiometric tracking) (5c)

Use the following formula to determine the lower track resistors, R_{TA}, using the TRACK pin voltage, V_{TRACK}, and the FB pin internal reference voltage, $V_{FB(REF)}$, both from the Electrical Characteristics:

$$R_{TA} = \frac{V_{TRACK}}{\frac{V_{FB(REF)}}{R_{FB}} + \frac{V_{FB(REF)}}{R_{FA}} - \frac{V_{TRACK}}{R_{TB}} + \frac{\Delta V}{R_{TB}}} \quad (6)$$

Note that large ratios of slave ramp rate to master ramp rate, S_S/S_M, may result in negative values for R_{TA}. In such cases increase the offset or delay, or reduce the slave ramp rate to realize positive values of R_{TA}.

Coincident Tracking Example

A typical three-supply application is shown in Figure 14. The master signal is 3.3V, the slave 1 supply is a 1.8V module, and the slave 2 supply is a 2.5V module. Allow for ±10% tolerance of the slave supply voltages. Both slave supplies track coincidently with the 3.3V master supply that is controlled by an external MOSFET. The ramp rate of the supplies is 100V/s. The slave supplies' minimum load resistances are 150Ω. The external configuration resistors

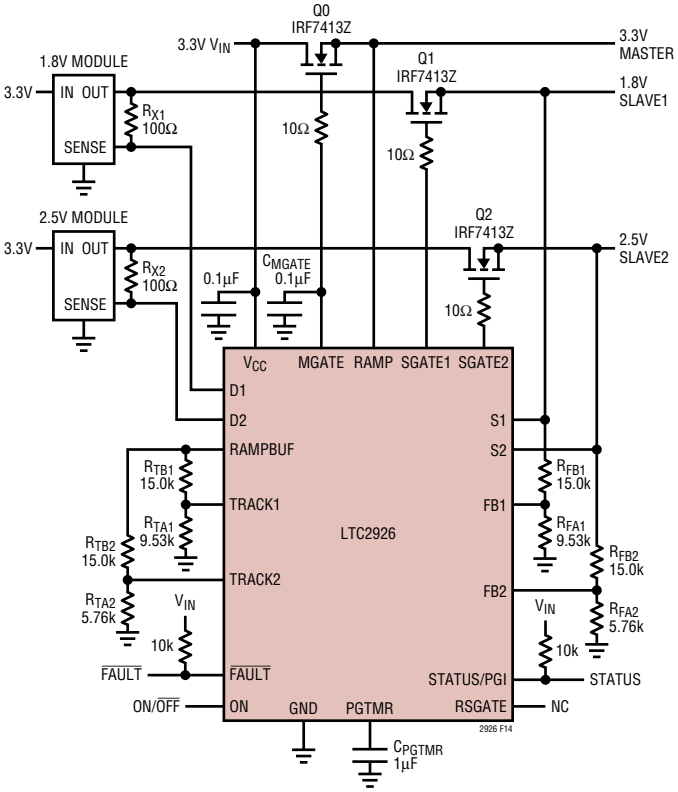


Figure 14. Coincident Tracking Example

APPLICATIONS INFORMATION

have 1% tolerance. The 3-step design procedure detailed above can be used to determine component values. Only the slave 1 supply is considered here, as the procedure is the same for the slave 2 supply.

1. *Set the ramp rate of the master signal.*

From Equation 1:

$$C_{MGATE} = \frac{10\mu A}{100\,V/s} = 0.1\mu F$$

2. *Choose the feedback resistors based on the slave supply voltage and slave load.*

$R_L = 150\Omega$

From Equation 2:

$R_{FB} \geq 100 \bullet 150\Omega = 15k\Omega$

Choose $R_{FB} = 15.0k\Omega$.

From Equation 3:

$$R_{FA} < 15.0k\Omega \bullet \left(\frac{0.99}{1.01}\right) \Big/ \left(\frac{1.98V}{0.784V} - 1\right) = 9.64k\Omega$$

Choose $R_{FA} = 9.53k\Omega$.

3. *Solve for the tracking resistors that set the desired ramp rate and voltage offset or time delay of the slave supply.*

From Equation 4:

$$R_{TB} = 15.0k\Omega \bullet \left(\frac{100\,V/s}{100\,V/s}\right) = 15.0k\Omega$$

Since no offset or delay is required, Equation 5c applies:

$\Delta V = 0V$

From Equation 6:

$$R_{TA} = \frac{0.8V}{\frac{0.8V}{15.0k\Omega} + \frac{0.8V}{9.53k\Omega} - \frac{0.8V}{15.0k\Omega} + \frac{0V}{15.0k\Omega}} = 9.53k\Omega$$

In this example, all supplies remain low while the ON pin is held below 1.23V. When the ON pin rises above 1.23V, 10µA pulls up C_{MGATE} and the gate of MOSFET Q0 at 100V/s. The source of Q0 follows the gate and pulls up the output to 3.3V at the rate of 100V/s. This output serves as the master ramp and is buffered from the RAMP pin to the RAMPBUF pin. As the master output and the RAMPBUF pin rise, the current from the TRACK pins is reduced. Consequently, the voltage at the FB pins begins to fall below 0.8V, which causes the SGATE pins to rise. The sources of the slave supply MOSFETs, Q1 and Q2, follow the rising SGATE signals, and the slave supplies track the master supply. When all the supplies have finished ramping, the RSGATE pin voltage rises to close the integrated remote sense switches, which allows the slave supply modules to compensate for voltage drops in the series MOSFETs. If the supplies have ramped within the power good timeout period (about 123ms in this example), the STATUS/PGI pin will rise, indicating completed ramping. When the ON pin is again pulled below 1.23V, the STATUS/PGI pin falls and the RSGATE pin falls, which opens the remote sense switches. Next, 10µA will pull down C_{MGATE} and the gate of MOSFET Q0 at 100V/s. If the loads on the outputs are sufficient, all outputs will track down coincidently at 100V/s.

APPLICATIONS INFORMATION

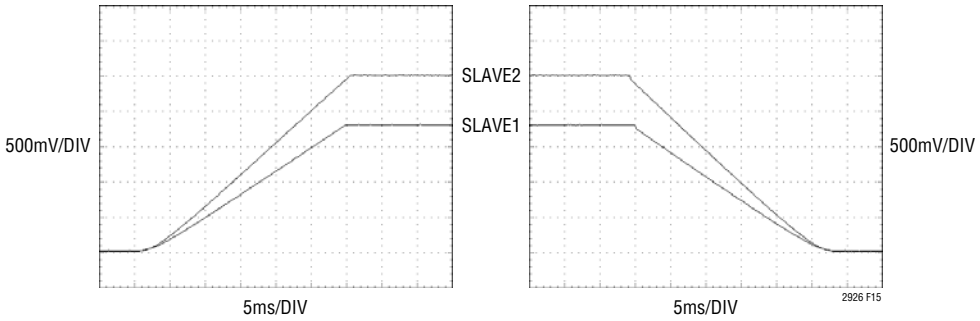


Figure 15. Ratiometric Tracking Waveforms from Figure 16 Circuit

Ratiometric Tracking Example

This example converts the coincident tracking example to the ratiometric tracking profile shown in Figure 15, using two slave supplies and a master ramp signal (not a master ramp supply). The ramp rate of the master signal remains unchanged (Step 1), the minimum load resistance of the slave loads remains unchanged (Step 2), and there is no delay in ratiometric tracking. Only Step 3 of the three-step design procedure needs to be considered. In this example, the ramp rate of the 1.8V slave supply is 60V/s, and the ramp rate of the 2.5V supply is 83.3V/s. Always verify that the chosen ramp rate will allow the supplies to ramp-up completely before RAMPBUF reaches V_{CC}. If the 1.8V slave supply were to ramp up at 50V/s it would only reach 1.65V because the RAMPBUF signal would reach its final value of V_{CC} = 3.3V before the slave supply reached 1.8V.

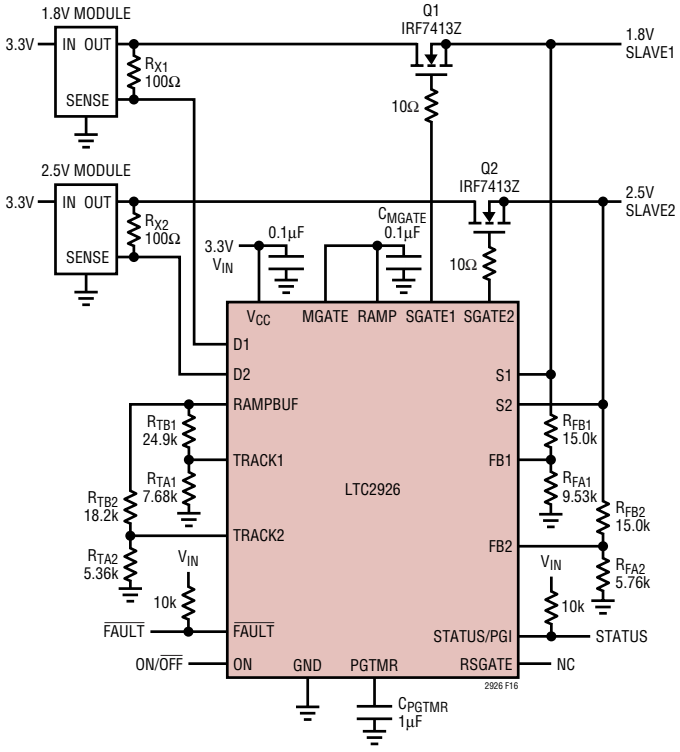


Figure 16. Ratiometric Tracking Example

3. *Solve for the tracking resistors that set the desired ramp rate and voltage offset or time delay of the slave supply.*

From Equation 4:

$$R_{TB} = 15.0k\Omega \bullet \left(\frac{100\,V/s}{60\,V/s} \right) = 25k\Omega$$

Choose R_{TB} = 24.9kΩ.

Since no offset or delay is required, Equation 5c applies:

$\Delta V = 0V$

From Equation 6:

$$R_{TA} = \frac{0.8V}{\frac{0.8V}{15.0k\Omega} + \frac{0.8V}{9.53k\Omega} - \frac{0.8V}{24.9k\Omega} + \frac{0V}{24.9k\Omega}} = 7.61k\Omega$$

Choose R_{TA} = 7.68kΩ.

APPLICATIONS INFORMATION

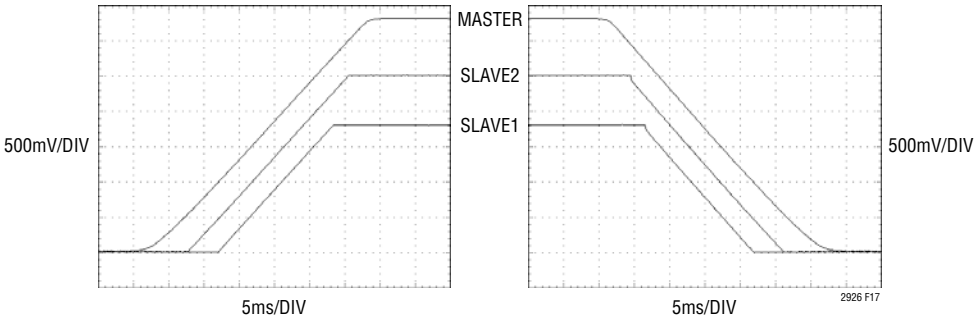


Figure 17. Offset Tracking Waveforms from Figure 18 Circuit

Offset Tracking Example

Converting the circuit in the coincident tracking example to the offset tracking profile shown in Figure 17 is relatively simple. Here the 1.8V slave supply ramps up 1V below the master, and the 2.5V slave supply ramps up 0.5V below the master. The ramp rate remains the same (100V/s), as do the slave supplies' minimum load resistances, so there are no changes necessary to steps 1 or 2 of the three-step design procedure. Only step 3 must be considered. Be sure to verify that the chosen voltage offsets will allow the slave supplies to ramp up completely. In this example, if the voltage offset on the 1.8V supply were 2V, it could ramp up only to 3.3V – 2V = 1.3V.

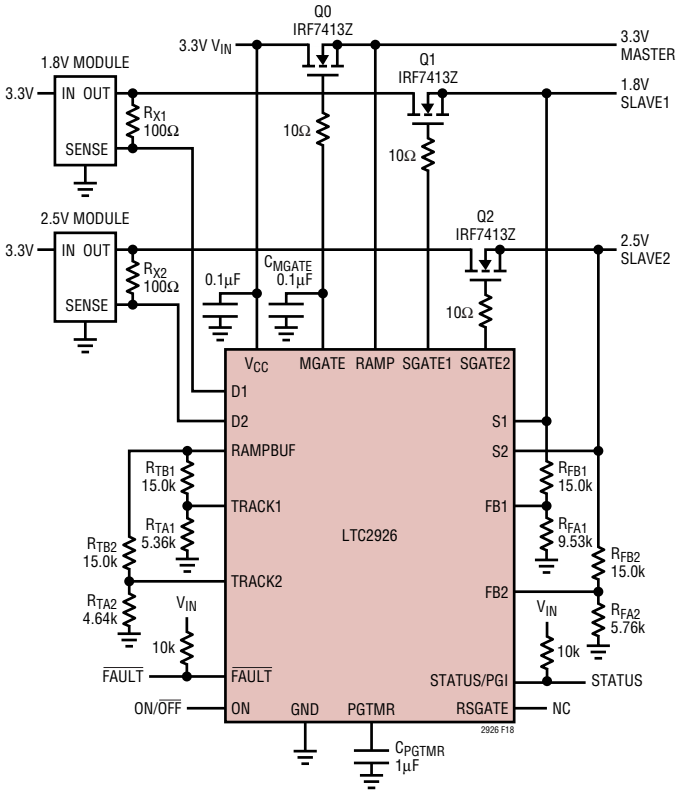


Figure 18. Offset Tracking Example

3. *Solve for the tracking resistors that set the desired ramp rate and voltage offset or time delay of the slave supply.*

From Equation 4:

$$R_{TB} = 15.0k\Omega \bullet \left(\frac{100\,V/s}{100\,V/s}\right) = 15k\Omega$$

Choose R_{TB} = 15.0kΩ.

Since offset is required, Equation 5a applies:

$\Delta V = 1.0V$

From Equation 6:

$$R_{TA} = \frac{0.8V}{\frac{0.8V}{15.0k\Omega} + \frac{0.8V}{9.53k\Omega} - \frac{0.8V}{15.0k\Omega} + \frac{1.0V}{15.0k\Omega}} = 5.31k\Omega$$

Choose R_{TA} = 5.36kΩ.

APPLICATIONS INFORMATION

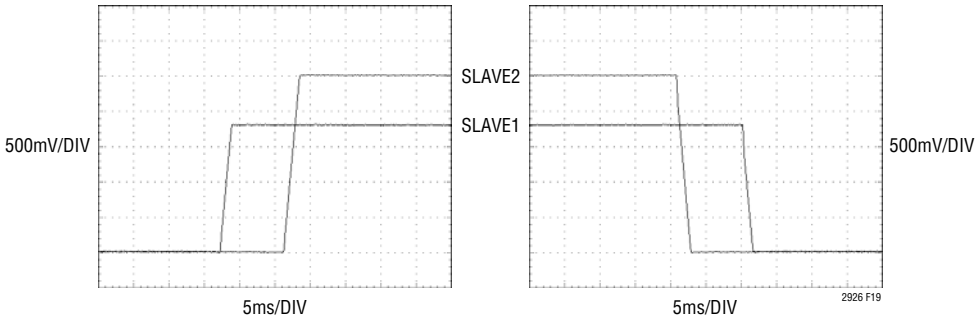


Figure 19. Supply Sequencing Waveforms from Figure 20 Circuit

Supply Sequencing Example

In Figure 19, the two slave supplies are sequenced using a master ramp signal. As in the ratiometric tracking example, the master signal ramps up at 100V/s, and the minimum slave loads are the same as the coincident example, so steps 1 and 2 remain the same. The 1.8V slave 1 supply ramps up at 1000V/s beginning 10ms after the master signal starts to ramp up. The 2.5V slave 2 supply ramps up at 1000V/s beginning 20ms after the master signal starts to ramp up. Note that not every combination of ramp rates and delays is possible. Small delays and large ratios of slave ramp rate to master ramp rate may result in solutions that require negative resistors. In such cases, either the delay must be increased or the ratio of slave ramp rate to master ramp rate must be reduced.

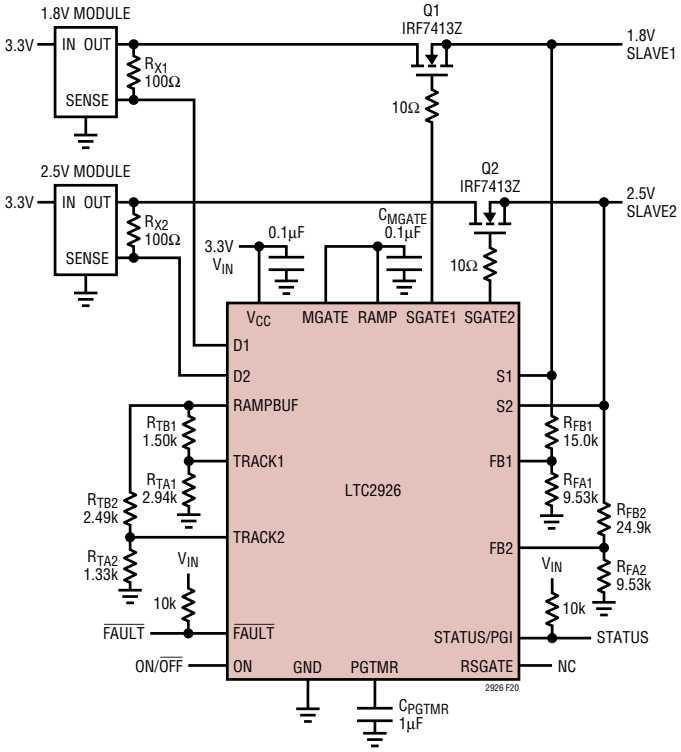


Figure 20. Supply Sequencing Example

3. *Solve for the tracking resistors that set the desired ramp rate and voltage offset or time delay of the slave supply.*

From Equation 4:

$$R_{TB} = 15.0k\Omega \bullet \left(\frac{100\,V/s}{1000\,V/s} \right) = 1.5k\Omega$$

Choose R_{TB} = 1.50kΩ.

Since a delay is required, Equation 5b applies:

$\Delta V = 100V/s \bullet 10ms = 1V$

From Equation 6:

$$R_{TA} = \frac{0.8V}{\frac{0.8V}{15.0k\Omega} + \frac{0.8V}{9.53k\Omega} - \frac{0.8V}{1.50k\Omega} + \frac{1V}{1.50k\Omega}} = 2.96k\Omega$$

Choose R_{TA} = 2.94kΩ.

Note that the values of R_{FA2} and R_{FB2} are larger than those of the Coincident Tracking Example. Larger feedback resistor values resulted in larger tracking resistor values for R_{TA2} and R_{TB2}, which limits the maximum TRACK2 pin current to <1mA; see Final Sanity Checks.

APPLICATIONS INFORMATION

Slave Control Without MOSFETs

The LTC2926 can control tracking and sequencing of a slave supply without a MOSFET if the supply generator's output voltage is set by an accessible resistive voltage divider and if its voltage reference is ground-based. Tracking currents mirrored to the FB pins are injected into the feedback nodes of the supply generators to control the output voltage. When master ramp signal has reached it maximum voltage, the FB pin current is zero, and the LTC2926 has no effect on the output voltage accuracy, transient response or stability of the generator.

To control a supply generator (e.g., DC/DC converter) with a feedback reference voltage $V_{FB(GEN)}$ of 0.75V or less, connect the FB pin of the LTC2926 to the tap point of the generator's resistive divider, as shown in Figure 21a. Follow steps 1 and 3 of the Three-Step Design Procedure to set the ramp rates and tracking profile. Use the feedback resistor values required by the supply generator for R_{FA} and R_{FB} in step 3.

A generator with $V_{FB(GEN)}$>0.75V may be controlled without a MOSFET if the slave voltage is large enough (see Figure 22). First follow steps 1 and 3 of the Three-Step Design Procedure to set the ramp rates and tracking profile. Use the feedback resistor values required by the supply generator in step 3. Next, split resistor R_{FA} as in Figure 21b, so that

$$R_{FAA} \le R_{FA} \bullet \frac{0.75V}{V_{FB(GEN)}} \text{ and}$$

$$R_{FAB} = R_{FA} - R_{FAA}$$

and tie the LTC2926's FB pin to the node in between. The new tap point allows the LTC2926's FB pin to see <0.75V at the end of ramp-up. Finally, scale the track resistors to match R_{FAA}:

$$R'_{TA} = \frac{R_{FAA}}{R_{FAA} + R_{FAB}} \bullet R_{TA} \text{ and}$$

$$R'_{TB} = \frac{R_{FAA}}{R_{FAA} + R_{FAB}} \bullet R_{TB}$$

Voltage regulators that force their reference voltage between their output and feedback nodes do not employ a ground-based reference, and thus will not be controllable by the LTC2926 without a series MOSFET.

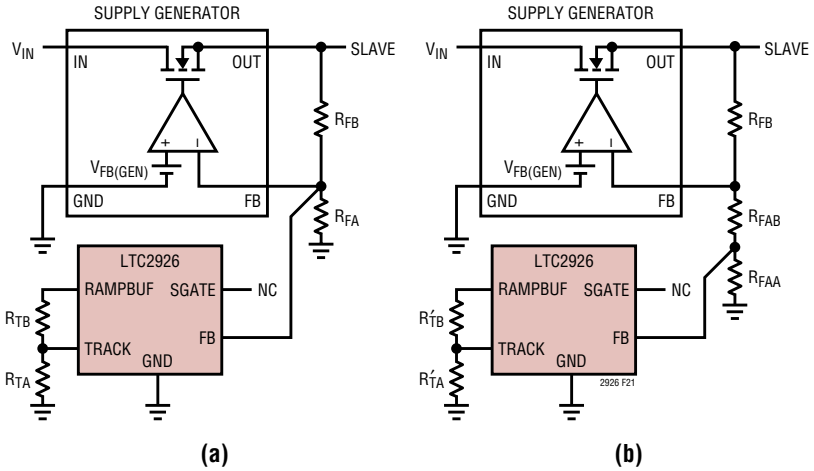


Figure 21. Slave Supply Control Without a MOSFET
(a) Generator Reference $V_{FB(GEN)} \le 0.75V$ and (b) Generator Reference $V_{FB(GEN)} > 0.75V$

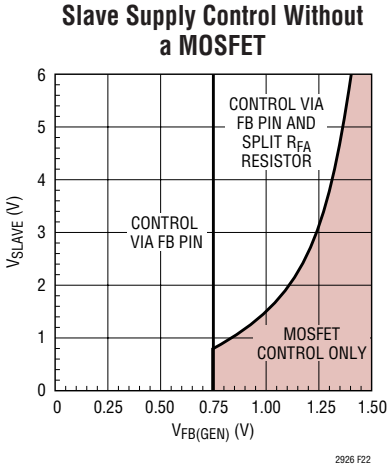


Figure 22. Regions of Possible Slave Control Without a MOSFET

APPLICATIONS INFORMATION

Final Sanity Checks

The collection of equations below is useful for identifying unrealizable solutions.

As stated in step 3 of the design procedure, the slave supply must finish ramping before the master signal has reached its final voltage. This can be verified with the following equation:

$$V_{MASTER} > V_{TRACK} \bullet \left(1 + \frac{R_{TB}}{R_{TA}}\right)$$

Here, V_{TRACK} = 0.8V. V_{MASTER} is the final voltage of the master signal, either the supply voltage ramped up through the optional external MOSFET or V_{CC} when no MOSFET is present.

It is possible to choose resistor values that require the LTC2926 to supply more current than the Electrical Characteristics table guarantees. To avoid this condition, check that each TRACK pin's current, I_{TRACKn}, does not exceed 1mA, and that the RAMPBUF pin current, $I_{RAMPBUF}$, does not exceed ±3mA.

To confirm that $I_{TRACKn} \leq 1mA$, verify that:

$$\frac{V_{TRACK}}{R_{TA} || R_{TB}} \leq 1mA$$

Check that the RAMPBUF pin will not be forced to sink more than 3mA when it is at 0V and will not be forced to source more than 3mA when it is at V_{MASTER}.

$$\frac{V_{TRACK}}{R_{TA1} || R_{TB1}} + \frac{V_{TRACK}}{R_{TA2} || R_{TB2}} \leq 3mA \text{ and}$$

$$\frac{V_{MASTER}}{R_{TA1} + R_{TB1}} + \frac{V_{MASTER}}{R_{TA2} + R_{TB2}} \leq 3mA$$

Load Requirements

A weak resistive load can cause static and dynamic tracking errors. The behavior of the source-follower topology of MOSFET-controlled tracking relies on the load's ability to support the ramp rates and tracking currents of a particular application. Consider the simplified slave load schematic in Figure 23.

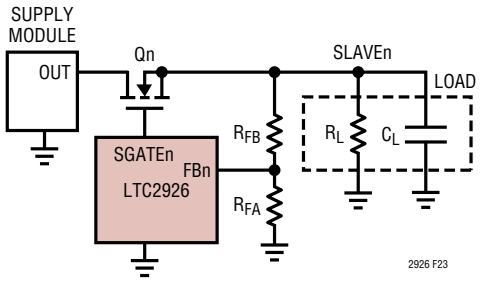


Figure 23. Simplified Slave Supply Load

When the supplies are ramped down quickly, the load must be capable of sinking enough current to support the ramp rate. For example, if there is a large output capacitance and a weak resistive load on a particular supply, that supply's falling rate will be limited by the RC time constant of the load. In Figure 24, the falling 2.5V slave cannot keep up with the falling master ramp.

When the supplies are near ground, the load must be capable of sinking the tracking current without creating a large offset voltage. For weak resistive loads and slave voltage levels near ground, the tracking current (at its maximum there) can be in excess of the load's current demand. Having no capability for sinking current, the MOSFET shuts off. All of the mirrored tracking current that flows through R_{FB} also flows through the load resistance, R_L, which creates a voltage offset between the slave and ground. In Figure 24, the 1.8V supply shows an offset from ground.

APPLICATIONS INFORMATION

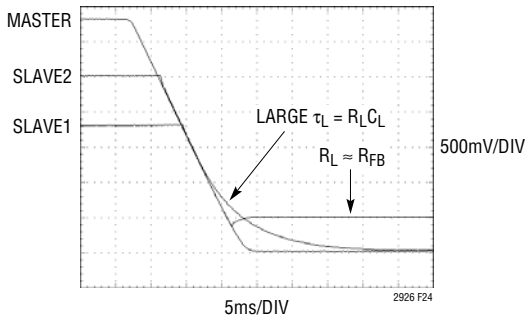


Figure 24. Tracking Effects of Weak Resistive Load

Under worst-case conditions, FB pin voltages may reach the maximum clamp voltage of 2.4V. To limit the slave voltage offset to below 100mV, choose $R_{FB} \geq 23 \bullet R_L$. Add a resistor in parallel with the load to strengthen weak resistive loads as required.

Start-Up Delays

Often power supplies do not start up immediately when their input supplies are applied. If the LTC2926 tries to ramp up these power supplies as soon as the input supply is present, the start-up of the outputs may be delayed, which defeats the tracking circuit. Make sure the ON pin does not initiate ramp-up until all supply sources are available.

RAMP Pin Clamp

The RAMP pin is weakly clamped to the V_{CC} pin. When MGATE and RAMP are tied together their pin voltages will not exceed V_{CC} + 1V. If the RAMP pin is driven by a low impedance source that can exceed V_{CC}, include a series resistor to limit the current to <20µA. Use 50kΩ per source volt above V_{CC}.

Layout Considerations

Be sure to place a 0.1µF bypass capacitor as near as possible to the supply pin of the LTC2926.

To minimize the noise on the slave supplies' outputs, keep the traces connecting the FB pins of the LTC2926 and the feedback nodes of the slave supplies' resistive voltage dividers as short as possible. In addition, do not route those traces next to signals with fast transitions times.

To get the best compensation of the series I • R drops of the external MOSFETs, make sure the supply output nodes and the supply generator sense connections use Kelvin-sensing. The feedback resistive voltage divider should Kelvin-sense the slave supply output node for accuracy, as well.

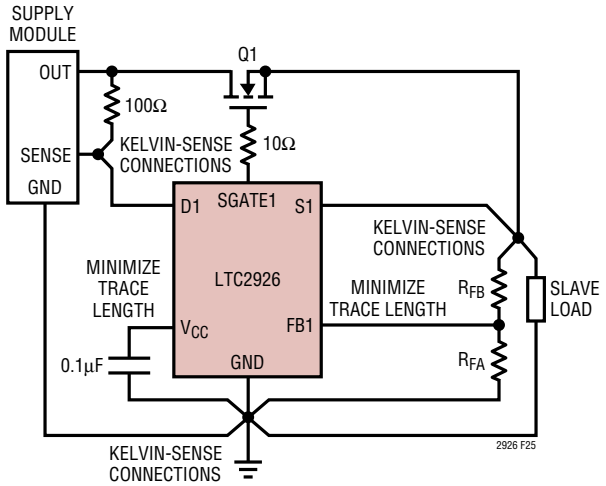
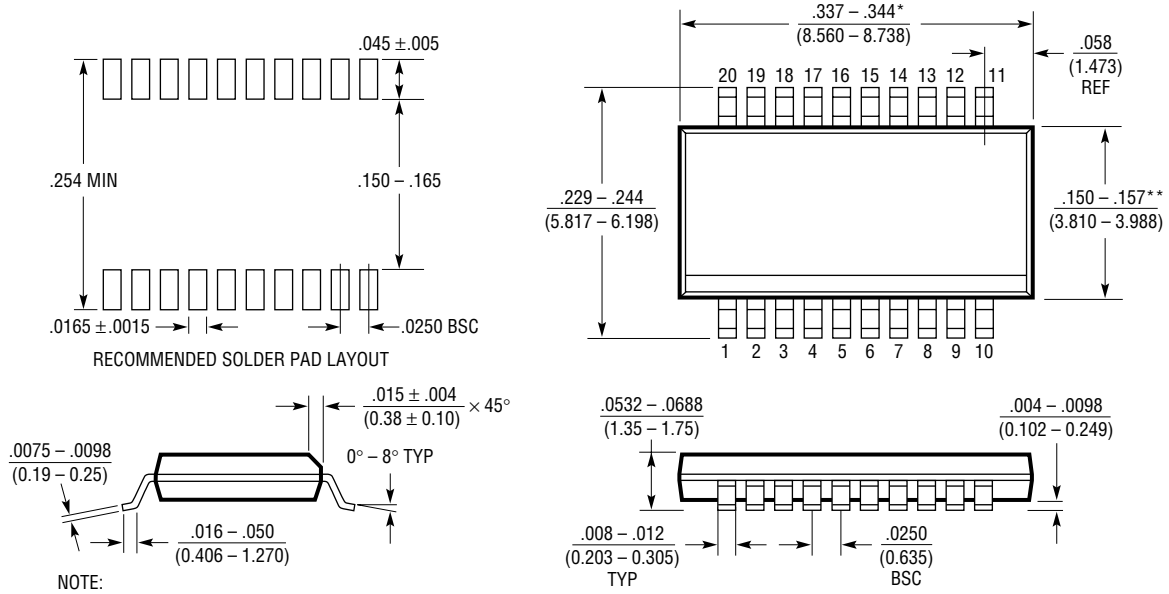


Figure 25. Layout Considerations

PACKAGE DESCRIPTION

GN Package
20-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



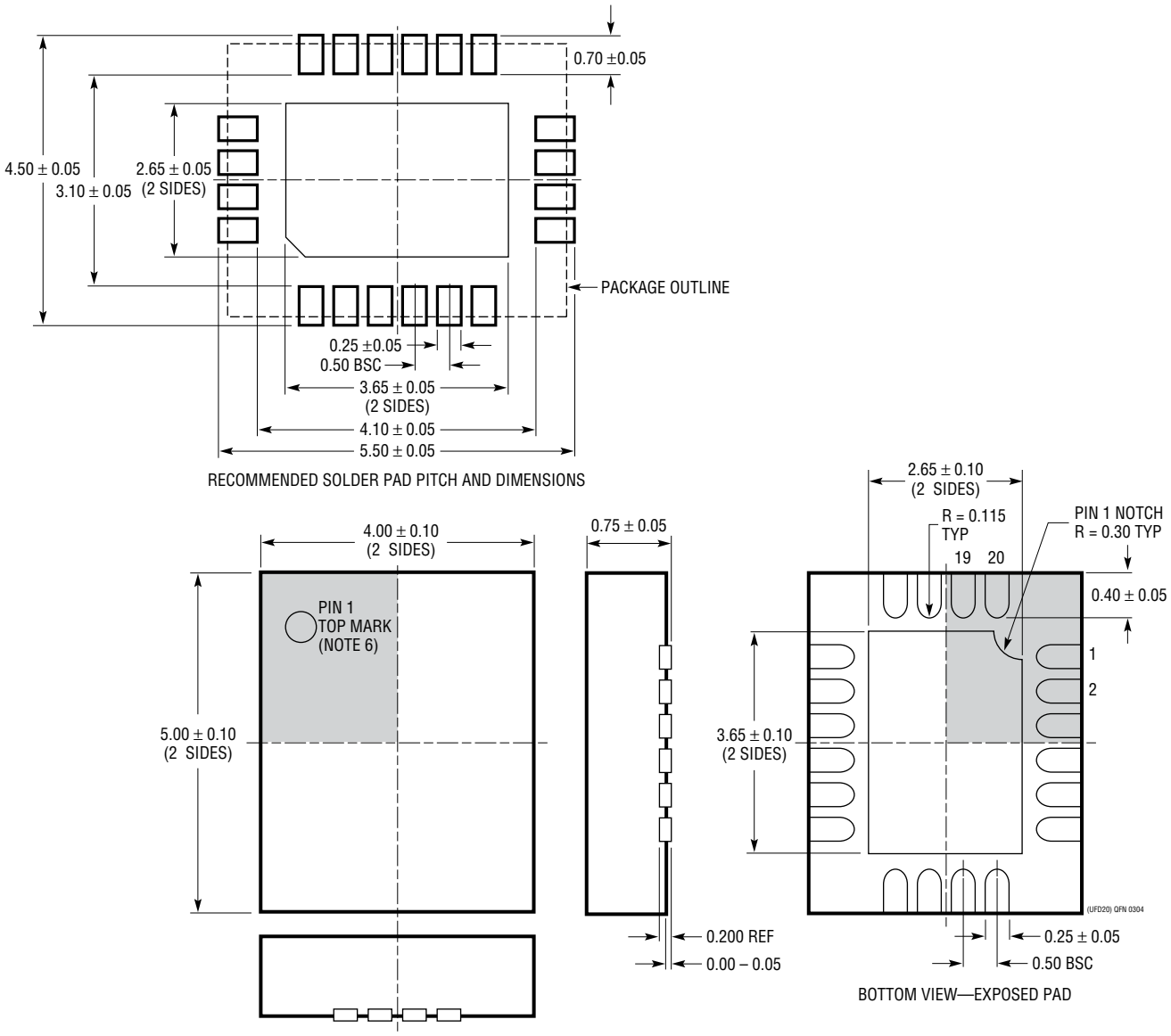
NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

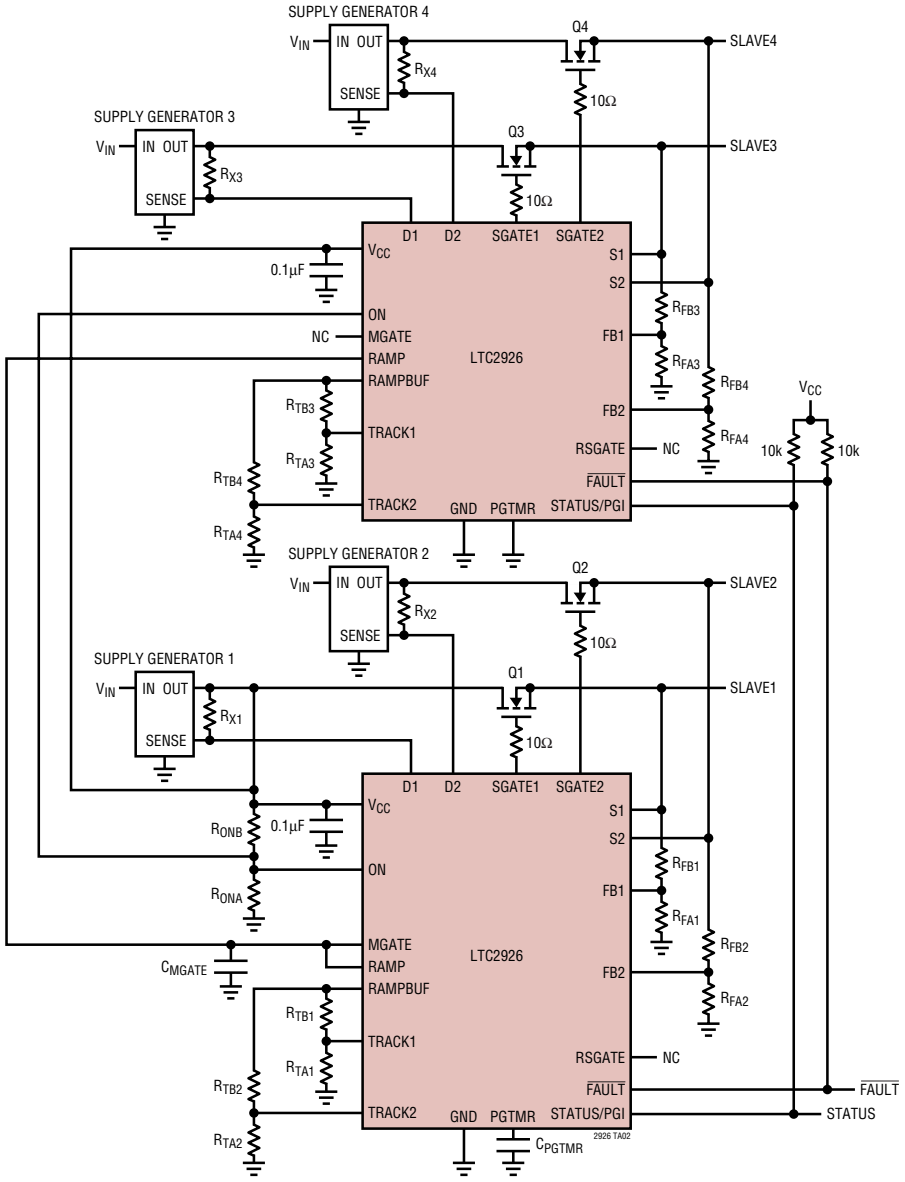
UFD Package
20-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1711)



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Chaining to Track/Sequence More Supplies



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2908	Precision Six Supply Monitor	Four Fixed (Various Levels) and Two Adjustable Input Thresholds
LTC2920-1/LTC2920-2	Single/Dual Power Supply Margining Controllers	Single or Dual, Symmetric/Asymmetric High and Low Margining
LTC2921/LTC2922	Power Supply Trackers with Input Monitors	Monitor up to Five Supplies, Includes Remote Sense Switches
LTC2923	Power Supply Tracking Controller	Controls Two Supplies Without FETs, MSOP-10 and DFN-12 Packages
LTC2925	Multiple Power Supply Tracking Controller with Power Good Timeout	Controls Three Supplies Without FETs, Includes Three Shutdown Control Pins
LTC2927	Single Power Supply Tracking Controller	Controls Single Supply Without FETs, Daisy-Chain for Multiple Supplies

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- Excess Inventory Management