THE DATASHEET OF

LTC2907ITS8#TRMPBF

Precision Dual Supply Monitors with One Pin-Selectable Threshold and One Adjustable Input

FEATURES

- **Monitors Two Inputs Simultaneously**
- **Three Threshold Selections for 5V, 3.3V or 2.5V Supplies**
- **Low Voltage Adjustable Input (0.5V)**
- **Three Supply Tolerances (5%, 7.5%, 10%)**
- **Guaranteed Threshold Accuracy: ±1.5% of Monitored Voltage Over Temperature**
- **Internal V_{CC} Auto Select**
- Power Supply Glitch Immunity
- 200ms Reset Time Delay (LTC2906 Only)
- Adjustable Reset Time Delay (LTC2907 Only)
- Open Drain $\overline{RST}$ Output
- Guaranteed $\overline{RST}$ for V1 ≥ 1V or V_{CC} ≥ 1V
- Low Profile (1mm) SOT-23 (ThinSOT™) and Plastic (3mm × 2mm) DFN Packages

APPLICATIONS

- Desktop and Notebook Computers
- Handheld Devices
- Network Servers
- Core, I/O Monitor

DESCRIPTION

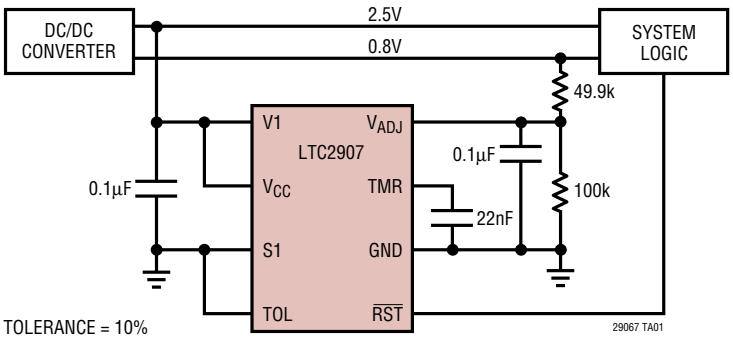
The LTC®2906/LTC2907 are dual supply monitors intended for systems with multiple supply voltages. The dual supply monitors have a common reset output with delay (200ms for the LTC2906 and adjustable using an external capacitor for the LTC2907). These products provide a precise, space-conscious and micropower solution for supply monitoring.

The LTC2906/LTC2907 feature a tight 1.5% threshold accuracy over the whole operating temperature range and glitch immunity to ensure reliable reset operation without false triggering. The open drain $\overline{RST}$ output state is guaranteed to be in the correct state for V1 and/or V_{CC} down to 1V.

The LTC2906/LTC2907 also feature one adjustable input with a nominal threshold level at 0.5V, another input with three possible input threshold levels, and three supply tolerances for possible margining. These features provide versatility for any kind of system requiring dual supply monitors. Two three-state input pins program the threshold and tolerance level without requiring any external components.

TYPICAL APPLICATION

Dual Supply Monitor with Adjustable Tolerance (2.5V, 0.8V)



Supply Selection Programming

V1	S1
5.0	V1
3.3	OPEN
2.5	GND

Tolerance Programming

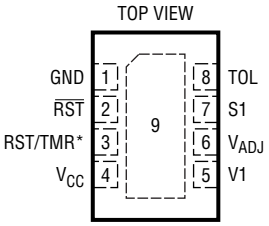
TOLERANCE	TOL
5%	V1
7.5%	OPEN
10%	GND

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Terminal Voltages
V1, V_{CC} ..... –0.3V to 7V
S1, V_{ADJ}, TOL ..... –0.3V to (V_{MAX} + 0.3V)
$\overline{RST}$ ..... –0.3V to 7V
RST (LTC2906) ..... –0.3V to 7V
TMR (LTC2907) ..... –0.3V to 7V

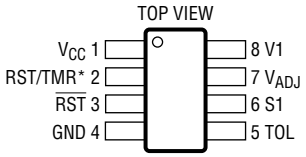
Operating Temperature Range
LTC2906C/LTC2907C ..... 0°C to 70°C
LTC2906I/LTC2907I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



DDB8 PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN
EXPOSED PAD IS GND (PIN 9),
MUST BE SOLDERED TO PCB
*RST FOR LTC2906
TMR FOR LTC2907
T_{JMAX} = 125°C, θ_{JA} = 250°C/W

ORDER PART NUMBER
LTC2906CDDB LTC2906IDDB LTC2907CDDB LTC2907IDDB
DDB8 PART MARKING
LBDC LBDD LBDF LBDG



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23
*RST FOR LTC2906
TMR FOR LTC2907
T_{JMAX} = 125°C, θ_{JA} = 250°C/W

ORDER PART NUMBER
LTC2906CTS8 LTC2906ITS8 LTC2907CTS8 LTC2907ITS8
TS8 PART MARKING
LTBCM LTBCN LTBCP LTBCQ

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = V1 = 2.5V, V_{ADJ} = 0.55V, S1 = TOL = 0V, unless otherwise noted. (Notes 2, 3, 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{RT50}	5V, 5% Reset Threshold	V1 Input Threshold	●	4.600	4.675	4.750	V
	5V, 7.5% Reset Threshold		●	4.475	4.550	4.625	V
	5V, 10% Reset Threshold		●	4.350	4.425	4.500	V
V_{RT33}	3.3V, 5% Reset Threshold	V1 Input Threshold	●	3.036	3.086	3.135	V
	3.3V, 7.5% Reset Threshold		●	2.954	3.003	3.053	V
	3.3V, 10% Reset Threshold		●	2.871	2.921	2.970	V
V_{RT25}	2.5V, 5% Reset Threshold	V1 Input Threshold	●	2.300	2.338	2.375	V
	2.5V, 7.5% Reset Threshold		●	2.238	2.275	2.313	V
	2.5V, 10% Reset Threshold		●	2.175	2.213	2.250	V
V_{RTADJ}	ADJ, 5% Reset Threshold	V_{ADJ} Input Threshold	●	0.492	0.500	0.508	V
	ADJ, 7.5% Reset Threshold		●	0.479	0.487	0.495	V
	ADJ, 10% Reset Threshold		●	0.465	0.473	0.481	V
$V_{MAX(MIN)}$	Minimum V_{MAX} Operating Voltage (Note 2)	RST, $\overline{RST}$ in Correct Logic State	●			1	V
I_{VCC}	V_{CC} Input Current	V_{CC} > V1	●		54	100	µA
		V1 > V_{CC}	●			±1	µA
I_{V1}	V1 Input Current	V_{CC} > V1	●		1	3	µA
		V1 > V_{CC}	●		55	100	µA
I_{VADJ}	V_{ADJ} Input Current		●			±15	nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = V1 = 2.5V, V_{ADJ} = 0.55V, S1 = TOL = 0V, unless otherwise noted. (Notes 2, 3, 4)

SYMBOL	PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$I_{TMR(UP)}$	TMR Pull-Up Current	(LTC2907)	V_{TMR} = 0V	●	–1.5	–2.1	–2.7	µA
$I_{TMR(DOWN)}$	TMR Pull-Down Current	(LTC2907)	V_{TMR} = 1.4V	●	1.5	2.1	2.7	µA
t_{RST}	Reset Time-Out Period	(LTC2906)		●	140	200	260	ms
t_{RST}	Reset Time-Out Period	(LTC2907)	C_{TMR} = 22nF	●	140	200	260	ms
t_{UV}	V_X Undervoltage Detect to $\overline{RST}$ or RST		V_X Less Than Reset Threshold V_{RTX} by More than 1%			150		µs
V_{OL}	Output Voltage Low $\overline{RST}$, RST		I = 2.5mA I = 100µA; V1 and/or V_{CC} = 1V ($\overline{RST}$ Only)	● ●		0.15 0.05	0.4 0.3	V V
V_{OH}	Output Voltage High $\overline{RST}$, RST (Notes 2, 5)		I = –1µA	●	V_{MAX} – 1			V
Three-State Inputs S1, TOL								
V_{IL}	Low Level Input Voltage			●			0.4	V
V_{IH}	High Level Input Voltage			●	1.4			V
V_Z	Pin Voltage when Left in Hi-Z State		I = –10µA I = 0µA I = 10µA	● ●	0.7	 0.9 	 1.1	V V V
I_{VPG}	Programming Input Current (Note 6)			●			±25	µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The greater of V1, V_{CC} is the internal supply voltage (V_{MAX}).

Note 3: All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

Note 4: For reset thresholds test conditions refer to the voltage threshold programming table in the Applications Information section.

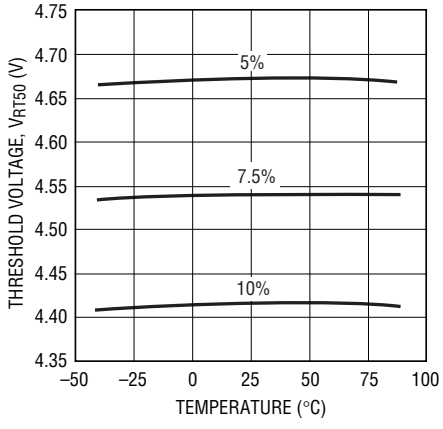
Note 5: The output pins RST and $\overline{RST}$ have an internal pull-up to V_{MAX} of typically –6µA. However, an external pull-up resistor may be used when faster rise time is required or for V_{OH} voltages greater than V_{MAX}.

Note 6: The input current to the three-state input pins are the pull-up and the pull-down current when the pins are either set to V1 or GND respectively. In the open state, the maximum leakage current to V1 or GND permissible is 10µA.

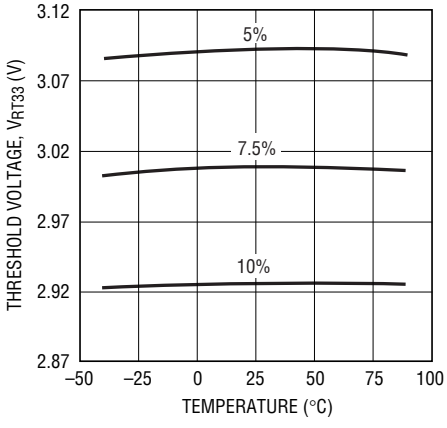
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C unless otherwise noted.

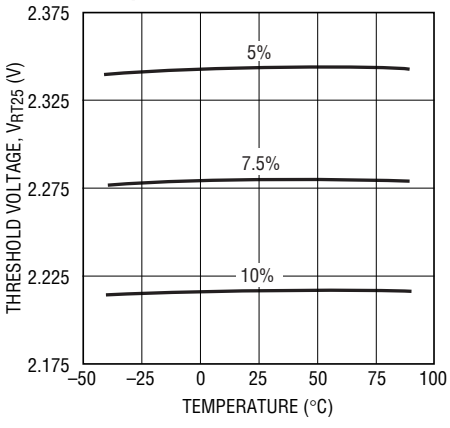
5V Threshold Voltage vs Temperature



3.3V Threshold Voltage vs Temperature



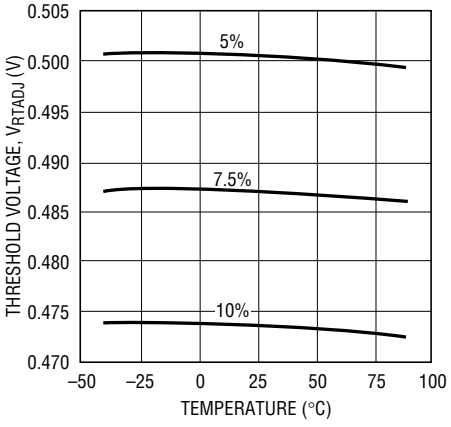
2.5V Threshold Voltage vs Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

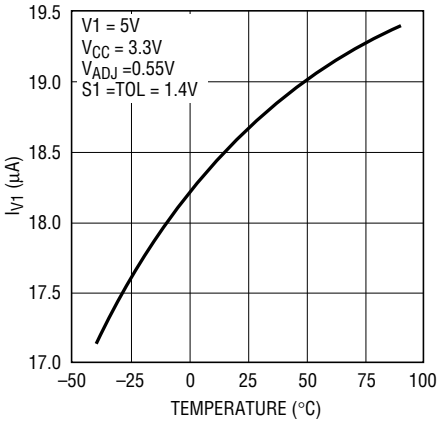
Specifications are at T_A = 25°C unless otherwise noted.

ADJ Threshold Voltage vs Temperature



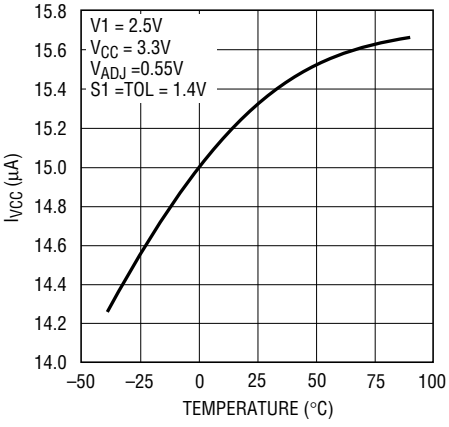
29067 G04

I_{V1} vs Temperature



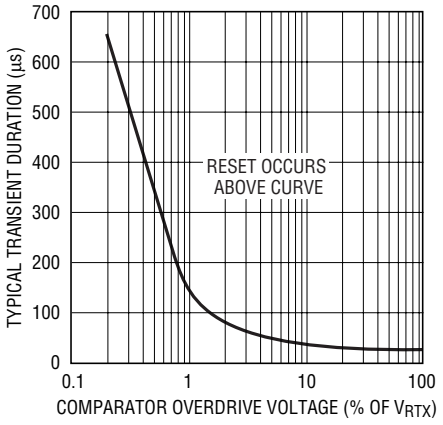
29067 G05

I_{VCC} vs Temperature



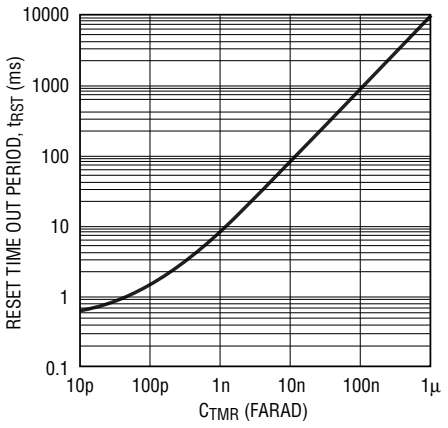
29067 G06

Typical Transient Duration vs Comparator Overdrive (V1, V_{ADJ})



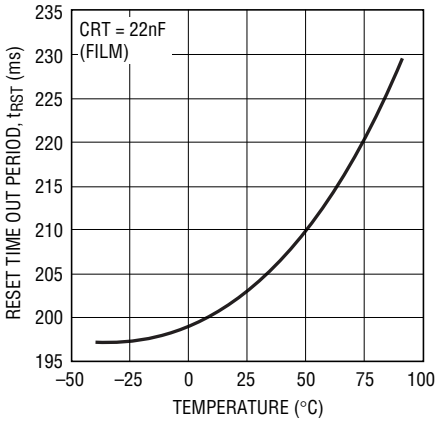
29067 G07

Reset Time Out Period (t_{RST}) vs Capacitance (C_{TMR})



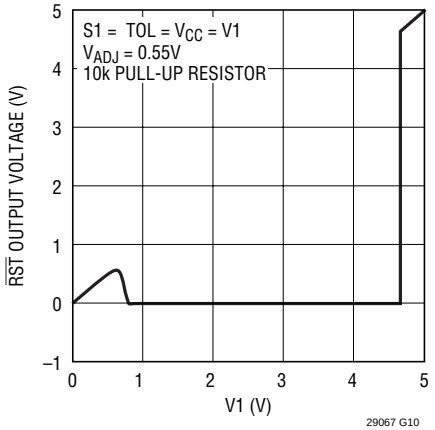
29067 G08

Reset Time Out Period (t_{RST}) vs Temperature



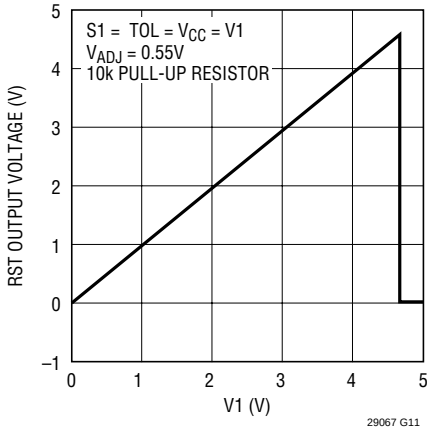
29067 G09

$\overline{RST}$ Output Voltage vs V1



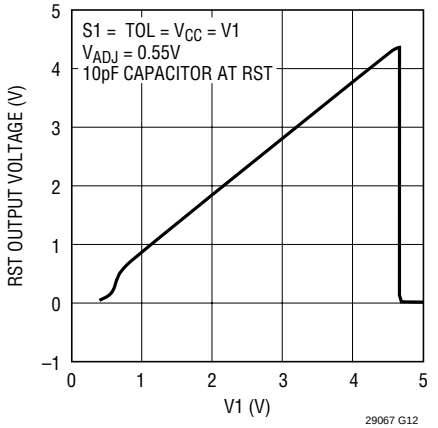
29067 G10

RST Output Voltage vs V1



29067 G11

RST Output Voltage vs V1

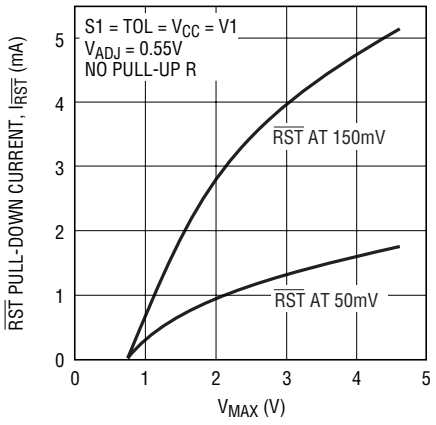


29067 G12

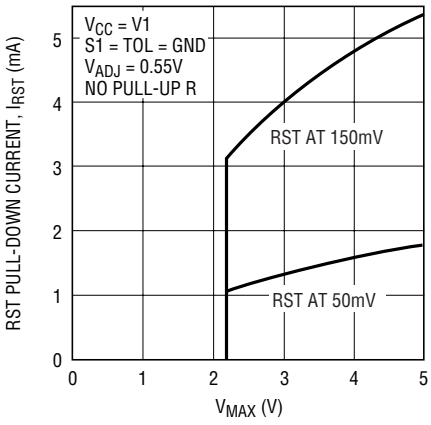
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C unless otherwise noted.

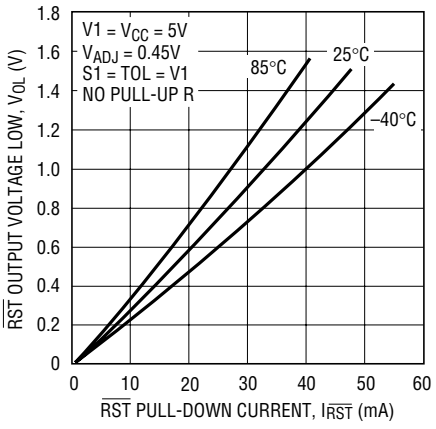
$\overline{RST}$ Pull-Down Current ($I_{\overline{RST}}$) vs V_{MAX}



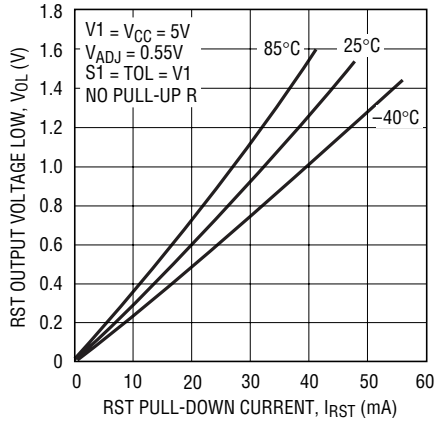
RST Pull-Down Current (I_{RST}) vs V_{MAX}



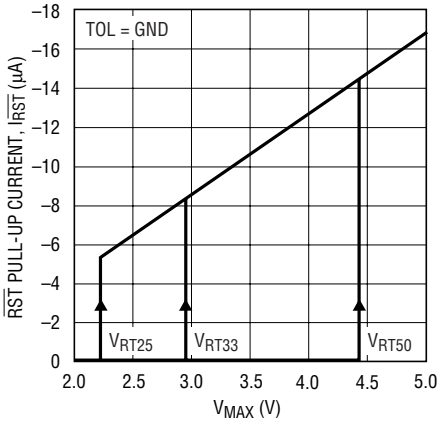
$\overline{RST}$ Output Voltage Low (V_{OL}) vs $\overline{RST}$ Pull-Down Current ($I_{\overline{RST}}$)



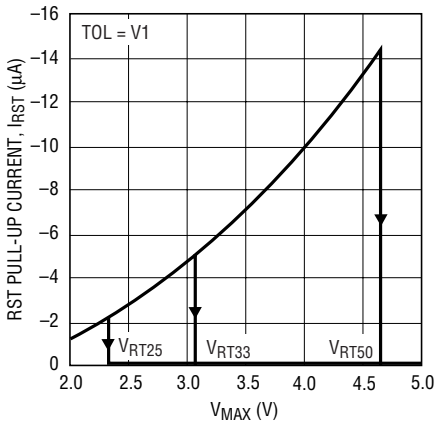
RST Output Voltage Low (V_{OL}) vs RST Pull-Down Current (I_{RST})



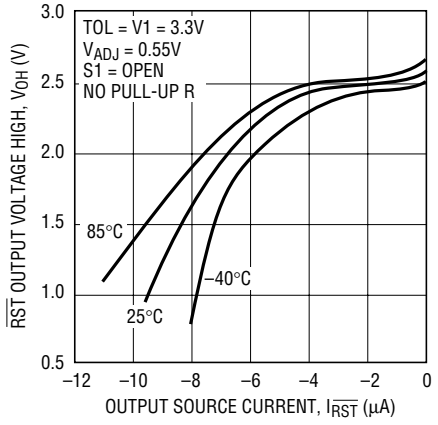
$\overline{RST}$ Pull-Up Current ($I_{\overline{RST}}$) vs V_{MAX}



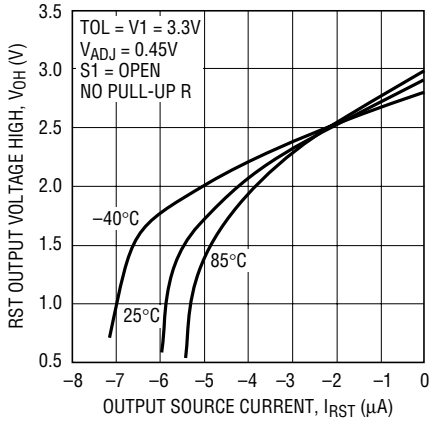
RST Pull-Up Current (I_{RST}) vs V_{MAX}



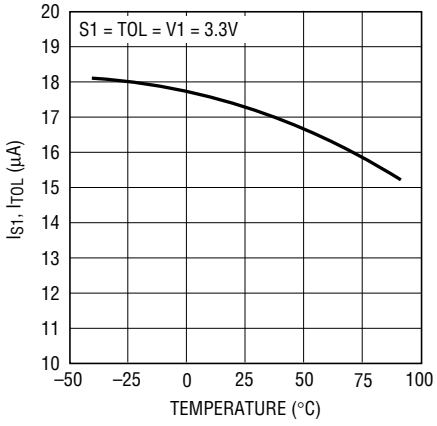
$\overline{RST}$ Output Voltage High (V_{OH}) vs $\overline{RST}$ Output Source Current ($I_{\overline{RST}}$)



RST Output Voltage High (V_{OH}) vs RST Output Source Current (I_{RST})



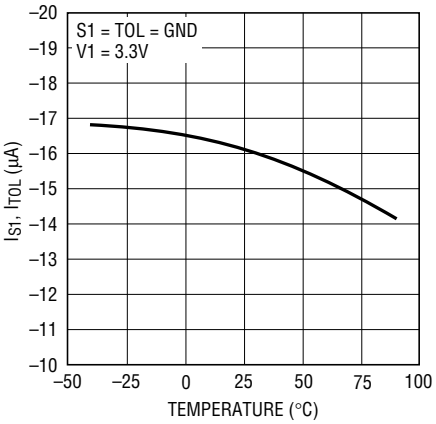
I_{S1}, I_{TOL} vs Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C unless otherwise noted.

I_{S1}, I_{TOL} vs Temperature



PIN FUNCTIONS (TS8 Package/DDB8 Package)

V_{CC} (Pin 1/Pin 4): Optional Power Supply Pin. V_{CC} powers and maintains the correct operation of the RST and $\overline{RST}$ pins in the complete absence of V1. If V1 is present, the greater of V_{CC} or V1 (V_{MAX}) powers the internal circuitry and the reset outputs. Bypass this pin to ground with a 0.1µF (or greater) capacitor. Tie to V1 when no optional power is available.

RST (Pin 2/Pin 3): (LTC2906 Only) Reset Logic Output. When all voltage inputs are above the reset threshold for at least the programmed delay time, this pin pulls low. This pin has a weak pull up to V_{MAX} and may be pulled above V_{MAX} using an external pull-up.

TMR (Pin 2/Pin 3): (LTC2907 Only) Reset Delay Time Programming Pin. Attach an external capacitor (C_{TMR}) to GND to set a reset delay time of 9ms/nF. Leaving the pin open generates a minimum delay of approximately 200µs. A 22nF capacitor will generate a 200ms reset delay time.

$\overline{RST}$ (Pin 3/Pin 2): Inverted Reset Logic Output. Pulls low when either V1 or V_{ADJ} is below the reset threshold and holds low for programmed delay time after all voltage inputs are above threshold. This pin has a weak pull up to V_{MAX} and may be pulled above V_{MAX} using an external pull-up.

GND (Pin 4/Pin 1 and Pin 9): Ground.

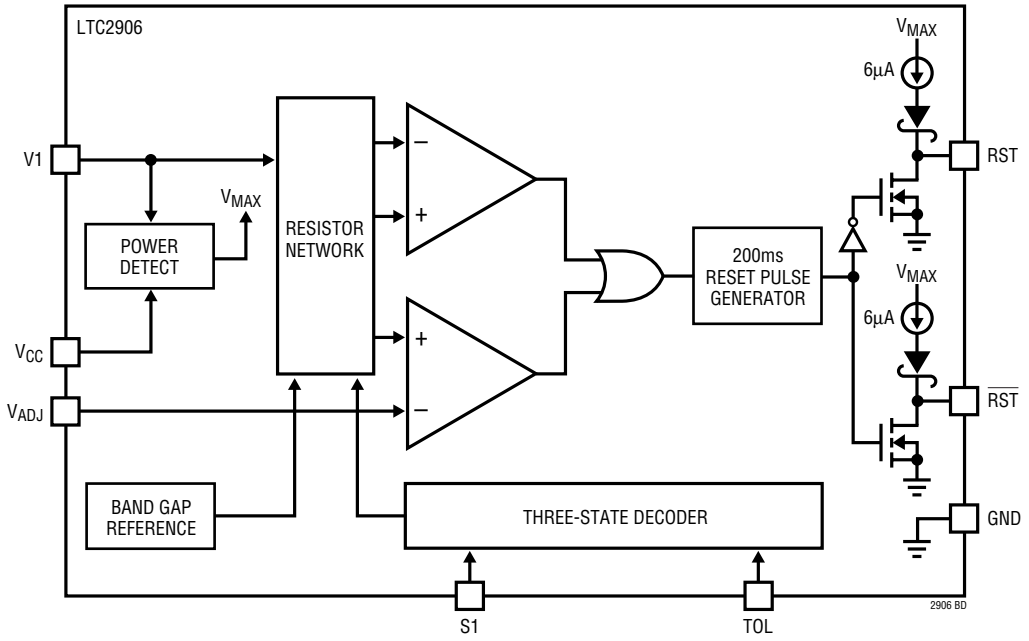
TOL (Pin 5/Pin 8): Three-State Input for Supply Tolerance Selection (5%, 7.5% or 10%). Refer to Applications Information for tolerance selection chart (Table 3).

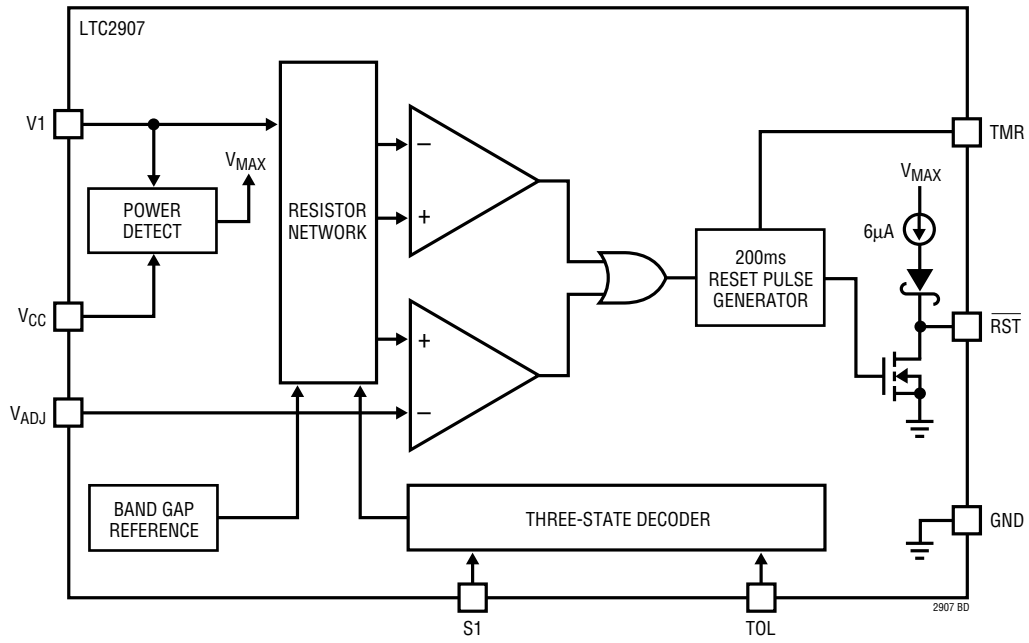
S1 (Pin 6/Pin 7): The Voltage Threshold Select Three-State Input. Connect to V1, GND or leave unconnected in open state to select one of three possible input threshold levels (refer to Table 1).

V_{ADJ} (Pin 7/Pin 6): Adjustable Voltage Input. Bypass this pin to ground with a 0.1µF (or greater) capacitor in a noisy environment.

V1 (Pin 8/Pin 1): Voltage Input 1. Select from 5V, 3.3V or 2.5V. Refer to Table 1 for details. The greater of (V1, V_{CC}) is also the internal V_{CC} (V_{MAX}). Bypass this pin to ground with a 0.1µF (or greater) capacitor.

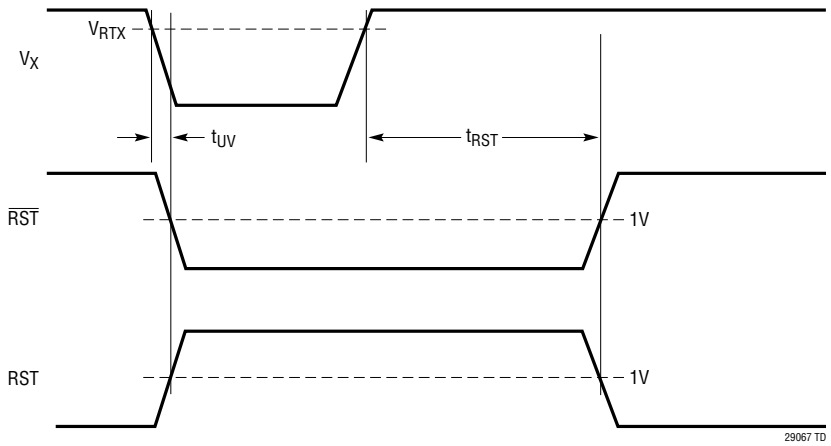
BLOCK DIAGRAM





TIMING DIAGRAM

Vx Monitor Timing



APPLICATIONS INFORMATION

Supply Monitoring

The LTC2906/LTC2907 are low power, high accuracy dual supply monitoring circuits with an adjustable input and another input with selectable threshold. Reset delay is set to a nominal of 200ms for LTC2906 and is adjustable using an external capacitor for LTC2907.

The three-state input pin (S1) selects one of three possible threshold voltage levels for V1. Another three-state input pin sets the supply tolerance (5%, 7.5% or 10%). Both input voltages (V1 and V_{ADJ}) must be above predetermined thresholds for the reset not to be invoked. The LTC2906/LTC2907 assert the reset outputs during power-up, power-down and brownout conditions on any one of the voltage inputs.

Power-Up

The greater of V1, V_{CC} is the internal supply voltage (V_{MAX}). V_{MAX} powers the drive circuits for the $\overline{RST}$ pin. Therefore, as soon as V1 or V_{CC} reaches 1V during power up, the $\overline{RST}$ output asserts low.

V_{MAX} also powers the drive circuits for the RST pin in the LTC2906. Therefore, RST weakly pulls high when either V1 or V_{CC} reaches at least 1V.

Threshold programming is complete, when V1 reaches at least 2.17V. After programming, if any one of the Vx inputs falls below its programmed threshold, $\overline{RST}$ asserts low (RST weakly pulls high) as long as V_{MAX} is at least 1V.

Once both V1 and V_{ADJ} inputs rise above their thresholds, an internal timer is started. After the programmed delay time, $\overline{RST}$ weakly pulls high (RST asserts low).

Power-Down

On power-down, once either V1 or V_{ADJ} drops below its threshold, $\overline{RST}$ asserts logic low and RST weakly pulls high. V_{MAX} of at least 1V guarantees a logic low of 0.4V at $\overline{RST}$.

Auxiliary Power

If an auxiliary power is available it can be connected to the V_{CC} pin. Since the internal supply voltage (V_{MAX}) is the greater of V1, V_{CC}; a V_{CC} of at least 1V guarantees logic low of 0.4V at $\overline{RST}$ for voltage inputs (V1 and/or V_{ADJ}) down to 0V.

Programming Pins

The two three-state input pins, S1 and TOL, should be connected to GND, V1 or left unconnected during normal operation. Note that when left unconnected, the maximum leakage current allowable from the pin to either GND or V1 is 10µA.

APPLICATIONS INFORMATION

In margining application, the three-state input pins can be driven using a three-state buffer. Note however, the low and high output of the three-state buffer has to satisfy the V_{IL} and V_{IH} of the three-state pin listed in the Electrical Characteristics Table. Moreover, when the three-state buffer is in the high impedance state, the maximum leakage current allowed from the pin to either GND or V1 is 10µA.

Monitor Programming

Connecting S1 to either GND, or V1, or leaving it in open state selects the LTC2906/LTC2907 V1 input voltage threshold. Table 1 shows the three possible selections of V1 nominal input voltage and their corresponding S1 connection.

Table 1. Supply Selection Programming

V1	S1
5.0	V1
3.3	OPEN
2.5	GND

Note: Open = open circuit or driven by a three-state buffer in high impedance state with leakage current less than 10µA.

The noninverting input on the V_{ADJ} comparator is set to 0.5V when the TOL pin is set high (5% tolerance) (Figure 1) and the high impedance inverting input directly ties to the V_{ADJ} pin.

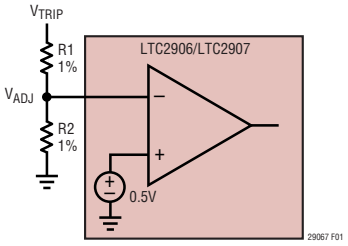


Figure 1. Setting the Adjustable Trip Point

In a typical application, the V_{ADJ} pin connects to a tap point on an external resistive divider between the positive voltage being monitored and ground. The following formula obtains R1 resistor value for a particular value of R2 and a desired trip voltage at 5% tolerance:

$$R1 = \left(\frac{V_{TRIP(5\%)}}{0.5V} - 1 \right) R2$$

R2 =100kΩ is recommended. Once the resistor divider is set in the 5% tolerance mode, there is no need to change the divider for the other tolerance modes (7.5%, 10%) because the internal reference at the noninverting input on the V_{ADJ} comparator is scaled accordingly, moving the trip point in 2.5% decrements.

Table 2 shows suggested 1% resistor values for various adjustable applications.

Table 2. Suggested 1% Resistor Values for the V_{ADJ} Inputs

V_{SUPPLY} (V)	V_{TRIP} (V)	R1 (kΩ)	R2 (kΩ)
12	11.25	2150	100
10	9.4	1780	100
8	7.5	1400	100
7.5	7	1300	100
6	5.6	1020	100
5	4.725	845	100
3.3	3.055	511	100
3	2.82	464	100
2.5	2.325	365	100
1.8	1.685	237	100
1.5	1.410	182	100
1.2	1.120	124	100
1	0.933	86.6	100
0.9	0.840	68.1	100
0.8	0.750	49.9	100
0.7	0.655	30.9	100
0.6	0.561	12.1	100

Tolerance Programming

The three-state input pin TOL, programs the common supply tolerance for both V1 and V_{ADJ} input voltages (5%, 7.5% or 10%). The larger the tolerance the lower the trip threshold. Table 3 shows the tolerances selection corresponding to a particular connection at the TOL pin.

Table 3. Tolerance Programming

TOLERANCE	TOL
5%	V1
7.5%	OPEN
10%	GND

APPLICATIONS INFORMATION

Threshold Accuracy

Reset threshold accuracy is of the utmost importance in a supply sensitive system. Ideally such a system should not reset while supply voltages are within a specified margin below the rated nominal level. Both of the LTC2906/LTC2907 inputs have the same relative threshold accuracy. The specification for LTC2906/LTC2907 is ±1.5% of the programmed nominal input voltage (over the full operating temperature range).

For example, when the LTC2906/LTC2907 are programmed to handle a 5V input with 10% tolerance (S1 = V1 and TOL = GND, refer to Table 1 and Table 3), it does not issue a reset command when V1 is above 4.5V. The typical 10% trip threshold is at 11.5% below the nominal input voltage level. Therefore, the typical trip threshold for the 5V input is 4.425V. With ±1.5% accuracy, the trip threshold range is 4.425V ±75mV over temperature (i.e. 10% to 13% below 5V). This implies that the monitored system must operate reliably down to 4.35V or 13% below 5V over temperature.

The same system using a supervisor with only ±2.5% accuracy needs to work reliably down to 4.25V (4.375V ±125mV) or 15% below 5V, requiring the monitored system to work over a much wider operating voltage range.

In any supervisory application, supply noise riding on the monitored DC voltage can cause spurious resets, particularly when the monitored voltage is near the reset threshold. A less desirable but common solution to this problem is to introduce hysteresis around the nominal threshold. Notice however, this hysteresis introduces an error term in the threshold accuracy. Therefore, a ±2.5% accurate monitor with ±1% hysteresis is equivalent to a ±3.5% monitor with no hysteresis.

The LTC2906/LTC2907 take a different approach to solve this problem of supply noise causing spurious reset. The first line of defense against this spurious reset is a first order low pass filter at the output of the comparator. Thus, the comparator output goes through a form of integration before triggering the output logic. Therefore, any kind of transient at the input of the comparator needs to be of sufficient magnitude and duration before it can trigger a change in the output logic.

The second line of defense is the programmed delay time t_{RST} (200ms for LTC2906 and adjustable using an external capacitor for LTC2907). This delay will eliminate the effect of any supply noise, whose frequency is above $1/t_{RST}$, on the $\overline{RST}$ and RST output.

When either V1 or V_{ADJ} drops below its programmed threshold, the $\overline{RST}$ pin asserts low (RST weakly pulls high). When the supply recovers above the programmed threshold, the reset-pulse-generator timer starts counting.

If the supply remains above the programmed threshold when the timer finishes counting, the $\overline{RST}$ pin weakly pulls high (RST asserts low). However, if the supply falls below the programmed threshold any time during the period when the timer is still counting, the timer resets and starts fresh when the supply next rises above the programmed threshold.

Note that this second line of defense is only effective for a rising supply and does not affect the sensitivity of the system to a falling supply. Therefore, the first line of defense that works for both cases of rising and falling is necessary. These two approaches prevent spurious reset caused by supply noise without sacrificing the threshold accuracy.

Selecting the Reset Timing Capacitor

The reset time-out period for LTC2907 is adjustable in order to accommodate a variety of microprocessor applications. Connecting a capacitor, C_{TMR}, between the TMR pin and ground sets the reset time-out period, t_{RST}. The following formula determines the value of capacitor needed for a particular reset time-out period:

$$C_{TMR} = t_{RST} \bullet 110 \bullet 10^{-9}\ [F/s]$$

For example, using a standard capacitor value of 22nF gives a 200ms delay.

The graph in Figure 2 shows the desired delay time as a function of the value of the timer capacitor that should be used:

APPLICATIONS INFORMATION

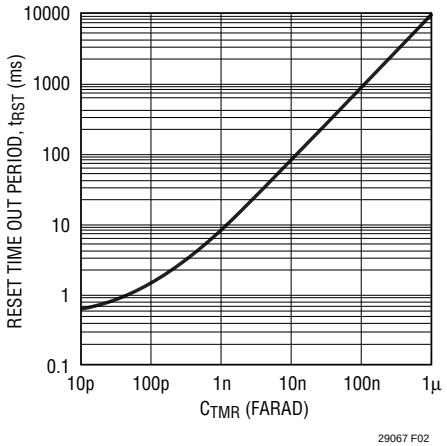


Figure 2. Reset Time-Out Period vs Capacitance

Leaving the TMR pin open with no external capacitor generates a reset time-out of approximately 200µs. For long reset time-out, the only limitation is the availability of a large value capacitor with low leakage. The TMR capacitor will never charge if the leakage current exceeds the TMR charging current of 2.1µA (typical).

RST and $\overline{RST}$ Output Characteristics

The DC characteristics of the RST and $\overline{RST}$ pull-up and pull-down strength are shown in the Typical Performance Characteristics section. Both RST and $\overline{RST}$ have a weak internal pull-up to V_{MAX} and a strong pull-down to ground.

The weak pull-up and strong pull-down arrangement allows these two pins to have open-drain behavior while possessing several other beneficial characteristics.

The weak pull-ups eliminate the need for external pull-up resistors when the rise time on these pins is not critical. On the other hand, the open-drain $\overline{RST}$ configuration allows for wired-OR connections and can be useful when more than one signal needs to pull-down on the $\overline{RST}$ line.

As noted in the Power-Up and Power-Down sections, the circuits that drive RST and $\overline{RST}$ are powered by V_{MAX} = MAX (V1, V_{CC}). During fault condition, V_{MAX} of at least 1V guarantees a maximum V_{OL} = 0.4V at $\overline{RST}$. However, at V_{MAX} = 1V the weak pull-up current on RST is barely turned on. Therefore, an external pull-up resistor of no more than 100k is recommended on the RST pin if the state and pull-up strength of the RST pin is crucial at very low V_{MAX}.

Note however, by adding an external pull-up resistor, the pull-up strength on the RST pin is increased. Therefore, if it is connected in a wired-OR connection, the pull-down strength of any single device needs to accommodate this additional pull-up strength.

Output Rise and Fall Time Estimation

The RST and $\overline{RST}$ output have strong pull-down capability. The following formula estimates the output fall time (90% to 10%) for a particular external load capacitance (C_{LOAD}):

$$t_{FALL} \approx 2.2 \bullet R_{PD} \bullet C_{LOAD}$$

where R_{PD} is the on-resistance of the internal pull-down transistor estimated to be typically 40Ω at V_{MAX} >1V, at room temperature (25°C), and C_{LOAD} is the external load capacitance on the pin. Assuming a 150pF load capacitance, the fall time is about 13ns.

The rise time on the RST and $\overline{RST}$ pins is limited by weak internal pull-up current sources to V_{MAX}. The following formula estimates the output rise time (10% to 90%) at the RST and $\overline{RST}$ pins:

$$t_{RISE} \approx 2.2 \bullet R_{PU} \bullet C_{LOAD}$$

where R_{PU} is the on-resistance of the pull-up transistor. Notice that this pull-up transistor is modeled as a 6µA current source in the Block Diagram as a typical representation.

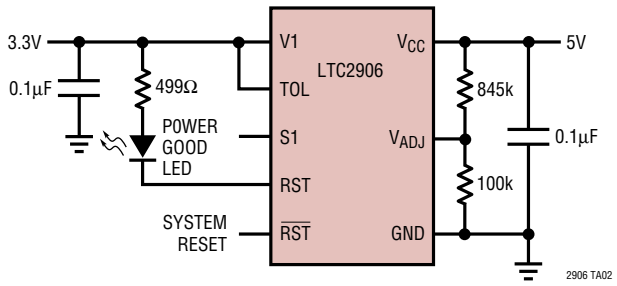
The on-resistance as a function of the V_{MAX} = MAX (V1, V_{CC}) voltage (for V_{MAX} > 1V) at room temperature is estimated as follows:

$$R_{PU} = \frac{6 \bullet 10^5}{MAX(V1, V_{CC}) - 1V} \Omega$$

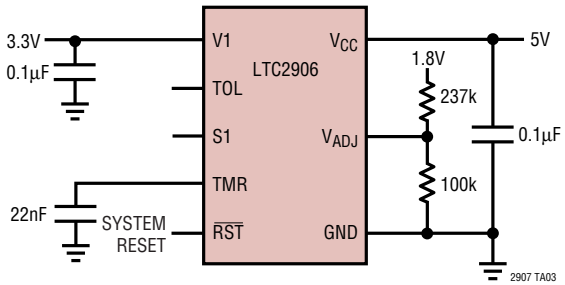
At V_{MAX} = 3.3V, R_{PU} is about 260k. Using 150pF for load capacitance, the rise time is 86µs. A smaller external pull-up resistor maybe used if the output needs to pull up faster and/or to a higher voltage. For example, the rise time reduces to 3.3µs for a 150pF load capacitance, when using a 10k pull-up resistor.

TYPICAL APPLICATIONS

5V, 3.3V Supply Monitor, 5% Tolerance with LED Power Good Indicator

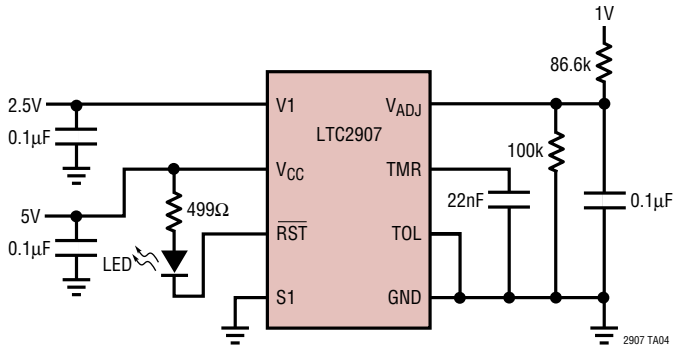


3.3V, 1.8V Monitor, 7.5% Tolerance with an Auxiliary 5V Supply (5V Not Monitored)

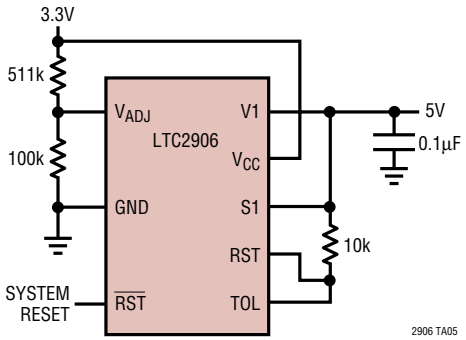


TYPICAL APPLICATIONS

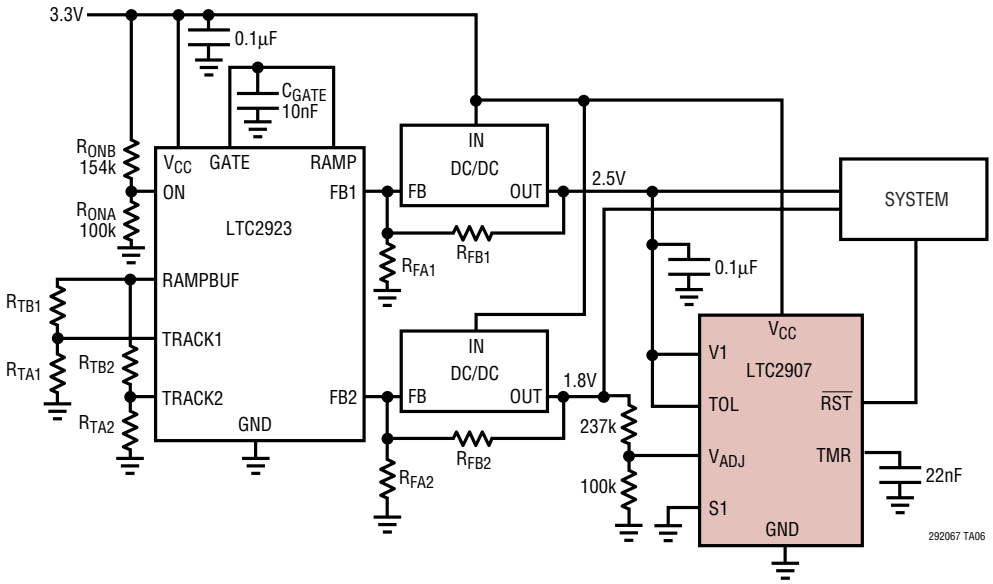
2.5V, 1V Monitor, 10% Tolerance with LED Undervoltage Indicator and 5V High Availability Auxiliary Supply (5V Not Monitored)



Dual Supply Monitor with Hysteresis, 5% Tolerance (Supplies Rising), 10% Tolerance (After RST Goes Low)

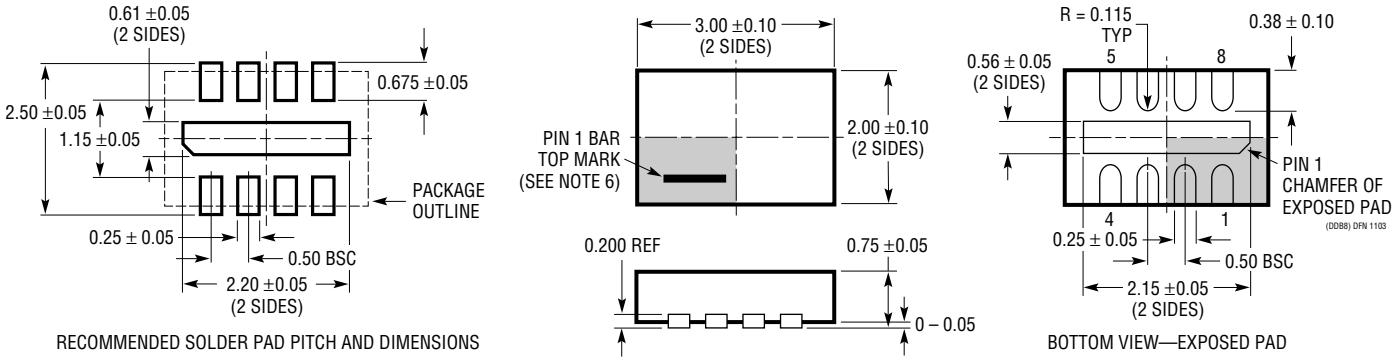


Dual Supply Monitor for Tracked/Sequenced Supply



PACKAGE DESCRIPTION

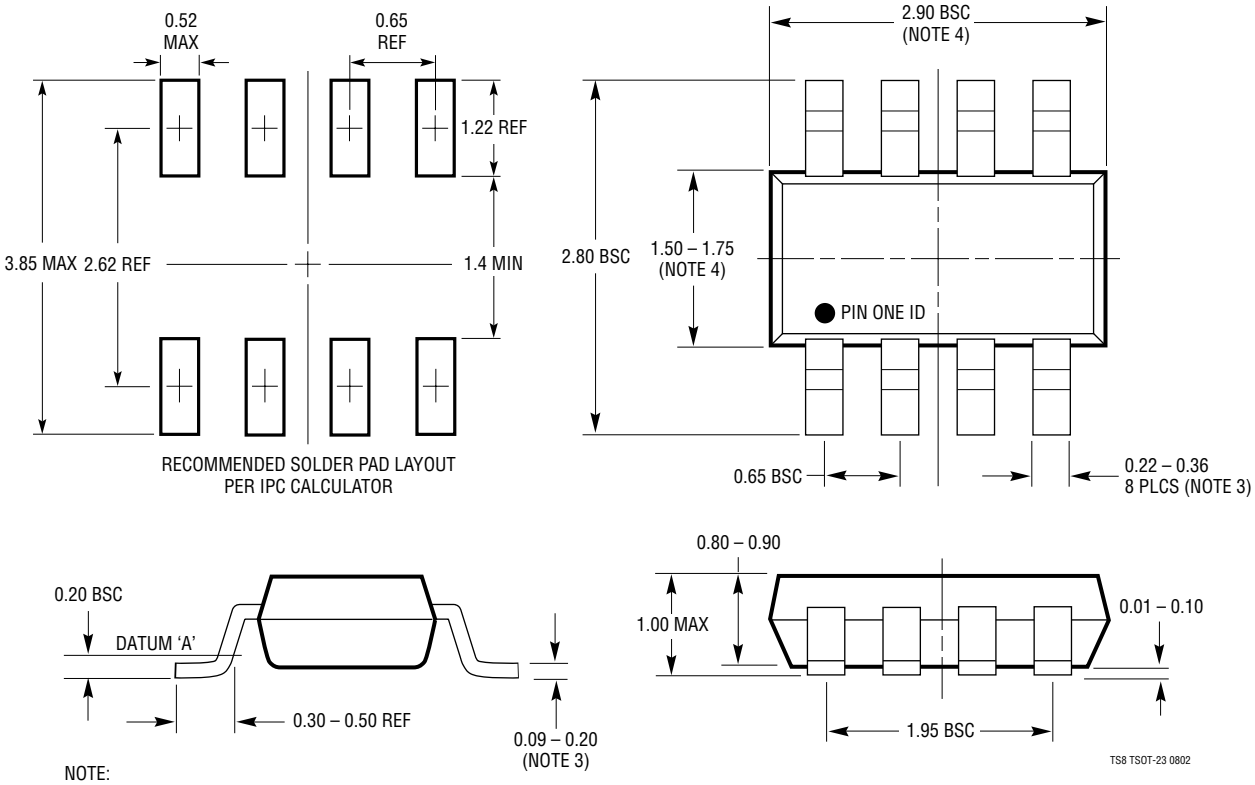
DDB Package
8-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1702)



NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

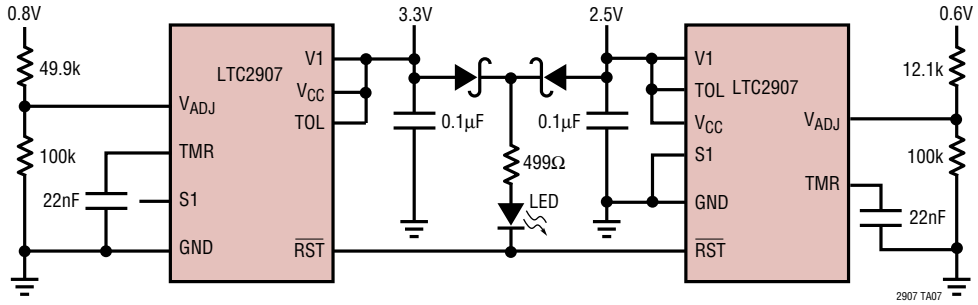
TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

TYPICAL APPLICATION

Quad Supply Monitor with LED Undervoltage Indicator, 5% Tolerance, 3.3V, 2.5V, 0.8V, 0.6V



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC690	5V Supply Monitor, Watchdog Timer and Battery Backup	4.65V Threshold
LTC694-3.3	3.3V Supply Monitor, Watchdog Timer and Battery Backup	2.9V Threshold
LTC699	5V Supply Monitor and Watchdog Timer	4.65V Threshold
LTC1232	5V Supply Monitor, Watchdog Timer and Push-Button Reset	4.37V/4.62V Threshold
LTC1326/LTC1326-2.5	Micropower Precision Triple Supply Monitor for 5V/2.5V, 3.3V and ADJ	4.725V, 3.118V, 1V Threshold (±0.75%)
LTC1536	Precision Triple Supply Monitor for PCI Applications	Meets PCI t_{FAIL} Timing Specifications
LTC1726-2.5/LTC1726-5	Micropower Triple Supply Monitor for 2.5V/5V, 3.3V and ADJ	Adjustable $\overline{\text{RESET}}$ and Watchdog Time-Outs
LTC1727-2.5/ LTC1727-5	Micropower Triple Supply Monitor with Open-Drain Reset	Individual Monitor Outputs in MSOP
LTC1728-1.8/ LTC1728-3.3	Micropower Triple Supply Monitor with Open-Drain Reset	5-Lead SOT-23 Package
LTC1728-2.5/ LTC1728-5	Micropower Triple Supply Monitor with Open-Drain Reset	5-Lead SOT-23 Package
LTC1985-1.8	Micropower Triple Supply Monitor with Push-Pull Reset Output	5-Lead SOT-23 Package
LTC2900	Programmable Quad Supply Monitor	Adjustable $\overline{\text{RESET}}$, 10-Lead MSOP and 3mm X 3mm 10-Lead DFN Packages
LTC2901	Programmable Quad Supply Monitor	Adjustable $\overline{\text{RESET}}$ and Watchdog Timer, 16-Lead SSOP Package
LTC2902	Programmable Quad Supply Monitor	Selectable Tolerance, $\overline{\text{RESET}}$ Disable for Margining Functions, 16-Lead SSOP Package
LTC2903	Precision Quad Supply Monitor	Ultralow Voltage $\overline{\text{RESET}}$, 6-Lead SOT-23 Package
LTC2904	Three-State Programmable Precision Dual Supply Monitor	Adjustable Tolerance, 8-Lead SOT-23 and 3mm × 2mm DFN Packages
LTC2905	Three-State Programmable Precision Dual Supply Monitor	Adjustable $\overline{\text{RESET}}$ and Tolerance, 8-Lead SOT-23 and 3mm × 2mm DFN Packages

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT/TP 0304 1K • PRINTED IN USA

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View LTC2907ITS8#TRMPBF on WIN SOURCE
- Linear Technology Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management