THE DATASHEET OF

LTC2902-2CGN#PBF

Programmable Quad Supply Monitor with Adjustable Reset Timer and Supply Tolerance

FEATURES

- **Simultaneously Monitors Four Supplies**
- **16 User Selectable Combinations of 5V, 3.3V, 3V, 2.5V, 1.8V, 1.5V and/or ±Adjustable Voltage Thresholds**
- **Guaranteed Threshold Accuracy: ±1.5% of Monitored Voltage Over Temperature**
- **Selectable Supply Tolerance: 5%, 7.5%, 10%, 12.5% Below Monitored Voltage**
- **Low Supply Current: 43µA Typ**
- **Adjustable Reset Time**
- **RESET Disable Pin for Margining Applications**
- Open-Drain RST Output (LTC2902-1)
- Push-Pull RST Output (LTC2902-2)
- Individual Nondelayed Monitor Outputs for Each Supply
- Power Supply Glitch Immunity
- Guaranteed RESET for $V_{CC} \geq 1V$

APPLICATIONS

- Desktop and Notebook Computers
- Multivoltage Systems
- Telecom Equipment
- Portable Battery-Powered Equipment
- Network Servers

DESCRIPTION

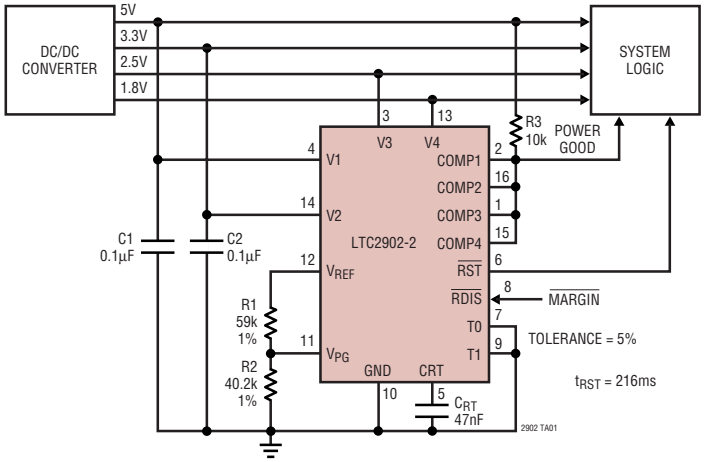
The LTC®2902 is a programmable supply monitor for systems with up to four supply voltages. One of 16 preset or adjustable voltage monitor combinations can be selected using an external resistor divider connected to the program pin. The preset voltage thresholds are digitally programmable to 5%, 7.5%, 10% or 12.5% below the nominal operating voltage, and are accurate to 1.5% over temperature. All four voltage comparator outputs are connected to separate pins for individual supply monitoring.

The reset delay time is adjustable using an external capacitor. Tight voltage threshold accuracy and glitch immunity ensure reliable reset operation without false triggering. The RST output is guaranteed to be in the correct state for V_{CC} down to 1V and may be disabled during supply margin testing. The LTC2902-1 features an open-drain RST output, while the LTC2902-2 has a push-pull RST output.

The 43µA supply current makes the LTC2902 ideal for power conscious systems and the part may be configured to monitor less than four inputs. The LTC2902-1/LTC2902-2 are available in the 16-lead narrow SSOP package.

TYPICAL APPLICATION

Quad Supply Monitor with Adjustable Tolerance (5V, 3.3V, 2.5V, 1.8V)

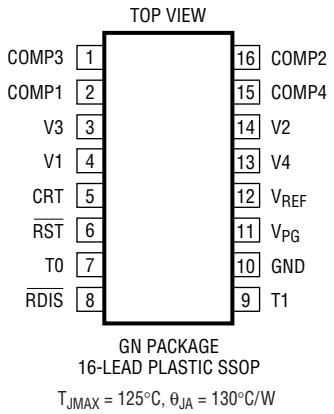


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3)

V1, V2, V3, V4, V_{PG} ..... –0.3V to 7V
$\overline{RST}$ (LTC2902-1) ..... –0.3V to 7V
$\overline{RST}$ (LTC2902-2) ..... –0.3V to (V2 + 0.3V)
COMPX, $\overline{RDIS}$ ..... –0.3V to 7V
T0, T1 ..... –0.3V to (V_{CC} + 0.3V)
CRT ..... –0.3V to (V_{CC} + 0.3V)
V_{REF} ..... –0.3V to (V_{CC} + 0.3V)
Reference Load Current (I_{VREF}) ..... ±1mA
V4 Input Current (–ADJ Mode) ..... –1mA
Operating Temperature Range
LTC2902-1C/LTC2902-2C ..... 0°C to 70°C
LTC2902-1I/LTC2902-2I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC2902-1CGN LTC2902-2CGN LTC2902-1IGN LTC2902-2IGN
GN16 PART MARKING
29021 29022 29021I 29022I

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{RT50}	5V, 5% Reset Threshold	V1 Input Threshold	●	4.600	4.675	4.750	V
	5V, 7.5% Reset Threshold		●	4.475	4.550	4.625	V
	5V, 10% Reset Threshold		●	4.350	4.425	4.500	V
	5V, 12.5% Reset Threshold		●	4.225	4.300	4.375	V
V_{RT33}	3.3V, 5% Reset Threshold	V1, V2 Input Threshold	●	3.036	3.086	3.135	V
	3.3V, 7.5% Reset Threshold		●	2.954	3.003	3.053	V
	3.3V, 10% Reset Threshold		●	2.871	2.921	2.970	V
	3.3V, 12.5% Reset Threshold		●	2.789	2.838	2.888	V
V_{RT30}	3V, 5% Reset Threshold	V2 Input Threshold	●	2.760	2.805	2.850	V
	3V, 7.5% Reset Threshold		●	2.685	2.730	2.775	V
	3V, 10% Reset Threshold		●	2.610	2.655	2.700	V
	3V, 12.5% Reset Threshold		●	2.535	2.580	2.625	V
V_{RT25}	2.5V, 5% Reset Threshold	V2, V3 Input Threshold	●	2.300	2.338	2.375	V
	2.5V, 7.5% Reset Threshold		●	2.238	2.275	2.313	V
	2.5V, 10% Reset Threshold		●	2.175	2.213	2.250	V
	2.5V, 12.5% Reset Threshold		●	2.113	2.150	2.188	V
V_{RT18}	1.8V, 5% Reset Threshold	V3, V4 Input Threshold	●	1.656	1.683	1.710	V
	1.8V, 7.5% Reset Threshold		●	1.611	1.638	1.665	V
	1.8V, 10% Reset Threshold		●	1.566	1.593	1.620	V
	1.8V, 12.5% Reset Threshold		●	1.521	1.548	1.575	V
V_{RT15}	1.5V, 5% Reset Threshold	V3, V4 Input Threshold	●	1.380	1.403	1.425	V
	1.5V, 7.5% Reset Threshold		●	1.343	1.365	1.388	V
	1.5V, 10% Reset Threshold		●	1.305	1.328	1.350	V
	1.5V, 12.5% Reset Threshold		●	1.268	1.290	1.313	V
V_{RTA}	ADJ, 5% Reset Threshold	V3, V4 Input Threshold	●	0.492	0.500	0.508	V
	ADJ, 7.5% Reset Threshold		●	0.479	0.487	0.494	V
	ADJ, 10% Reset Threshold		●	0.466	0.473	0.481	V
	ADJ, 12.5% Reset Threshold		●	0.453	0.460	0.467	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{RTAN}	–ADJ Reset Threshold	V4 Input Threshold	●	–18	0	18	mV
V_{CC}	Minimum Internal Operating Voltage	$\overline{RST}$, COMPX in Correct Logic State; V_{CC} Rising Prior to Program	●			1	V
V_{CCMINP}	Minimum Required for Programming	V_{CC} Rising	●			2.42	V
V_{CCMINC}	Minimum Required for Comparators	V_{CC} Falling	●			2.32	V
V_{REF}	Reference Voltage	$V_{CC} \geq 2.3V$, $I_{VREF} = \pm 1mA$, $C_{REF} \leq 1000pF$					
		T0 Low, T1 Low	●	1.192	1.210	1.228	V
		T0 Low, T1 High	●	1.160	1.178	1.195	V
		T0 High, T1 Low	●	1.128	1.146	1.163	V
		T0 High, T1 High	●	1.096	1.113	1.130	V
V_{PG}	Programming Voltage Range	$V_{CC} \geq V_{CCMINP}$	●	0		V_{REF}	V
I_{VPG}	V_{PG} Input Current	$V_{PG} = V_{REF}$	●			±20	nA
I_{V1}	V1 Input Current	V1 = 5V, I_{VREF} = 12µA, (Note 4)	●		43	75	µA
I_{V2}	V2 Input Current	V2 = 3.3V	●		0.8	2	µA
I_{V3}	V3 Input Current	V3 = 2.5V	●		0.52	1.2	µA
		V3 = 0.55V (ADJ Mode)		–15		15	nA
I_{V4}	V4 Input Current	V4 = 1.8V	●		0.34	0.8	µA
		V4 = 0.55V (ADJ Mode)	●	–15		15	nA
		V4 = –0.05V (–ADJ Mode)	●	–15		15	nA
$I_{CRT(UP)}$	CRT Pull-Up Current	V_{CRT} = 0V	●	–1.4	–2	–2.6	µA
$I_{CRT(DN)}$	CRT Pull-Down Current	V_{CRT} = 1.3V	●	10	20	30	µA
t_{RST}	Reset Time-Out Period	C_{RT} = 1500pF	●	5	7	9	ms
t_{UV}	V_X Undervoltage Detect to $\overline{RST}$ or COMPX	V_X Less Than Reset Threshold V_{RTX} by More Than 1%			150		µs
V_{OL}	Output Voltage Low $\overline{RST}$, COMPX	I_{SINK} = 2.5mA; V1 = 3V, V2 = 3V; V3, V4 = 0V; V_{PG} = 0V	●		0.15	0.4	V
		I_{SINK} = 100µA; V2 = 1V; V1, V3, V4 = 0V	●		0.05	0.3	V
		I_{SINK} = 100µA; V1 = 1V; V2, V3, V4 = 0V	●		0.05	0.3	V
V_{OH}	Output Voltage High $\overline{RST}$, COMPX (Note 5)	I_{SOURCE} = 1µA	●	V2 – 1			V
V_{OH}	Output Voltage High $\overline{RST}$ (LTC2902-2) (Note 6)	I_{SOURCE} = 200µA	●	0.8 • V2			V
Digital Inputs T0, T1, $\overline{RDIS}$							
V_{IL}	T0, T1 Low Level Input Voltage	V_{CC} = 3.3V to 5.5V	●			$0.3V_{CC}$	V
V_{IH}	T0, T1 High Level Input Voltage	V_{CC} = 3.3V to 5.5V	●	$0.7V_{CC}$			V
I_{INTOL}	T0, T1 Input Current	T0 = 0V, T1 = V_{CC}	●		±0.1	±1	µA
V_{IL}	$\overline{RDIS}$ Input Threshold Low	V_{CC} = 3.3V to 5.5V	●	0.4			V
V_{IH}	$\overline{RDIS}$ Input Threshold High	V_{CC} = 3.3V to 5.5V	●			1.6	V
I_{RDIS}	$\overline{RDIS}$ Pull-Up Current	V_{RDIS} = 0V			–10		µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: The greater of V1, V2 is the internal supply voltage (V_{CC}).

Note 4: Under static no-fault conditions, V1 will necessarily supply quiescent current. If at any time V2 is larger than V1, V2 must be capable of supplying the quiescent current, programming (transient) current and reference load current.

Note 5: The output pins $\overline{RST}$ and COMPX have internal pull-ups to V2 of typically 6µA. However, external pull-up resistors may be used when faster rise times are required or for V_{OH} voltages greater than V2.

Note 6: The push-pull $\overline{RST}$ output pin on the LTC2902-2 is *actively* pulled up to V2.

TEST CIRCUITS

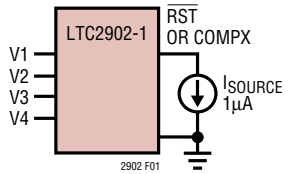


Figure 1. $\overline{RST}$, COMPX V_{OH} Test

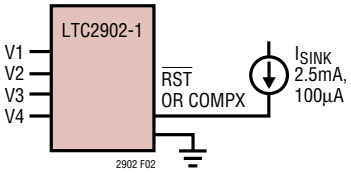


Figure 2. $\overline{RST}$, COMPX V_{OL} Test

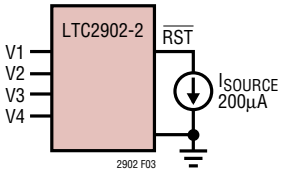
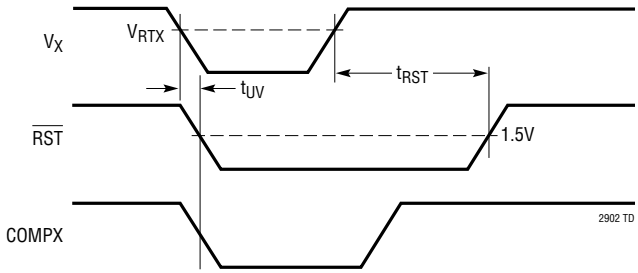


Figure 3. Active Pull-Up $\overline{RST}$ V_{OH} Test

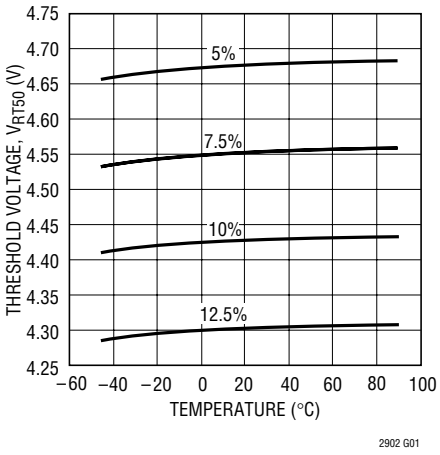
TIMING DIAGRAM

V_X Monitor Timing

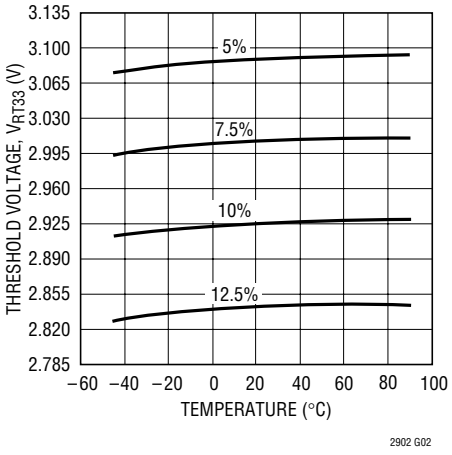


TYPICAL PERFORMANCE CHARACTERISTICS

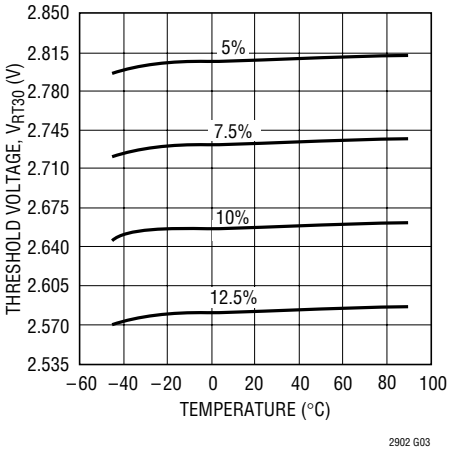
5V Threshold Voltage vs Temperature



3.3V Threshold Voltage vs Temperature

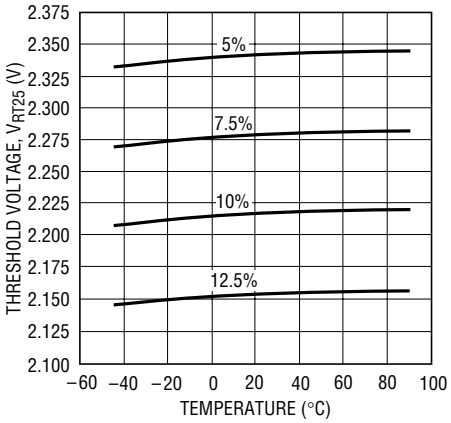


3V Threshold Voltage vs Temperature

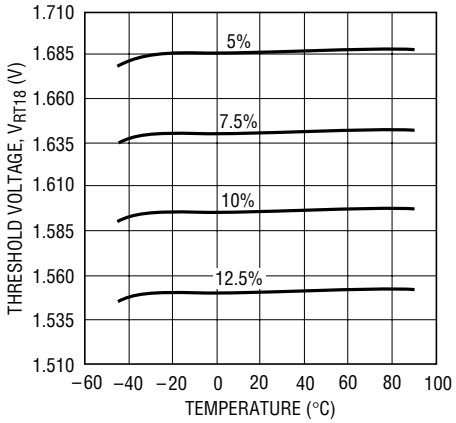


TYPICAL PERFORMANCE CHARACTERISTICS

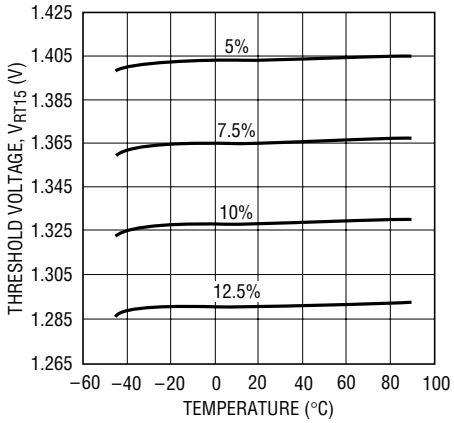
2.5V Threshold Voltage vs Temperature



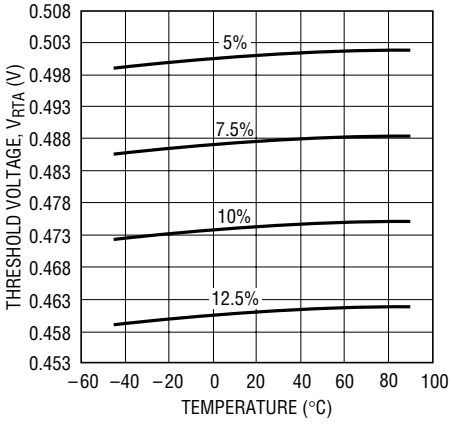
1.8V Threshold Voltage vs Temperature



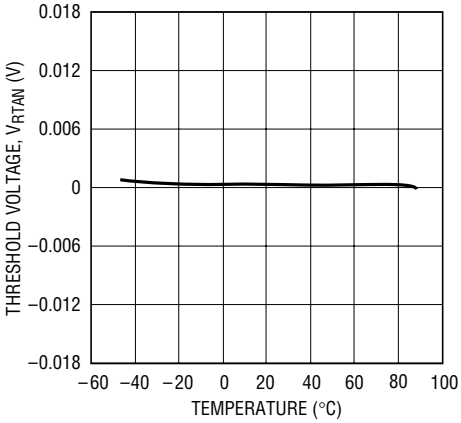
1.5V Threshold Voltage vs Temperature



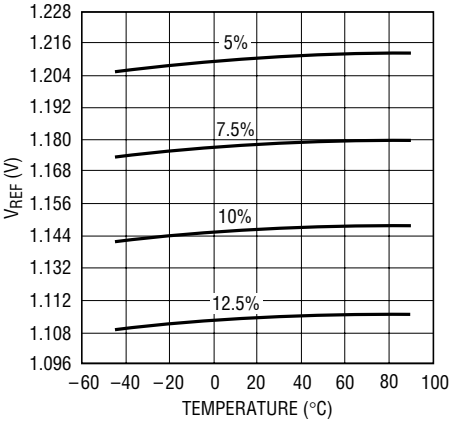
ADJ Threshold Voltage vs Temperature



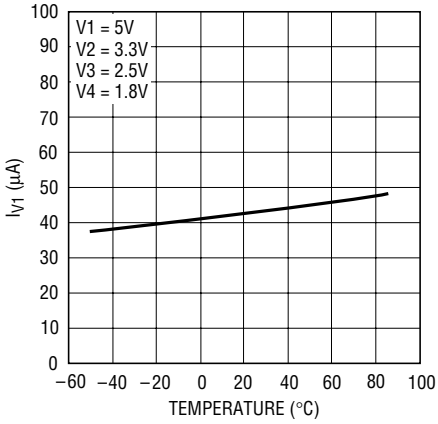
–ADJ Threshold Voltage vs Temperature



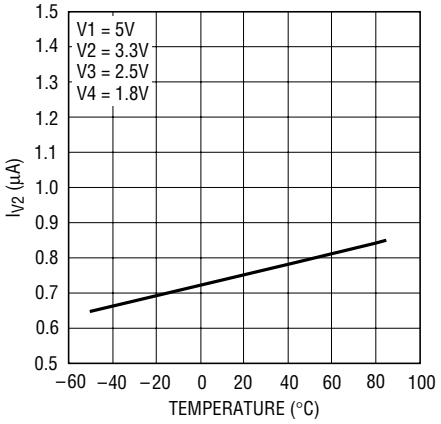
V_{REF} vs Temperature



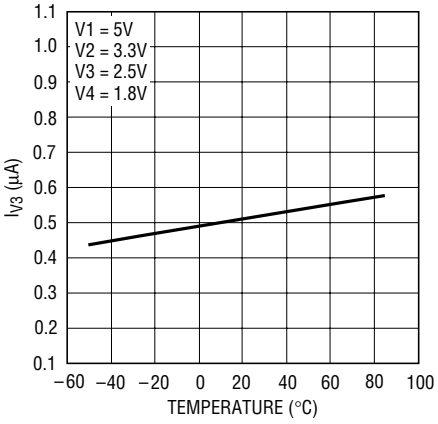
I_{V1} vs Temperature



I_{V2} vs Temperature

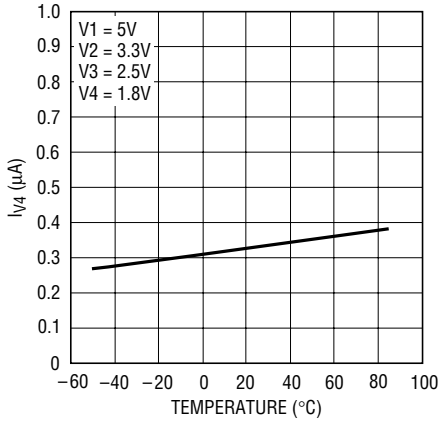


I_{V3} vs Temperature



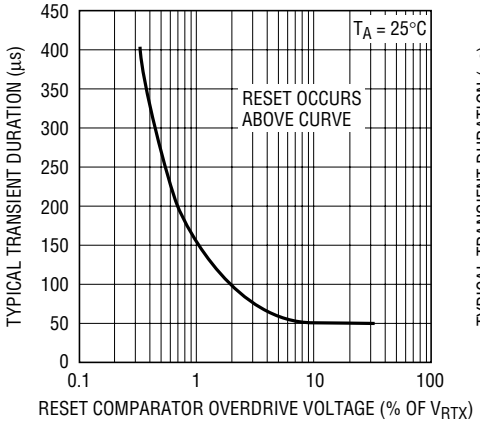
TYPICAL PERFORMANCE CHARACTERISTICS

I_{V4} vs Temperature



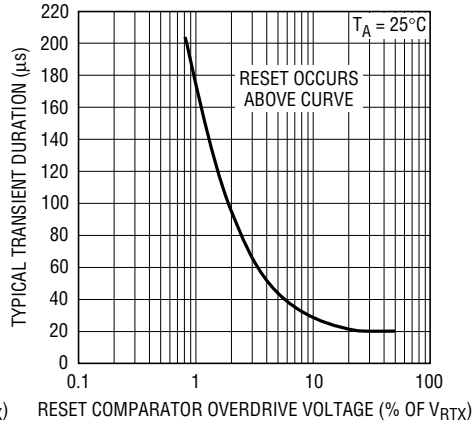
2902 G13

Typical Transient Duration vs Comparator Overdrive (V1, V2)



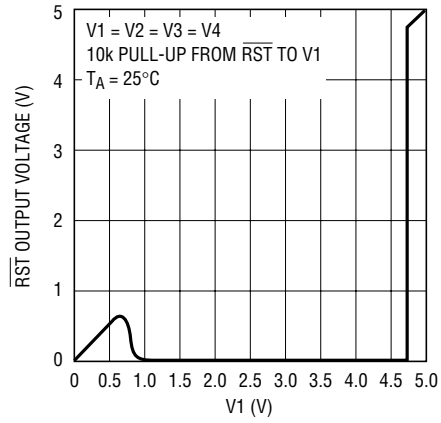
2902 G14

Typical Transient Duration vs Comparator Overdrive (V3, V4)



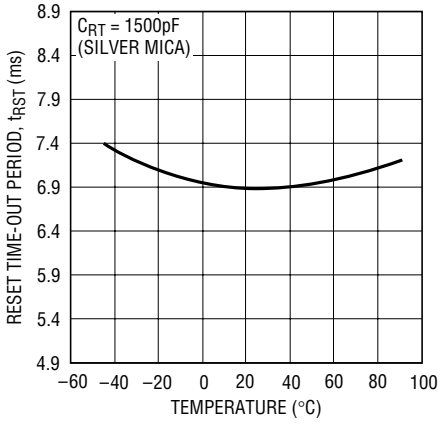
2902 G25

$\overline{RST}$ Output Voltage vs V1, V_{PG} = 0V



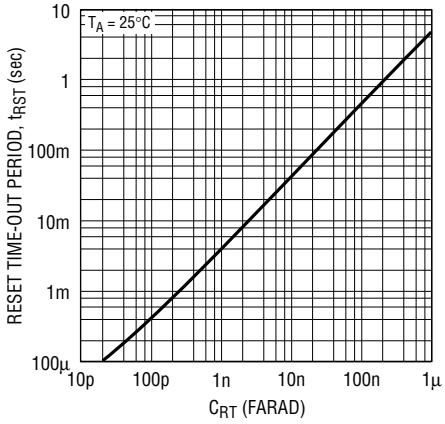
2902 G15

Reset Time-Out Period vs Temperature



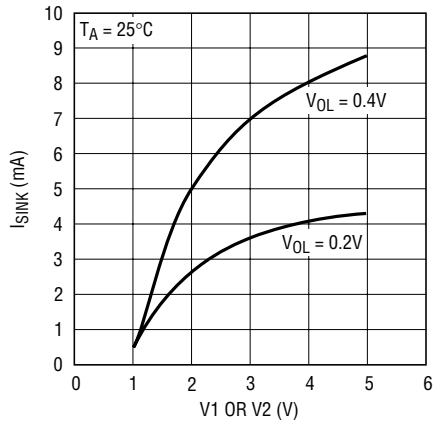
2902 G16

Reset Time-Out Period vs Capacitance



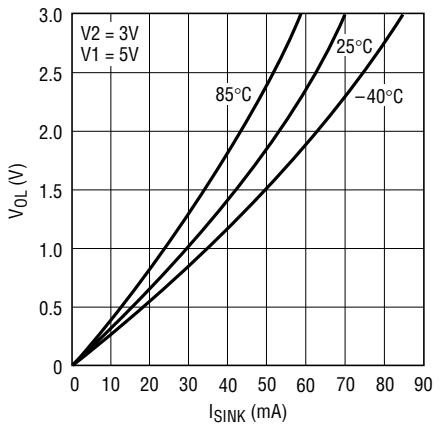
2902 G17

$\overline{RST}$, COMPX I_{SINK} vs Supply Voltage



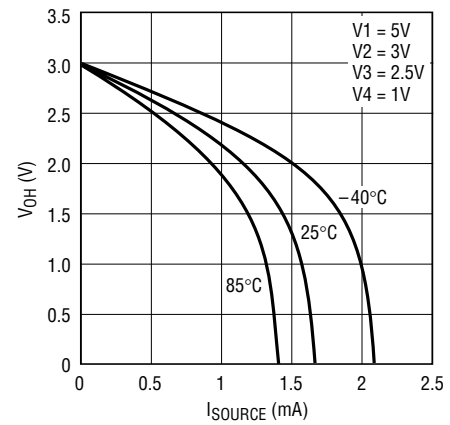
2902 G18

$\overline{RST}$, COMPX Voltage Output Low vs Output Sink Current



2902 G19

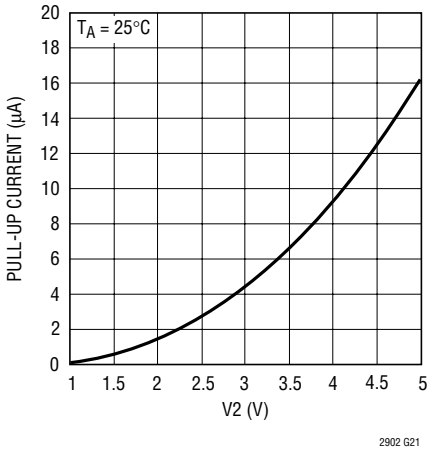
$\overline{RST}$ High Level Output Voltage vs Output Source Current (LTC2902-2)



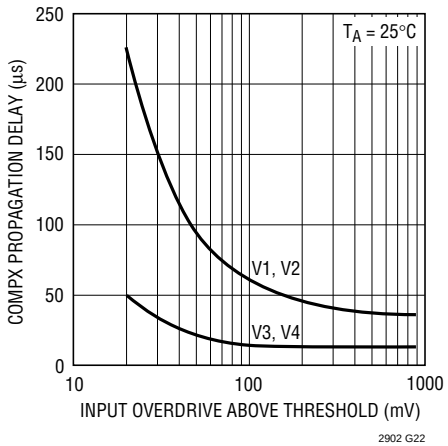
2902 G20

TYPICAL PERFORMANCE CHARACTERISTICS

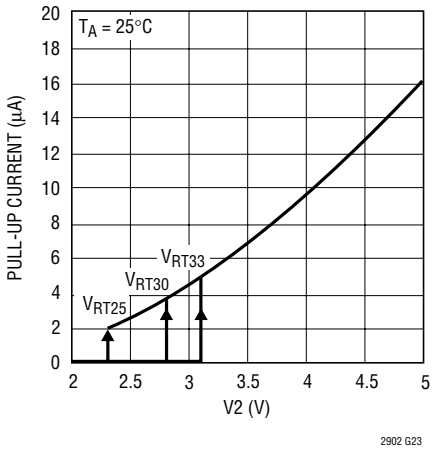
COMPX Pull-Up Current vs V2 (COMPX Held at 0V)



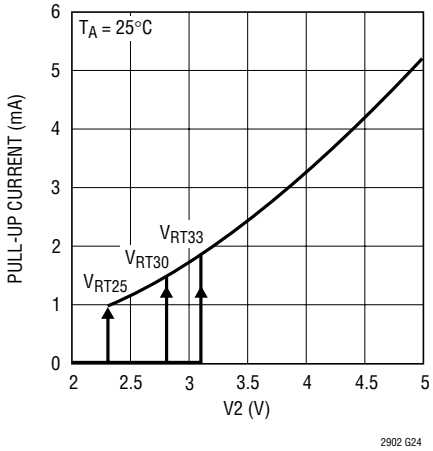
COMPX Propagation Delay vs Input Overdrive Above Threshold



$\overline{RST}$ Pull-Up Current vs V2 (LTC2902-1)



$\overline{RST}$ Pull-Up Current vs V2 (LTC2902-2)



PIN FUNCTIONS

COMP3 (Pin 1): Comparator Output 3. Nondelayed, active high logic output with weak pull-up to V2. Pulls high when V3 is above reset threshold. May be pulled greater than V2 using external pull-up.

COMP1 (Pin 2): Comparator Output 1. Nondelayed, active high logic output with weak pull-up to V2. Pulls high when V1 is above reset threshold. May be pulled greater than V2 using external pull-up.

V3 (Pin 3): Voltage Input 3. Select from 2.5V, 1.8V, 1.5V or ADJ. See Table 1 for details.

V1 (Pin 4): Voltage Input 1. Select from 5V or 3.3V. See Table 1 for details. The greater of (V1, V2) is also V_{CC} for the chip. Bypass this pin to ground with a 0.1µF (or greater) capacitor.

CRT (Pin 5): Reset Delay Time Programming Pin. Attach an external capacitor (C_{RT}) to GND to set a reset delay time of 4.6ms/nF. Leaving the pin open generates a minimum delay of approximately 50µs. A 47nF capacitor will generate a 216ms reset delay time.

PIN FUNCTIONS

$\overline{\text{RST}}$ (Pin 6): Reset Logic Output. Active low with weak pull-up to V2 (LTC2902-1) or active pull-up to V2 (LTC2902-2). Pulls low when any voltage input is below the reset threshold and held low for programmed delay time after all voltage inputs are above threshold. May be pulled above V2 using an external pull-up (LTC2902-1 only).

T0 (Pin 7): Digital Input for Supply Tolerance Selection (5%, 7.5%, 10% or 12.5%). Used in conjunction with T1 (Pin 9). See Applications Information for tolerance selection chart (Table 4).

$\overline{\text{RDIS}}$ (Pin 8): Digital Input for $\overline{\text{RST}}$ Disable. A low input on this pin forces the $\overline{\text{RST}}$ output to V2 (or pull-up voltage). Useful for determining supply margins without issuing reset command to processor. A weak internal pull-up allows pin to be left floating for normal monitor operation.

T1 (Pin 9): Digital Input for Supply Tolerance Selection (5%, 7.5%, 10% or 12.5%). Used in conjunction with T0 (Pin 7). See Applications Information for tolerance selection chart (Table 4).

GND (Pin 10): Ground.

V_{PG} (Pin 11): Voltage Threshold Combination Select Input. Connect to an external 1% resistive divider between V_{REF} and GND to select 1 of 16 combinations of preset and/or ±adjustable voltage thresholds (see Table 1). Do not add capacitance on the V_{PG} pin.

V_{REF} (Pin 12): Buffered Reference Voltage. A 1.210V nominal reference used for programming voltage (V_{PG}) and for the offset of negative adjustable applications. The buffered reference can source and sink up to 1mA. The reference can drive a bypass capacitor of up to 1000pF without oscillation.

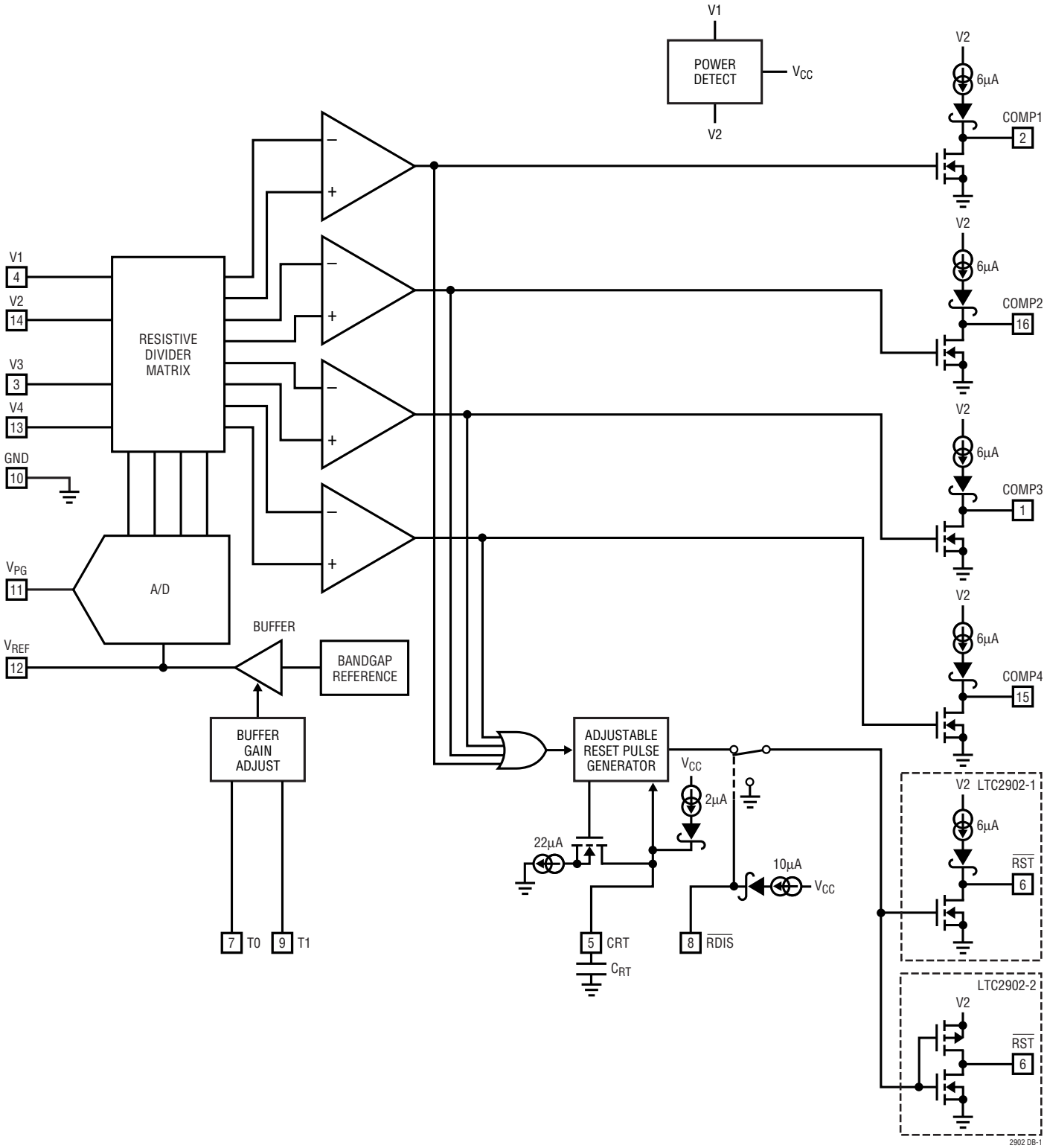
V4 (Pin 13): Voltage Input 4. Select from 1.8V, 1.5V, ADJ or –ADJ. See Table 1 for details.

V2 (Pin 14): Voltage Input 2. Select from 3.3V, 3V or 2.5V. See Table 1 for details. The greater of (V1, V2) is also V_{CC} for chip. Bypass this pin to ground with a 0.1µF (or greater) capacitor. All logic outputs (COMP1, COMP2, COMP3, COMP4) are weakly pulled up to V2. $\overline{\text{RST}}$ is weakly pulled up to V2 in the LTC2902-1 and $\overline{\text{RST}}$ is actively pulled up to V2 in the LTC2902-2.

COMP4 (Pin 15): Comparator Output 4. Nondelayed, active high logic output with weak pull-up to V2. Pulls high when V4 is above reset threshold. May be pulled greater than V2 using external pull-up.

COMP2 (Pin 16): Comparator Output 2. Nondelayed, active high logic output with weak pull-up to V2. Pulls high when V2 is above reset threshold. May be pulled greater than V2 using external pull-up.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Power-Up

On power-up, the larger of V1 or V2 will power the drive circuits for the $\overline{RST}$ and the COMPX pins. This ensures that the $\overline{RST}$ and COMPX outputs will be low as soon as V1 or V2 reaches 1V. The $\overline{RST}$ and COMPX outputs will remain low until the part is programmed. After programming, if any one of the V_X inputs is below its programmed threshold, $\overline{RST}$ will be a logic low. Once all the V_X inputs rise above their thresholds, an internal timer is started and $\overline{RST}$ is released after the programmed delay time. If V_{CC} < (V3 – 1) and V_{CC} < 2.4V, the V3 input impedance will be low (1kΩ typ).

Monitor Programming

The LTC2902 input voltage combination is selected by placing the recommended resistor divider from V_{REF} to GND and connecting the tap point to V_{PG}, as shown in Figure 4. Table 1 offers recommended 1% resistor values for the various modes. The last column in Table 1 specifies optimum V_{PG}/V_{REF} ratios (±0.01) to be used when programming with a ratiometric DAC.

During power-up, once V1 or V2 reaches 2.4V (max), the monitor enters a programming period of approximately 150µs during which the voltage on the V_{PG} pin is sampled and the monitor is configured to the desired input combination. Do not add capacitance to the V_{PG} pin. Immediately after programming, the comparators are enabled and supply monitoring will begin.

Supply Monitoring

The LTC2902 is a low power, high accuracy programmable quad supply monitoring circuit with four nondelayed monitor outputs, a common reset output and selectable supply thresholds. Reset timing is adjustable using an external capacitor. Single pin programming selects 1 of 16 input voltage monitor combinations. Two digital inputs select one of four supply tolerances (5%, 7.5%, 10% or 12.5%). All four voltage inputs must be above predetermined thresholds for the reset not to be invoked. The LTC2902 will assert the reset and comparator outputs during power-up, power-down and brownout conditions on any one of the voltage inputs.

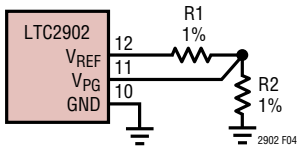


Figure 4. Monitor Programming

Table 1. Voltage Threshold Programming

MODE	V1 (V)	V2 (V)	V3 (V)	V4 (V)	R1 (kΩ)	R2 (kΩ)	$\frac{V_{PG}}{V_{REF}}$
0	5.0	3.3	ADJ	ADJ	Open	Short	0.000
1	5.0	3.3	ADJ	–ADJ	93.1	9.53	0.094
2	3.3	2.5	ADJ	ADJ	86.6	16.2	0.156
3	3.3	2.5	ADJ	–ADJ	78.7	22.1	0.219
4	3.3	2.5	1.5	ADJ	71.5	28.0	0.281
5	5.0	3.3	2.5	ADJ	66.5	34.8	0.344
6	5.0	3.3	2.5	1.8	59.0	40.2	0.406
7	5.0	3.3	2.5	1.5	53.6	47.5	0.469
8	5.0	3.0	2.5	ADJ	47.5	53.6	0.531
9	5.0	3.0	ADJ	ADJ	40.2	59.0	0.594
10	3.3	2.5	1.8	1.5	34.8	66.5	0.656
11	3.3	2.5	1.8	ADJ	28.0	71.5	0.719
12	3.3	2.5	1.8	–ADJ	22.1	78.7	0.781
13	5.0	3.3	1.8	–ADJ	16.2	86.6	0.844
14	5.0	3.3	1.8	ADJ	9.53	93.1	0.906
15	5.0	3.0	1.8	ADJ	Short	Open	1.000

The inverting inputs on the V3 and/or V4 comparators are set to 0.5V when the positive adjustable modes are selected and with T0 and T1 low (5% tolerance) (Figure 5). The tap point on an external resistive divider, connected between the positive voltage being sensed and ground, is connected to the high impedance noninverting inputs (V3, V4). The trip voltage is calculated from:

$$V_{TRIP} = 0.5V\left(1+\frac{R3}{R4}\right)$$

Once the resistor divider is set in the 5% tolerance mode, there is no need to change the divider for the other tolerance modes (7.5%, 10%, 12.5%) because the internal reference is scaled accordingly, moving the trip point in –2.5% increments.

APPLICATIONS INFORMATION

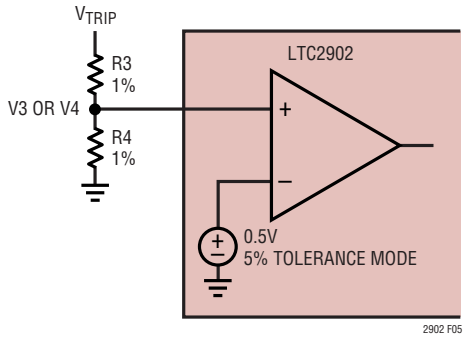


Figure 5. Setting the Positive Adjustable Trip Point

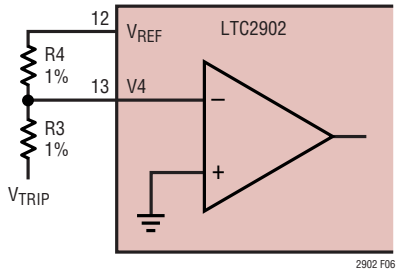


Figure 6. Setting the Negative Adjustable Trip Point

In the negative adjustable mode, the noninverting input on the V4 comparator is connected to ground (Figure 6). The tap point on an external resistive divider, connected between the negative voltage being sensed and the V_{REF} pin, is connected to the high impedance inverting input (V4). V_{REF} provides the necessary level shift required to operate at ground. The trip voltage is calculated from:

$$V_{TRIP} = -V_{REF}\left(\frac{R3}{R4}\right); V_{REF} = 1.210V$$

T0,T1 Low (5% Tolerance Mode)

Once the resistor divider is set in the 5% tolerance mode, there is no need to change the divider for the other tolerance modes (7.5%, 10%, 12.5%) because V_{REF} is scaled accordingly, moving the trip point in –2.5% increments.

In a negative adjustable application, the minimum value for R4 is limited by the sourcing capability of V_{REF} (±1mA). With no other load on V_{REF}, R4 (minimum) is:

1.21V ÷ 1mA = 1.21kΩ

Tables 2 and 3 offer suggested 1% resistor values for various adjustable applications.

Table 2. Suggested 1% Resistor Values for the ADJ Inputs

V_{SUPPLY} (V)	V_{TRIP} (V)	R3 (kΩ)	R4 (kΩ)
12	11.25	2150	100
10	9.4	1780	100
8	7.5	1400	100
7.5	7	1300	100
6	5.6	1020	100
5	4.725	845	100
3.3	3.055	511	100
3	2.82	464	100
2.5	2.325	365	100
1.8	1.685	237	100
1.5	1.410	182	100
1.2	1.120	124	100
1	0.933	86.6	100
0.9	0.840	68.1	100

Table 3. Suggested 1% Resistor Values for the –ADJ Input

V_{SUPPLY} (V)	V_{TRIP} (V)	R3 (kΩ)	R4 (kΩ)
–2	–1.87	187	121
–5	–4.64	464	121
–5.2	–4.87	487	121
–10	–9.31	931	121
–12	–11.30	1130	121

Although all four supply monitor comparators have built-in glitch immunity, bypass capacitors on V1 and V2 are recommended because the greater of V1 or V2 is also the V_{CC} for the chip. Filter capacitors on the V3 and V4 inputs are allowed.

Power-Down

On power-down, once any of the V_X inputs drop below their threshold, $\overline{RST}$ and COMPX are held at a logic low. A logic low of 0.4V is guaranteed until both V1 and V2 drop below 1V. If the bandgap reference becomes invalid (V_{CC} < 2V typ), the part will reprogram once V_{CC} rises above 2.4V (max).

Monitor Output Rise and Fall Time Estimation

All of the outputs ($\overline{RST}$, COMPX) have strong pull-down capability. If the external load capacitance (C_{LOAD}) for a

APPLICATIONS INFORMATION

particular output is known, output fall time (10% to 90%) is estimated using:

$$t_{FALL} \approx 2.2 \bullet R_{PD} \bullet C_{LOAD}$$

where R_{PD} is the on-resistance of the internal pull-down transistor. The typical performance curve (V_{OL} vs I_{SINK}) demonstrates that the pull-down current is somewhat linear versus output voltage. Using the 25°C curve, R_{PD} is estimated to be approximately 40Ω. Assuming a 150pF load capacitance, the fall time is about 13.2ns.

Although the outputs are considered to be "open-drain," they do have a weak pull-up capability (see COMPX or $\overline{RST}$ Pull-Up Current vs V2 curve). Output rise time (10% to 90%) is estimated using:

$$t_{RISE} \approx 2.2 \bullet R_{PU} \bullet C_{LOAD}$$

where R_{PU} is the on-resistance of the pull-up transistor. The on-resistance as a function of the V2 voltage at room temperature is estimated using:

$$R_{PU} = \frac{6 \bullet 10^5}{V2 - 1} \Omega$$

with V2 = 3.3V, R_{PU} is about 260k. Using 150pF for load capacitance, the rise time is 86µs. If the output needs to pull up faster and/or to a higher voltage, a smaller external pull-up resistor may be used. Using a 10k pull-up resistor, the rise time is reduced to 3.3µs for a 150pF load capacitance.

The LTC2902-2 has an active pull-up to V2 on the $\overline{RST}$ output. The typical performance curve ($\overline{RST}$ Pull-Up Current vs V2 curve) demonstrates that the pull-up current is somewhat linear versus the V2 voltage and R_{PU} is estimated to be approximately 625Ω. A 150pF load capacitance makes the rise time about 206ns.

Selecting the Reset Timing Capacitor

The reset time-out period is adjustable in order to accommodate a variety of microprocessor applications. The reset time-out period, t_{RST}, is adjusted by connecting a capacitor, C_{RT}, between the CRT pin and ground. The value of this capacitor is determined by:

$$C_{RT} = t_{RST} \bullet 217 \bullet 10^{-9}$$

with C_{RT} in Farads and t_{RST} in seconds. The C_{RT} value per millisecond of delay can also be expressed as C_{RT}/ms = 217 (pF/ms).

Leaving the CRT pin unconnected will generate a minimum reset time-out of approximately 50µs. Maximum reset time-out is limited by the largest available low leakage capacitor. The accuracy of the time-out period will be affected by capacitor leakage (the nominal charging current is 2µA) and capacitor tolerance. A low leakage ceramic capacitor is recommended.

Tolerance Programming and the RESET Disable

Using the two digital inputs T0 and T1, the user can program the global supply tolerance for the LTC2902 (5%, 7.5%, 10%, 12.5%). The larger tolerances provide more headroom by lowering the trip thresholds.

Table 4. Tolerance Programming

T0	T1	TOLERANCE (%)	V_{REF} (V)
Low	Low	5	1.210
Low	High	7.5	1.178
High	Low	10	1.146
High	High	12.5	1.113

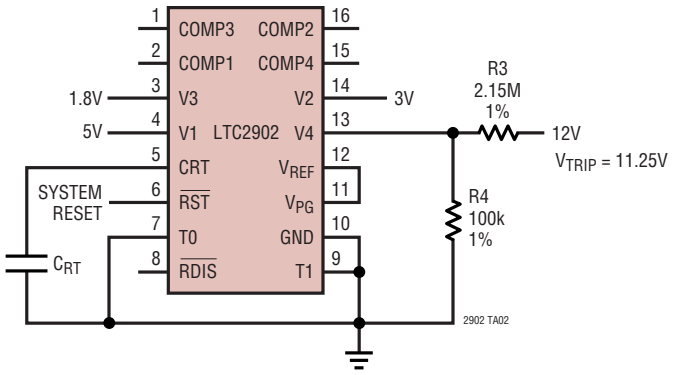
Under conventional operation, $\overline{RST}$ and COMPX will go low when V_X is below its threshold. At any time, the $\overline{RDIS}$ pin can be pulled low, overriding the reset operation and forcing the $\overline{RST}$ pin high. This feature is useful when determining supply margins under processor control since the reset command will not be invoked. The $\overline{RDIS}$ pin is connected to a weak internal pull-up to V_{CC} (10µA typ), allowing the pin to be left floating if unused.

Ensuring $\overline{RST}$ Valid for V_{CC} Down to 0V (LTC2902-2)

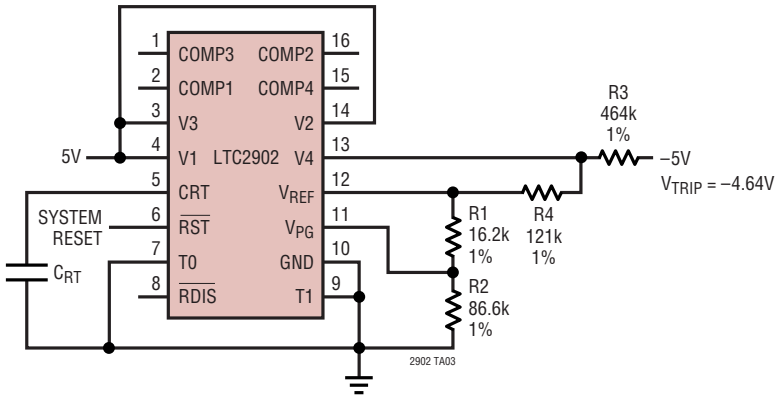
When V_{CC} is below 1V the $\overline{RST}$ pull-down capability is drastically reduced. The $\overline{RST}$ pin may float to undetermined voltages when connected to high impedance (such as CMOS logic inputs). The addition of a pull-down resistor from $\overline{RST}$ to ground will provide a path for stray charge and/or leakage currents. The resistor value should be small enough to provide effective pull-down without excessively loading the pull-up circuitry. Too large a value may not pull down well enough. A 100k resistor from $\overline{RST}$ to ground is satisfactory for most applications.

TYPICAL APPLICATIONS

Quad Supply Monitor, 5% Tolerance
5V, 3V, 1.8V, 12V (ADJ)

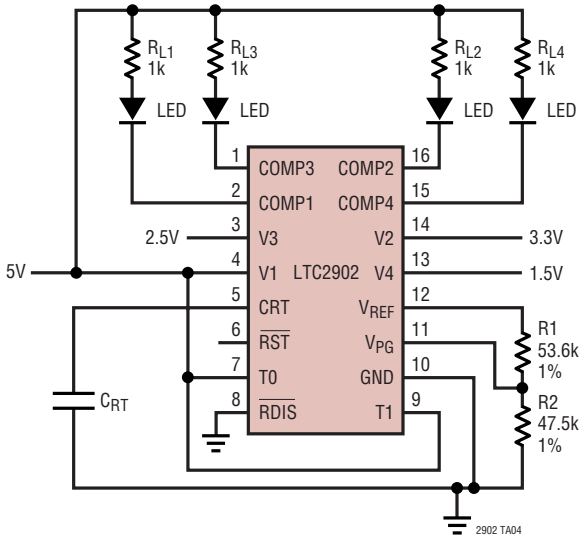


5V, –5V Monitor with Unused V2, V3 Inputs Pulled Above Trip Thresholds (5% Tolerance)



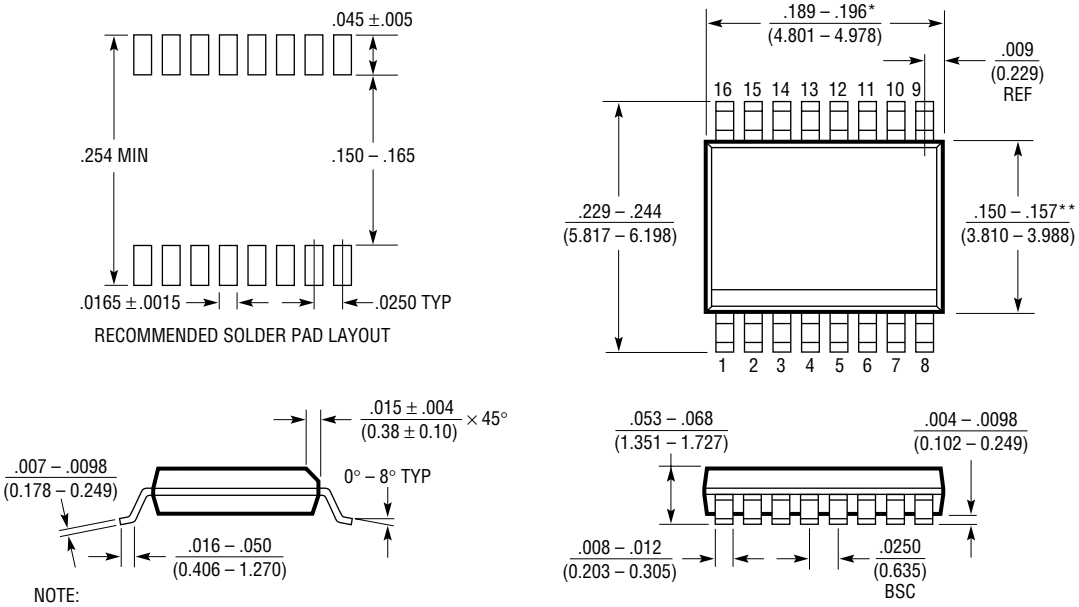
TYPICAL APPLICATIONS

Quad Supply Monitor with LED Undervoltage Indicators, 12.5% Tolerance, Reset Disabled 5V, 3.3V, 2.5V, 1.5V



PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

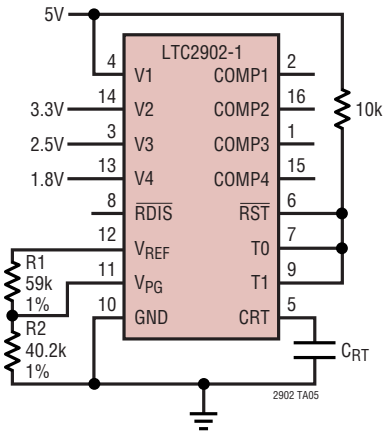
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 0502

TYPICAL APPLICATION

Quad Supply Monitor with Hysteresis
5% Tolerance (Supplies Rising)
12.5% Tolerance (After $\overline{RST}$ Goes High)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC690	5V Supply Monitor, Watchdog Timer and Battery Backup	4.65V Threshold
LTC694-3.3	3.3V Supply Monitor, Watchdog Timer and Battery Backup	2.9V Threshold
LTC699	5V Supply Monitor and Watchdog Timer	4.65V Threshold
LTC1232	5V Supply Monitor, Watchdog Timer and Push-Button Reset	4.37V/4.62V Threshold
LTC1326	Micropower Precision Triple Supply Monitor for 5V, 3.3V and ADJ	4.725V, 3.118V, 1V Thresholds (±0.75%)
LTC1326-2.5	Micropower Precision Triple Supply Monitor for 2.5V, 3.3V and ADJ	2.363V, 3.118V, 1V Thresholds (±0.75%)
LTC1536	Precision Triple Supply Monitor for PCI Applications	Meets PCI t_{FAIL} Timing Specifications
LTC1726-2.5	Micropower Triple Supply Monitor for 2.5V, 3.3V and ADJ	Adjustable $\overline{RESET}$ and Watchdog Time-Outs
LTC1726-5	Micropower Triple Supply Monitor for 5V, 3.3V and ADJ	Adjustable $\overline{RESET}$ and Watchdog Time-Outs
LTC1727-2.5/LTC1727-5	Micropower Triple Supply Monitor with Open-Drain Reset	Individual Monitor Outputs in MSOP
LTC1728-1.8/LTC1728-3.3	Micropower Triple Supply Monitor with Open-Drain Reset	5-Lead SOT-23 Package
LTC1728-2.5/LTC1728-5	Micropower Triple Supply Monitor with Open-Drain Reset	5-Lead SOT-23 Package
LTC1985-1.8	Micropower Triple Supply Monitor with Push-Pull Reset Output	5-Lead SOT-23 Package
LTC2900	Programmable Quad Supply Monitor	Adjustable $\overline{RESET}$, 10-Lead MSOP Package
LTC2901	Programmable Quad Supply Monitor	Adjustable $\overline{RESET}$ and Watchdog Timer, 16-Lead SSOP Package

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