



**THE DATASHEET OF  
LTC1446LIN8#PBF**



## FEATURES

- Dual DACs with 12-Bit Resolution
- SO-8 Package
- Rail-to-Rail Output Amplifiers
- Internal Reference
- Maximum DNL Error: 0.5LSB
- 3V Operation (LTC1446L):  $I_{CC} = 650\mu\text{A Typ}$
- 5V Operation (LTC1446):  $I_{CC} = 1000\mu\text{A Typ}$
- Settling Time:  $14\mu\text{s}$  to  $\pm 0.5\text{LSB}$
- Power-On Reset Clears DACs to 0V
- 3-Wire Cascadable Serial Interface with 500kHz Update Rate
- Schmitt Trigger On Input Allows Direct Optocoupler Interface
- Low Cost

## APPLICATIONS

- Digital Calibration
- Industrial Process Control
- Automatic Test Equipment
- Cellular Telephones

## DESCRIPTION

The LTC<sup>®</sup>1446/LTC1446L are dual 12-bit digital-to-analog converters (DACs) available in an SO-8 package. They are complete with a rail-to-rail voltage output amplifier, an internal reference and an easy-to-use 3-wire cascadable serial interface.

The LTC1446 has an internal reference and a full-scale output of 4.095V. It operates from a single 4.5V to 5.5V supply.

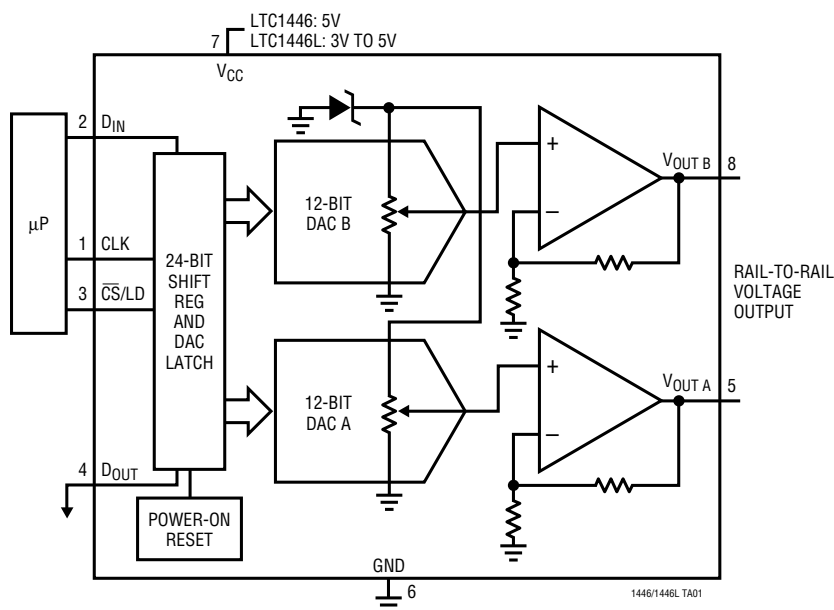
The LTC1446L has an internal reference and a full-scale output of 2.5V. It operates from a single 2.7V to 5.5V supply.

The low power supply current makes the LTC1446 family ideal for battery-powered applications. These DACs are available in space saving 8-pin SO and PDIP packages and require no external components for operation.

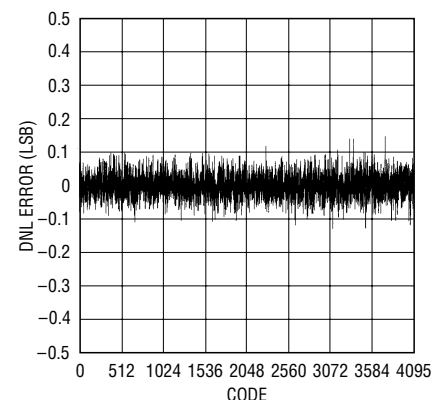
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## TYPICAL APPLICATION

Functional Block Diagram: Dual 12-Bit Rail-to-Rail DAC



Differential Nonlinearity vs Input Code



1446/46L G13

# LTC1446/LTC1446L

## ABSOLUTE MAXIMUM RATINGS (Note 1)

$V_{CC}$ to GND .....	-0.5 to 7.5V	$V_{OUT A}/V_{OUT B}$ .....	-0.5V to $V_{CC} + 0.5V$
Logic Inputs to GND .....	-0.5 to 7.5V	Maximum Junction Temperature .....	125°C
Operating Temperature Range		Storage Temperature Range .....	-65°C to 150°C
LTC1446C/LTC1446LC .....	0°C to 70°C	Lead Temperature (Soldering, 10 sec) .....	300°C
LTC1446I/LTC1446LI .....	-40°C to 85°C		

## PACKAGE/ORDER INFORMATION

TOP VIEW	ORDER PART NUMBER	TOP VIEW	ORDER PART NUMBER
<p>N8 PACKAGE 8-LEAD PDIP <math>T_{JMAX} = 125^{\circ}C, \theta_{JA} = 100^{\circ}C/W</math></p>	LTC1446CN8 LTC1446IN8 LTC1446LCN8 LTC1446LIN8	<p>S8 PACKAGE 8-LEAD PLASTIC SO <math>T_{JMAX} = 125^{\circ}C, \theta_{JA} = 150^{\circ}C/W</math></p>	LTC1446CS8 LTC1446IS8 LTC1446LCS8 LTC1446LIS8
		<b>S8 PART MARKING</b>	
		1446	1446L
		1446I	1446LI

Consult factory for Military grade parts.

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range.  $V_{CC} = 4.5V$  to  $5.5V$  (LTC1446),  $2.7V$  to  $5.5V$  (LTC1446L),  $V_{OUT A}$  and  $V_{OUT B}$  unloaded,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>DAC</b>							
	Resolution		● 12			Bits	
DNL	Differential Nonlinearity	Guaranteed Monotonic (Note 2)	●	±0.2	±0.5	LSB	
INL	Integral Nonlinearity	$T_A = 25^{\circ}C$	●	±2.0 ±2.5	4.5 5.0	LSB LSB	
ZSE	Zero-Scale Error		● 0	3	18	mV	
$V_{OS}$	Offset Error		●	±2	±18	mV	
$V_{OS TC}$	Offset Error Tempco			±15		$\mu V/^{\circ}C$	
$V_{FS}$	Full-Scale Voltage	LTC1446, $T_A = 25^{\circ}C$ LTC1446 LTC1446L, $T_A = 25^{\circ}C$ LTC1446L	●	4.065 4.045 2.470 2.460	4.095 4.095 2.500 2.500	4.125 4.145 2.530 2.540	V V V V
$V_{FS TC}$	Full-Scale Voltage Tempco			±0.1		LSB/ $^{\circ}C$	
<b>Power Supply (LTC1446)</b>							
$V_{CC}$	Positive Supply Voltage	For Specified Performance	● 4.5		5.5	V	
$I_{CC}$	Supply Current	$4.5V \leq V_{CC} \leq 5.5V$ (Note 5)	●	1000	1500	$\mu A$	
<b>Power Supply (LTC1446L)</b>							
$V_{CC}$	Positive Supply Voltage	For Specified Performance	● 2.7		5.5	V	
$I_{CC}$	Supply Current	$2.7V \leq V_{CC} \leq 5.5V$ (Note 5)	●	650	1000	$\mu A$	

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range.  $V_{CC} = 4.5V$  to  $5.5V$  (LTC1446),  $2.7V$  to  $5.5V$  (LTC1446L),  $V_{OUTA}$  and  $V_{OUTB}$  unloaded,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>Op Amp DC Performance</b>							
	Short-Circuit Current Low	$V_{OUT}$ Shorted to GND	●		55	120	mA
	Short-Circuit Current High	$V_{OUT}$ Shorted to $V_{CC}$	●		70	120	mA
	Output Impedance to GND	Input Code = 0	●		40	160	$\Omega$
<b>AC Performance</b>							
	Voltage Output Slew Rate	(Note 3)	●	0.5	1		V/ $\mu$ s
	Voltage Output Settling Time	(Notes 3, 4) to $\pm 0.5LSB$			14		$\mu$ s

The ● denotes the specifications which apply over the full operating temperature range.  $V_{CC} = 5V$  (LTC1446),  $V_{CC} = 3V$  (LTC1446L),  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LTC1446			LTC1446L			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>Digital I/O</b>									
$V_{IH}$	Digital Input High Voltage		●	2.4			2		V
$V_{IL}$	Digital Input Low Voltage		●			0.8		0.6	V
$V_{OH}$	Digital Output High Voltage	$I_{OUT} = -1mA$	●	$V_{CC} - 1.0$			$V_{CC} - 0.7$		V
$V_{OL}$	Digital Output Low Voltage	$I_{OUT} = 1mA$	●			0.4		0.4	V
$I_{LEAK}$	Digital Input Leakage	$V_{IN} = GND$ to $V_{CC}$	●			$\pm 10$		$\pm 10$	$\mu A$
$C_{IN}$	Digital Input Capacitance	Guaranteed by Design	●			10		10	pF
<b>Switching</b>									
$t_1$	$D_{IN}$ Valid to CLK Setup		●	40			60		ns
$t_2$	$D_{IN}$ Valid to CLK Hold		●	0			0		ns
$t_3$	CLK High Time		●	40			60		ns
$t_4$	CLK Low Time		●	40			60		ns
$t_5$	$\overline{CS}/LD$ Pulse Width		●	50			80		ns
$t_6$	LSB CLK to $\overline{CS}/LD$		●	40			60		ns
$t_7$	$\overline{CS}/LD$ Low to CLK		●	20			30		ns
$t_8$	$D_{OUT}$ Output Delay	$C_{LOAD} = 15pF$	●			150		220	ns
$t_9$	CLK Low to $\overline{CS}/LD$ Low		●	20			30		ns

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to code 4095 (full scale).

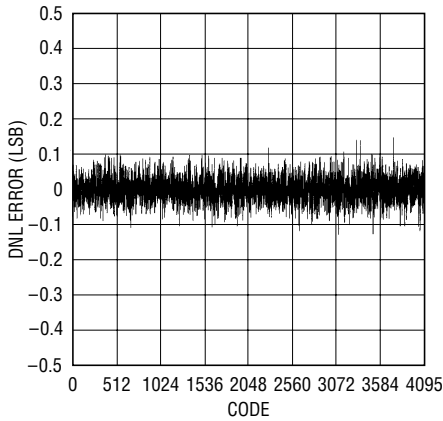
**Note 3:** Load is  $5k\Omega$  in parallel with  $100pF$ .

**Note 4:** DAC switched between all 1s and the code corresponding to  $V_{OS}$  for the part.

**Note 5:** Digital inputs at  $0V$  or  $V_{CC}$ .

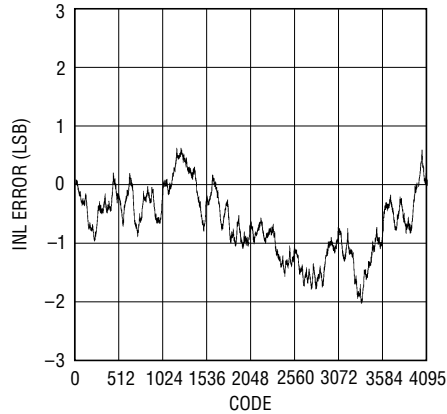
## TYPICAL PERFORMANCE CHARACTERISTICS

**LTC1446 Differential Nonlinearity (DNL)**



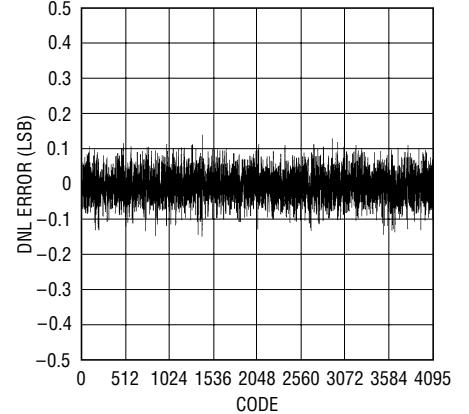
1446/46L G01

**LTC1446 Integral Nonlinearity (INL)**



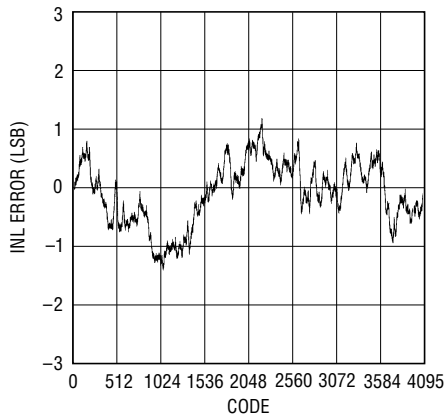
1446/46L G02

**LTC1446L Differential Nonlinearity**



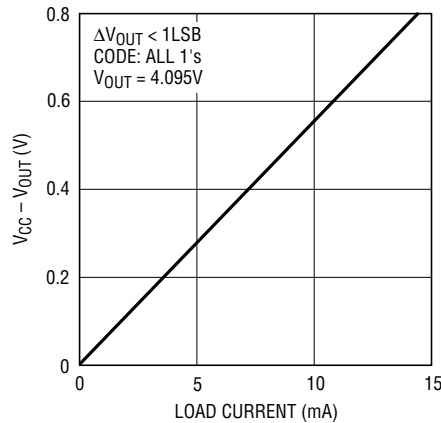
1446/46L G03

**LTC1446L Integral Nonlinearity**



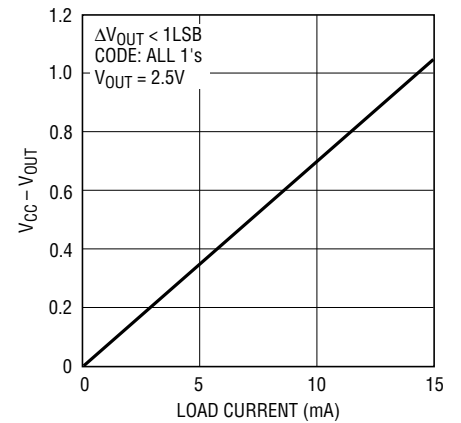
1446/46L G04

**LTC1446 Min Supply Headroom for Full Output Swing vs Load Current**



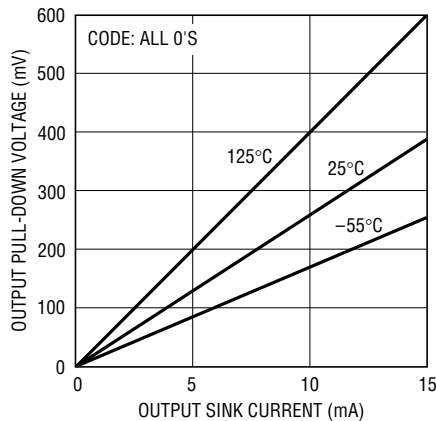
LTC1446/46L • TPC05

**LTC1446L Min Supply Headroom for Full Output Swing vs Load Current**



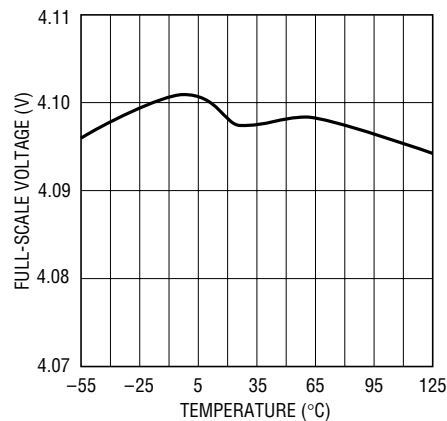
LTC1446/46L • TPC06

**LTC1446 Min Output Voltage vs Output Sink Current**



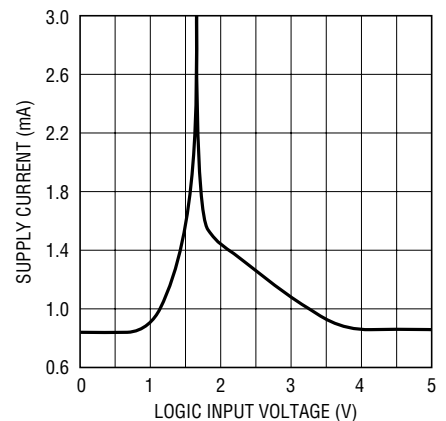
LTC1446/46L • TPC07

**LTC1446 Full-Scale Voltage vs Temperature**



1446/46L G09

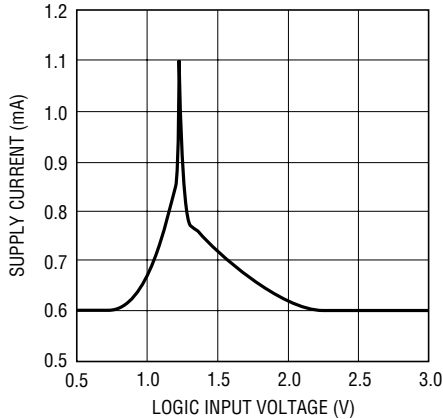
**LTC1446 Supply Current vs Logic Input Voltage**



1446/46L G09

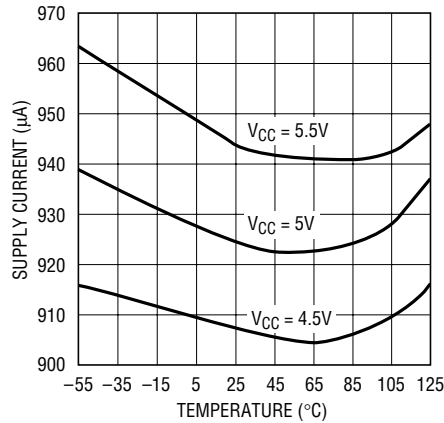
## TYPICAL PERFORMANCE CHARACTERISTICS

LTC1446L Supply Current vs Logic Input Voltage



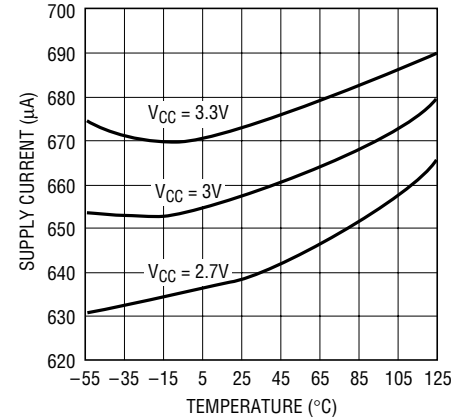
1446/46L G10

LTC1446 Supply Current vs Temperature



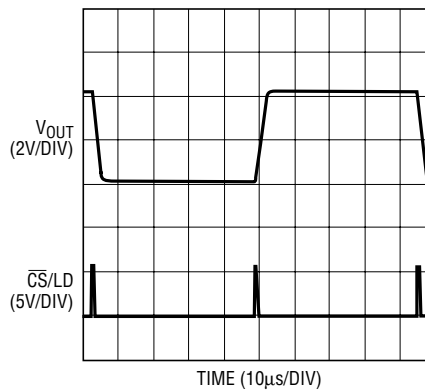
1446/46L G11

LTC1446L Supply Current vs Temperature



1446/46L G12

Large Signal Transient Response



1446L G13

## PIN FUNCTIONS

**CLK:** The Serial Interface Clock.

**D<sub>IN</sub>:** The Serial Interface Data.

**$\overline{\text{CS/LD}}$ :** The Serial Interface Enable and Load Control. When  $\overline{\text{CS/LD}}$  is low the CLK signal is enabled, so the data can be clocked in. When  $\overline{\text{CS/LD}}$  is pulled high data is loaded from the shift register into the DAC registers, updating the DAC outputs.

**D<sub>OUT</sub>:** The output of the shift register which becomes valid on the rising edge of the serial clock.

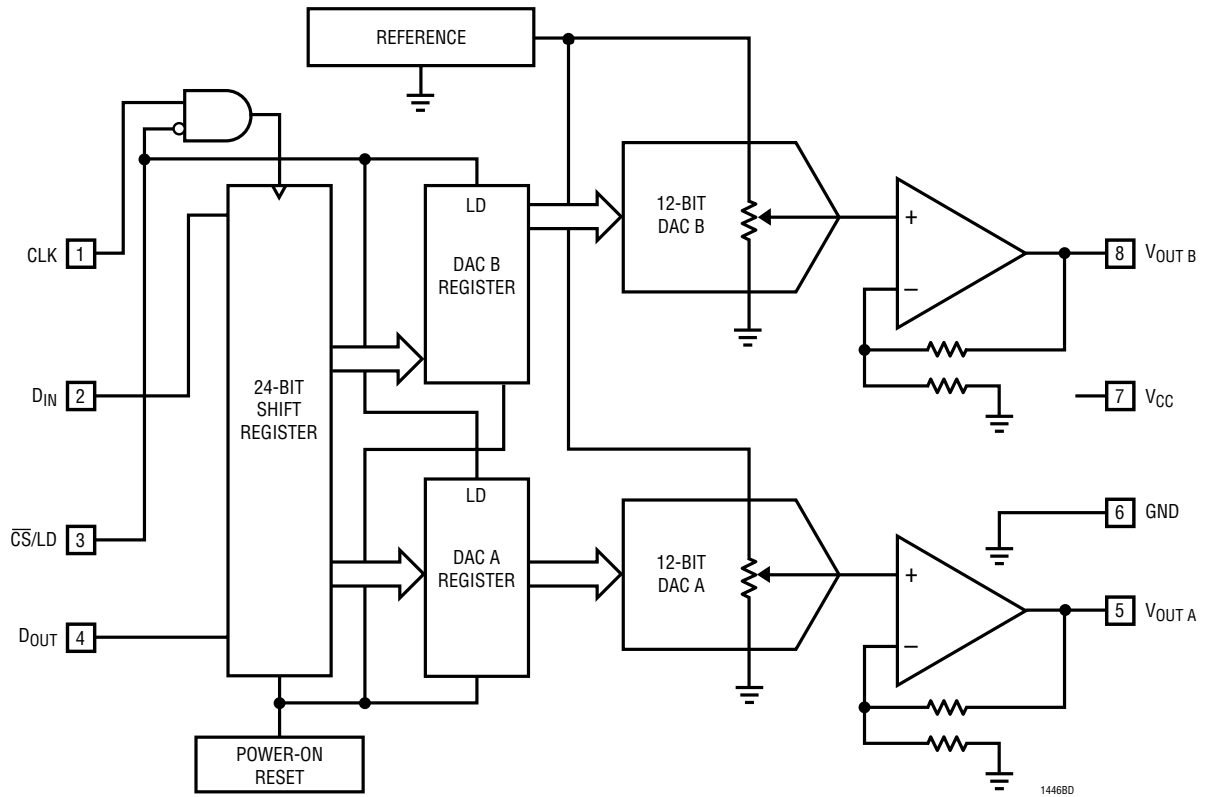
**GND:** Ground.

**V<sub>OUT A</sub>, V<sub>OUT B</sub>:** Buffered DAC Outputs.

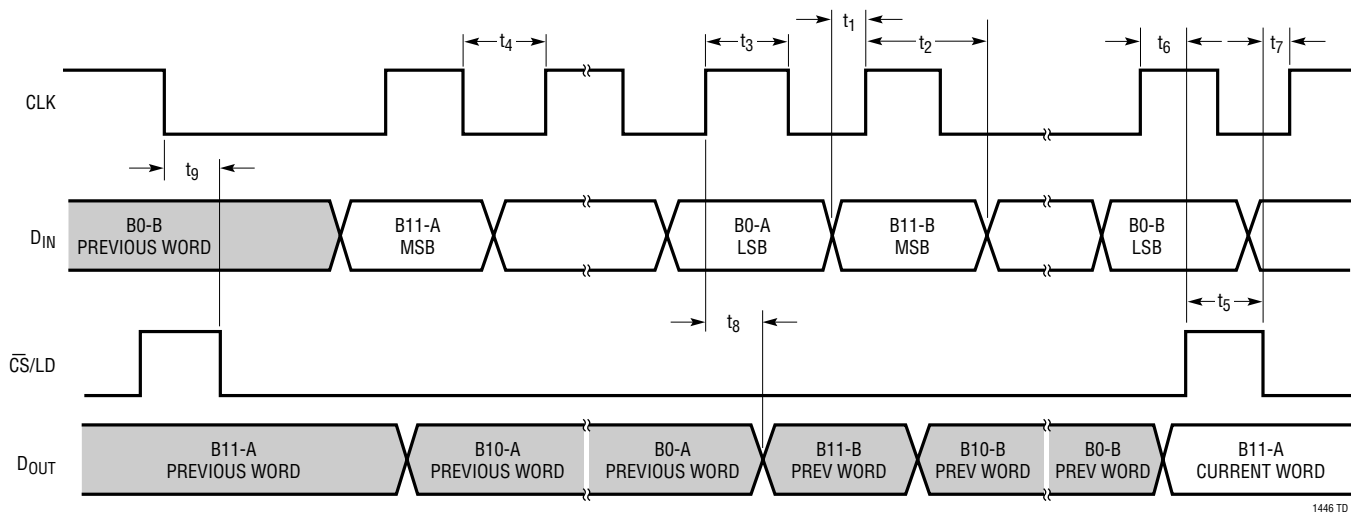
**V<sub>CC</sub>:** Positive Supply Input.

$4.5\text{V} \leq V_{\text{CC}} \leq 5.5\text{V}$  (LTC1446),  $2.7\text{V} \leq V_{\text{CC}} \leq 5.5\text{V}$  (LTC1446L). Requires a  $0.1\mu\text{F}$  bypass capacitor to ground.

## BLOCK DIAGRAM



## TIMING DIAGRAM



## DEFINITIONS

### Resolution (n)

Resolution is defined as the number of digital input bits, n. It defines the number of DAC output states ( $2^n$ ) that divide the full-scale range. The resolution does not imply linearity.

### Full-Scale Voltage ( $V_{FS}$ )

This is the output of the DAC when all bits are set to one.

### Voltage Offset Error ( $V_{OS}$ )

The theoretical voltage at the output when the DAC is loaded with all zeros. The output amplifier can have a true negative offset, but because the part is operated from a single supply, the output cannot go below zero. If the offset is negative, the output will remain near 0V resulting in the transfer curve shown in Figure 1.

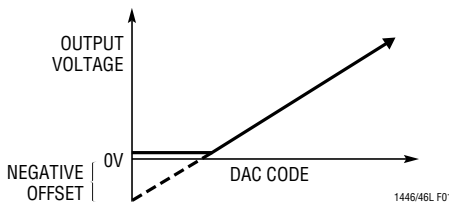


Figure 1. Effect of Negative Offset

The offset of the part is measured at the code that corresponds to the maximum offset specification:

$$V_{OS} = V_{OUT} - [(Code)(V_{FS})/(2^n - 1)]$$

### Least Significant Bit (LSB)

One LSB is the ideal voltage difference between two successive codes.

$$LSB = (V_{FS} - V_{OS})/(2^n - 1) = (V_{FS} - V_{OS})/4095$$

Nominal LSBs:

$$LTC1446 \quad LSB = 4.095V/4095 = 1mV$$

$$LTC1446L \quad LSB = 2.5V/4095 = 0.610mV$$

### Zero Scale Error (ZSE)

The output voltage when the DAC is loaded with all zeros. Since this is a single supply part this value cannot be less than 0V.

### Integral Nonlinearity (INL)

End-point INL is the maximum deviation from a straight line passing through the end points of the DAC transfer curve. Because the part operates from a single supply and the output cannot go below 0, the linearity is measured between full scale and the code corresponding to the maximum offset specification. The INL error at a given input code is calculated as follows :

$$INL = [V_{OUT} - V_{OS} - (V_{FS} - V_{OS})(Code/4095)]/LSB$$

$V_{OUT}$  = the output voltage of the DAC measured at the given input code

### Differential Nonlinearity (DNL)

DNL is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$DNL = (\Delta V_{OUT} - LSB)/LSB$$

$\Delta V_{OUT}$  = The measured voltage difference between two adjacent codes

## OPERATION

### Serial Interface

The data on the  $D_{IN}$  input is loaded into the shift register on the rising edge of the clock. Data is loaded as one 24-bit word where the first 12 bits are for DAC A and the second 12 are for DAC B. For each 12-bit segment the MSB is loaded first. Data from the shift register is loaded into the DAC register when  $\overline{CS/LD}$  is pulled high. The clock is disabled internally when  $\overline{CS/LD}$  is high. Note: CLK must be low before  $\overline{CS/LD}$  is pulled low to avoid an extra internal clock pulse.

The buffered output of the 24-bit shift register is available on the  $D_{OUT}$  pin which swings from GND to  $V_{CC}$ .

Multiple LTC1446/LTC1446L's may be daisy-chained together by connecting the  $D_{OUT}$  pin to the  $D_{IN}$  pin of the next chip, while the clock and  $\overline{CS/LD}$  signals remain common to all chips in the daisy chain. The serial data is clocked to all of the chips, then the  $\overline{CS/LD}$  signal is pulled high to update all of them simultaneously.

### Voltage Output

The LTC1446/LTC1446L include an internal voltage reference which is connected to each DAC. The LTC1446 has a full scale of 4.095V making 1LSB equal to 1mV. The LTC1446L has a full scale of 2.5V making 1LSB equal to 0.61mV.

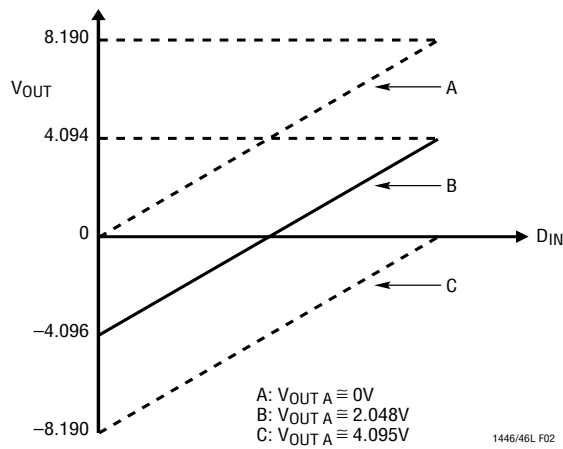
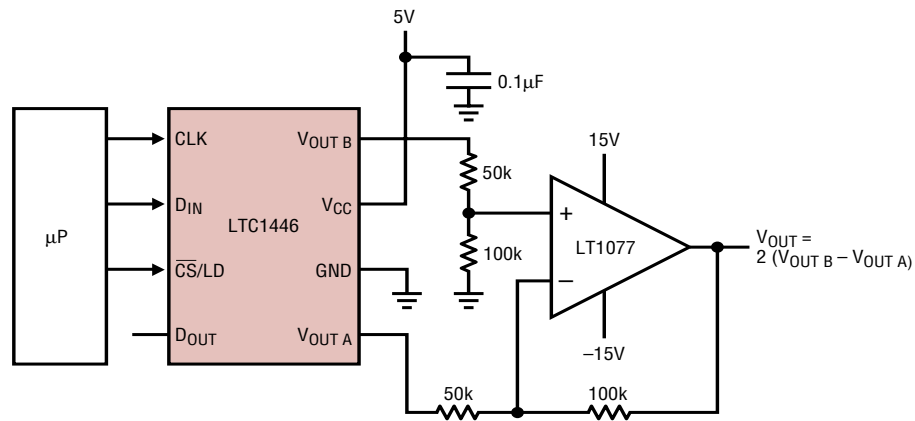
The LTC1446/LTC1446L rail-to-rail buffered outputs can source or sink 5mA when operating with a 5V supply while pulling to within 300mV of the positive supply voltage or ground. The outputs swing to within a few millivolts of either supply rail when unloaded and have an equivalent output resistance of  $40\Omega$  when driving a load to the rails. The buffer amplifiers can drive 1000pF without going into oscillation. The output noise spectral density is  $600\text{nV}/\sqrt{\text{Hz}}$  at 1kHz.

## TYPICAL APPLICATIONS

This circuit shows how to use an LTC1446 and an LT<sup>®</sup>1077 to make a wide bipolar output swing 12-bit DAC with an offset that can be digitally programmed.  $V_{OUT A}$ , which can be set by loading the appropriate digital code

for DAC A, sets the offset. As this value changes, the transfer curve for the output moves up and down as illustrated in the graph below.

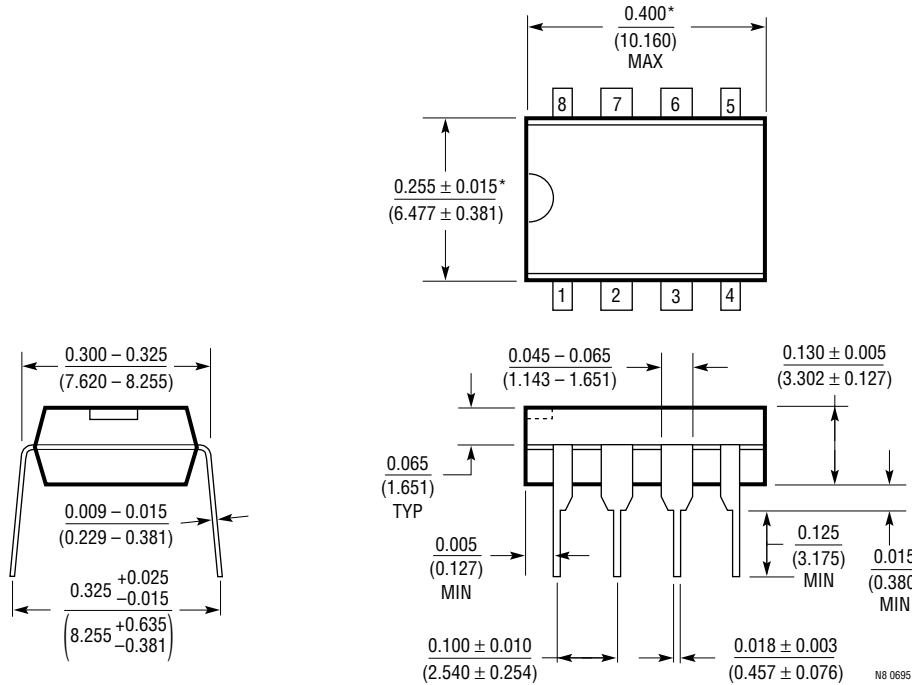
**A Wide Swing, Bipolar Output DAC with Digitally Controlled Offset**





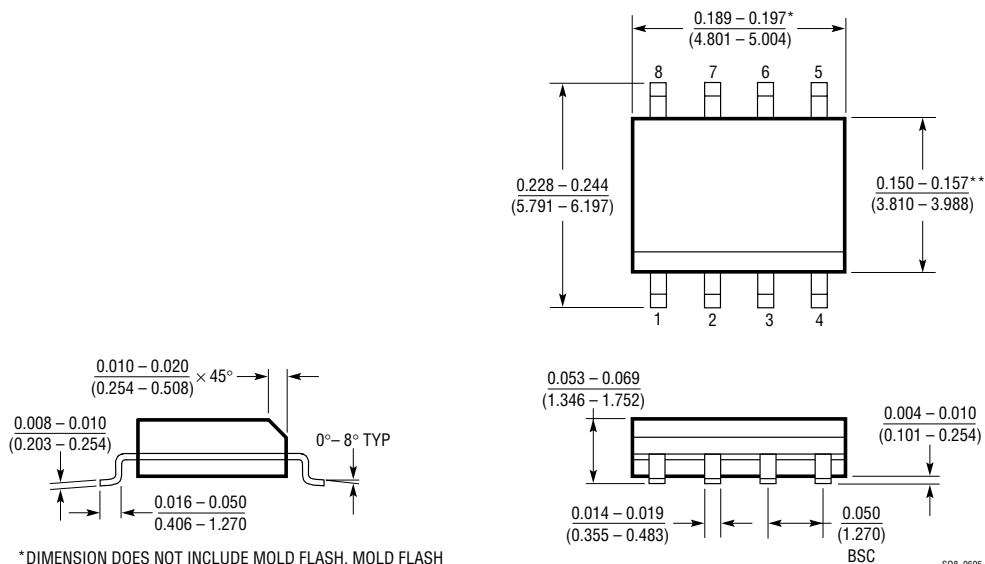
**PACKAGE DESCRIPTION** Dimensions in inches (millimeters) unless otherwise noted.

**N8 Package**  
**8-Lead PDIP (Narrow 0.300)**  
 (LTC DWG# 05-08-1510)



\*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

**S8 Package**  
**8-Lead Plastic Small Outline (Narrow 0.150)**  
 (LTC DWG # 05-08-1610)



\*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE



\*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

**RELATED PARTS**

PART NUMBER	DESCRIPTION	COMMENTS
LTC1257	Single 12-Bit $V_{OUT}$ DAC, Full Scale: 2.048V, $V_{CC}$ : 4.75V to 15.75V, Reference Can Be Overdriven up to 12V, i.e., FS Max = 12V	5V to 15V Single Supply, Complete $V_{OUT}$ DAC in SO-8 Package
LTC1451	Single Rail-to-Rail Output 12-Bit DAC, Full Scale: 4.095V, $V_{CC}$ : 4.5V to 5.5V Internal 2.048V Reference Brought Out to Pin	Low Power, Complete $V_{OUT}$ DAC in SO-8 Package
LTC1452	Single Rail-to-Rail 12-Bit $V_{OUT}$ Multiplying DAC, $V_{CC}$ : 2.7V to 5.5V	Low Power, Multiplying $V_{OUT}$ DAC with Rail-to-Rail Buffer Amplifier in SO-8 Package
LTC1453	Single Rail-to-Rail 12-Bit $V_{OUT}$ DAC, Full Scale: 2.5V, $V_{CC}$ : 2.7V to 5.5V	3V, Low Power, Complete $V_{OUT}$ DAC in SO-8 Package
LTC1454/LTC1454L	Dual 12-Bit $V_{OUT}$ DACs in a 16-Lead SO Package with Added Functionality	LTC1454: $V_{CC}$ = 4.5V to 5.5V, $V_{OUT}$ = 0V to 4.095V LTC1454L: $V_{CC}$ = 2.7V to 5.5V, $V_{OUT}$ = 0V to 2.5V
LTC1456	Single Rail-to-Rail Output 12-Bit DAC with Clear Pin Full Scale: 4.095V, $V_{CC}$ : 4.5V to 5.5V	Low Power, Complete $V_{OUT}$ DAC in SO-8 Package with Clear Pin
LTC1458/LTC1458L	Quad 12-Bit $V_{OUT}$ DACs in 28-Lead SW and SSOP Packages	LTC1458: $V_{CC}$ = 4.5V to 5.5V, $V_{OUT}$ = 0V to 4.095V LTC1458L: $V_{CC}$ = 2.7V to 5.5V, $V_{OUT}$ = 0V to 2.5V
LTC1654	Dual 14-Bit DAC in SSOP	Variable Speed, Variable Gain, 1LSB DNL
LTC1661	Dual 10-Bit $V_{OUT}$ DAC in MSOP	Low Cost, 0.75LSB DNL
LTC1662	Dual 10-Bit $V_{OUT}$ DAC in MSOP	Ultra Low Power = 1.5 $\mu$ A Supply Current

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

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-  [Linear Technology](#) Information

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-  Obsolete Management
-  Cost Control Management
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