THE DATASHEET OF

LTC1426CMS8#TRPBF

Micropower Dual 6-Bit PWM DAC

FEATURES

- Wide Supply Range: 2.7V ≤ V_{CC} ≤ 5.5V
- Wide Reference Voltage Range: 0V to 5.5V
- **Two Interface Modes:**
  - **Pulse Mode (Increment Only)**
  - **Pushbutton Mode (Increment/Decrement)**
- **Low Supply Current: 50µA**
- 0.2µA Supply Current in Shutdown
- Available in 8-Pin MSOP and SO Packages
- **DAC Contents Are Retained in Shutdown**
- DACs Power-Up at Midrange
- Low Output Impedance: <100Ω
- Output Frequency: 5kHz Typ

APPLICATIONS

- LCD Contrast and Backlight Brightness Control
- Power Supply Voltage Adjustment
- Battery Charger Voltage and Current Adjustment
- GaAs FET Bias Adjustment
- Trimmer Pot Elimination

DESCRIPTION

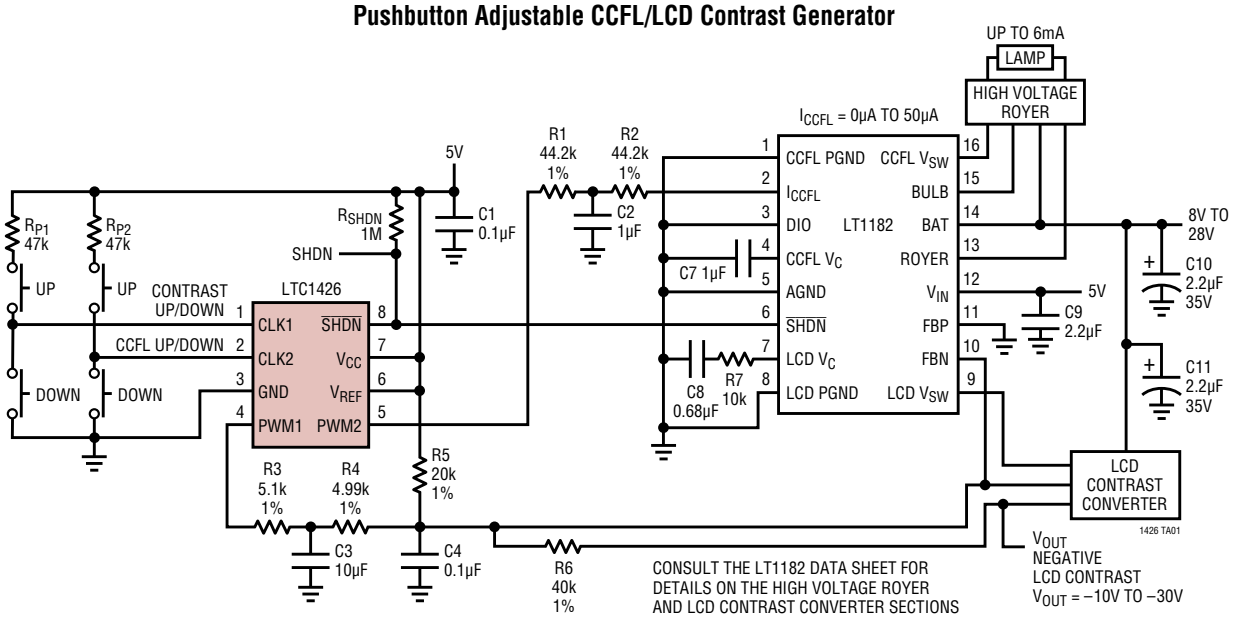
The LTC®1426 is a dual micropower 6-bit PWM DAC featuring versatile PWM outputs and a flexible pushbutton compatible digital interface. The DAC outputs provide a PWM signal that swings from 0V to V_{REF}, allowing the full-scale output to be varied by adjusting the voltage at V_{REF}. The PWM output frequency is typically 5kHz, easing output filtering requirements. V_{CC} supply current is typically 50µA and drops to 0.2µA in shutdown.

The LTC1426 can be controlled using one of two interface modes: pushbutton and pulse. The LTC1426 automatically configures itself into the appropriate mode at start-up by monitoring the state of the CLK pins. In pushbutton mode, the CLK pins can be directly connected to external pushbuttons to control the DAC output. In pulse mode, the CLK pins can be connected to CMOS compatible logic. The DAC outputs initially power up at half scale and the contents of the internal DAC registers are retained in shutdown.

The LTC1426 is available in 8-pin MSOP and SO packages.

TYPICAL APPLICATION

Pushbutton Adjustable CCFL/LCD Contrast Generator



Rev A

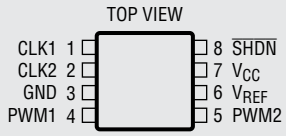
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V_{CC}) 7V
Reference Voltage (V_{REF}) ..... –0.3 to 7V
Input Voltage (All Inputs) ..... – 0.3 to (V_{CC} + 0.3V)
DAC Output Short-Circuit Duration ..... Indefinite
$I_{PWM(MAX)}$ 100mA

Operating Temperature Range
LTC1426C ..... 0°C to 70°C
LTC1426I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

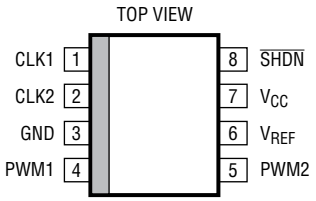
PIN CONFIGURATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 100°C, θ_{JA} = 200°C/W

OBSOLETE PACKAGE



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 100°C, θ_{JA} = 130°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1426CMS8#PBF	LTC1426CMS8#TRPBF	LTBQ	8-Lead Plastic MSOP	0°C to 70°C
LTC1426CS8#PBF	LTC1426CS8#TRPBF	1426	8-Lead Plastic SO	0°C to 70°C
LTC1426IS8#PBF	LTC1426IS8#TRPBF	1426I	8-Lead Plastic SO	–40°C to 85°C

Consult ADI Marketing for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
V_{REF}	Reference Voltage		●	0		5.5	V
I_{CC}	Supply Current	Pulse Mode: V_{SHDN} = V_{CC}, V_{CLK1} = V_{CLK2} = 0V, PWM1 = PWM2 = NC Pushbutton Mode: V_{SHDN} = V_{CC}, V_{CLK1} = V_{CLK2} = PWM1 = PWM2 = NC $\overline{SHDN}$ = 0 (Note 3)	● ● ●		40 50 0.2	100 100 ±10	µA µA µA
I_{REF}	Reference Current	Pulse Mode: V_{SHDN} = V_{CC}, V_{CLK1} = V_{CLK2} = 0V, PWM1 = PWM2 = NC Pushbutton Mode: V_{SHDN} = V_{CC}, V_{CLK1} = V_{CLK2} = PWM1 = PWM2 = NC $\overline{SHDN}$ = 0 (Note 3)	● ● ●		75 75 0.2	150 150 ±10	µA µA µA
	DAC Resolution				6		bits

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
	DAC Frequency	0°C ≤ T_A ≤ 70°C –40°C ≤ T_A ≤ 85°C		● ●	3 2	5 5	6 6	kHz kHz
	DAC Output Impedance	V_{CC} = 2.7V, V_{REF} = 0.5V		●		20	100	Ω
	DAC Full-Scale Duty Cycle					98.44		%
	DAC Zero-Scale Duty Cycle					0		%
DNL	DAC Differential Nonlinearity	Monotonicity Guaranteed (Note 4)		●			±0.05	LSB
INL	DAC Integral Nonlinearity	(Note 4)		●			±0.05	LSB
FS Error	DAC Full-Scale Error			●			±0.50	LSB
I_{IN}	Logic Input Current	Pulse Mode: 0V ≤ V_{IN} ≤ V_{CC}	$\overline{SHDN}$ CLK1, CLK2	● ●			±5 ±5	µA µA
		Pushbutton Mode: 0V ≤ V_{IN} ≤ V_{CC}	$\overline{SHDN}$ CLK1, CLK2	● ●			±5 ±10	µA µA
V_{IH}	CLK High Level Input Voltage (Note 5)	V_{CC} = 5.5V	$\overline{SHDN}$ CLK1, CLK2	● ●	2.0 4.4			V V
		V_{CC} = 3.6V	$\overline{SHDN}$ CLK1, CLK2	● ●	1.9 2.9			V V
V_{IL}	CLK Low Level Input Voltage (Note 5)	V_{CC} = 4.5V	$\overline{SHDN}$ CLK1, CLK2	● ●			0.8 0.8	V V
		V_{CC} = 2.7V	$\overline{SHDN}$ CLK1, CLK2	● ●			0.45 0.45	V V
I_{OZ}	Three-State Output Leakage	$\overline{SHDN}$ = 0		●			±5	µA
Z_{IN}	CLK Input Resistance	Pushbutton Mode, CLK1/CLK2				2.5		MΩ
f_{CLK}	Clock Frequency	Pulse Mode, V_{CC} = 3.3V Pulse Mode, V_{CC} = 2.7V		● ●			1 750	MHz kHz
t_{CKHI}	Clock High Time	Pulse Mode, V_{CC} = 3.3V Pulse Mode, V_{CC} = 2.7V		● ●	450 600			ns ns
t_{CKLO}	Clock Low Time	Pulse Mode, V_{CC} = 3.3V Pulse Mode, V_{CC} = 2.7V		● ●	450 600			ns ns
t_{PW}	Pulse Width	Pushbutton Mode		●	670			µs
t_{DEB}	Debounce Time	Pushbutton Mode		●	10.7	12.8	21.3	ms
t_{DELAY}	Repeat Rate Delay	Pushbutton Mode		●	340	410	680	ms
f_{REPEAT}	Repeat Frequency	Pushbutton Mode		●	11.7	19.5	23.4	Hz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground, unless otherwise specified. All typicals are given for V_{CC} = V_{REF} = 5V, T_A = 25°C and PWM1/PWM2 output to GND, C_{PWM} = 10pF.

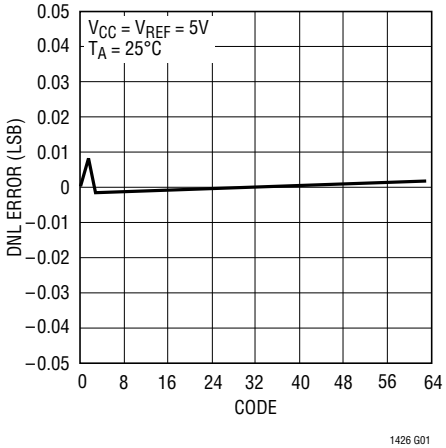
Note 3: Shutdown current can be negative due to leakage currents if V_{CC} > V_{REF} or V_{REF} > V_{CC}.

Note 4: Guaranteed by Design. Decouple the V_{CC} and V_{REF} pins to GND using high quality, low ESR, low ESL 0.1µF capacitors to eliminate PWM switching noise that may otherwise get coupled into the CLK1/CLK2 high impedance input buffers. The decoupling capacitors should be located in close proximity to these pins and the ground line to have maximum effect.

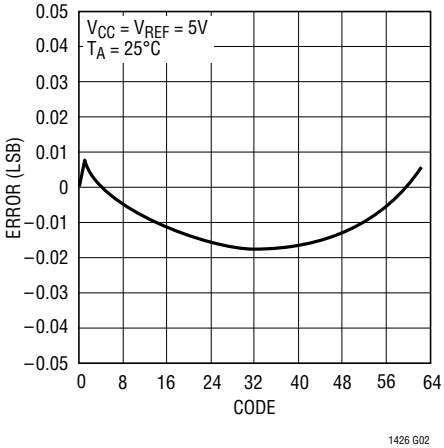
Note 5: Input thresholds apply for both pushbutton and pulse modes.

TYPICAL PERFORMANCE CHARACTERISTICS

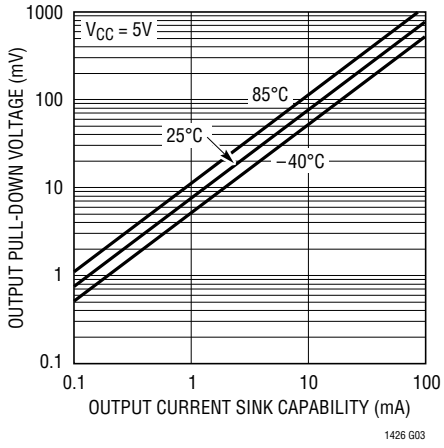
Differential Nonlinearity (DNL)



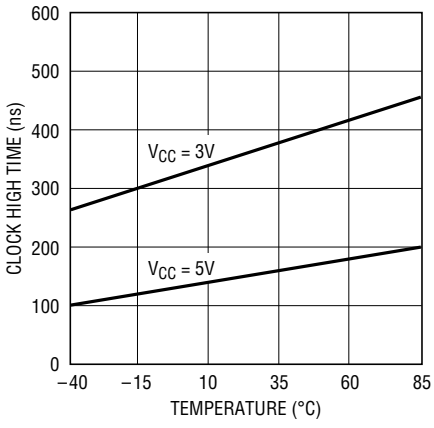
Integral Nonlinearity (INL)



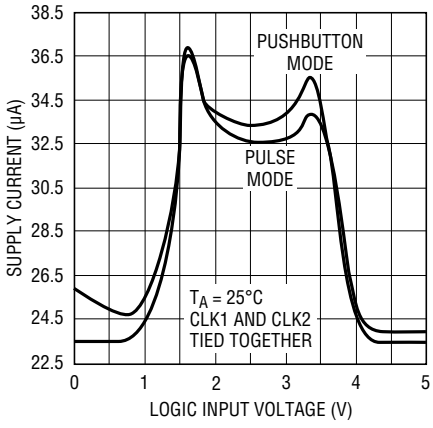
Output Pull-Down Voltage vs Output Current Sink Capability



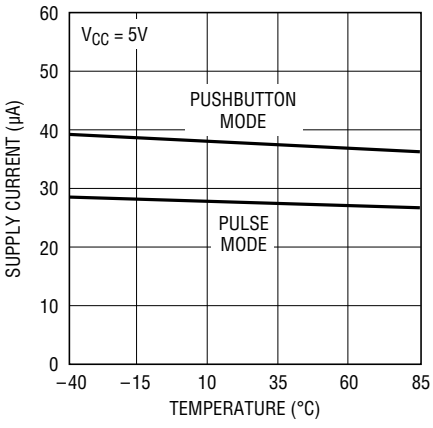
Minimum Clock High Time vs Temperature



Supply Current vs Logic Input Voltage



Supply Current vs Temperature



PIN FUNCTIONS

CLK1 (Pin 1): Channel 1 Clock/Pushbutton Input.

CLK2 (Pin 2): Channel 2 Clock/Pushbutton Input.

GND (Pin 3): Ground. It is recommended that GND be tied to a ground plane.

PWM1 (Pin 4): Channel 1 PWM Output.

PWM2 (Pin 5): Channel 2 PWM Output.

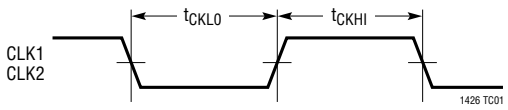
V_{REF} (Pin 6): Voltage Reference Input. V_{REF} powers the DAC output buffers and can be used to control the output span. Bypass V_{REF} to GND with an external capacitor to minimize output errors. V_{REF} can be tied to V_{CC} if desired.

V_{CC} (Pin 7): Voltage Supply. This supply must be kept free from noise and ripple by bypassing directly to the ground plane.

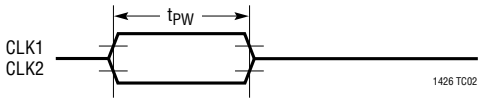
$\overline{SHDN}$ (Pin 8): Shutdown. A logic low puts the chip into shutdown mode with the PWM outputs in high impedance. The digital settings for the DACs are retained in shutdown.

TIMING DIAGRAMS

Pulse Mode Timing



Pushbutton Mode Timing



BLOCK DIAGRAM

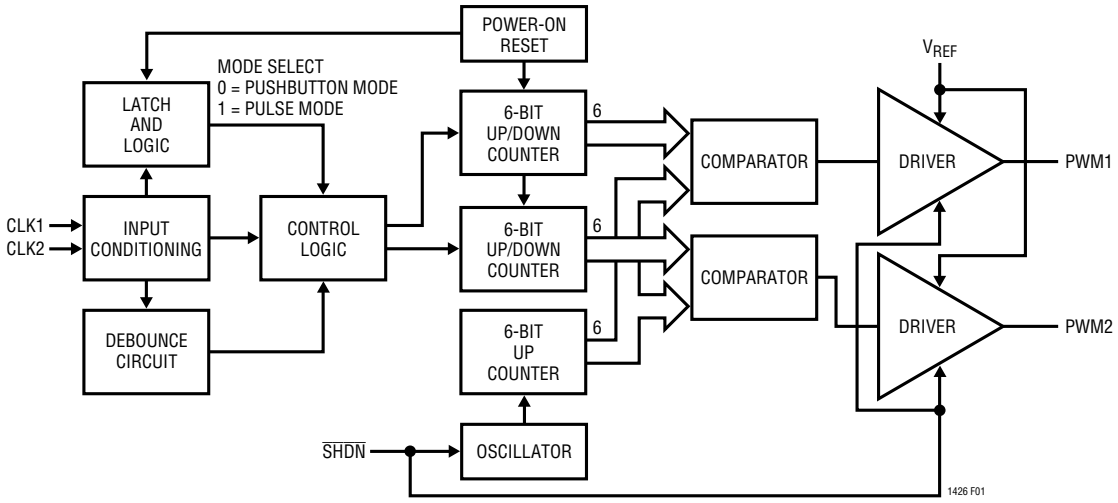


Figure 1. LTC1426 Block Diagram

DEFINITIONS

LSB: The least significant bit or the ideal duty cycle difference between two successive codes.

$LSB = DC_{MAX}/64$
DC_{MAX} = The DAC output maximum duty cycle

Resolution: The resolution is the number of DAC output states (64) that divide the full-scale output duty cycle range. The resolution does not necessarily imply linearity.

INL: End point integral nonlinearity is the maximum deviation from a straight line passing through the end points of the DAC transfer curve. The INL error at a given code is calculated as follows:

$INL = (DC_{OUT} – DC_{IDEAL})/LSB$
$DC_{IDEAL} = (Code)(LSB)$
DC_{OUT} = the DAC output duty cycle measured at the given number of clocked in pulses.

DNL: Differential nonlinearity is the difference between the measured duty cycle change and the ideal 1LSB duty cycle change between any two adjacent codes. The DNL error between any two codes is calculated as follows:

$DNL = (\Delta DC_{OUT} – LSB)/LSB$
ΔDC_{OUT} = The measured duty cycle difference between two adjacent codes.

Full-Scale Error: Full-scale error is the difference between the ideal and measured DAC output duty cycles with all bits set to one (Code = 63). The full-scale error is calculated as follows:

$FSE = (DC_{OUT} – DC_{IDEAL})/LSB$
$DC_{IDEAL} = DC_{MAX}$

APPLICATIONS INFORMATION

Dual 6-Bit PWM DAC

Figure 1 shows a block diagram of the LTC1426. Each 6-bit PWM DAC is guaranteed monotonic and is digitally adjustable in 64 equal steps, which corresponds from 0% to 98.5% duty cycle full scale. At power-up, the counters reset to 100000B and both DAC outputs assume midscale duty cycle. The PWM outputs have an output impedance of less than 100Ω. The DAC outputs swing from 0V to the reference voltage, V_{REF}, which can be biased from 0V to 5.5V. The frequency of the DAC outputs is above 3kHz, easing output filtering.

In the case of a pure resistive load, the voltage measured across load RL is given by:

$$V = (V_{PWM})R_L/(R_L + R_{OUT})$$

where V_{PWM} is the no load DAC output voltage, R_L is the resistive load and R_{OUT} is the DAC output impedance. Therefore, the resistive load R_L should be sufficiently large to ignore the effect of output impedance on the load voltage.

Figure 2 shows a typical lowpass filter recommended to filter the PWM outputs. Without filtering, results obtained from unfiltered outputs can be erroneous when taking measurements from a voltmeter. The ratio of the filter time constant, t, to the PWM frequency determines the amount of output ripple frequency that feeds into the system. In addition, the loading of the output also determines an additional error voltage drop across R1.

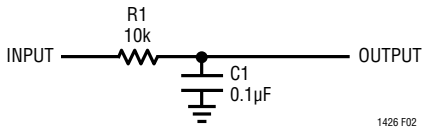


Figure 2. Lowpass Filter for PWM Averaging

Digital Interface

The LTC1426 can be controlled by using one of two interface modes: pulse mode and pushbutton mode. The operating interface mode is determined during power-up. If both CLK1 and CLK2 inputs are floating on power-up, then an interface mode detect circuit configures the chip in pushbutton mode until the next V_{CC} reset (Figure 3). However, if either of CLK1 or CLK2 is at logic 0 or 1 at power-up, then the chip configures in pulse mode until the next V_{CC} reset.

Figure 3 shows the simplified logic for determining the interface mode at power-up. A set of pull-up/pull-down resistors allow the LTC1426 to sense the state of the CLK pins at power-up. If both CLK1 and CLK2 pins are floating on power-up then the control signal from the LTC1426 leaves these resistors in place, allowing the LTC1426 to detect three operating states at each CLK pin: high, low and “middle” (floating). If the CLK pins are tied to either logic 0 or 1 at power-up, then the control signal will disconnect these resistors, making CLK1 and CLK2 CMOS compatible input pins.

Note that both CLK pins will always be in the same mode. If one pin is floating and the other is at logic high/low on power-up, the LTC1426 will assume pulse mode.

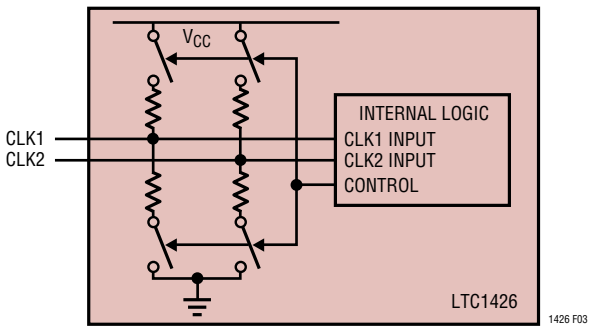


Figure 3. Interface Mode Detect Circuit

TYPICAL APPLICATIONS

Typical applications for this part include digital calibration, industrial process control, automatic test equipment, cellular telephones and portable battery-powered applications. Figures 4 and 5 show how easy this part is to use. In all applications, the PWM full-scale output voltage is set by V_{REF}. This makes interfacing convenient when a variety of reference spans are needed.

Pulse Mode

Figure 4 shows the LTC1426 in a pulse mode, stand-alone application. The LTC1426 can interface directly with minimum external components to most popular microprocessors (MPUs). The Intel 8051 was chosen to demonstrate direct interface for the LTC1426, as this microprocessor has "quasi-bidirectional" ports that eliminate additional pull-up resistors to V_{CC}. However, external pull-up resistors should be used if the microprocessor doesn't pull the port pins high during reset.

In pulse mode, each clock pulse applied to the CLK1 or CLK2 input increments the respective counter by one count. When the counter increases beyond full scale (111111B), the counter rolls over and becomes zero scale (000000B). In this way, a single pulse applied to the CLK1 or CLK2 input increases the respective counter by one count, and 63 pulses decrease that counter by one count.

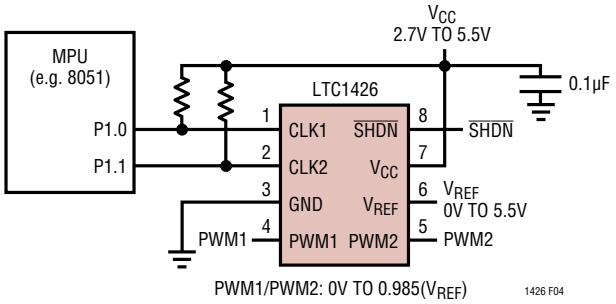
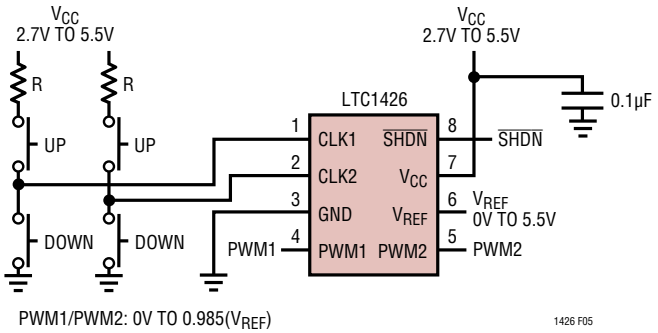


Figure 4. Stand-Alone Pulse Mode Interface

Pushbutton Mode

Figure 5 shows how to use the LTC1426 in a typical pushbutton application. In pushbutton mode, a logic 1 pulse applied to the CLK1 or CLK2 input increments the respective counter by one count, and stops incrementing when the counter reaches full scale (111111B). A logic 0 pulse applied to the CLK1 or CLK2 input decrements the respective counter by one count, and stops decrementing when the counter reaches zero scale (000000B). An on-chip debouncing circuit has a debounce time of 12.8ms to prevent unintended counts with bouncing pushbuttons. After a time delay of 410ms, the counter will begin to increment/decrement at a repeat rate of 19.5Hz if the pushbutton remains pressed.

Care should be taken to avoid running the CLK and PWM traces close to one another. Since the CLK pins are high impedance input nodes in pushbutton mode, current spikes caused by the switching of the PWM outputs feedthrough via any stray capacitance between PWM and CLK lines if not properly routed. Use of proper grounding techniques and spacing of these lines are highly recommended for optimal performance.



LIMITING RESISTOR R PREVENTS SHORTING OF V_{CC} AND GND WHEN BOTH BUTTONS ARE SIMULTANEOUSLY PUSHED. THIS RESISTOR CAN BE PLACED EITHER IN THE V_{CC} OR GND LEG AND THIS DETERMINES THE FUNCTION WHEN BOTH BUTTONS ARE PUSHED. VALUE OF R < 50k

Figure 5. Pushbutton Mode Interface

TYPICAL APPLICATIONS

Figure 6 shows a dual digitally programmable current source using the LT®1013 dual precision op amp and two NPN transistors (2N3904). After the lowpass filter combination of R1, C1 (R2, C2), its output swings from 0V to 4.93V. In the configuration shown, this voltage will be forced across the resistor R_{A1} (R_{A2}). If R_{A1} (R_{A2}) is chosen to be 493Ω, the output current will range from 0mA at zero scale to 10mA at full scale. The minimum voltage for V_S is determined by the load resistor R_{L1} (R_{L2}) and Q1(Q2)'s V_{CESAT} voltage. With a load resistor of 50Ω, the voltage source can be as low as 5V.

Shutdown Mode

Upon the application of a logic low shutdown signal, the entire IC converts to micropower shutdown mode where V_{CC} supply current reduces to less than 0.3µA typical. The shutdown function features the data retention of the current PWM1 and PWM2 codes so that upon release from a shutdown condition, these states are reinstated. This is a functional difference in comparison to the half-scale preset for both PWM1 and PWM2 outputs upon power-up.

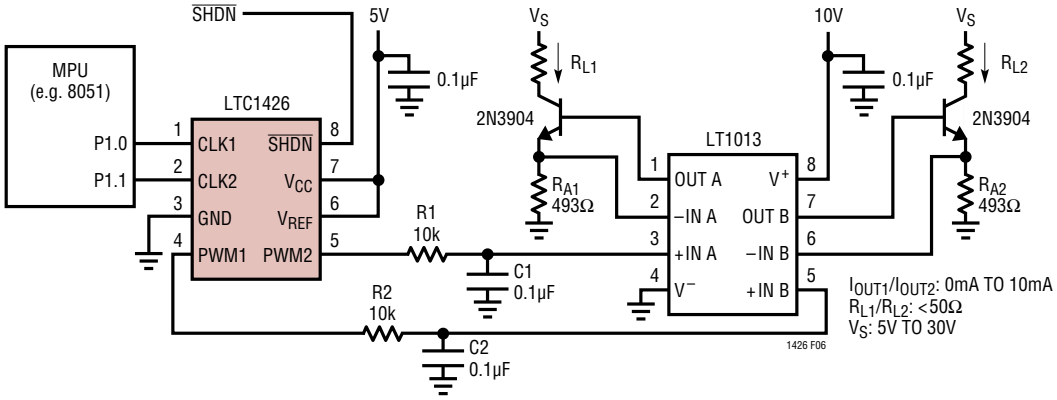
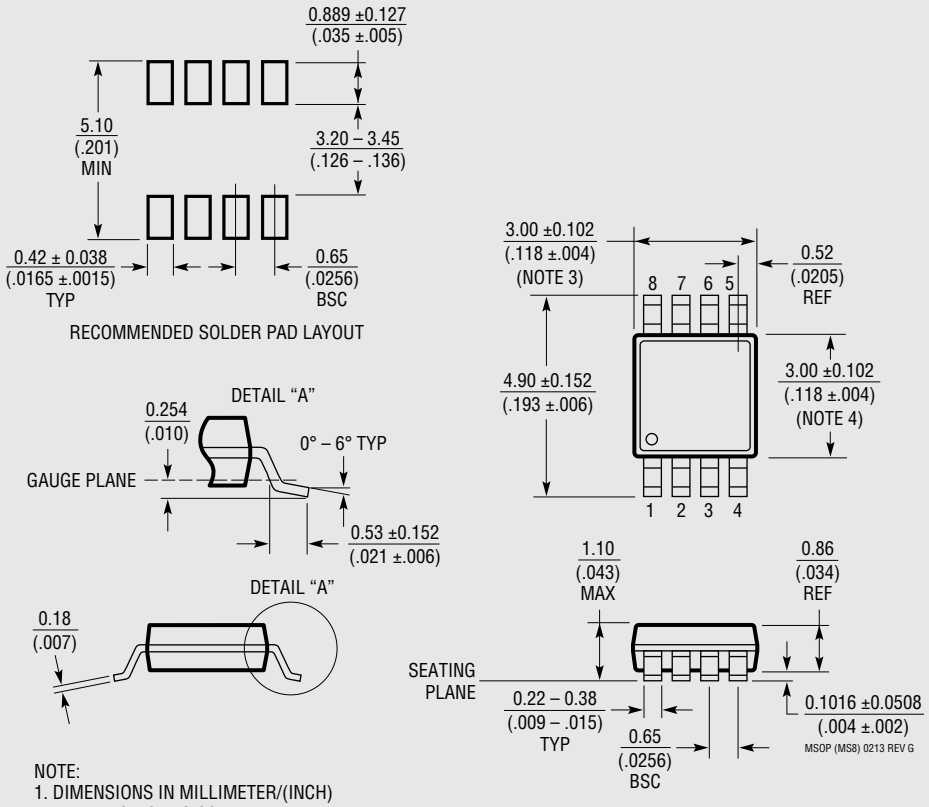


Figure 6. Dual Digitally Programmable Current Source

PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev G)

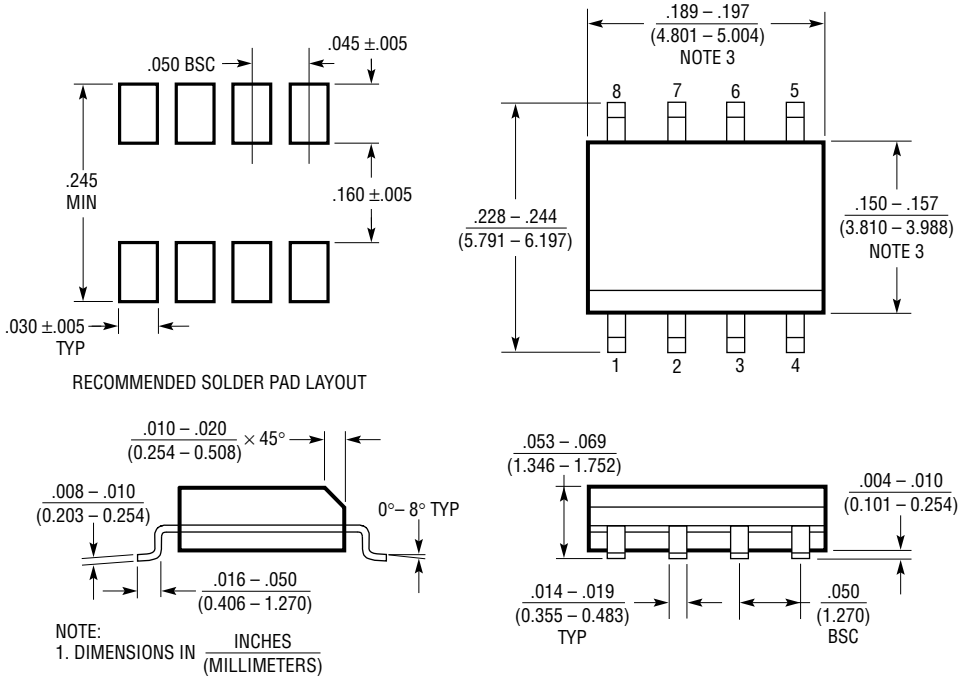


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

OBSOLETE PACKAGE

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

S08 REV G 0212

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	06/18	Obsoleted MS8 package option	2, 9

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1182/LT1183	CCFL/LCD Contrast Switching Regulators	3V to 30V Single Supply in 16-Pin SO
LTC1257	Single 12-Bit V_{OUT} DAC, Full Scale: 2.048V, V_{CC}: 4.75V to 15.75V. Reference Can Be Overdriven Up to 12V, i.e., FS Max = 12V	5V to 15V Single Supply, Complete V_{OUT} DAC in SO-8
LTC1329/ LTC1329-10/ LTC1329-50	Micropower I_{OUT} 8-Bit Current DAC	2.7V to 6.5V Single Supply in SO-8
LTC1446/ LTC1446L	Dual, Serial I/O V_{OUT} 12-Bit DAC in SO-8	Rail-to-Rail V_{OUT}, 5V/3V Single Supply
LTC1451/LTC1452/ LTC1453	Complete Serial I/O V_{OUT} 12-Bit DACs	Rail-to-Rail V_{OUT}, 3V/5V Single Supply in S0-8
LTC1590	Dual, Serial I/O Multiplying I_{OUT} 12-Bit DAC	5V Single Supply in 16-Pin SO Package
LTC8043	Serial I/O Mulitplying I_{OUT} 12-Bit DAC	5V Single Supply in SO-8

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View LTC1426CMS8#TRPBF on WIN SOURCE
- Linear Technology Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management