THE DATASHEET OF

LTC1164-5CN#PBF

www.win-source.net 0086-755-83957316

Low Power 8th Order Pin Selectable Butterworth or Bessel Lowpass Filter

FEATURES

- Pin Selectable Butterworth or Bessel Response
- 4mA Supply Current with ±5V Supplies
- f_{CUTOFF} up to 20kHz
- 100μV_{RMS} Wideband Noise
- THD < 0.02% (50:1, $V_S = \pm 7.5V$, $V_{IN} = 2V_{RMS}$)
- Operates with a Single 5V Supply (1V_{RMS} Input Range)
- 60μV_{RMS} Clock Feedthrough (Single 5V Supply)
- Operates up to ±8V Supplies
- TTL/CMOS-Compatible Clock Input
- No External Components
- Available in 14-Pin DIP and 16-Pin SO Wide Packages

APPLICATIONS

- Anti-Aliasing Filters
- Battery-Operated Instruments
- Telecommunications Filters
- Smoothing Filters

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DESCRIPTION

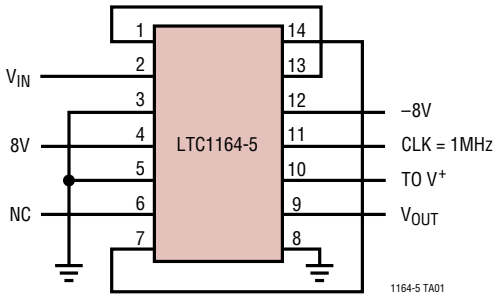
The LTC®1164-5 is a monolithic 8th order filter; it approximates either a Butterworth or a Bessel lowpass response. The LTC1164-5 features clock-tunable cutoff frequency and low power consumption (4.5mA with ±5V supplies and 2.5mA with single 5V supply).

Low power operation is achieved without compromising noise or distortion performance. With ±5V supplies and 10kHz cutoff frequency, the operating signal-to-noise ratio is 86dB and the THD throughout the passband is 0.015%. Under the same conditions, a 77dB signal-to-noise ratio and distortion is obtained with a single 5V supply while the clock feedthrough is kept below the noise level. The maximum signal-to-noise ratio is 92dB.

The LTC1164-5 approximates an 8th order Butterworth response with a clock-to-cutoff frequency ratio of 100:1 (Pin 10 to V^-) or 50:1 double-sampled (Pin 10 to V^+ and Pin 1 shorted to Pin 13). Double-sampling allows the input signal frequency to reach the clock frequency before any aliasing occurrence. An 8th order Bessel response can also be approximated with a clock-to-cutoff frequency ratio of 140:1 (Pin 10 to ground). With ±7.5V supply, ±5V supply and single 5V supply, the maximum clock frequency of the LTC1164-5 is 1.5MHz, 1MHz and 1MHz respectively. The LTC1164-5 is pin-compatible with the LTC1064-2 and LTC-1064-3.

TYPICAL APPLICATION

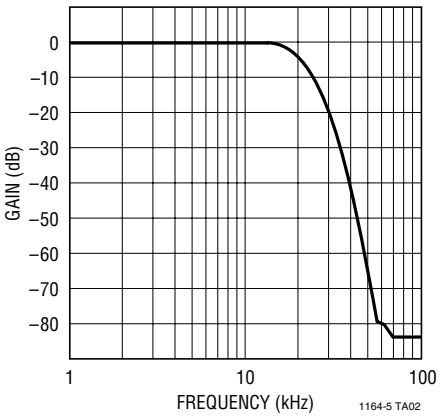
Butterworth 20kHz Anti-Aliasing Filter



WIDEBAND NOISE = 110μV_{RMS}
THD IN PASSBAND < 0.02% AT $V_{IN} = 2V_{RMS}$

NOTE: THE CONNECTION FROM PIN 7 TO PIN 14 SHOULD BE MADE UNDER THE PACKAGE. FOR 50:1 OPERATION CONNECT PIN 1 TO PIN 13 AS SHOWN. FOR 100:1 OR 150:1 OPERATION PINS 1 AND 13 SHOULD FLOAT. THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1µF CAPACITOR AS CLOSE TO THE PACKAGE AS POSSIBLE.

Frequency Response

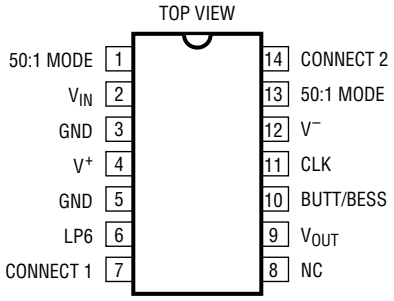


ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 16V
Input Voltage (Note 2) ..... (V^++ 0.3V) to (V^- – 0.3V)
Output Short-Circuit Duration ..... Indefinite
Power Dissipation 400mW
Burn-In Voltage 16V

Operating Temperature Range
LTC1164-5C ..... –40°C to 85°C
LTC1164-5M **(OBSOLETE)** ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



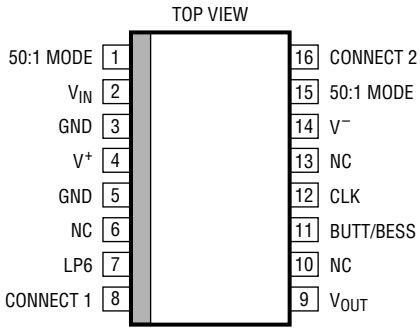
N PACKAGE
14-LEAD PDIP
T_{JMAX} = 110°C, θ_{JA} = 65°C/W

ORDER PART NUMBER
LTC1164-5CN

J PACKAGE 14-LEAD CERDIP
T_{JMAX} = 110°C, θ_{JA} = 65°C/W

LTC1164-5CJ
LTC1164-5MJ

OBSOLETE PACKAGE
Consider the N Package as an Alternate Source



SW PACKAGE
16-LEAD PLASTIC SO WIDE
T_{JMAX} = 110°C, θ_{JA} = 85°C/W

ORDER PART NUMBER
LTC1164-5CSW

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = Operating Temperature Range. V_S = ±7.5V, R_L = 10k, f_{CLK} = 400kHz, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain 0.1Hz at $0.25f_{CUTOFF}$ (Note 3)	f_{IN} = 1kHz, (f_{CLK}/f_C) = 100:1 f_{IN} = 1kHz, (f_{CLK}/f_C) = 50:1	● ●	–0.5 –0.5	–0.10 0.10	0.25 0.25	dB dB
Gain at $0.50f_{CUTOFF}$ (Note 3)	f_{IN} = 2kHz, (f_{CLK}/f_C) = 100:1 f_{IN} = 4kHz, (f_{CLK}/f_C) = 50:1	● ●	–0.45 –0.35	–0.20 –0.10	0.17 0.40	dB dB
Gain at $0.90f_{CUTOFF}$ (Note 3)	f_{IN} = 3.6kHz, (f_{CLK}/f_C) = 100:1	●	–2.50	–1.90	–1.0	dB
Gain at $0.95f_{CUTOFF}$ (Note 3)	f_{IN} = 3.8kHz, (f_{CLK}/f_C) = 100:1			–2.60		dB
Gain at f_{CUTOFF} (Note 3)	f_{IN} = 4kHz, (f_{CLK}/f_C) = 100:1 f_{IN} = 8kHz, (f_{CLK}/f_C) = 50:1	● ●	–4.10 –4.20	–3.40 –3.80	–2.75 –2.75	dB dB
Gain at $1.44f_{CUTOFF}$ (Note 3)	f_{IN} = 5.76kHz, (f_{CLK}/f_C) = 100:1	●	–20.5	–19.0	–17.0	dB
Gain at $2.0f_{CUTOFF}$ (Note 3)	f_{IN} = 8kHz, (f_{CLK}/f_C) = 100:1	●	–45.0	–43.0	–41.0	dB
Gain with f_{CLK} = 20kHz (Note 3)	f_{IN} = 200Hz, (f_{CLK}/f_C) = 100:1	●	–4.50	–3.40	–2.75	dB
Gain with V_S = 2.375V (Note 3)	f_{IN} = 400kHz, f_{IN} = 2kHz, (f_{CLK}/f_C) = 100:1 f_{IN} = 400kHz, f_{IN} = 4kHz, (f_{CLK}/f_C) = 100:1		–0.50 –4.20	–0.10 –3.40	0.35 –2.00	dB dB
Input Frequency Range	(f_{CLK}/f_C) = 100:1 (f_{CLK}/f_C) = 50:1			0 – <f_{CLK}/2 0 – <f_{CLK}		kHz kHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = Operating Temperature Range. $V_S = \pm 7.5V$, R_L = 10k, f_{CLK} = 400kHz, unless otherwise specified.

PARAMETER	CONDITIONS		LTC1164-5C MIN	TYP	MAX	UNITS
Maximum f_{CLK}	$V_S \geq \pm 7.5V$ $V_S = \pm 5.0V$ V_S = Single 5V (GND = 2V)			1.5 1.0 1.0		MHz MHz MHz
Clock Feedthrough	Input at GND, f = f_{CLK}, Square Wave ±5V, (f_{CLK}/f_C) = 100:1 ±5V, (f_{CLK}/f_C) = 50:1			 200 100		 μV_{RMS} μV_{RMS}
Wideband Noise	Input at GND, 1Hz ≥ f < f_{CLK} ±5V, (f_{CLK}/f_C) = 100:1 ±5V, (f_{CLK}/f_C) = 50:1			 100 ±5% 115 ±5%		 μV_{RMS} μV_{RMS}
Input Impedance			70	100	160	kΩ
Output DC Voltage Swing	$V_S = \pm 2.375V$ $V_S = \pm 5.0V$ $V_S = \pm 7.5V$	● ● ●	±1.25 ±3.70 ±5.40	±1.50 ±4.10 ±5.90		V V V
Output DC Offset	$V_S = \pm 5V$, (f_{CLK}/f_C) = 100:1			±50	±160	mV
Output DC Offset TempCo	$V_S = \pm 5V$, (f_{CLK}/f_C) = 100:1			±100		µV/°C
Power Supply Current	$V_S = \pm 2.375V$, $T_A \geq 25°C$ $V_S = \pm 5.0V$, $T_A \geq 25°C$ $V_S = \pm 7.5V$, $T_A \geq 25°C$ 	 ● ● ● 		2.5 4.5 7.0	4.0 4.5 7.0 8.0 11.0 12.5	mA mA mA mA mA mA
Power Supply Range			±2.375		±8	V

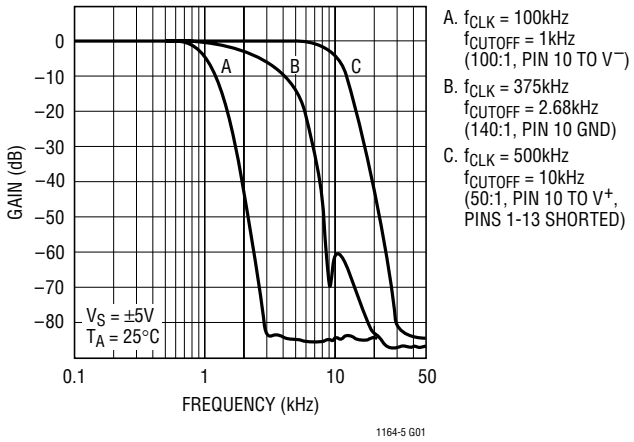
Note 1: Absolute Maximum Ratings are those values beyond which life of the device may be impaired.

Note 2: Connecting any pin to voltages greater than V^+ or less than V^- may cause latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1164-5.

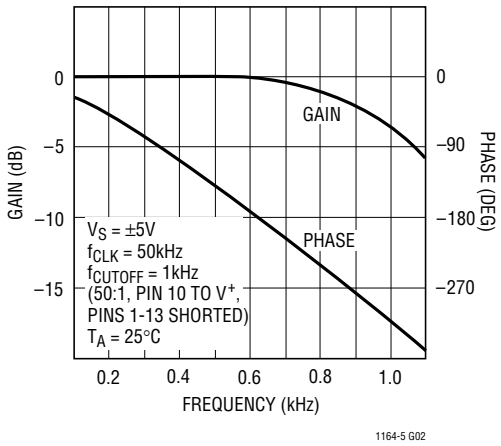
Note 3: All gains are measured relative to passband gain. The filter cutoff frequency is abbreviated as f_{CUTOFF} or f_C.

TYPICAL PERFORMANCE CHARACTERISTICS

Gain vs Frequency

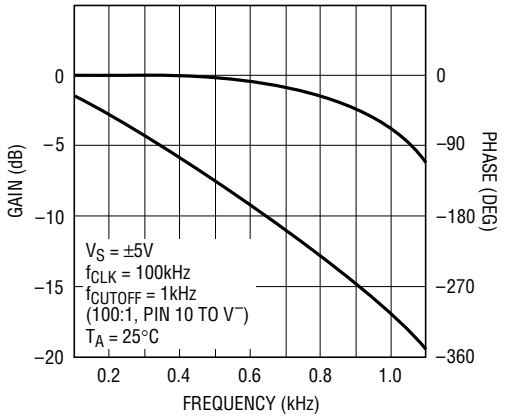


Passband Gain and Phase vs Frequency

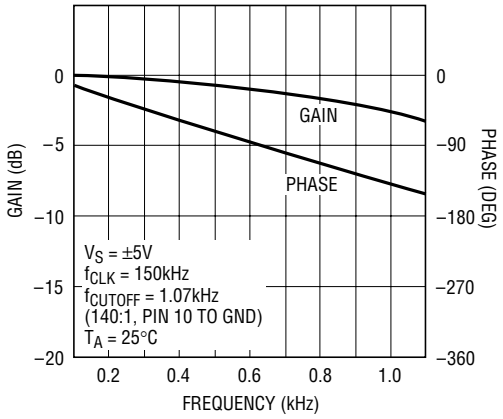


TYPICAL PERFORMANCE CHARACTERISTICS

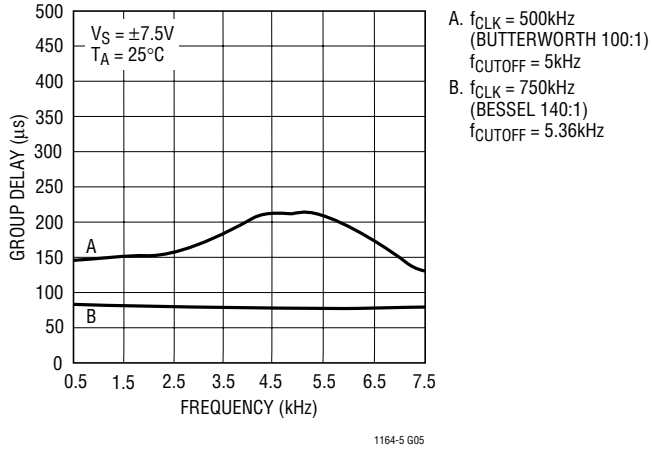
Passband Gain and Phase vs Frequency



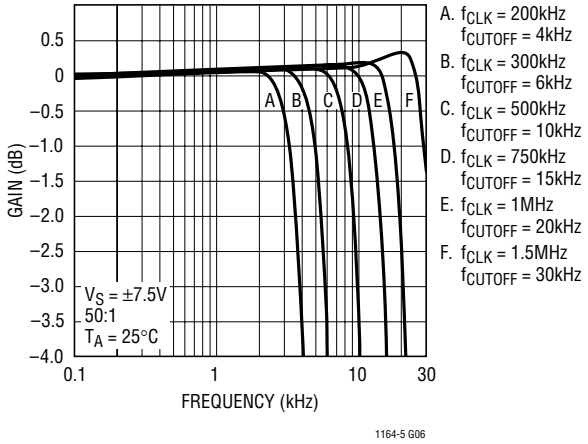
Passband Gain and Phase vs Frequency



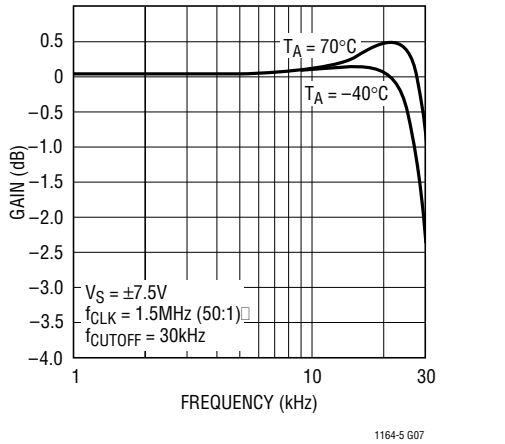
Group Delay vs Frequency



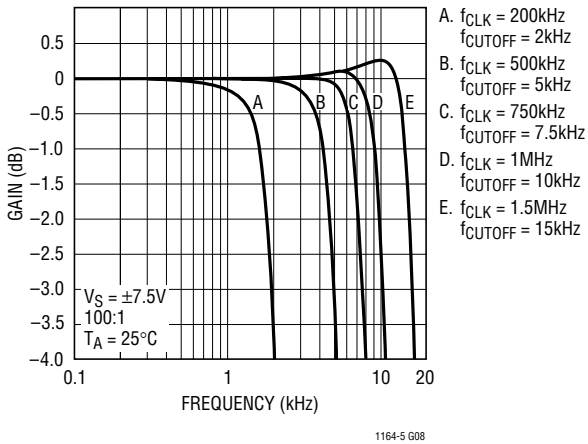
Passband vs Frequency and f_{CLK}



Maximum Passband over Temperature for V_S = ±7.5V, 50:1

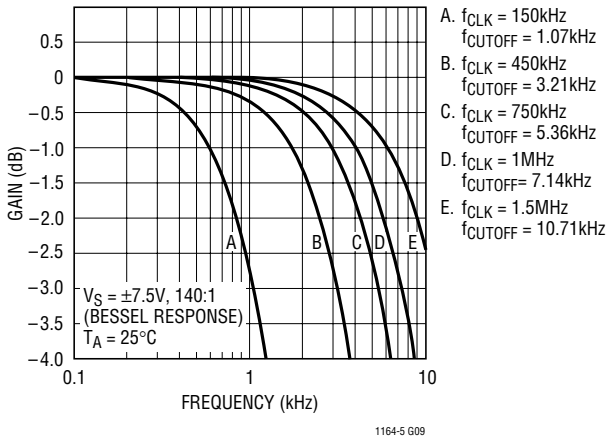


Passband vs Frequency and f_{CLK}

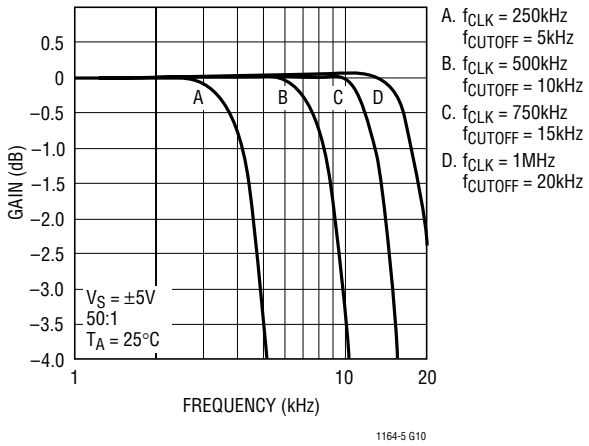


TYPICAL PERFORMANCE CHARACTERISTICS

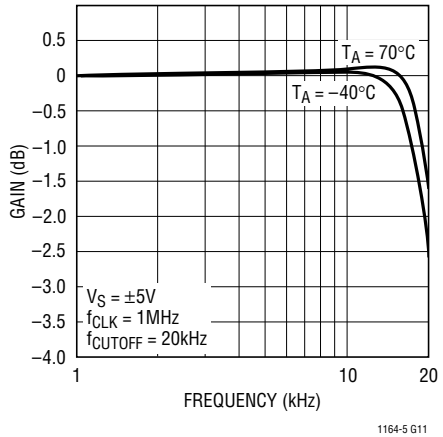
Passband vs Frequency and f_{CLK}



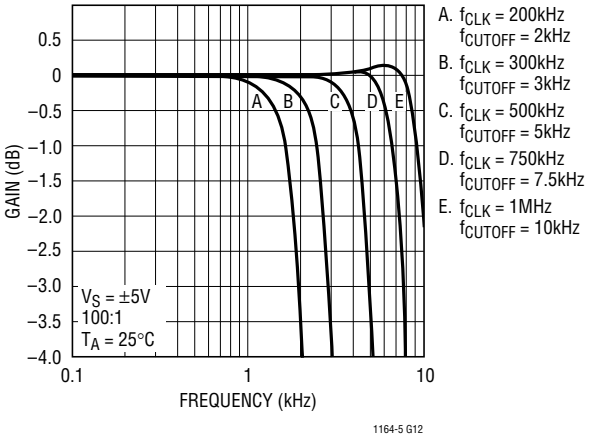
Passband vs Frequency and f_{CLK}



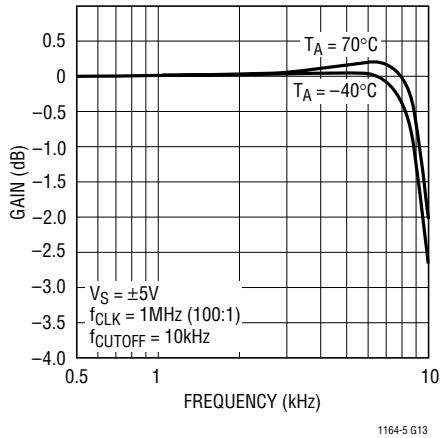
Maximum Passband over Temperature for V_S = ±5V, 50:1



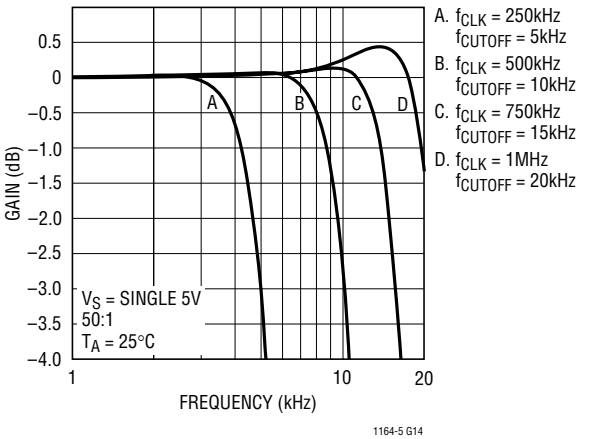
Passband vs Frequency and f_{CLK}



Maximum Passband over Temperature for V_S = ±5V, 100:1

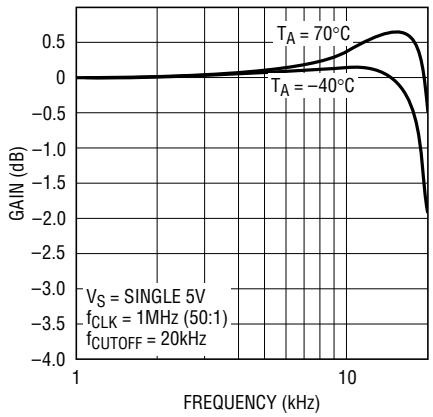


Passband vs Frequency and f_{CLK}

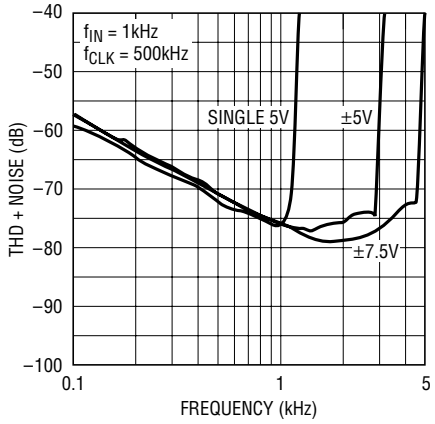


TYPICAL PERFORMANCE CHARACTERISTICS

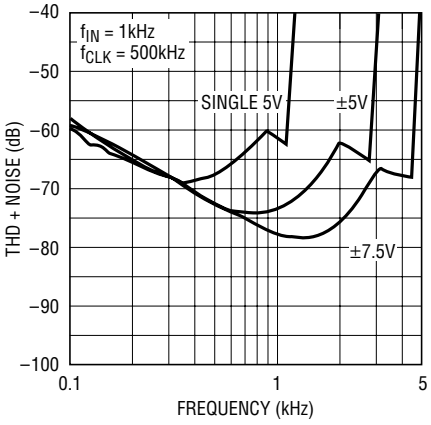
Maximum Passband over Temperature for Single 5V, 50:1*



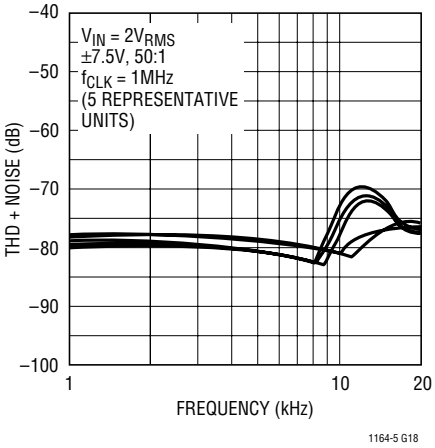
THD + Noise vs RMS Input, 50:1



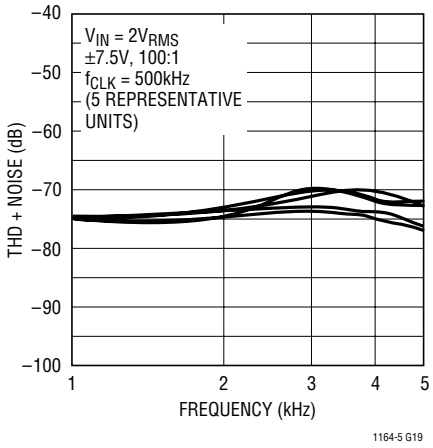
THD + Noise vs RMS Input, 100:1



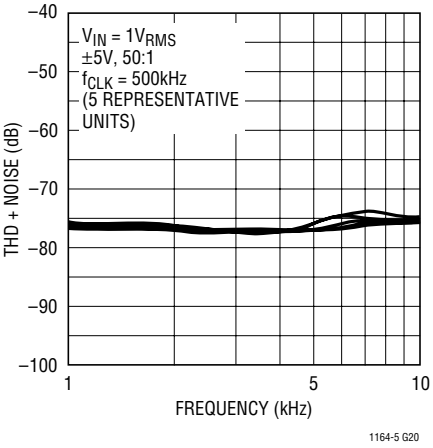
THD + Noise vs Frequency



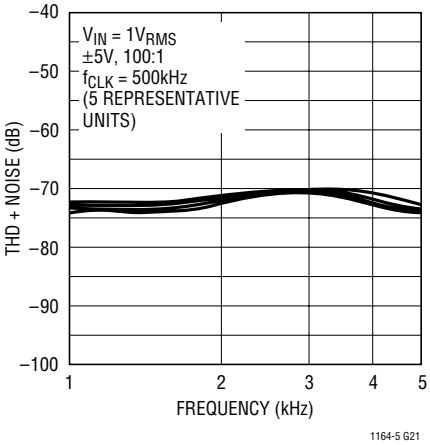
THD + Noise vs Frequency



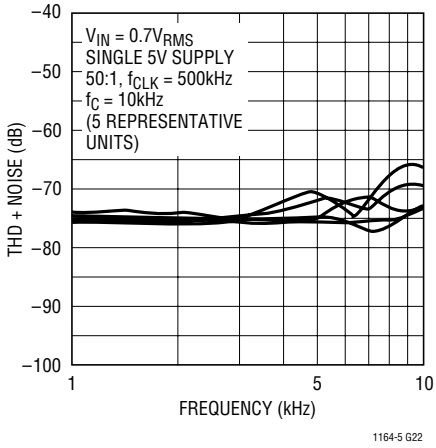
THD + Noise vs Frequency



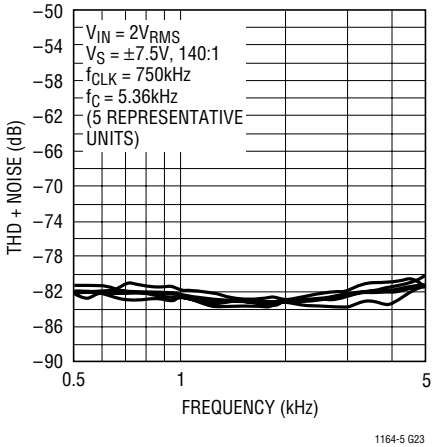
THD + Noise vs Frequency



THD + Noise vs Frequency



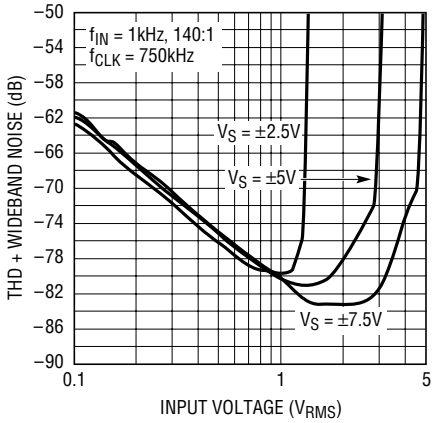
THD + Noise vs Frequency



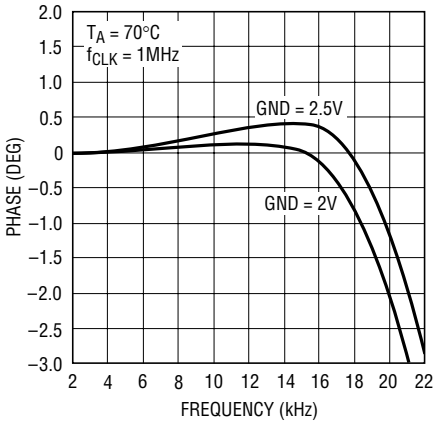
* See also Passband vs Frequency and f_{CLK} for Single 5V, 50:1; THD + Noise vs RMS Input for Single 5V, 50:1; and Maximum Passband for Single 5V, 50:1, for Two Ground Bias Levels.

TYPICAL PERFORMANCE CHARACTERISTICS

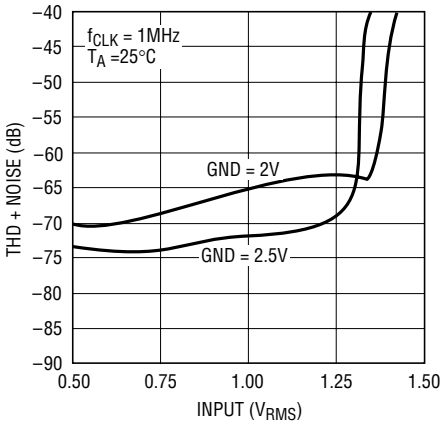
THD + Noise vs Input Voltage



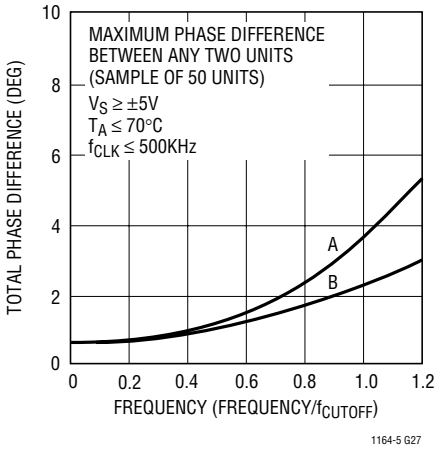
Maximum Passband for Single 5V, 50:1, for Two Ground Bias Levels



THD + Noise vs RMS Input for Single 5V, 50:1

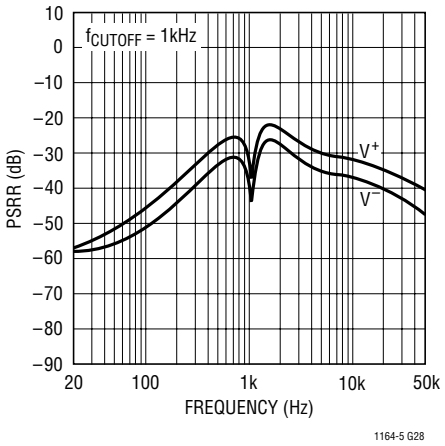


Phase Matching vs Frequency

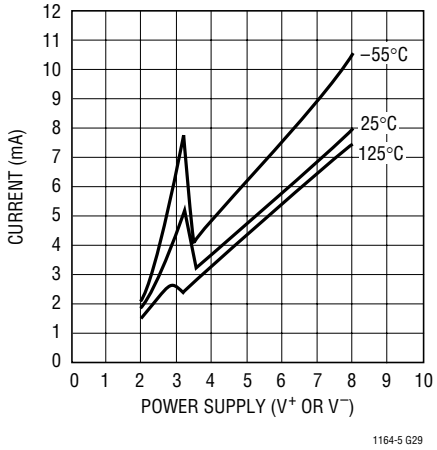


A. BUTTERWORTH (f_{CLK}/f_{CUTOFF} = 100:1 OR 50:1)
B. BESSEL (f_{CLK}/f_{CUTOFF} = 140:1)

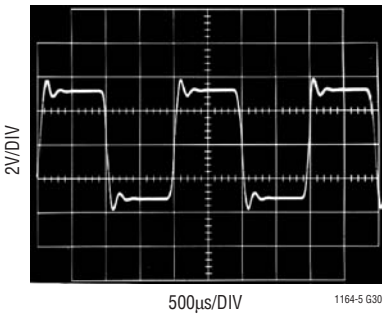
Power Supply Rejection Ratio vs Frequency



Power Supply Current vs Power Supply Voltage

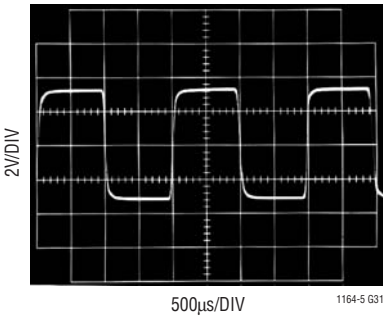


Transient Response V_{IN} = ±3V, 500Hz Square Wave



BUTTERWORTH RATIO = 100:1
f_{CLK} = 500kHz
f_C = 5kHz
V_S = ±7.5V

Transient Response V_{IN} = ±3V, 500Hz Square Wave



BESSEL RATIO = 140:1
f_{CLK} = 700kHz
f_C = 5kHz
V_S = ±7.5V

PIN FUNCTIONS

Power Supply (Pins 4, 12)

The V^+ (Pin 4) and the V^- (Pin 12) should be bypassed with a 0.1µF capacitor to an adequate analog ground. The filter's power supplies should be isolated from other digital or high voltage analog supplies. A low noise linear supply is recommended. Using a switching power supply will lower the signal-to-noise ratio of the filter. The supply during power-up should have a slew rate less than 1V/µs. When V^+ is applied before V^-, and V^- can be more positive than ground, a signal diode must be used to clamp V^-. Figures 1 and 2 show typical connections for dual and single supply operation.

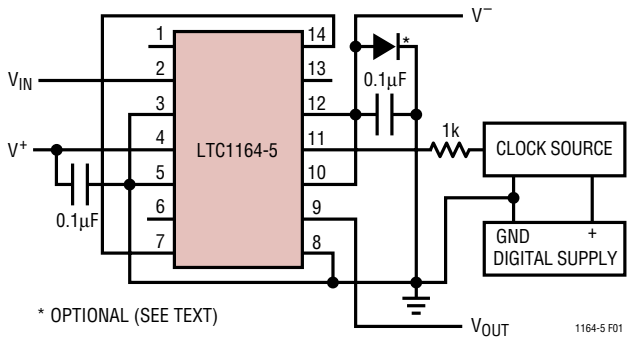


Figure 1. Dual Supply Operation for f_{CLK}/f_{CUTOFF} = 100:1

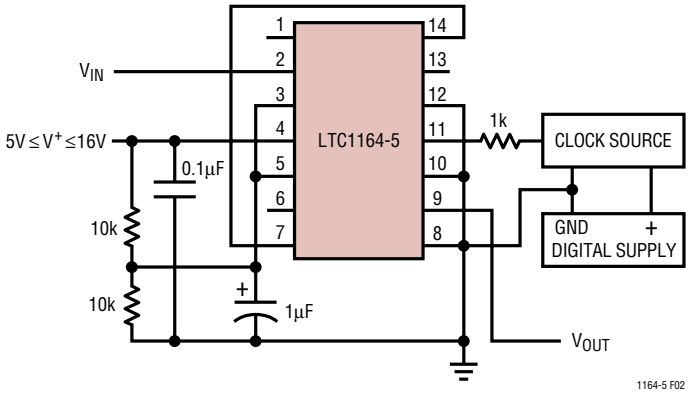


Figure 2. Single Supply Operation for f_{CLK}/f_{CUTOFF} = 100:1

Clock Input (Pin 11)

Any TTL or CMOS clock source with a square-wave output and 50% duty cycle (±10%) is an adequate clock source for the device. The power supply for the clock source should not be the filter's power supply. The analog ground for the filter should be connected to clock's ground at a single point only. Table 1 shows the clock's low and high level threshold value for a dual or single supply operation. A pulse generator can be used as a clock source provided the high level ON time is greater than 0.5µs. Sine waves are not recommended for clock input frequencies less than 100kHz, since excessively slow clock rise or fall times generate internal clock jitter (maximum clock rise or fall time ≤1µs). The clock signal should be routed from the right side of the IC package to avoid coupling into any input or output analog signal path. A 1k resistor between clock source and Pin 11 will slow down the rise and fall times of the clock to further reduce charge coupling, Figures 1 and 2.

Table 1. Clock Source High and Low Threshold Levels

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
Dual Supply > ±3.4V	$\geq V^+/3$	≤ 0.5V
Dual Supply ≤ ±3.4V	$\geq V^+/3$	$\leq V^- + 0.5V$
Single Supply V^+ > 6.8V, V^- = 0V	$\geq V^+ \bullet 0.65$	$\leq 0.5V + 1/2V^+$
Single Supply V^+ < 6.8V, V^- = 0V	$\geq V^+/3$	≤ 0.5V

Analog Ground (Pins 3, 5)

The filter performance depends on the quality of the analog signal ground. For either dual or single supply operation, an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For dual supply operation, Pins 3 and 5 should be connected to the analog ground plane. For single supply operation Pins 3 and 5 should be biased at 1/2 supply and they should be bypassed to the analog ground plane with at least a 1µF capacitor (Figure 2). For single 5V operation at the highest f_{CLK} of 1MHz, Pins 3 and 5 should be biased at 2V. This minimizes passband gain and phase variations (see Typical Performance Characteristics curves: Maximum Passband for Single 5V, 50:1; and THD + Noise vs RMS Input for Single 5V, 50:1).

PIN FUNCTIONS

Butterworth/Bessel (Pin 10)

The DC level at Pin 10 determines the ratio of the clock frequency to the cutoff frequency of the filter. Pin 10 at V^+ gives a 50:1 ratio and a Butterworth response (pins 1 to 13 are shorted for 50:1 only). Pin 10 at V^- gives a 100:1 Butterworth response. Pin 10 at ground gives a Bessel response and a ratio of 140:1. For single supply operation the ratio is 50:1 when Pin 10 is at V^+ (Pins 1 to 13 shorted), 100:1 when Pin 10 is at ground, and 140:1 when at 1/2 supply. When Pin 10 is not tied to ground, it should be bypassed to analog ground with a 0.1µF capacitor. If the DC level at Pin 10 is switched mechanically or electrically at slew rates greater than 1V/µs while the device is operating, a 10k resistor should be connected between Pin 10 and the DC source.

Filter Input (Pin 2)

The input pin is connected internally through a 100k resistor tied to the inverting input of an op amp.

Filter Output (Pins 9, 6)

Pin 9 is the specified output of the filter; it can typically source or sink 1mA. Driving coaxial cables or resistive loads less than 20k will degrade the total harmonic distortion of the filter. When evaluating the device's distortion an output buffer is required. A noninverting buffer, Figure 3, can be used provided that its input common mode range is well within the filter's output swing. Pin 6 is an intermediate filter output providing an unspecified 6th order lowpass filter. Pin 6 should not be loaded.

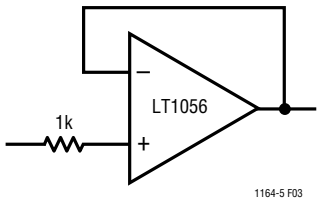


Figure 3. Buffer for Filter Output

External Connection (Pins 7, 14 and 1, 13)

Pins 7 and 14 should be connected together. In a printed circuit board the connection should be done under the IC package through a short trace surrounded by the analog ground plane. When the clock to cutoff frequency ratio is set at 50:1, Pin 1 should be shorted to Pin 13; if not, the passband will exhibit 1dB of gain peaking and it will deviate from a Butterworth response. Pin 1 is the inverting input of an internal op amp and it should preferably be 0.2 inches away from any other circuit trace.

NC (Pin 8)

Pin 8 is not connected to any internal circuit point on the device and should be preferably tied to analog ground.

APPLICATIONS INFORMATION

Clock Feedthrough

Clock feedthrough is defined as, the RMS value of the clock frequency and its harmonics that are present at the filter's output pin (Pin 9). The clock feedthrough is tested with the input pin (Pin 2) grounded and, it depends on PC board layout and on the value of the power supplies. With proper layout techniques the values of the clock feedthrough are shown in Table 2.

Table 2. Output Clock Feedthrough

V_S	50:1	100:1
±2.5V	$60\mu V_{RMS}$	$60\mu V_{RMS}$
±5V	$100\mu V_{RMS}$	$200\mu V_{RMS}$
±7.5V	$150\mu V_{RMS}$	$500\mu V_{RMS}$

Note: The clock feedthrough at ±2.5V supplies is imbedded in the wideband noise of the filter. The clock waveform is a square wave.

APPLICATIONS INFORMATION

Any parasitic switching transients during the rise and fall edges of the incoming clock are not part of the clock feedthrough specifications. Switching transients have frequency contents much higher than the applied clock; their amplitude strongly depends on scope probing techniques as well as grounding and power supply bypassing. The clock feedthrough, if bothersome, can be greatly reduced by adding a simple R/C lowpass network at the output of the filter pin (Pin 9). This R/C will completely eliminate any switching transient.

Wideband Noise

The wideband noise of the filter is the total RMS value of the device's noise spectral density and it is used to determine the operating signal-to-noise ratio. Most of its frequency contents lie within the filter passband and it cannot be reduced with post filtering. For instance, the LTC1164-5 wideband noise at ±2.5V supply is $100\mu V_{RMS}$, $95\mu V_{RMS}$ of which have frequency contents from DC up to the filter's cutoff frequency. The total wideband noise (μRMS) is nearly independent of the value of the clock. The clock feedthrough specifications are not part of the wideband noise.

Speed Limitations

The LTC1164-5 optimizes AC performance versus power consumption. To avoid op amp slew rate limiting at maximum clock frequencies, the signal amplitude should be kept below a specified level as shown in Table 3.

Table 3. Maximum V_{IN} vs V_S and f_{CLK}

POWER SUPPLY	MAXIMUM f_{CLK}	MAXIMUM V_{IN}
V_S = ±7.5V	1.5MHz	$1V_{RMS}$ (f_{IN} > 35kHz) $0.5V_{RMS}$ (f_{IN} > 250kHz)
V_S = ±7.5V	1.0MHz	$3V_{RMS}$ (f_{IN} > 25kHz) $0.7V_{RMS}$ (f_{IN} > 250kHz)
V_S = ±5.0V	1.0MHz	$2.5V_{RMS}$ (f_{IN} > 25kHz) $0.5V_{RMS}$ (f_{IN} > 100kHz)
Single 5V	1.0MHz	$0.7V_{RMS}$ (f_{IN} > 25kHz) $0.5V_{RMS}$ (f_{IN} > 100kHz)

Aliasing

Aliasing is an inherent phenomenon of sampled data systems and it occurs when input frequencies close to the sampling frequency are applied. For the LTC1164-5 case at 100:1, an input signal whose frequency is in the range of f_{CLK} ±2.5% will be aliased back into the filter's passband. If, for instance, an LTC1164-5 operating with a 100kHz clock and 1kHz cutoff frequency receives a 98kHz 10mV input signal, a 2kHz 56μV alias signal will appear at its output. When the LTC1164-5 operates with a clock-to-cutoff frequency of 50:1, aliasing occurs at twice the clock frequency. Table 4 shows details.

Table 4. Aliasing Data (f_{CLK} = 100kHz, V_S = ±5V)

INPUT FREQUENCY (V_{IN} = $1V_{RMS}$)	OUTPUT LEVEL (Relative to Input)	OUTPUT FREQUENCY (Aliased Frequency)
(f_{CLK}/f_C) = 100:1, f_{CUTOFF} = 1kHz		
97.0kHz	–102.0dB	3.0kHz
97.5kHz	–65.0dB	2.5kHz
98.0kHz	–45.0dB	2.0kHz
98.5kHz	–23.0dB	1.5kHz
99.0kHz	–4.0dB	1.0kHz
99.5kHz	–0.3dB	0.5kHz
(f_{CLK}/f_C) = 50:1, f_{CUTOFF} = 2kHz		
197.0kHz	–23.0dB	3.0kHz
197.5kHz	–12.0dB	2.5kHz
198.0kHz	–5.0dB	2.0kHz
198.5kHz	–1.8dB	1.5kHz
199.0kHz	–1.0dB	1.0kHz
199.5kHz	–0.8dB	0.5kHz

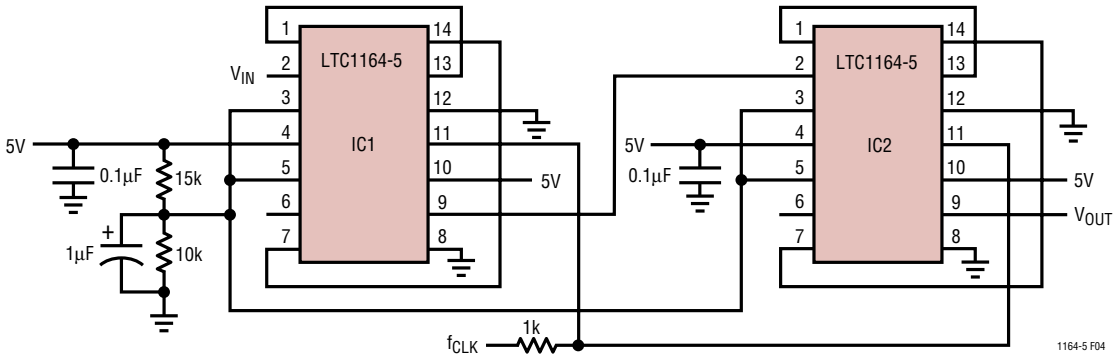
Table 5. Transient Response of LTC Lowpass Filters

LOWPASS FILTER	DELAY TIME* (SEC)	RISE TIME** (SEC)	SETTLING TIME*** (SEC)	OVER-SHOOT (%)
LTC1064-3 Bessel	$0.50/f_C$	$0.34/f_C$	$0.80/f_C$	0.5
LTC1164-5 Bessel	$0.43/f_C$	$0.34/f_C$	$0.85/f_C$	0
LTC1164-6 Bessel	$0.43/f_C$	$0.34/f_C$	$1.15/f_C$	1
LTC1264-7 Linear Phase	$1.15/f_C$	$0.36/f_C$	$2.05/f_C$	5
LTC1164-7 Linear Phase	$1.20/f_C$	$0.39/f_C$	$2.20/f_C$	5
LTC1064-7 Linear Phase	$1.20/f_C$	$0.39/f_C$	$2.20/f_C$	5
LTC1164-5 Butterworth	$0.80/f_C$	$0.48/f_C$	$2.40/f_C$	11
LTC1164-6 Elliptic	$0.85/f_C$	$0.54/f_C$	$4.30/f_C$	18
LTC1064-4 Elliptic	$0.90/f_C$	$0.54/f_C$	$4.50/f_C$	20
LTC1064-1 Elliptic	$0.85/f_C$	$0.54/f_C$	$6.50/f_C$	20

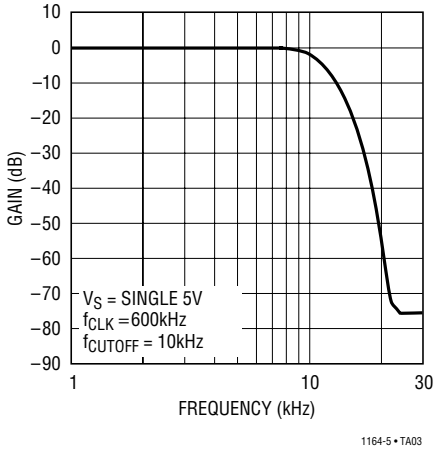
* To 50% ±5%, ** 10% to 90% ±5%, *** To 1% ±0.5%

TYPICAL APPLICATIONS

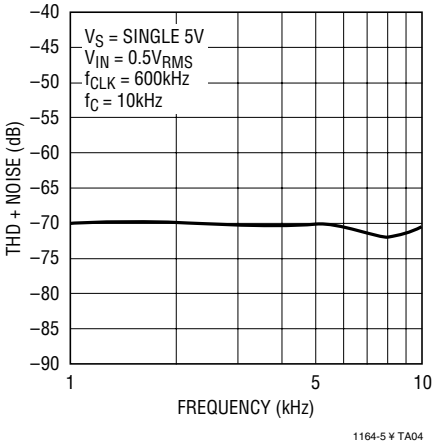
Single 5V, I_S = 5.2mA, 16th Order Clock-Tunable Lowpass Filter, f_{CLK}/f_{CUTOFF} = 60:1, –75dB Attenuation at 2.3 f_{CUTOFF}



Gain vs Frequency

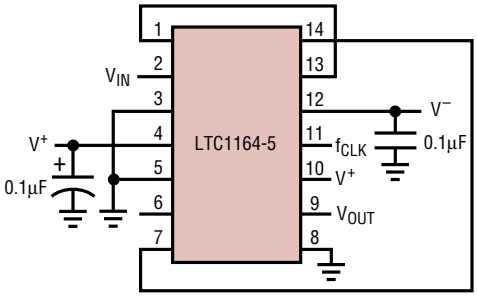


THD + Noise vs Frequency



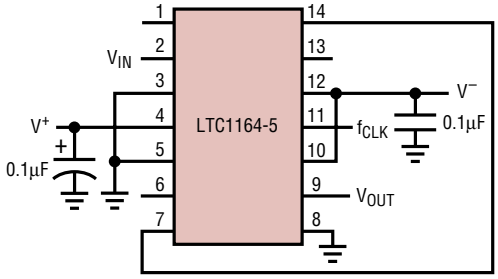
TYPICAL APPLICATIONS

8th Order Butterworth Lowpass Filter
f_{CLK}/f_C = 50:1



1164-5 TA05

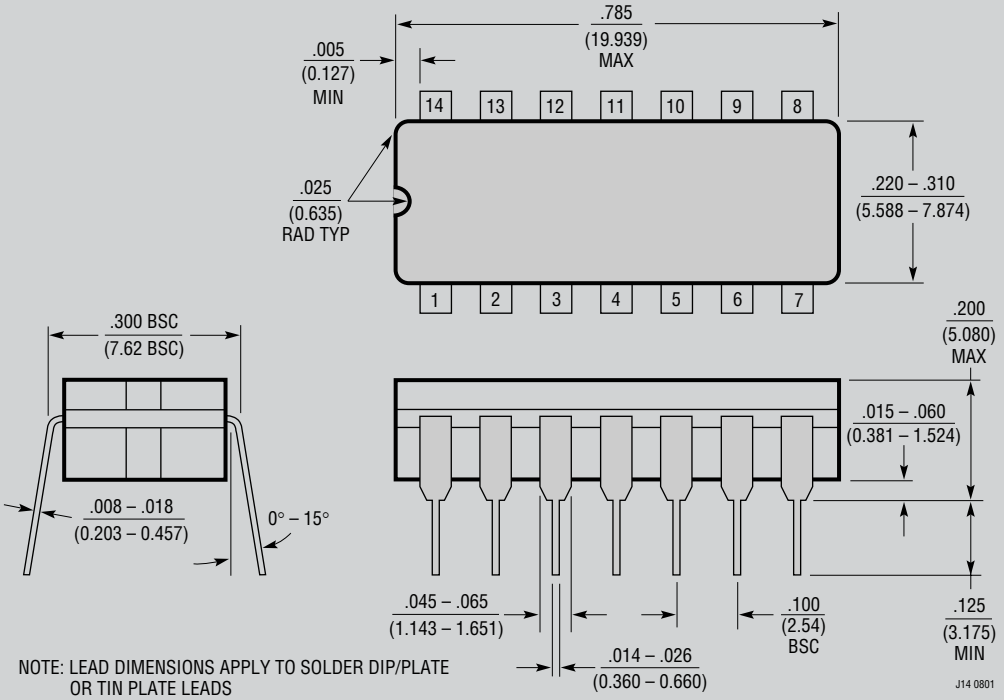
8th Order Butterworth Lowpass Filter
f_{CLK}/f_C = 100:1



1164-5 TA06

PACKAGE DESCRIPTION

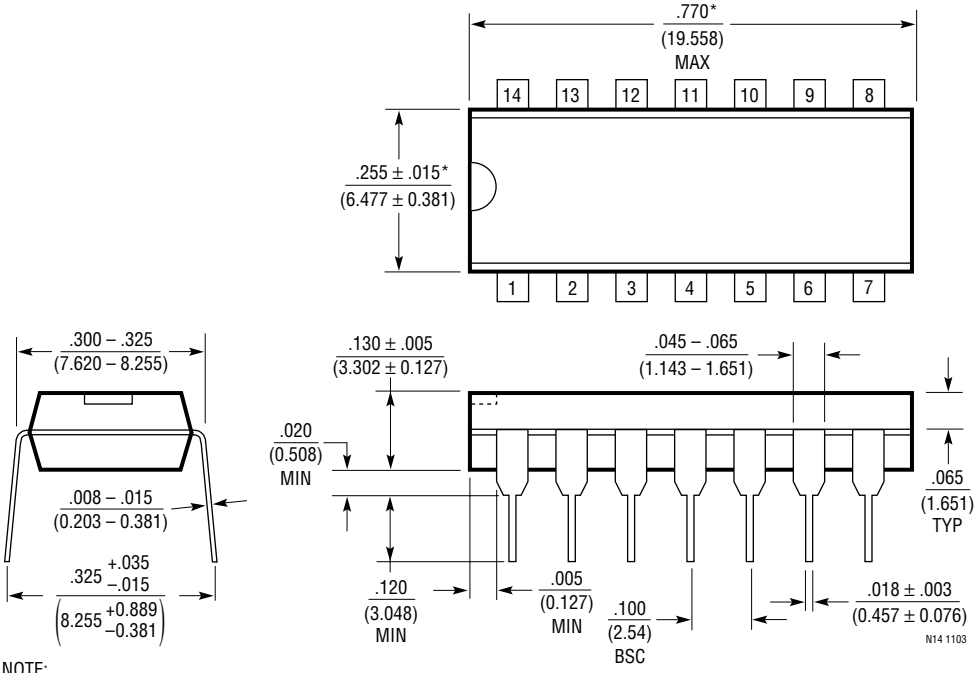
J Package
14-Lead CERDIP (Narrow 0.300, Hermetic)
(LTC DWG # 05-08-1110)



OBSOLETE PACKAGE

PACKAGE DESCRIPTION

N Package
14-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

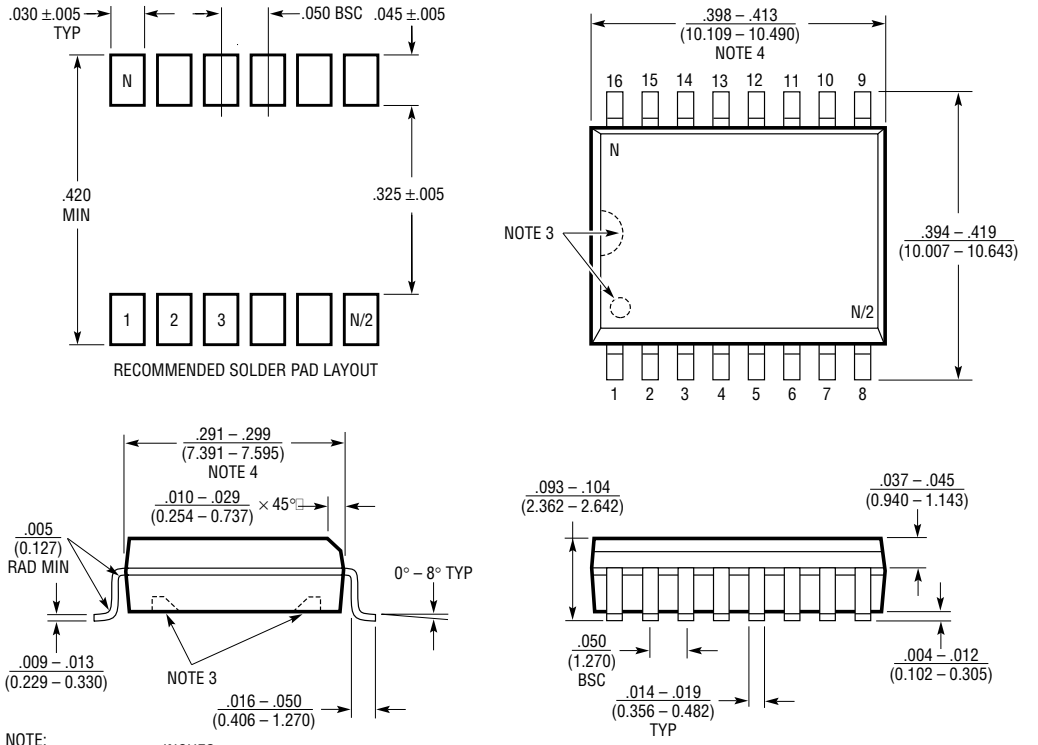


NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

SW Package
16-Lead Plastic Small Outline (Wide 0.300)
(LTC DWG # 05-08-1620)

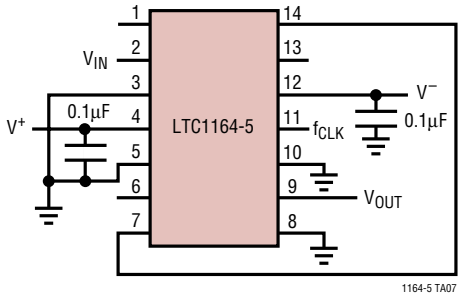


NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

8th Order Linear Phase Lowpass Filter
f_{CLK}/f_C = 140:1



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1069-1	Low Power, 8th Order Elliptic Lowpass Filter	Operates from a Single 3.3V to ±5V Supply
LTC1069-6	Very Low Power, 8th Order Elliptic Lowpass Filter	Optimized for 3V/5V Single Supply Operation, Consumes 1mA at 3V

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

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