WINSOURCE ELECTRONICS

THE DATASHEET OF

LT1794IFE#PBF

Dual 500mA, 200MHz xDSL Line Driver Amplifier

FEATURES

- **Exceeds All Requirements For Full Rate, Downstream ADSL Line Drivers**
- **±500mA Minimum I_{OUT}**
- **±11.1V Output Swing, V_S = ±12V, R_L = 100Ω**
- **±10.9V Output Swing, V_S = ±12V, I_L = 250mA**
- **Low Distortion: –82dBc at 1MHz, $2V_{P-P}$ Into 50Ω**
- Power Saving Adjustable Supply Current
- Power Enhanced Small Footprint Packages: 20-Lead TSSOP and 20-Lead SW
- 200MHz Gain Bandwidth
- 500V/µs Slew Rate
- Specified at ±15V, ±12V and ±5V

APPLICATIONS

- High Density ADSL Central Office Line Drivers
- High Efficiency ADSL, HDSL2, G.lite, SHDSL Line Drivers
- Buffers
- Test Equipment Amplifiers
- Cable Drivers

DESCRIPTION

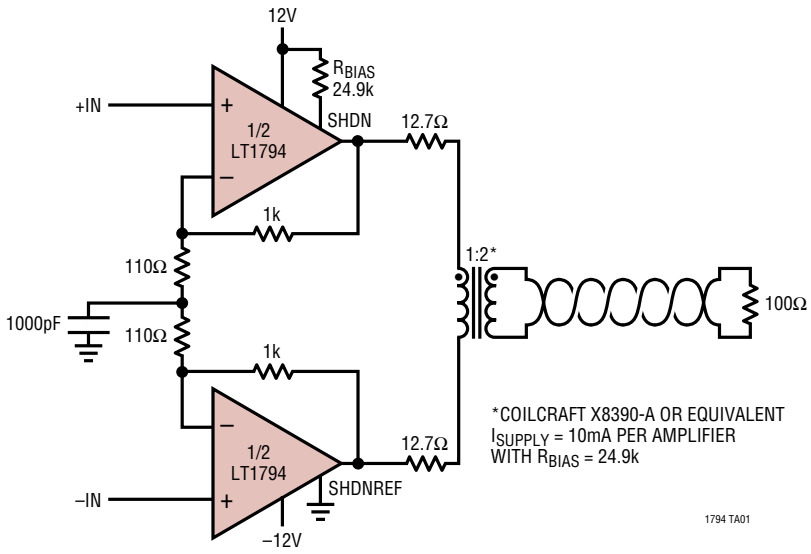
The LT®1794 is a 500mA minimum output current, dual op amp with outstanding distortion performance. The amplifiers are gain-of-ten stable, but can be easily compensated for lower gains. The extended output swing allows for lower supply rails to reduce system power. Supply current is set with an external resistor to optimize power dissipation. The LT1794 features balanced, high impedance inputs with low input bias current and input offset voltage. Active termination is easily implemented for further system power reduction. Short-circuit protection and thermal shutdown insure the device's ruggedness.

The outputs drive a 100Ω load to ±11.1V with ±12V supplies, and ±10.9V with a 250mA load. The LT1794, with its increased swing on lower supplies, can be used to upgrade LT1795 line driver applications.

The LT1794 is available in the very small, thermally enhanced, 20-lead TSSOP for maximum port density in line driver applications. The 20-lead SW is also available.

TYPICAL APPLICATION

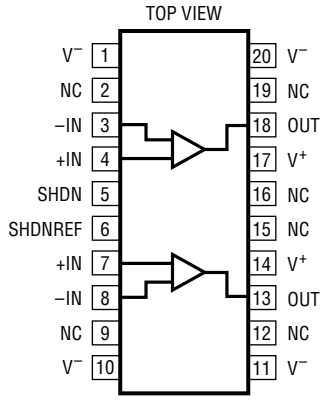
High Efficiency ±12V Supply ADSL Central Office Line Driver



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V^+ to V^-) ..... ±18V
Input Current ..... ±10mA
Output Short-Circuit Duration (Note 2) ..... Indefinite
Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range (Note 3) .. –40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

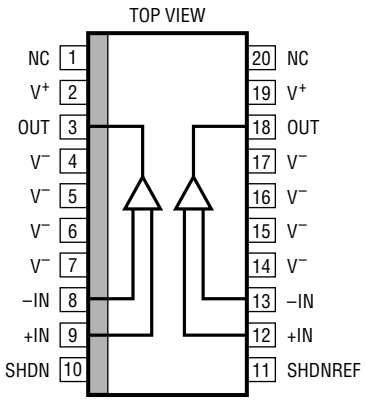


FE PACKAGE
20-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JA} = 40°C/W, θ_{JC} = 3°C/W (Note 4)
UNDERSIDE METAL CONNECTED TO V^-

ORDER PART NUMBER

LT1794CFE
LT1794IFE



SW PACKAGE
20-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 40°C/W, θ_{JC} = 3°C/W (Note 4)

ORDER PART NUMBER

LT1794CSW
LT1794ISW

Consult factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. V_{CM} = 0V, pulse tested, ±5V ≤ V_S ≤ ±15V, $V_{SHDNREF}$ = 0V, R_{BIAS} = 24.9k between V^+ and SHDN unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		 ●		1	5.0 7.5	mV mV
	Input Offset Voltage Matching		 ●		0.3	5.0 7.5	mV mV
	Input Offset Voltage Drift		●		10		µV/°C
I_{OS}	Input Offset Current		 ●		100	500 800	nA nA
I_B	Input Bias Current		 ●		±0.1	±4 ±6	µA µA
	Input Bias Current Matching		 ●		100	500 800	nA nA
e_n	Input Noise Voltage Density	f = 10kHz			8		nV/√Hz
i_n	Input Noise Current Density	f = 10kHz			0.8		pA/√Hz
R_{IN}	Input Resistance	V_{CM} = (V^+ – 2V) to (V^- + 2V) Differential	●	5	50 6.5		MΩ MΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. V_{CM} = 0V, pulse tested, ±5V ≤ V_S ≤ ±15V, $V_{SHDNREF}$ = 0V, R_{BIAS} = 24.9k between V^+ and SHDN unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance				3		pF
	Input Voltage Range (Positive) Input Voltage Range (Negative)	(Note 5) (Note 5)	● ●	$V^+ - 2$	$V^+ - 1$ $V^- + 1$	 $V^- + 2$	V V
CMRR	Common Mode Rejection Ratio	V_{CM} = ($V^+ - 2V$) to ($V^- + 2V$)	 ●	74 66	83		dB dB
PSRR	Power Supply Rejection Ratio	V_S = ±4V to ±15V	 ●	74 66	88		dB dB
A_{VOL}	Large-Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±13V, R_L = 100Ω	 ●	70 64	82		dB dB
		V_S = ±12V, V_{OUT} = ±10V, R_L = 40Ω	 ●	63 57	76		dB dB
		V_S = ±5V, V_{OUT} = ±3V, R_L = 25Ω	 ●	60 54	70		dB dB
V_{OUT}	Output Swing	V_S = ±15V, R_L = 100Ω	 ●	13.8 13.6	14.0		±V ±V
		V_S = ±15V, I_L = 250mA	 ●	13.6 13.4	13.9		±V ±V
		V_S = ±12V, R_L = 100Ω	 ●	10.9 10.7	11.1		±V ±V
		V_S = ±12V, I_L = 250mA	 ●	10.6 10.4	10.9		±V ±V
		V_S = ±5V, R_L = 25Ω	 ●	3.7 3.5	4.0		±V ±V
		V_S = ±5V, I_L = 250mA	 ●	3.6 3.4	3.9		±V ±V
I_{OUT}	Maximum Output Current	V_S = ±15V, R_L = 1Ω		500	720		mA
I_S	Supply Current per Amplifier	V_S = ±15V, R_{BIAS} = 24.9k (Note 6)	 ●	10 8	13	18 20	mA mA
		V_S = ±12V, R_{BIAS} = 24.9k (Note 6) V_S = ±12V, R_{BIAS} = 32.4k (Note 6) V_S = ±12V, R_{BIAS} = 43.2k (Note 6) V_S = ±12V, R_{BIAS} = 66.5k (Note 6)	 ● 	8.0 6.7	10 8 6 4	13.5 15.0	mA mA mA mA mA
		V_S = ±5V, R_{BIAS} = 24.9k (Note 6)	 ●	2.2 1.8	3.4	5.0 5.8	mA mA
	Supply Current in Shutdown	V_{SHDN} = 0.4V			0.1	1	mA
	Output Leakage in Shutdown	V_{SHDN} = 0.4V			0.3	1	mA
	Channel Separation	V_S = ±12V, V_{OUT} = ±10V, R_L = 40Ω	 ●	80 77	110		dB dB
SR	Slew Rate	V_S = ±15V, A_V = –10, (Note 7)		300	600		V/µs
		V_S = ±5V, A_V = –10, (Note 7)		100	200		V/µs
HD2	Differential 2nd Harmonic Distortion	V_S = ±12V, A_V = 10, $2V_{P-P}$, R_L = 50Ω, 1MHz			–85		dBc
HD3	Differential 3rd Harmonic Distortion	V_S = ±12V, A_V = 10, $2V_{P-P}$, R_L = 50Ω, 1MHz			–82		dBc
GBW	Gain Bandwidth	f = 1MHz			200		MHz

ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Applies to short circuits to ground only. A short circuit between the output and either supply may permanently damage the part when operated on supplies greater than ±10V.

Note 3: The LT1794C is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet these extended temperature limits, but is not tested at –40°C and 85°C. The LT1794I is guaranteed to meet the extended temperature limits.

Note 4: Thermal resistance varies depending upon the amount of PC board metal attached to the device. If the maximum dissipation of the package is exceeded, the device will go into thermal shutdown and be protected.

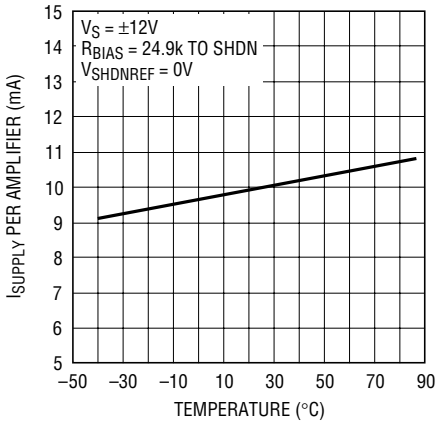
Note 5: Guaranteed by the CMRR tests.

Note 6: R_{BIAS} is connected between V^+ and the SHDN pin.

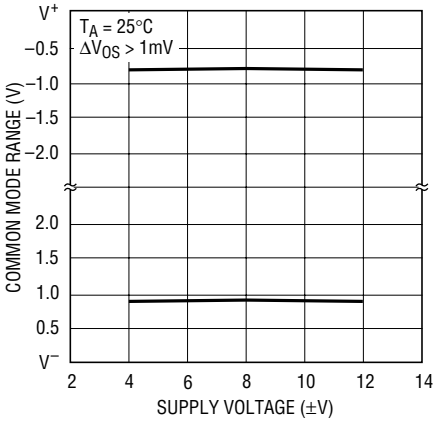
Note 7: Slew rate is measured at ±5V on a ±10V output signal while operating on ±15V supplies and ±1V on a ±3V output signal while operating on ±5V supplies.

TYPICAL PERFORMANCE CHARACTERISTICS

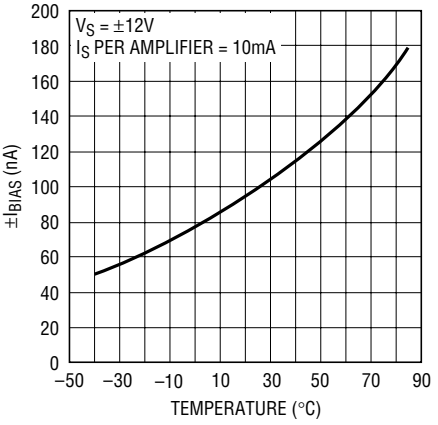
Supply Current vs Ambient Temperature



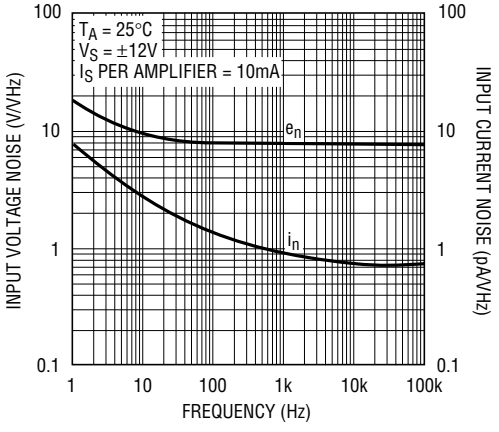
Input Common Mode Range vs Supply Voltage



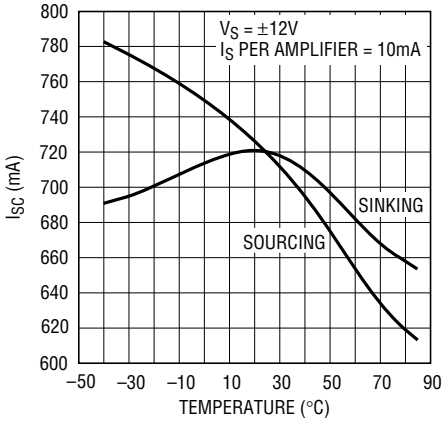
Input Bias Current vs Ambient Temperature



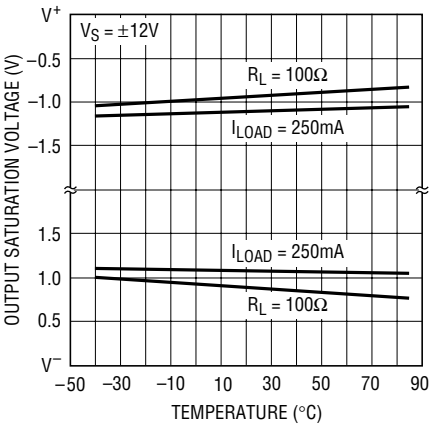
Input Noise Spectral Density



Output Short-Circuit Current vs Ambient Temperature

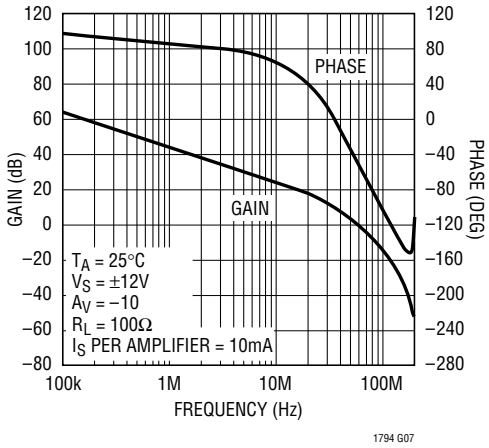


Output Saturation Voltage vs Ambient Temperature

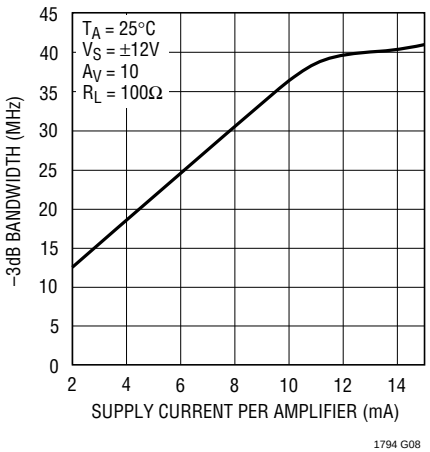


TYPICAL PERFORMANCE CHARACTERISTICS

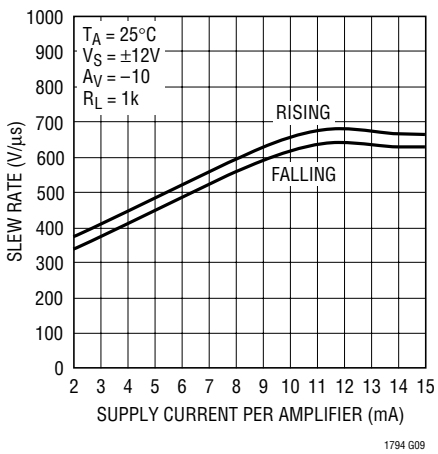
Open-Loop Gain and Phase vs Frequency



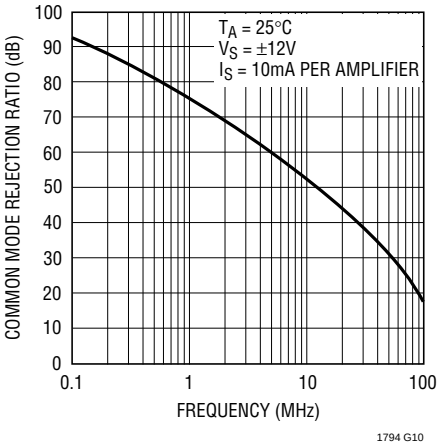
–3dB Bandwidth vs Supply Current



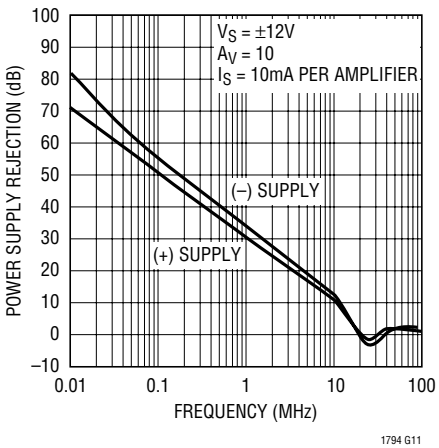
Slew Rate vs Supply Current



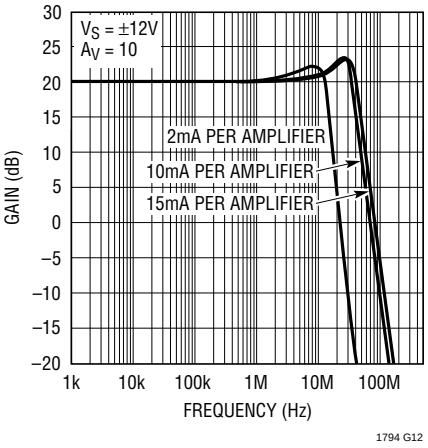
CMRR vs Frequency



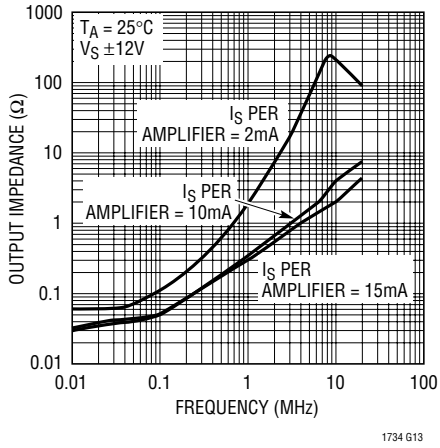
PSRR vs Frequency



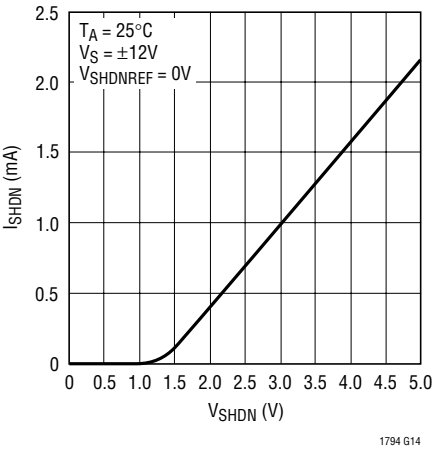
Frequency Response vs Supply Current



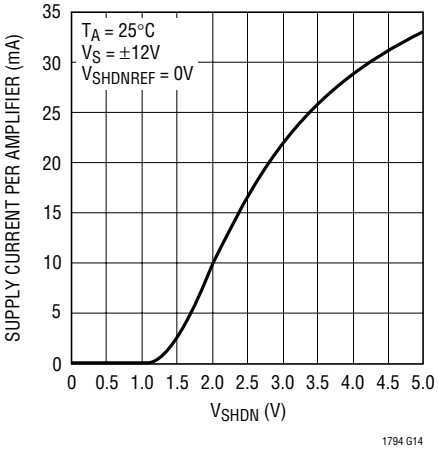
Output Impedance vs Frequency



I_{SHDN} vs V_{SHDN}

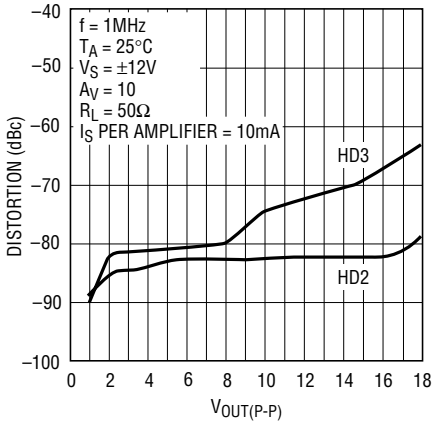


Supply Current vs V_{SHDN}



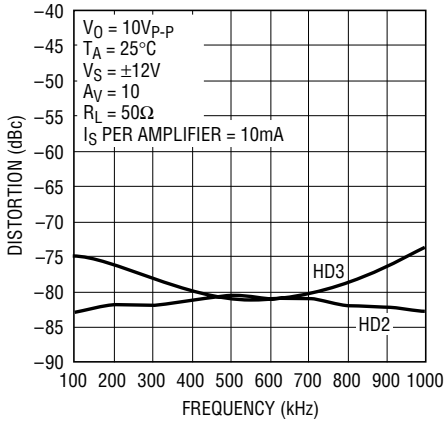
TYPICAL PERFORMANCE CHARACTERISTICS

Differential Harmonic Distortion vs Output Amplitude



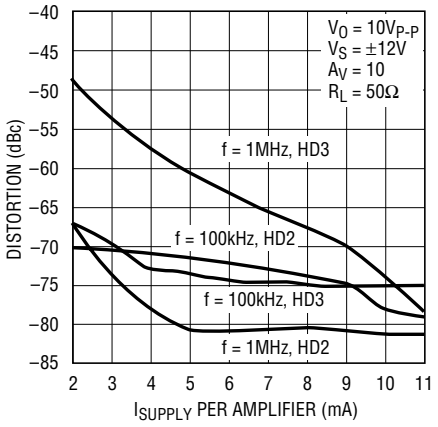
1794 G16

Differential Harmonic Distortion vs Frequency



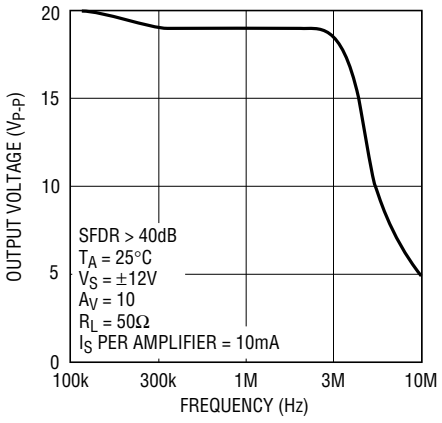
1794 G17

Differential Harmonic Distortion vs Supply Current



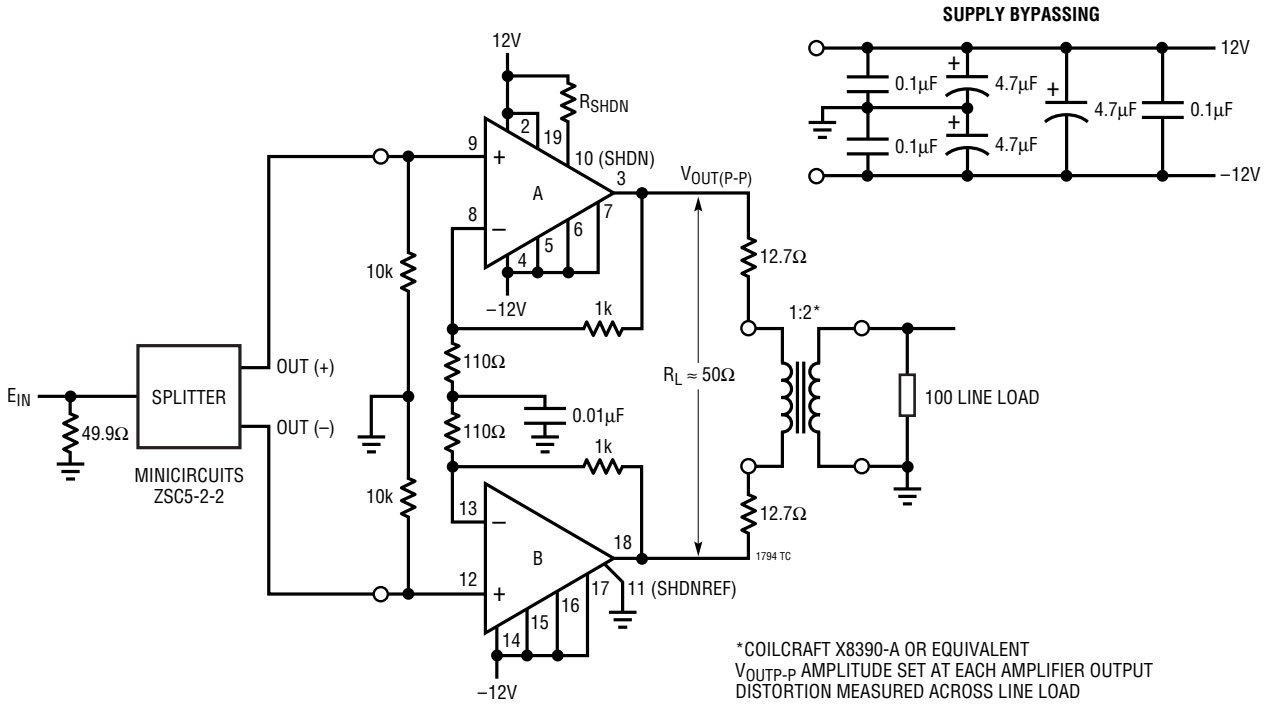
1794 G18

Undistorted Output Swing vs Frequency



1794 G19

TEST CIRCUIT



APPLICATIONS INFORMATION

The LT1794 is a high speed, 200MHz gain bandwidth product, dual voltage feedback amplifier with high output current drive capability, 500mA source and sink. The LT1794 is ideal for use as a line driver in xDSL data communication applications. The output voltage swing has been optimized to provide sufficient headroom when operating from ±12V power supplies in full-rate ADSL applications. The LT1794 also allows for an adjustment of the operating current to minimize power consumption. In addition, the LT1794 is available in small footprint surface mount packages to minimize PCB area in multiport central office DSL cards.

To minimize signal distortion, the LT1794 amplifiers are decompensated to provide very high open-loop gain at high frequency. As a result each amplifier is frequency stable with a closed-loop gain of 10 or more. If a closed-loop gain of less than 10 is desired, external frequency compensating components can be used.

Setting the Quiescent Operating Current

Power consumption and dissipation are critical concerns in multiport xDSL applications. Two pins, Shutdown (SHDN) and Shutdown Reference (SHDNREF), are provided to control quiescent power consumption and allow for the complete shutdown of the driver. The quiescent current should be set high enough to prevent distortion induced errors in a particular application, but not so high that power is wasted in the driver unnecessarily. A good starting point to evaluate the LT1794 is to set the quiescent current to 10mA per amplifier.

The internal biasing circuitry is shown in Figure 1. Grounding the SHDNREF pin and directly driving the SHDN pin with a voltage can control the operating current as seen in the Typical Performance Characteristics. When the SHDN pin is less than SHDNREF + 0.4V, the driver is shut down and consumes typically only 100µA of supply current and the

APPLICATIONS INFORMATION

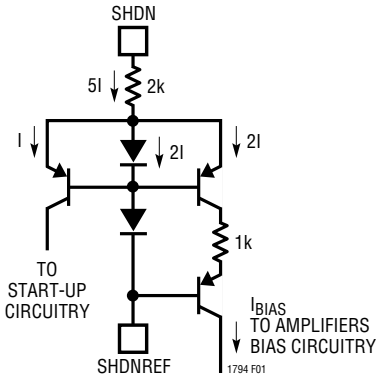


Figure 1. Internal Current Biasing Circuitry

outputs are in a high impedance state. Part to part variations however, will cause inconsistent control of the quiescent current if direct voltage drive of the SHDN pin is used.

Using a single external resistor, R_{BIAS}, connected in one of two ways provides a much more predictable control of the quiescent supply current. Figure 2 illustrates the effect on supply current per amplifier with R_{BIAS} connected between the SHDN pin and the 12V V^+ supply of the LT1794 and the approximate design equations. Figure 3 illustrates the same control with R_{BIAS} connected between the SHDNREF pin and ground while the SHDN pin is tied to V^+. Either approach is equally effective.

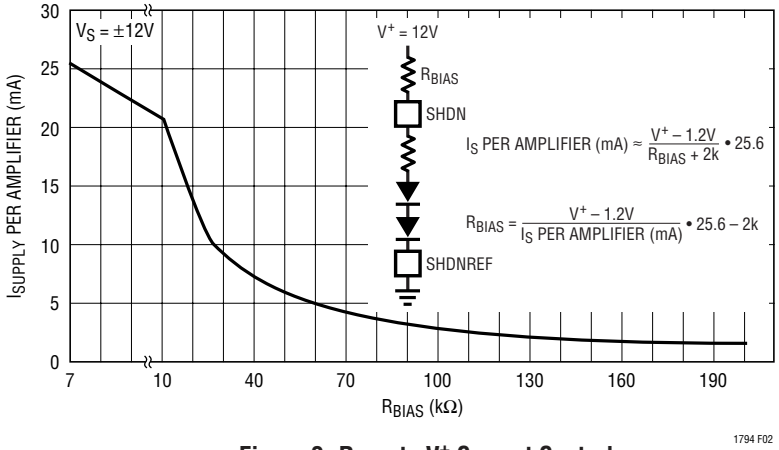


Figure 2. R_{BIAS} to V^+ Current Control

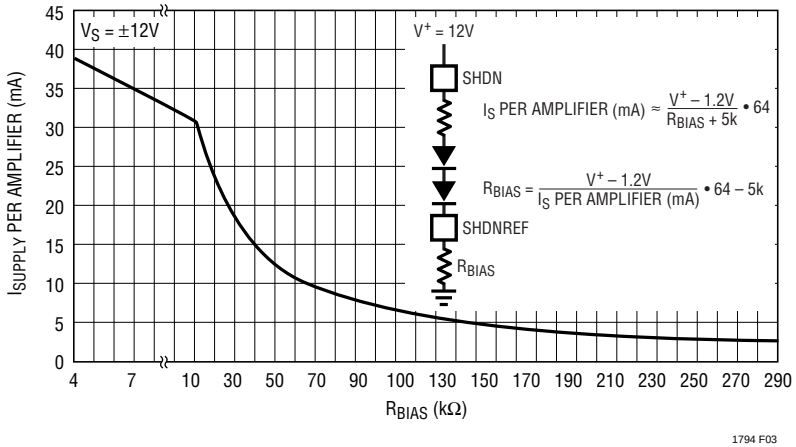


Figure 3. R_{BIAS} to Ground Current Control

APPLICATIONS INFORMATION

Logic Controlled Operating Current

The DSP controller in a typical xDSL application can have I/O pins assigned to provide logic control of the LT1794 line driver operating current. As shown in Figure 4 one or two logic control inputs can control two or four different operating modes. The logic inputs add or subtract current to the SHDN input to set the operating current. The one logic input example selects the supply current to be either full power, 10mA per amplifier or just 2mA per amplifier, which significantly reduces the driver power consumption while maintaining less than 2Ω output impedance to frequencies less than 1MHz. This low power mode retains termination impedance at the amplifier outputs and the line driving back termination resistors. With this termination, while a DSL port is not transmitting data, it can still sense a received signal from the line across the back-termination resistors and respond accordingly.

The two logic input control provides two intermediate (approximately 7mA per amplifier and 5mA per amplifier) operating levels between full power and termination modes. These modes can be useful for overall system power management when full power transmissions are not necessary.

Shutdown and Recovery

The ultimate power saving action on a completely idle port is to fully shut down the line driver by pulling the SHDN pin to within 0.4V of the SHDNREF potential. As shown in Figure 5 complete shutdown occurs in less than 10µs and, more importantly, complete recovery from the shut down state to full operation occurs in less than 2µs. The biasing circuitry in the LT1794 reacts very quickly to bring the amplifiers back to normal operation.

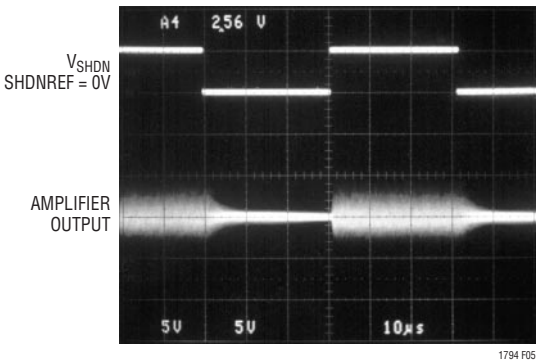


Figure 5. Shutdown and Recovery Timing

Two Control Inputs

		RESISTOR VALUES (kΩ)					
		R_{SHDN} TO V_{CC} (12V)			R_{SHDN} TO V_{LOGIC}		
	V_{LOGIC}	3V	3.3V	5V	3V	3.3V	5V
	R_{SHDN}	40.2	43.2	60.4	4.99	6.81	19.6
	R_{C1}	11.5	13.0	21.5	8.66	10.7	20.5
	R_{C0}	19.1	22.1	36.5	14.3	17.8	34.0
V_{C1}	V_{C0}	SUPPLY CURRENT PER AMPLIFIER (mA)					
H	H	10	10	10	10	10	10
H	L	7	7	7	7	7	7
L	H	5	5	5	5	5	5
L	L	2	2	2	2	2	2

One Control Input

		RESISTOR VALUES (kΩ)					
		R_{SHDN} TO V_{CC} (12V)			R_{SHDN} TO V_{LOGIC}		
	V_{LOGIC}	3V	3.3V	5V	3V	3.3V	5V
	R_{SHDN}	40.2	43.2	60.4	4.99	6.81	19.6
	R_C	7.32	8.25	13.7	5.49	6.65	12.7
	V_C	SUPPLY CURRENT PER AMPLIFIER (mA)					
H		10	10	10	10	10	10
L		2	2	2	2	2	2

1794 F04

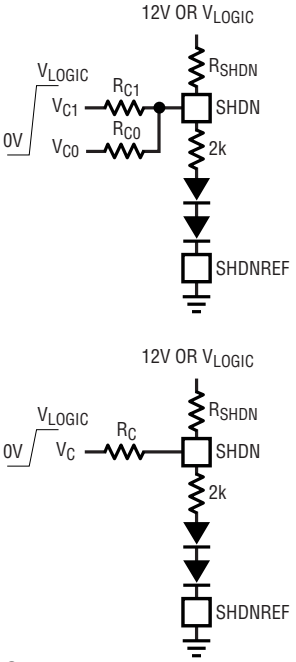


Figure 4. Providing Logic Input Control of Operating Current

APPLICATIONS INFORMATION

Power Dissipation and Heat Management

xDSL applications require the line driver to dissipate a significant amount of power and heat compared to other components in the system. The large peak to RMS variations of DMT and CAP ADSL signals require high supply voltages to prevent clipping, and the use of a step-up transformer to couple the signal to the telephone line can require high peak current levels. These requirements result in the driver package having to dissipate on the order of 1W. Several multiport cards inserted into a rack in an enclosed central office box can add up to many, many watts of power dissipation in an elevated ambient temperature environment. The LT1794 has built-in thermal shutdown circuitry that will protect the amplifiers if operated at excessive temperatures, however data transmissions will be seriously impaired. It is important in the design of the PCB and card enclosure to take measures to spread the heat developed in the driver away to the ambient environment to prevent thermal shutdown (which occurs when the junction temperature of the LT1794 exceeds 165°C).

Estimating Line Driver Power Dissipation

Figure 6 is a typical ADSL application shown for the purpose of estimating the power dissipation in the line driver. Due to the complex nature of the DMT signal, which looks very much like noise, it is easiest to use the RMS values of voltages and currents for estimating the driver power dissipation. The voltage and current levels shown for this example are for a full-rate ADSL signal driving 20dBm or $100mW_{RMS}$ of power on to the 100Ω telephone line and assuming a 0.5dBm insertion loss in the transformer. The quiescent current for the LT1794 is set to 10mA per amplifier.

The power dissipated in the LT1794 is a combination of the quiescent power and the output stage power when driving a signal. The two amplifiers are configured to place a differential signal on to the line. The Class AB output stage in each amplifier will simultaneously dissipate power in the upper power transistor of one amplifier, while sourcing current, and the lower power transistor of the other amplifier, while sinking current. The total device power dissipation is then:

$$P_D = P_{QUIESCENT} + P_{Q(UPPER)} + P_{Q(LOWER)}$$

$$P_D = (V^+ - V^-) \bullet I_Q + (V^+ - V_{OUTARMS}) \bullet I_{LOAD} + (V^- - V_{OUTBRMS}) \bullet I_{LOAD}$$

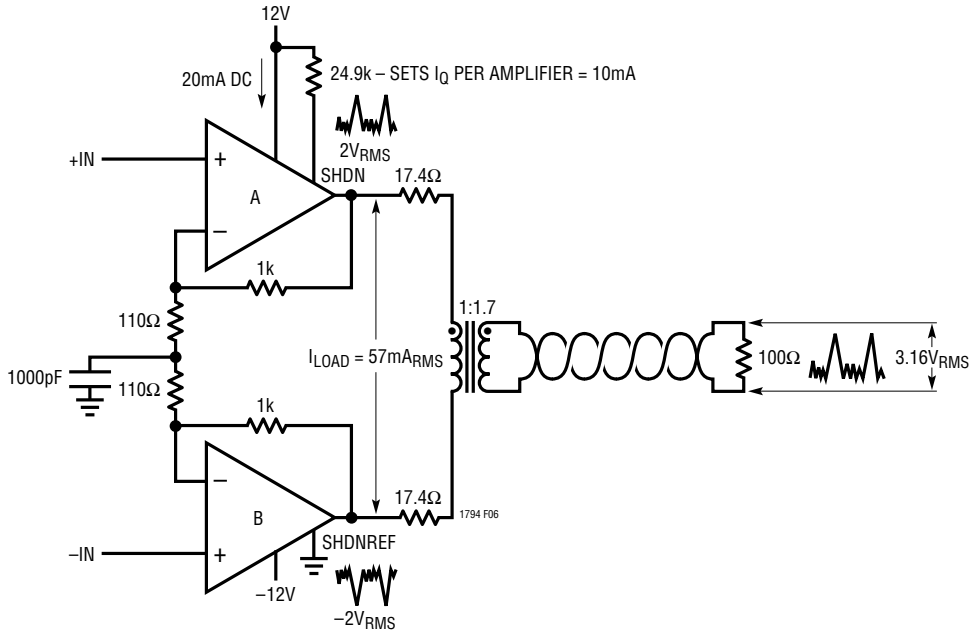


Figure 6. Estimating Line Driver Power Dissipation

APPLICATIONS INFORMATION

With no signal being placed on the line and the amplifier biased for 10mA per amplifier supply current, the quiescent driver power dissipation is:

$$P_{DQ} = 24V \bullet 20mA = 480mW$$

This can be reduced in many applications by operating with a lower quiescent current value.

When driving a load, a large percentage of the amplifier quiescent current is diverted to the output stage and becomes part of the load current. Figure 7 illustrates the total amount of biasing current flowing between the + and – power supplies through the amplifiers as a function of load current. As much as 60% of the quiescent no load operating current is diverted to the load.

At full power to the line the driver power dissipation is:

$$P_{D(FULL)} = 24V \bullet 8mA + (12V - 2V_{RMS}) \bullet 57mA_{RMS} + [|-12V - (-2V_{RMS})|] \bullet 57mA_{RMS}$$

$$P_{D(FULL)} = 192mW + 570mW + 570mW = 1.332W$$

The junction temperature of the driver must be kept less than the thermal shutdown temperature when processing a signal. The junction temperature is determined from the following expression:

$$T_J = T_{AMBIENT}\ (°C) + P_{D(FULL)}\ (W) \bullet \theta_{JA}\ (°C/W)$$

θ_{JA} is the thermal resistance from the junction of the LT1794 to the ambient air, which can be minimized by heat-spreading PCB metal and airflow through the enclosure as required. For the example given, assuming a maximum ambient temperature of 85°C and keeping the junction temperature of the LT1794 to 140°C maximum, the maximum thermal resistance from junction to ambient required is:

$$\theta_{JA(MAX)} = \frac{140°C - 85°C}{1.332W} = 41.3°C/W$$

Heat Sinking Using PCB Metal

Designing a thermal management system is often a trial and error process as it is never certain how effective it is until it is manufactured and evaluated. As a general rule, the more copper area of a PCB used for spreading heat away from the driver package, the more the operating junction temperature of the driver will be reduced. The limit to this approach however is the need for very compact circuit layout to allow more ports to be implemented on any given size PCB.

Fortunately xDSL circuit boards use multiple layers of metal for interconnection of components. Areas of metal beneath the LT1794 connected together through several small 13 mil vias can be effective in conducting heat away from the driver package. The use of inner layer metal can free up top and bottom layer PCB area for external component placement.

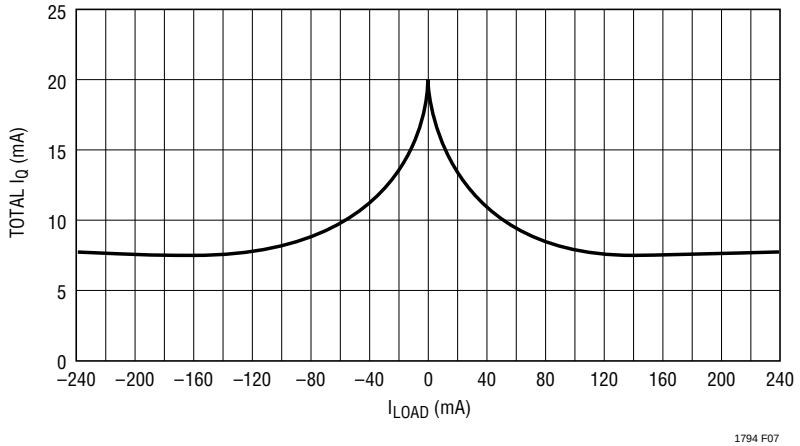
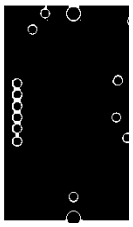
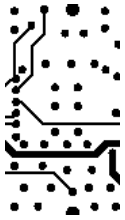
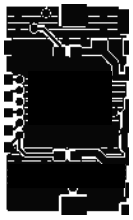
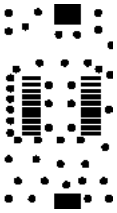
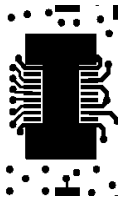
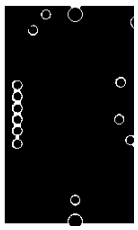
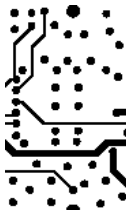
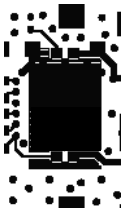
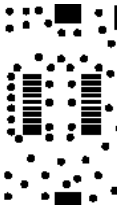
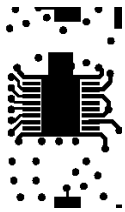
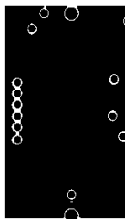
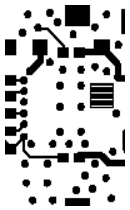
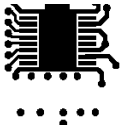
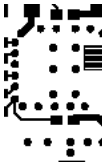
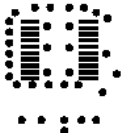


Figure 7. I_Q vs I_{LOAD}

APPLICATIONS INFORMATION

Figure 8 shows four examples of PCB metal being used for heat spreading. These are provided as a reference for what might be expected when using different combinations of metal area on different layers of a PCB. These examples are with a 4-layer board using 1oz copper on each. The most effective layers for spreading heat are those closest to the LT1794 junction. The LT1794IFE is used because the small TSSOP package is most effective for very compact line driver designs. This package also has an exposed metal heat sinking pad on the bottom side which, when soldered to the PCB top layer metal, directly conducts heat away from the IC junction. Soldering the thermal pad to the board produces a thermal resistance from junction to case, θ_{JC}, of approximately 3°C/W.

Example A utilizes the most total metal area and provides the lowest thermal resistance. Example B however uses less metal on the top and bottom layers and still achieves reasonable thermal performance. For the most compact board design, inner layer metal can be used for heat dissipation. This is shown in examples C and D where minimum metal is used on the top and none on the bottom layers, only the 2nd and 3rd layers have a heat-conducting plane. Example C, with the larger metal areas performs better.

TOPOLOGY	TOP LAYER	2nd LAYER	3rd LAYER	BOTTOM LAYER	VIA PATTERN
EXAMPLE A θ_{JA} **= 40°C/W** 13MIL VIAS USED: 30					
EXAMPLE B θ_{JA} **= 47°C/W** 13MIL VIAS USED: 35					
EXAMPLE C θ_{JA} **= 51°C/W** 13MIL VIAS USED: 32					
EXAMPLE D θ_{JA} **= 60°C/W** 13MIL VIAS USED: 22					

1794 F08

SCALE: 1 INCH

Figure 8. Examples of PCB Metal Used for Heat Dissipation. LT1794IFE Driver Mounted on Top Layer. Heat Sink Pad Soldered to Top Layer Metal. External Components Mounted on Bottom Layer

APPLICATIONS INFORMATION

Similar results can be obtained with the LT1794CSW in the wide SO-20 package. With this package heat is conducted primarily through the V^- pins, Pins 4 to 7 and 14 to 17; these pins should be soldered directly to the PCB metal plane.

Important Note: The metal planes used for heat sinking the LT1794 are electrically connected to the negative supply potential of the driver, typically –12V. These planes must be isolated from any other power planes used in the board design.

When PCB cards containing multiple ports are inserted into a rack in an enclosed cabinet, it is often necessary to provide airflow through the cabinet and over the cards. This is also very effective in reducing the junction-to-ambient thermal resistance of each line driver. To a limit, this thermal resistance can be reduced approximately 5°C/W for every 100lfpm of laminar airflow.

Layout and Passive Components

With a gain bandwidth product of 200MHz the LT1794 requires attention to detail in order to extract maximum performance. Use a ground plane, short lead lengths and a combination of RF-quality supply bypass capacitors (i.e., 0.1µF). As the primary applications have high drive current, use low ESR supply bypass capacitors (1µF to 10µF).

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole that can cause frequency peaking. In general, use feedback resistors of 1k or less.

Compensation

The LT1794 is stable in a gain 10 or higher for any supply and resistive load. It is easily compensated for lower gains with a single resistor or a resistor plus a capacitor.

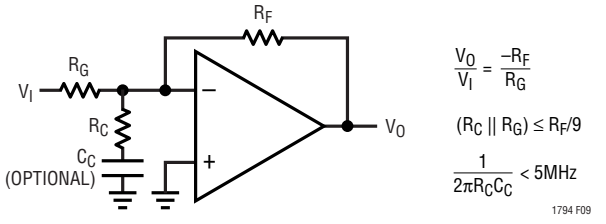


Figure 9. Compensation for Inverting Gains

Figure 9 shows that for inverting gains, a resistor from the inverting node to AC ground guarantees stability if the parallel combination of R_C and R_G is less than or equal to $R_F/9$. For lowest distortion and DC output offset, a series capacitor, C_C, can be used to reduce the noise gain at lower frequencies. The break frequency produced by R_C and C_C should be less than 5MHz to minimize peaking.

Figure 10 shows compensation in the noninverting configuration. The R_C, C_C network acts similarly to the inverting case. The input impedance is not reduced because the network is bootstrapped. This network can also be placed between the inverting input and an AC ground.

Another compensation scheme for noninverting circuits is shown in Figure 11. The circuit is unity gain at low frequency and a gain of $1 + R_F/R_G$ at high frequency. The DC output offset is reduced by a factor of ten. The techniques of Figures 10 and 11 can be combined as shown in Figure 12. The gain is unity at low frequencies, $1 + R_F/R_G$ at mid-band and for stability, a gain of 10 or greater at high frequencies.

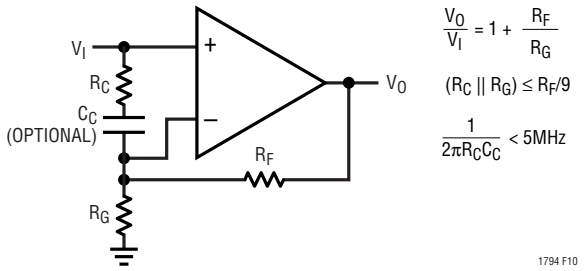


Figure 10. Compensation for Noninverting Gains

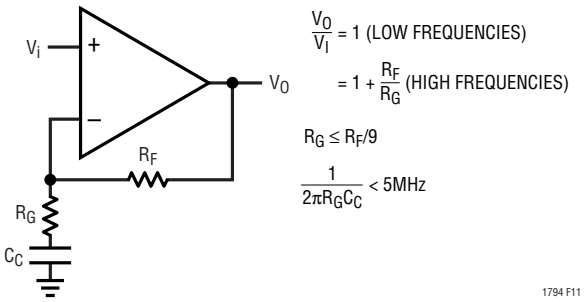


Figure 11. Alternate Noninverting Compensation

APPLICATIONS INFORMATION

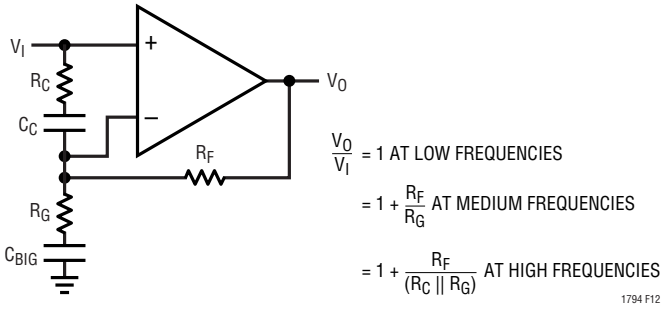


Figure 12. Combination Compensation

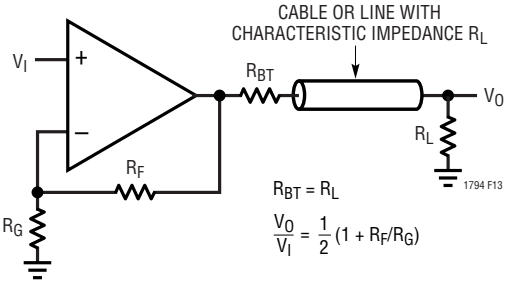


Figure 13. Standard Cable/Line Back Termination

In differential driver applications, as shown on the first page of this data sheet, it is recommended that the gain setting resistor be comprised of two equal value resistors connected to a good AC ground at high frequencies. This ensures that the feedback factor of each amplifier remains less than 0.1 at any frequency. The midpoint of the resistors can be directly connected by ground, with the resulting DC gain to the V_{OS} of the amplifiers, or just bypassed to ground with a 1000pF or larger capacitor.

Line Driving Back-Termination

The standard method of cable or line back-termination is shown in Figure 13. The cable/line is terminated in its characteristic impedance (50Ω, 75Ω, 100Ω, 135Ω, etc.). A back-termination resistor also equal to the chararacteristic impedance should be used for maximum pulse fidelity of outgoing signals, and to terminate the line for incoming signals in a full-duplex application. There are three main drawbacks to this approach. First, the power dissipated in the load and back-termination resistors is equal so half of the power delivered by the amplifier is wasted in the termination resistor. Second, the signal is halved so the gain of the amplifer must be doubled to have the same overall gain to the load. The increase in gain increases noise and decreases bandwidth (which can also increase distortion). Third, the output swing of the amplifier is doubled which can limit the power it can deliver to the load for a given power supply voltage.

An alternate method of back-termination is shown in Figure 14. Positive feedback increases the effective back-termination resistance so R_{BT} can be reduced by a factor

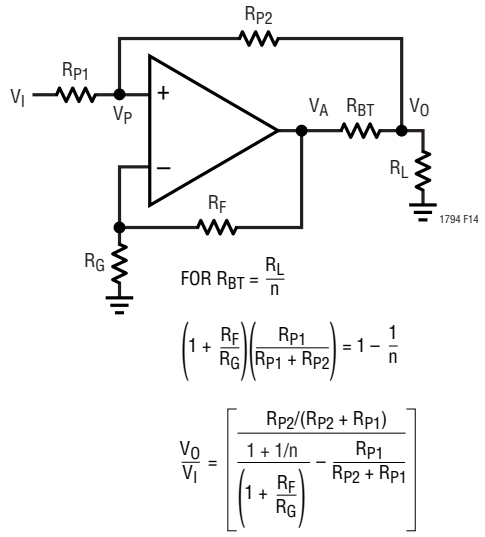


Figure 14. Back Termination Using Postive Feedback

of n. To analyze this circuit, first ground the input. As $R_{BT} = R_L/n$, and assuming $R_{P2} >> R_L$ we require that:

$V_A = V_O\ (1 - 1/n)$ to increase the effective value of R_{BT} by n.

$V_P = V_O\ (1 - 1/n)/(1 + R_F/R_G)$

$V_O = V_P\ (1 + R_{P2}/R_{P1})$

Eliminating V_P, we get the following:

$(1 + R_{P2}/R_{P1}) = (1 + R_F/R_G)/(1 - 1/n)$

For example, reducing R_{BT} by a factor of n = 4, and with an amplifer gain of $(1 + R_F/R_G) = 10$ requires that $R_{P2}/R_{P1} = 12.3$.

APPLICATIONS INFORMATION

Note that the overall gain is increased:

$$\frac{V_O}{V_I} = \frac{R_{P2} / (R_{P2} + R_{P1})}{\left[(1+1/n) / (1+R_F/R_G)\right] - \left[R_{P1}/(R_{P2}+R_{P1})\right]}$$

A simpler method of using positive feedback to reduce the back-termination is shown in Figure 15. In this case, the drivers are driven differentially and provide complementary outputs. Grounding the inputs, we see there is inverting gain of $-R_F/R_P$ from $-V_O$ to V_A

$$V_A = V_O (R_F/R_P)$$

and assuming $R_P >> R_L$, we require

$$V_A = V_O (1 - 1/n)$$

solving

$$R_F/R_P = 1 - 1/n$$

So to reduce the back-termination by a factor of 3 choose $R_F/R_P = 2/3$. Note that the overall gain is increased to:

$$V_O/V_I = (1 + R_F/R_G + R_F/R_P)/[2(1 - R_F/R_P)]$$

Using positive feedback is often referred to as active termination.

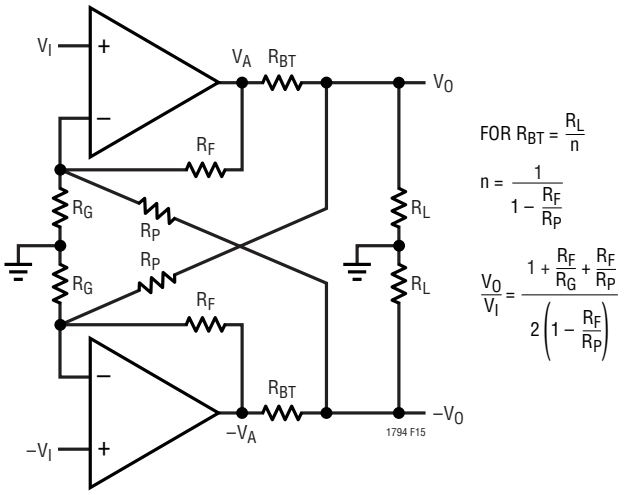


Figure 15. Back Termination Using Differential Postive Feedback

Figure 17 shows a full-rate ADSL line driver incorporating positive feedback to reduce the power lost in the back termination resistors by 40% yet still maintains the proper impedance match to the100Ω characteristic line impedance. This circuit also reduces the transformer turns ratio over the standard line driving approach resulting in lower peak current requirements. With lower current and less power loss in the back termination resistors, this driver dissipates only 1W of power, a 30% reduction.

While the power savings of positive feedback are attractive there is one important system consideration to be addressed, received signal sensitivity. The signal received from the line is sensed across the back termination resistors. With positive feedback, signals are present on both ends of the R_{BT} resistors, reducing the sensed amplitude. Extra gain may be required in the receive channel to compensate, or a completely separate receive path may be implemented through a separate line coupling transformer.

A demo board, DC306A, is available for the LT1794. This demo board is a complete line driver with an LT1361 receiver included. It allows the evaluation of both standard and active termination approaches. It also has circuitry built in to evaluate the effects of operating with reduced supply current.

Considerations for Fault Protection

The basic line driver design, shown on the front page of this data sheet, presents a direct DC path between the outputs of the two amplifiers. An imbalance in the DC biasing potentials at the noninverting inputs through either a fault condition or during turn-on of the system can create a DC voltage differential between the two amplifier outputs. This condition can force a considerable amount of current to flow as it is limited only by the small valued back-termination resistors and the DC resistance of the transformer primary. This high current can possibly cause the power supply voltage source to drop significantly impacting overall system performance. If left unchecked, the high DC current can heat the LT1794 to thermal shutdown.

APPLICATIONS INFORMATION

Using DC blocking capacitors, as shown in Figure 16, to AC couple the signal to the transformer eliminates the possibility for DC current to flow under any conditions. These capacitors should be sized large enough to not impair the frequency response characteristics required for the data transmission.

Another important fault related concern has to do with very fast high voltage transients appearing on the telephone line (lightning strikes for example). TransZorbs®, varistors and other transient protection devices are often used to absorb the transient energy, but in doing so also create fast voltage transitions themselves that can be coupled through the transformer to the outputs of the line driver. Several hundred volt transient signals can appear at the primary windings of the transformer with current into the driver outputs limited only by the back termination resistors. While the LT1794 has clamps to the supply rails at the output pins, they may not be large enough to handle the significant transient energy. External clamping diodes, such as BAV99s, at each end of the transformer primary help to shunt this destructive transient energy away from the amplifier outputs.

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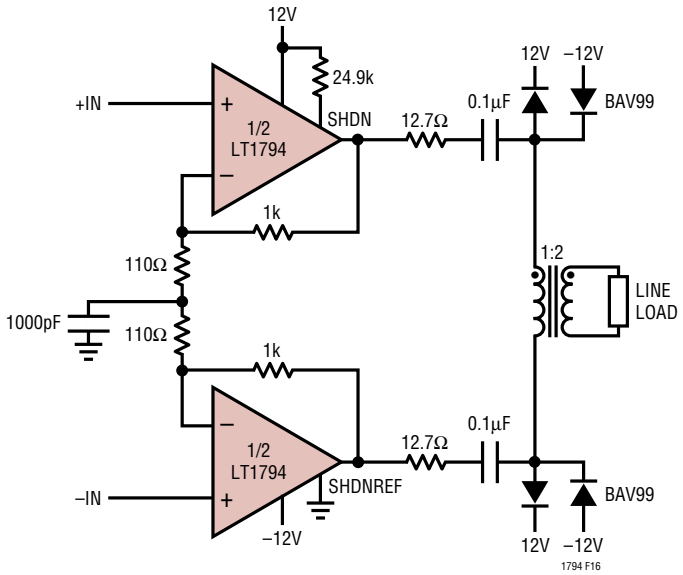
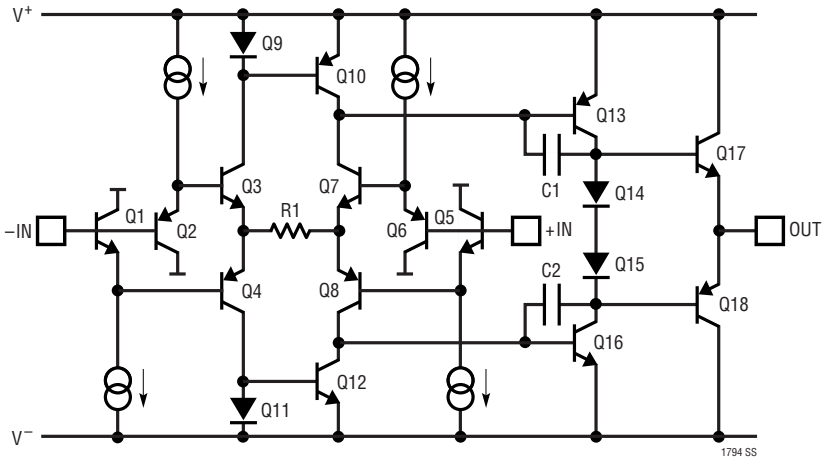


Figure 16. Protecting the Driver Against Load Faults and Line Transients

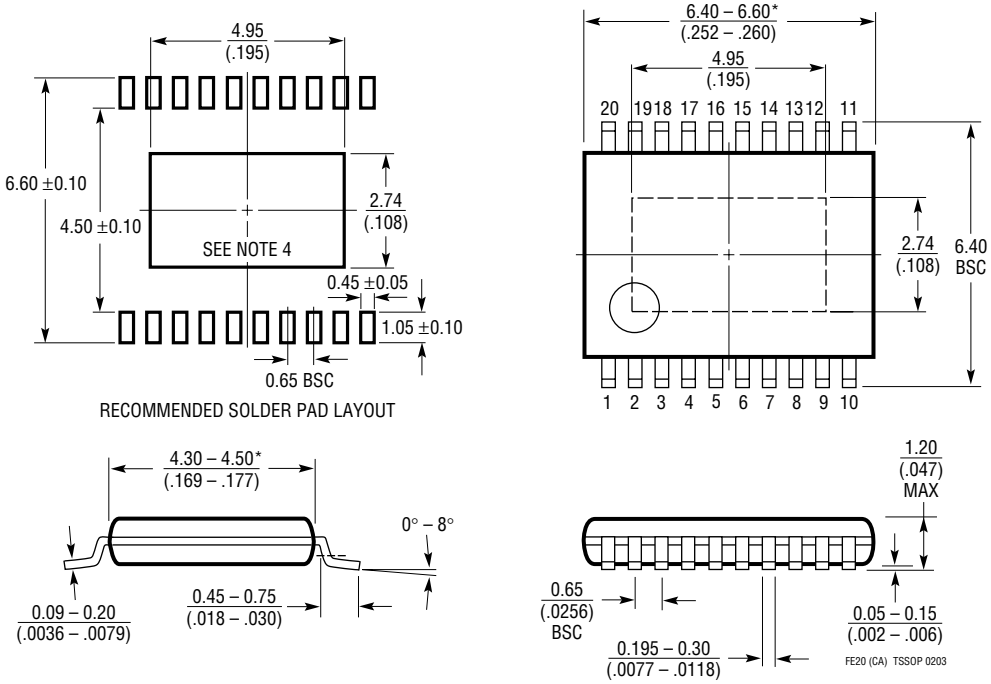
SIMPLIFIED SCHEMATIC (one amplifier shown)



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation CA



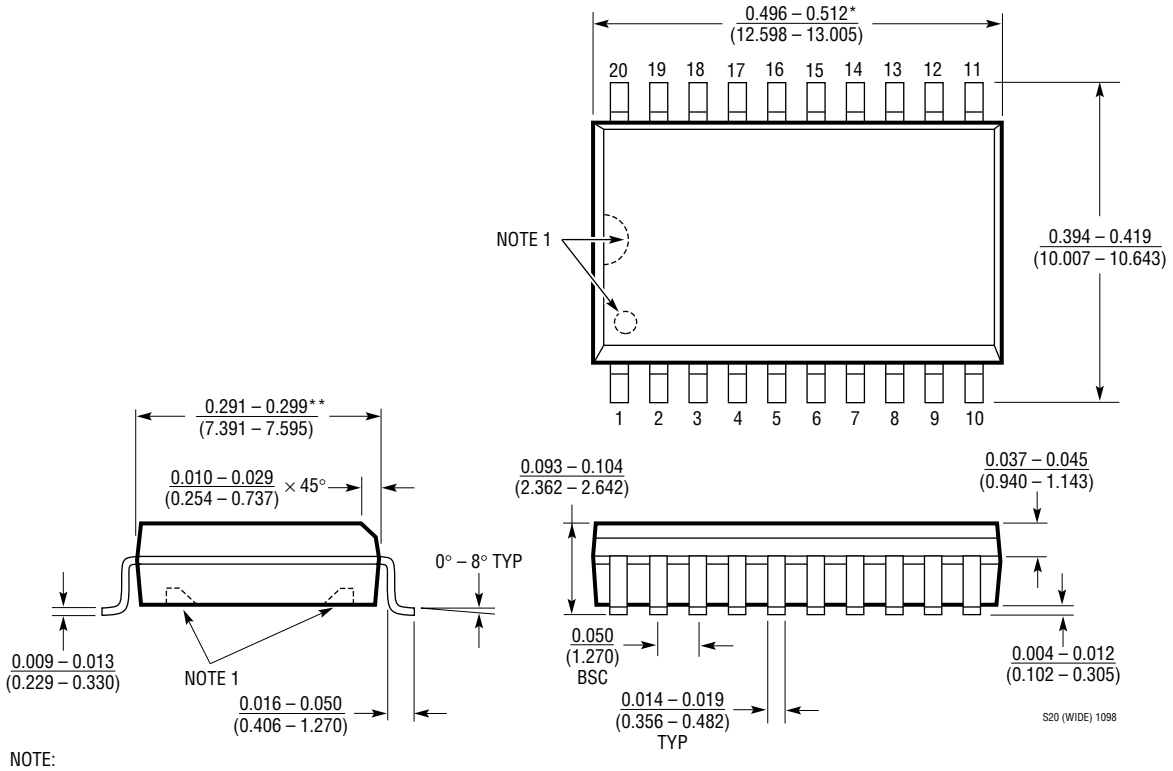
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

SW Package
20-Lead Plastic Small Outline (Wide 0.300)
(LTC DWG # 05-08-1620)



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

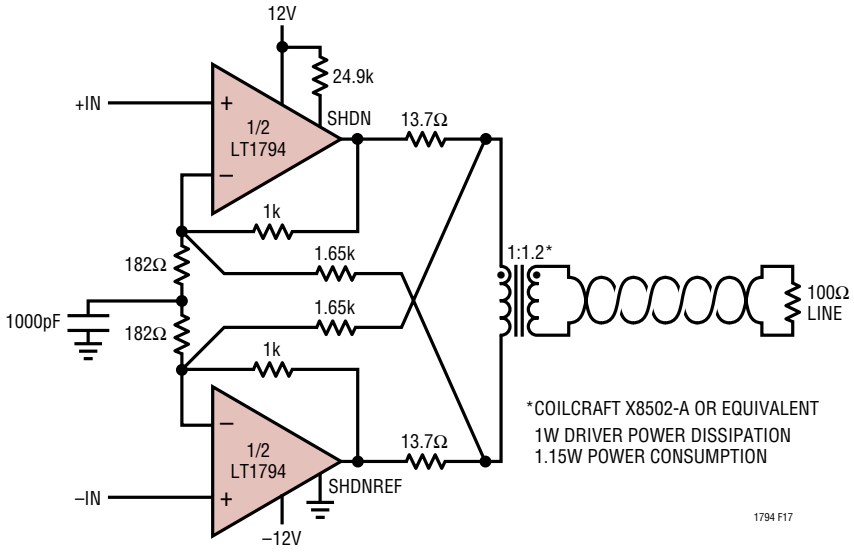


Figure 17. ADSL Line Driver Using Active Termination

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1361	Dual 50MHz, 800V/µs Op Amp	±15V Operation, 1mV V_{OS}, 1µA I_B
LTC®1563-2	Low Cost Active RC Lowpass Filter	f_C Up to 360kHz, Differential Operation, ±5V Supplies
LT1795	Dual 500mA, 50MHz Current Feedback Amplifier	Shutdown/Current Set Function, ADSL CO Driver
LT1813	Dual 100MHz, 750V/µs, 8nV/√Hz Op Amp	Low Noise, Low Power Differential Receiver, 4mA/Amplifier
LT1886	Dual 200mA, 700MHz Op Amp	12V Operation, 7mA/Amplifier, ADSL Modem Line Driver

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