



**THE DATASHEET OF  
LT1351CN8#PBF**



## FEATURES

- 3MHz Gain Bandwidth
- 200V/ $\mu$ s Slew Rate
- 250 $\mu$ A Supply Current
- Available in Tiny MSOP Package
- C-Load™ Op Amp Drives All Capacitive Loads
- Unity-Gain Stable
- Power Saving Shutdown Feature
- Maximum Input Offset Voltage: 600 $\mu$ V
- Maximum Input Bias Current: 50nA
- Maximum Input Offset Current: 15nA
- Minimum DC Gain,  $R_L = 2k$ : 30V/mV
- Input Noise Voltage: 14nV/ $\sqrt{\text{Hz}}$
- Settling Time to 0.1%, 10V Step: 700ns
- Settling Time to 0.01%, 10V Step: 1.25 $\mu$ s
- Minimum Output Swing into 1k:  $\pm$ 13V
- Minimum Output Swing into 500 $\Omega$ :  $\pm$ 3.4V
- Specified at  $\pm$ 2.5V,  $\pm$ 5V and  $\pm$ 15V

## APPLICATIONS

- Battery-Powered Systems
- Wideband Amplifiers
- Buffers
- Active Filters
- Data Acquisition Systems
- Photodiode Amplifiers

## DESCRIPTION

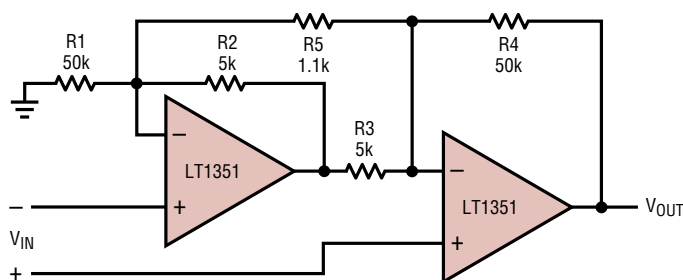
The LT<sup>®</sup>1351 is a low power, high speed, high slew rate operational amplifier with outstanding AC and DC performance. The LT1351 features lower supply current, lower input offset voltage, lower input bias current and higher DC gain than devices with comparable bandwidth. The circuit combines the slewing performance of a current feedback amplifier in a true operational amplifier with matched high impedance inputs. The high slew rate ensures that the large-signal bandwidth is not degraded. The amplifier is a single gain stage with outstanding settling characteristics which make the circuit an ideal choice for data acquisition systems. The output drives a 1k $\Omega$  load to  $\pm$ 13V with  $\pm$ 15V supplies and a 500 $\Omega$  load to  $\pm$ 3.4V on  $\pm$ 5V supplies. The amplifier is also stable with any capacitive load which makes it useful in buffer or cable driver applications.

The LT1351 is a member of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced complementary bipolar processing. For dual and quad amplifier versions of the LT1351 see the LT1352/LT1353 data sheet. For higher bandwidth devices with higher supply current see the LT1354 through LT1365 data sheets. Singles, duals and quads of each amplifier are available.

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C-Load is a trademark of Linear Technology Corporation.

## TYPICAL APPLICATION

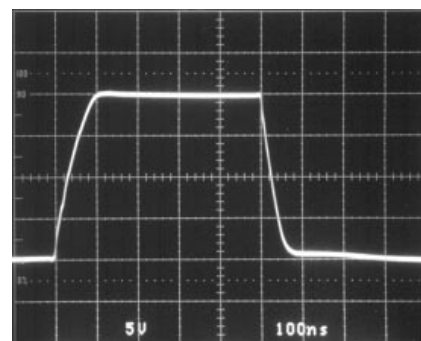
Instrumentation Amplifier



GAIN =  $[R4/R3][1 + (1/2)(R2/R1 + R3/R4) + (R2 + R3)/R5] = 102$   
 TRIM R5 FOR GAIN  
 TRIM R1 FOR COMMON MODE REJECTION  
 BW = 30kHz

1351 TA01

Large-Signal Response



$A_V = -1$

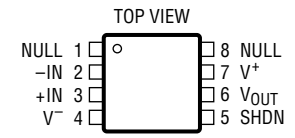
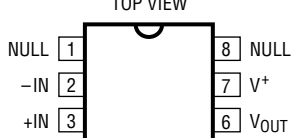
1351 TA02

# LT1351

## ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage ( $V^+$ to $V^-$ ) .....	36V	Specified Temperature Range (Note 6) .....	$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$
Differential Input Voltage (Transient Only, Note 1) ...	$\pm 10\text{V}$	Maximum Junction Temperature (See Below)	
Input Voltage .....	$\pm V_S$	Plastic Package .....	$150^{\circ}\text{C}$
Output Short-Circuit Duration (Note 2) .....	Indefinite	Storage Temperature Range .....	$-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$
Operating Temperature Range .....	$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	Lead Temperature (Soldering, 10 sec) .....	$300^{\circ}\text{C}$

## PACKAGE/ORDER INFORMATION

 <p>MS8 PACKAGE 8-LEAD PLASTIC MSOP</p> <p><math>T_{JMAX} = 150^{\circ}\text{C}</math>, <math>\theta_{JA} = 250^{\circ}\text{C}/\text{W}</math></p>	ORDER PART NUMBER	 <p>N8 PACKAGE 8-LEAD PDIP S8 PACKAGE 8-LEAD PLASTIC SO</p> <p><math>T_{JMAX} = 150^{\circ}\text{C}</math>, <math>\theta_{JA} = 130^{\circ}\text{C}/\text{W}</math> (N8) <math>T_{JMAX} = 150^{\circ}\text{C}</math>, <math>\theta_{JA} = 190^{\circ}\text{C}/\text{W}</math> (S)</p>	ORDER PART NUMBER
	LT1351CMS8		LT1351CN8 LT1351CS8
	MS8 PART MARKING		S8 PART MARKING
	LTBT		1351

Consult factory for Industrial and Military grade parts.

## ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}\text{C}$ , $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	$V_{SUPPLY}$	MIN	TYP	MAX	UNITS
$V_{OS}$	Input Offset Voltage		$\pm 15\text{V}$	0.2	0.6		mV
			$\pm 5\text{V}$	0.2	0.6		mV
			$\pm 2.5\text{V}$	0.3	0.8		mV
$I_{OS}$	Input Offset Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	5	15		nA
$I_B$	Input Bias Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	20	50		nA
$e_n$	Input Noise Voltage	$f = 10\text{kHz}$	$\pm 2.5\text{V}$ to $\pm 15\text{V}$	14			$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input Noise Current	$f = 10\text{kHz}$	$\pm 2.5\text{V}$ to $\pm 15\text{V}$	0.5			$\text{pA}/\sqrt{\text{Hz}}$
$R_{IN}$	Input Resistance	$V_{CM} = \pm 12\text{V}$ Differential	$\pm 15\text{V}$	300	600		$\text{M}\Omega$
			$\pm 15\text{V}$		20		$\text{M}\Omega$
$C_{IN}$	Input Capacitance		$\pm 15\text{V}$		3		pF
	Positive Input Voltage Range		$\pm 15\text{V}$	12.0	13.5		V
			$\pm 5\text{V}$	2.5	3.5		V
			$\pm 2.5\text{V}$	0.5	1.0		V
	Negative Input Voltage Range		$\pm 15\text{V}$	-13.5	-12.0		V
			$\pm 5\text{V}$	-3.5	-2.5		V
			$\pm 2.5\text{V}$	-1.0	-0.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12\text{V}$	$\pm 15\text{V}$	80	94		dB
		$V_{CM} = \pm 2.5\text{V}$	$\pm 5\text{V}$	78	86		dB
		$V_{CM} = \pm 0.5\text{V}$	$\pm 2.5\text{V}$	68	77		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5\text{V}$ to $\pm 15\text{V}$		90	106		dB

**ELECTRICAL CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = 0\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	$V_{SUPPLY}$	MIN	TYP	MAX	UNITS
A <sub>VOL</sub>	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}$ , $R_L = 5\text{k}$	$\pm 15\text{V}$	40	80		V/mV
		$V_{OUT} = \pm 10\text{V}$ , $R_L = 2\text{k}$	$\pm 15\text{V}$	30	60		V/mV
		$V_{OUT} = \pm 10\text{V}$ , $R_L = 1\text{k}$	$\pm 15\text{V}$	20	40		V/mV
		$V_{OUT} = \pm 2.5\text{V}$ , $R_L = 5\text{k}$	$\pm 5\text{V}$	30	60		V/mV
		$V_{OUT} = \pm 2.5\text{V}$ , $R_L = 2\text{k}$	$\pm 5\text{V}$	25	50		V/mV
		$V_{OUT} = \pm 2.5\text{V}$ , $R_L = 1\text{k}$	$\pm 5\text{V}$	15	30		V/mV
		$V_{OUT} = \pm 1\text{V}$ , $R_L = 5\text{k}$	$\pm 2.5\text{V}$	20	40		V/mV
V <sub>OUT</sub>	Output Swing	$R_L = 5\text{k}$ , $V_{IN} = \pm 10\text{mV}$	$\pm 15\text{V}$	13.5	14.0		$\pm\text{V}$
		$R_L = 2\text{k}$ , $V_{IN} = \pm 10\text{mV}$	$\pm 15\text{V}$	13.4	13.8		$\pm\text{V}$
		$R_L = 1\text{k}$ , $V_{IN} = \pm 10\text{mV}$	$\pm 15\text{V}$	13.0	13.4		$\pm\text{V}$
		$R_L = 1\text{k}$ , $V_{IN} = \pm 10\text{mV}$	$\pm 5\text{V}$	3.5	4.0		$\pm\text{V}$
		$R_L = 500\Omega$ , $V_{IN} = \pm 10\text{mV}$	$\pm 5\text{V}$	3.4	3.8		$\pm\text{V}$
		$R_L = 5\text{k}$ , $V_{IN} = \pm 10\text{mV}$	$\pm 2.5\text{V}$	1.3	1.7		$\pm\text{V}$
I <sub>OUT</sub>	Output Current	$V_{OUT} = \pm 13\text{V}$	$\pm 15\text{V}$	13.0	13.4		mA
		$V_{OUT} = \pm 3.4\text{V}$	$\pm 5\text{V}$	6.8	7.6		mA
I <sub>SC</sub>	Short-Circuit Current	$V_{OUT} = 0\text{V}$ , $V_{IN} = \pm 3\text{V}$	$\pm 15\text{V}$	30	45		mA
SR	Slew Rate	$A_V = -1$ , $R_L = 5\text{k}$ (Note 3)	$\pm 15\text{V}$	120	200		V/ $\mu\text{s}$
			$\pm 5\text{V}$	30	50		V/ $\mu\text{s}$
GBW	Gain Bandwidth	$f = 200\text{kHz}$ , $R_L = 10\text{k}$	$\pm 15\text{V}$		3.2		MHz
			$\pm 5\text{V}$		2.6		MHz
t <sub>r</sub> , t <sub>f</sub>	Rise Time, Fall Time	$A_V = 1$ , 10% to 90%, 0.1V	$\pm 15\text{V}$		46		ns
			$\pm 5\text{V}$		53		ns
			$\pm 15\text{V}$		13		%
	Overshoot	$A_V = 1$ , 0.1V	$\pm 5\text{V}$		16		%
			$\pm 15\text{V}$		41		ns
	Propagation Delay	50% $V_{IN}$ to 50% $V_{OUT}$ , 0.1V	$\pm 5\text{V}$		52		ns
			$\pm 15\text{V}$		700		ns
t <sub>s</sub>	Settling Time	10V Step, 0.1%, $A_V = -1$	$\pm 15\text{V}$		1250		ns
			$\pm 5\text{V}$		950		ns
			$\pm 15\text{V}$		1400		ns
			$\pm 5\text{V}$		1400		ns
R <sub>O</sub>	Output Resistance	$A_V = 1$ , $f = 20\text{kHz}$	$\pm 15\text{V}$		1.5		$\Omega$
I <sub>SHDN</sub>	Shutdown Input Current	SHDN = $V_{EE} + 0.1\text{V}$ SHDN = $V_{CC}$	$\pm 15\text{V}$		-10		$\mu\text{A}$
			$\pm 15\text{V}$		0.1	2	$\mu\text{A}$
I <sub>S</sub>	Supply Current	SHDN = $V_{EE} + 0.1\text{V}$	$\pm 15\text{V}$		250	330	$\mu\text{A}$
			$\pm 5\text{V}$		220	300	$\mu\text{A}$
			$\pm 5\text{V}$		10		$\mu\text{A}$

$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ,  $V_{CM} = 0\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	$V_{SUPPLY}$	MIN	TYP	MAX	UNITS
V <sub>OS</sub>	Input Offset Voltage		$\pm 15\text{V}$			0.8	mV
			$\pm 5\text{V}$			0.8	mV
			$\pm 2.5\text{V}$			1.0	mV
	Input V <sub>OS</sub> Drift	(Note 5)	$\pm 2.5\text{V}$ to $\pm 15\text{V}$		3	8	$\mu\text{V}/^\circ\text{C}$
I <sub>OS</sub>	Input Offset Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$			20	nA
I <sub>B</sub>	Input Bias Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$			75	nA

**ELECTRICAL CHARACTERISTICS**  $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ,  $V_{CM} = 0\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V <sub>SUPPLY</sub>	MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12\text{V}$	$\pm 15\text{V}$	78			dB
		$V_{CM} = \pm 2.5\text{V}$	$\pm 5\text{V}$	77			dB
		$V_{CM} = \pm 0.5\text{V}$	$\pm 2.5\text{V}$	67			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5\text{V to } \pm 15\text{V}$		89			dB
A <sub>VOL</sub>	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}, R_L = 5\text{k}$	$\pm 15\text{V}$	25			V/mV
		$V_{OUT} = \pm 10\text{V}, R_L = 2\text{k}$	$\pm 15\text{V}$	20			V/mV
		$V_{OUT} = \pm 2.5\text{V}, R_L = 5\text{k}$	$\pm 5\text{V}$	20			V/mV
		$V_{OUT} = \pm 2.5\text{V}, R_L = 2\text{k}$	$\pm 5\text{V}$	15			V/mV
		$V_{OUT} = \pm 2.5\text{V}, R_L = 1\text{k}$	$\pm 5\text{V}$	10			V/mV
		$V_{OUT} = \pm 1\text{V}, R_L = 5\text{k}$	$\pm 2.5\text{V}$	15			V/mV
V <sub>OUT</sub>	Output Swing	$R_L = 5\text{k}, V_{IN} = \pm 10\text{mV}$	$\pm 15\text{V}$	13.4			$\pm \text{V}$
		$R_L = 2\text{k}, V_{IN} = \pm 10\text{mV}$	$\pm 15\text{V}$	13.3			$\pm \text{V}$
		$R_L = 1\text{k}, V_{IN} = \pm 10\text{mV}$	$\pm 15\text{V}$	12.0			$\pm \text{V}$
		$R_L = 1\text{k}, V_{IN} = \pm 10\text{mV}$	$\pm 5\text{V}$	3.4			$\pm \text{V}$
		$R_L = 500\Omega, V_{IN} = \pm 10\text{mV}$	$\pm 5\text{V}$	3.3			$\pm \text{V}$
		$R_L = 5\text{k}, V_{IN} = \pm 10\text{mV}$	$\pm 2.5\text{V}$	1.2			$\pm \text{V}$
I <sub>OUT</sub>	Output Current	$V_{OUT} = \pm 12\text{V}$	$\pm 15\text{V}$	12.0			mA
		$V_{OUT} = \pm 3.3\text{V}$	$\pm 5\text{V}$	6.6			mA
I <sub>SC</sub>	Short-Circuit Current	$V_{OUT} = 0\text{V}, V_{IN} = \pm 3\text{V}$	$\pm 15\text{V}$	24			mA
SR	Slew Rate	$A_V = -1, R_L = 5\text{k}$ (Note 3)	$\pm 15\text{V}$	100			V/ $\mu\text{s}$
			$\pm 5\text{V}$	21			V/ $\mu\text{s}$
GBW	Gain Bandwidth	$f = 200\text{kHz}, R_L = 10\text{k}$	$\pm 15\text{V}$	1.8			MHz
			$\pm 5\text{V}$	1.6			MHz
I <sub>SHDN</sub>	Shutdown Input Current	SHDN = $V_{EE} + 0.1\text{V}$ SHDN = $V_{CC}$	$\pm 15\text{V}$		-20		$\mu\text{A}$
			$\pm 15\text{V}$			3	$\mu\text{A}$
I <sub>S</sub>	Supply Current	SHDN = $V_{EE} + 0.1\text{V}$	$\pm 15\text{V}$			380	$\mu\text{A}$
			$\pm 5\text{V}$			355	$\mu\text{A}$
			$\pm 5\text{V}$		20		$\mu\text{A}$

**$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ,  $V_{CM} = 0\text{V}$  unless otherwise noted (Note 6).**

SYMBOL	PARAMETER	CONDITIONS	V <sub>SUPPLY</sub>	MIN	TYP	MAX	UNITS
V <sub>OS</sub>	Input Offset Voltage		$\pm 15\text{V}$			1.0	mV
			$\pm 5\text{V}$			1.0	mV
			$\pm 2.5\text{V}$			1.2	mV
	Input V <sub>OS</sub> Drift	(Note 5)	$\pm 2.5\text{V to } \pm 15\text{V}$		3	8	$\mu\text{V}/^{\circ}\text{C}$
I <sub>OS</sub>	Input Offset Current		$\pm 2.5\text{V to } \pm 15\text{V}$			30	nA
I <sub>B</sub>	Input Bias Current		$\pm 2.5\text{V to } \pm 15\text{V}$			100	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12\text{V}$ $V_{CM} = \pm 2.5\text{V}$ $V_{CM} = \pm 0.5\text{V}$	$\pm 15\text{V}$	76			dB
			$\pm 5\text{V}$	76			dB
			$\pm 2.5\text{V}$	66			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5\text{V to } \pm 15\text{V}$		87			dB
A <sub>VOL</sub>	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}, R_L = 5\text{k}$	$\pm 15\text{V}$	20			V/mV
		$V_{OUT} = \pm 10\text{V}, R_L = 2\text{k}$	$\pm 15\text{V}$	15			V/mV
		$V_{OUT} = \pm 2.5\text{V}, R_L = 5\text{k}$	$\pm 5\text{V}$	15			V/mV
		$V_{OUT} = \pm 2.5\text{V}, R_L = 2\text{k}$	$\pm 5\text{V}$	10			V/mV
		$V_{OUT} = \pm 2.5\text{V}, R_L = 1\text{k}$	$\pm 5\text{V}$	8			V/mV
		$V_{OUT} = \pm 1\text{V}, R_L = 5\text{k}$	$\pm 2.5\text{V}$	10			V/mV

**ELECTRICAL CHARACTERISTICS**  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ,  $V_{\text{CM}} = 0\text{V}$  unless otherwise noted (Note 6).

SYMBOL	PARAMETER	CONDITIONS	V <sub>SUPPLY</sub>	MIN	TYP	MAX	UNITS
V <sub>OUT</sub>	Output Swing	R <sub>L</sub> = 5k, V <sub>IN</sub> = ±10mV	±15V	13.3			±V
		R <sub>L</sub> = 2k, V <sub>IN</sub> = ±10mV	±15V	13.2			±V
		R <sub>L</sub> = 1k, V <sub>IN</sub> = ±10mV	±15V	10.0			±V
		R <sub>L</sub> = 1k, V <sub>IN</sub> = ±10mV	±5V	3.3			±V
		R <sub>L</sub> = 500Ω, V <sub>IN</sub> = ±10mV	±5V	3.2			±V
		R <sub>L</sub> = 5k, V <sub>IN</sub> = ±10mV	±2.5V	1.1			±V
I <sub>OUT</sub>	Output Current	V <sub>OUT</sub> = ±10V	±15V	10.0			mA
		V <sub>OUT</sub> = ±3.2V	±5V	6.4			mA
I <sub>SC</sub>	Short-Circuit Current	V <sub>OUT</sub> = 0V, V <sub>IN</sub> = ±3V	±15V	20			mA
SR	Slew Rate	A <sub>V</sub> = -1, R <sub>L</sub> = 5k (Note 3)	±15V	50			V/μs
			±5V	15			V/μs
GBW	Gain Bandwidth	f = 200kHz, R <sub>L</sub> = 10k	±15V	1.6			MHz
			±5V	1.4			MHz
I <sub>SHDN</sub>	Shutdown Input Current	SHDN = V <sub>EE</sub> + 0.1V SHDN = V <sub>CC</sub>	±15V		-30		μA
			±15V			5	μA
I <sub>S</sub>	Supply Current	SHDN = V <sub>EE</sub> + 0.1V	±15V			390	μA
			±5V			380	μA
			±5V		30		μA

**Note 1:** Differential inputs of ±10V are appropriate for transient operation only, such as during slewing. Large, sustained differential inputs will cause excessive power dissipation and may damage the part. See Input Considerations in the Applications Information section of this data sheet for more details.

**Note 2:** A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

**Note 3:** Slew rate is measured between ±8V on the output with ±12V input for ±15V supplies and ±2V on the output with ±3V input for ±5V supplies.

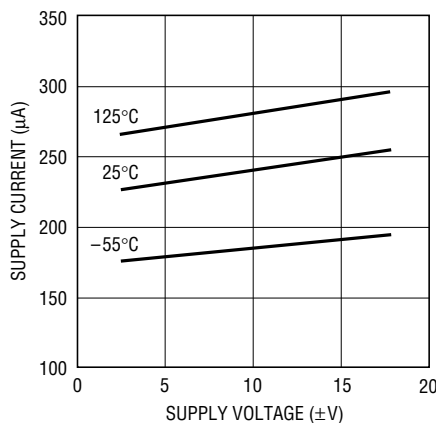
**Note 4:** Full-power bandwidth is calculated from the slew rate measurement:  $\text{FPBW} = (\text{Slew Rate})/2\pi V_p$ .

**Note 5:** This parameter is not 100% tested.

**Note 6:** The LT1351 is designed, characterized and expected to meet these extended temperature limits, but is not tested at -40°C and at 85°C. Guaranteed I grade parts are available; consult factory.

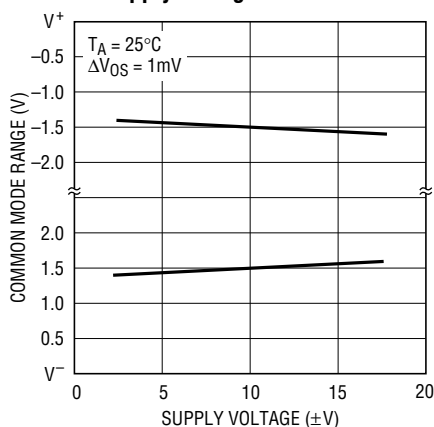
**TYPICAL PERFORMANCE CHARACTERISTICS**

Supply Current vs Supply Voltage and Temperature



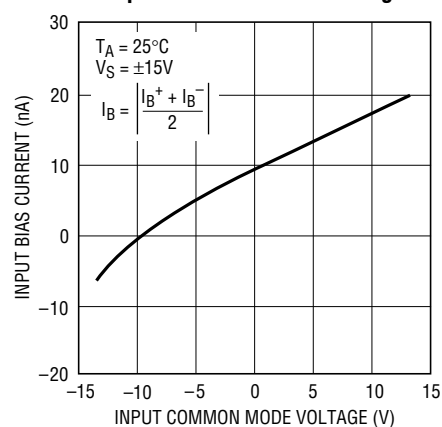
1351 G01

Input Common Mode Range vs Supply Voltage



1351 G02

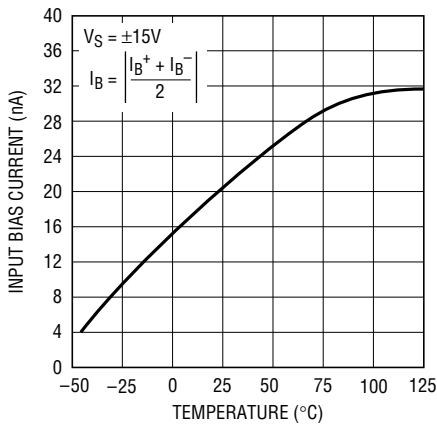
Input Bias Current vs Input Common Mode Voltage



1351 G03

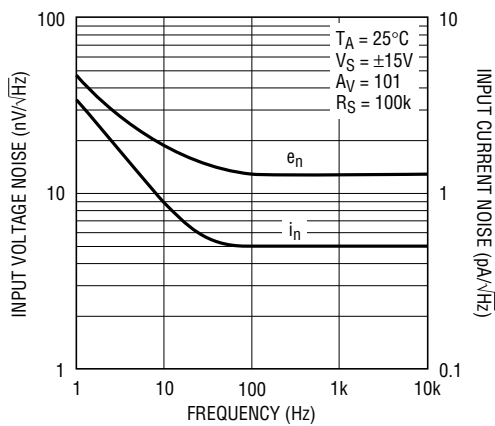
# TYPICAL PERFORMANCE CHARACTERISTICS

**Input Bias Current vs Temperature**



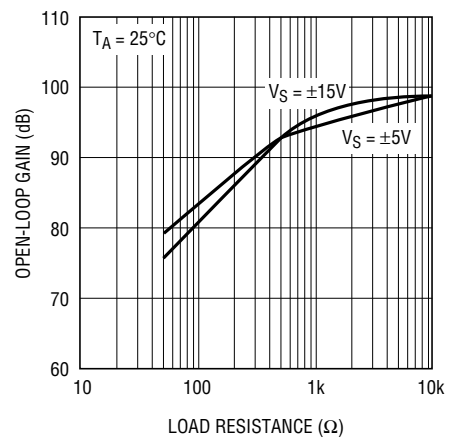
1351 G04

**Input Noise Spectral Density**



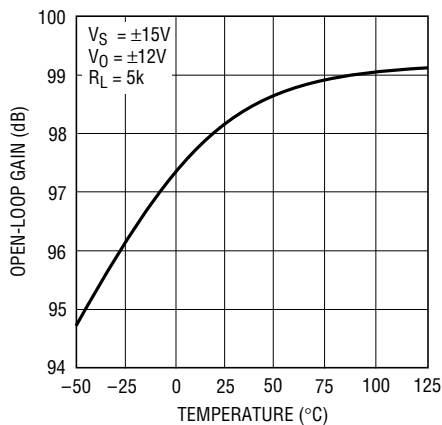
1351 G05

**Open-Loop Gain vs Resistive Load**



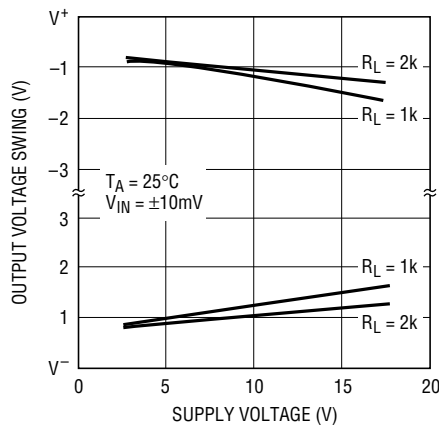
1351 G06

**Open-Loop Gain vs Temperature**



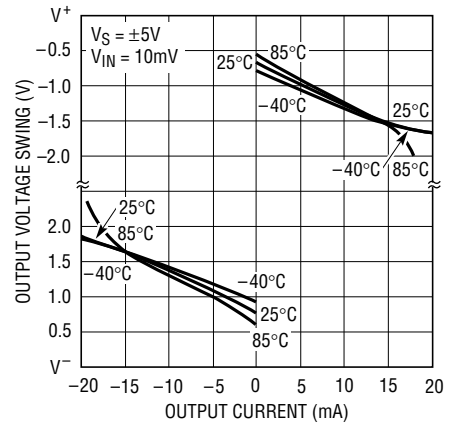
1351 G07

**Output Voltage Swing vs Supply Voltage**



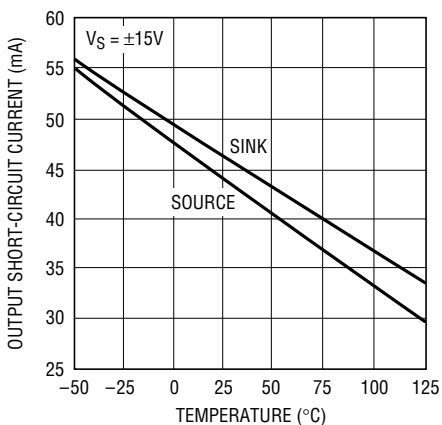
1351 G08

**Output Voltage Swing vs Load Current**



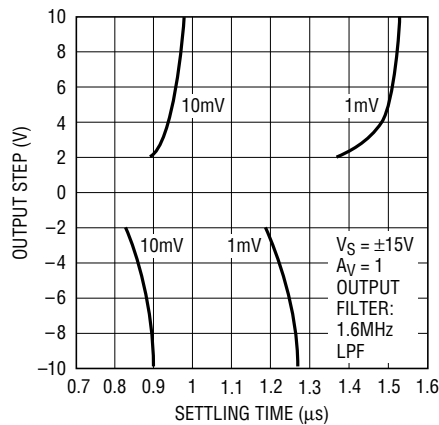
1351 G09

**Output Short-Circuit Current vs Temperature**



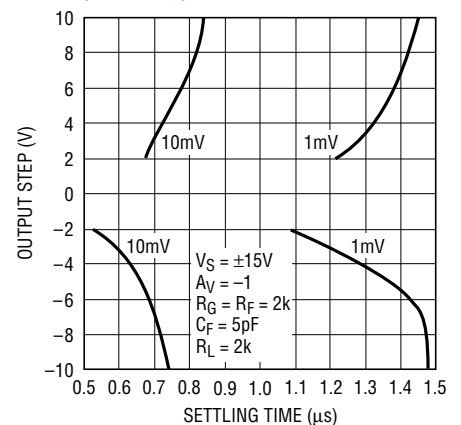
1351 G10

**Settling Time vs Output Step (Noninverting)**



1351 G11

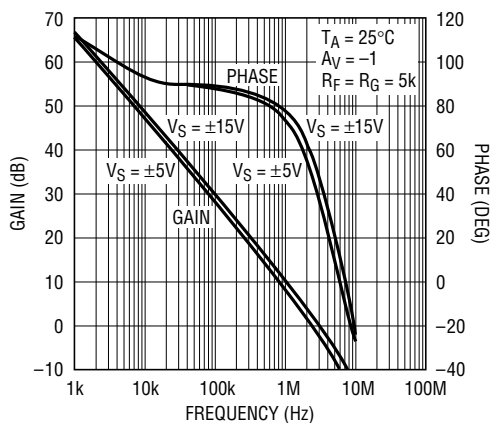
**Settling Time vs Output Step (Inverting)**



1351 G12

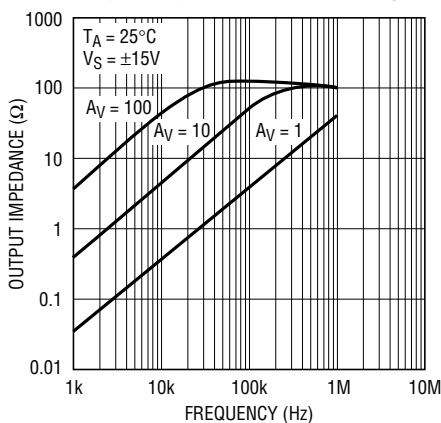
# TYPICAL PERFORMANCE CHARACTERISTICS

**Gain and Phase vs Frequency**



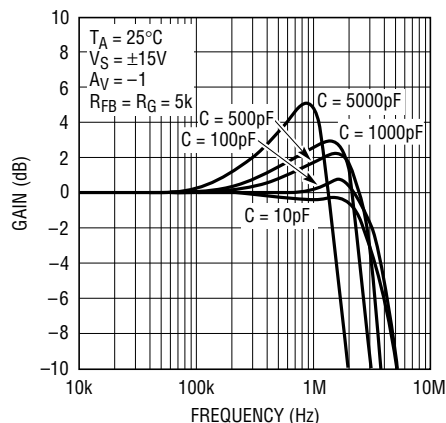
1351 G13

**Output Impedance vs Frequency**



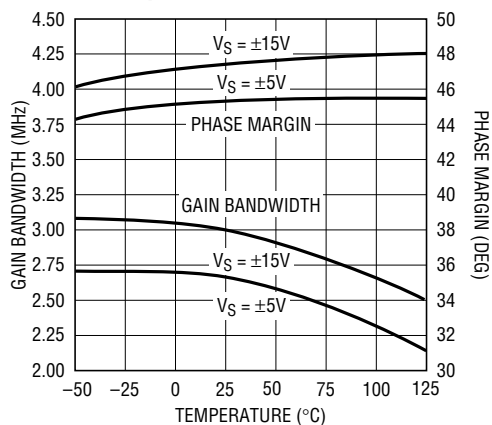
1351 G14

**Frequency Response vs Capacitive Load**



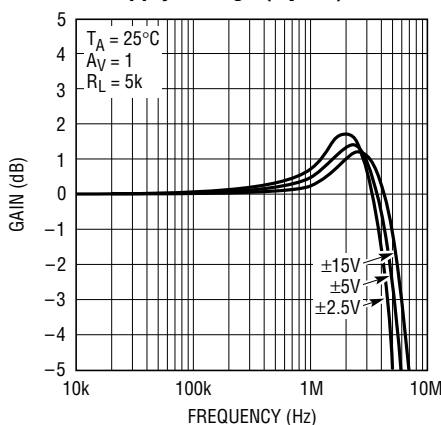
1351 G15

**Gain Bandwidth and Phase Margin vs Temperature**



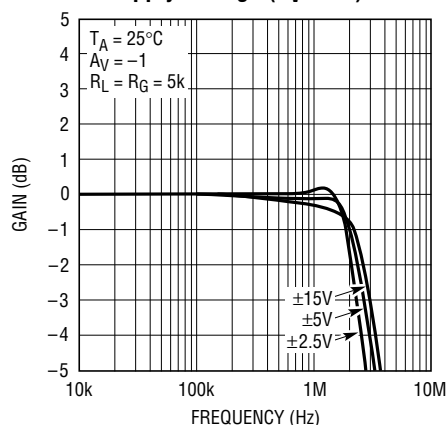
1351 G16

**Frequency Response vs Supply Voltage (AV = 1)**



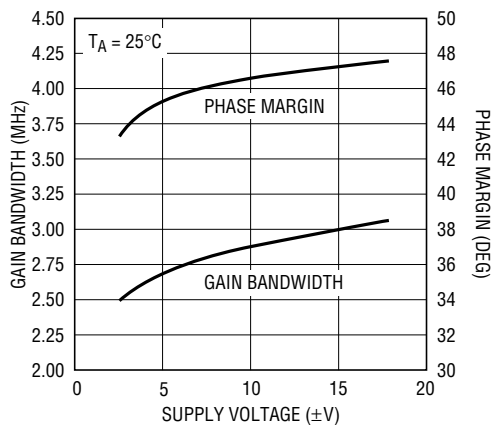
1351 G17

**Frequency Response vs Supply Voltage (AV = -1)**



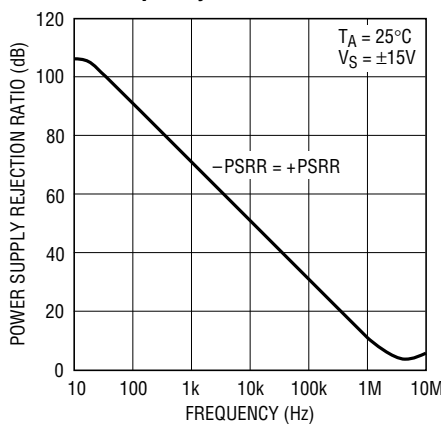
1351 G18

**Gain Bandwidth and Phase Margin vs Supply Voltage**



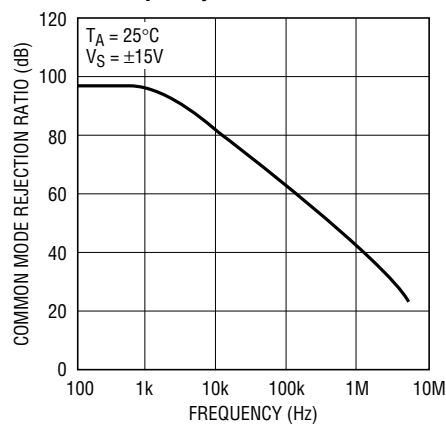
1351 G19

**Power Supply Rejection Ratio vs Frequency**



1351 G20

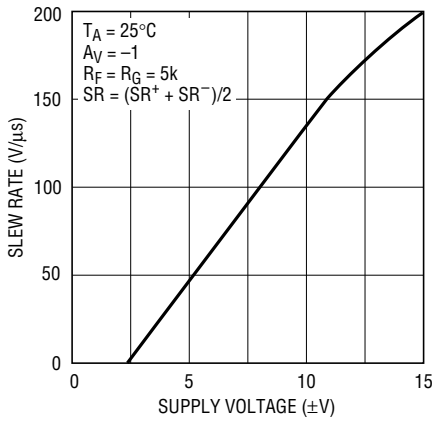
**Common Mode Rejection Ratio vs Frequency**



1351 G21

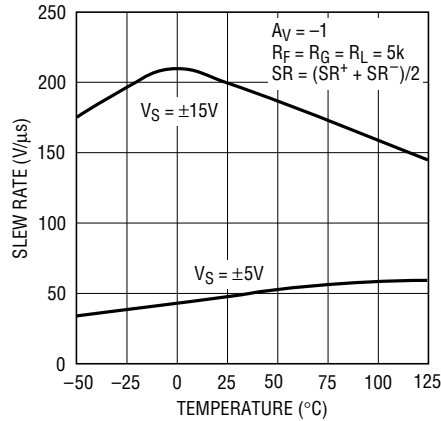
# TYPICAL PERFORMANCE CHARACTERISTICS

**Slew Rate vs Supply Voltage**



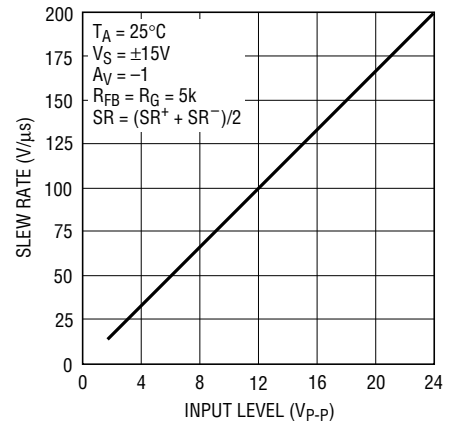
1351 G22

**Slew Rate vs Temperature**



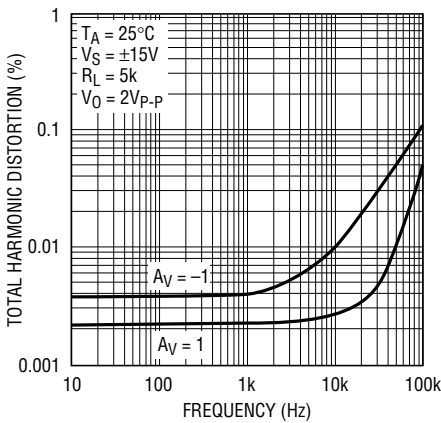
1351 G23

**Slew Rate vs Input Level**



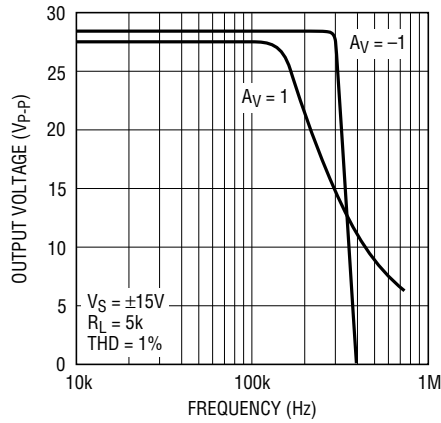
1351 G24

**Total Harmonic Distortion vs Frequency**



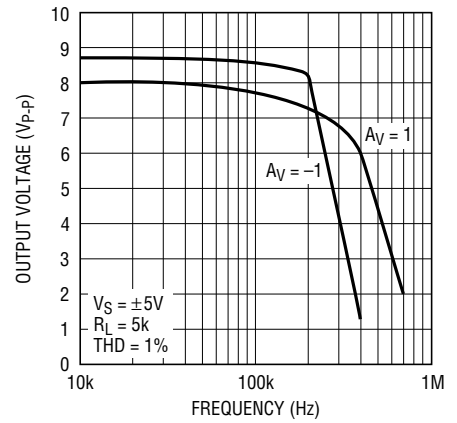
1351 G25

**Undistorted Output Swing vs Frequency (±15V)**



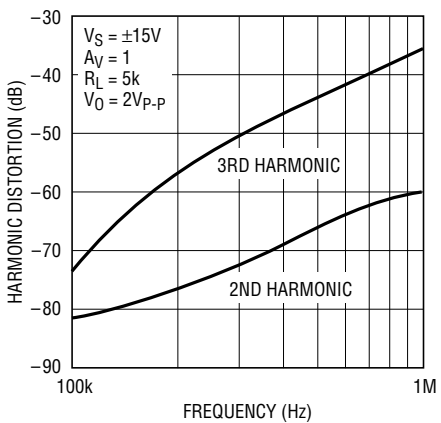
1351 G26

**Undistorted Output Swing vs Frequency (±5V)**



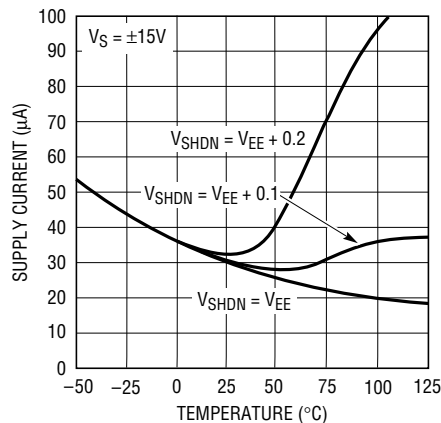
1351 G27

**2nd and 3rd Harmonic Distortion vs Frequency**



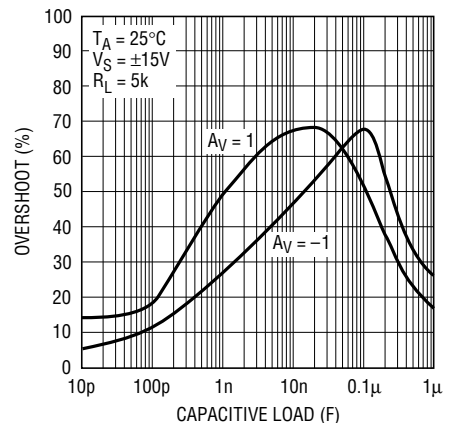
1351 G28

**Shutdown Supply Current vs Temperature**



1351 G29

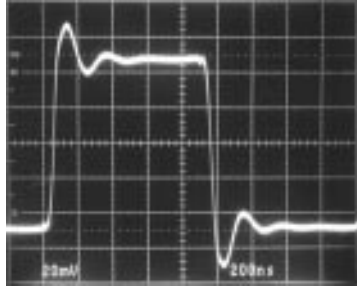
**Capacitive Load Handling**



1351 G30

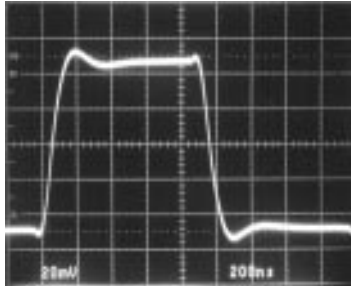
## TYPICAL PERFORMANCE CHARACTERISTICS

Small-Signal Transient  
( $A_V = 1$ )



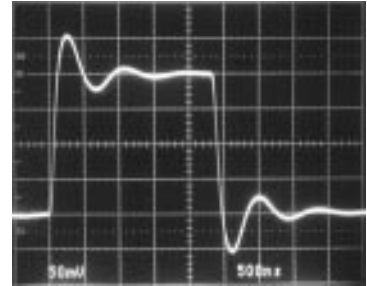
1351 G31

Small-Signal Transient  
( $A_V = -1$ )



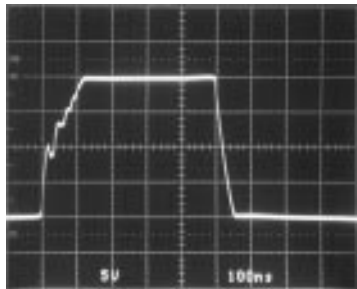
1351 G32

Small-Signal Transient  
( $A_V = -1, C_L = 1000\text{pF}$ )



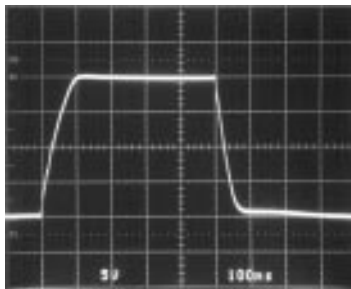
1351 G33

Large-Signal Transient  
( $A_V = 1$ )



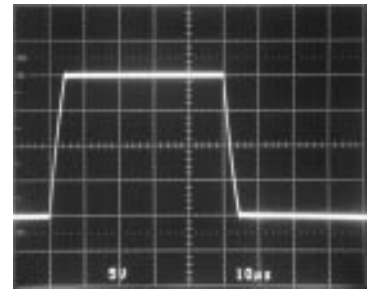
1351 G34

Large-Signal Transient  
( $A_V = -1$ )



1351 G35

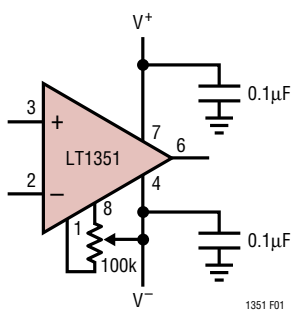
Large-Signal Transient  
( $A_V = 1, C_L = 10,000\text{pF}$ )



1351 G36

## APPLICATIONS INFORMATION

The LT1351 may be inserted directly into many high speed amplifier applications improving both DC and AC performance, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1351 is shown in Figure 1.



1351 F01

Figure 1. Offset Nulling

### Layout and Passive Components

The LT1351 amplifier is easy to apply and tolerant of less than ideal layouts. For maximum performance (for example fast settling time) use a ground plane, short lead lengths and RF-quality bypass capacitors (0.01µF to 0.1µF). For high drive current applications use low ESR bypass capacitors (1µF to 10µF tantalum). For details see Design Note 50.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole which can cause peaking or even oscillations. For feedback resistors greater than 10k, a parallel capacitor of value,  $C_F > (R_G)(C_{IN}/R_F)$  should be used to cancel the input pole and optimize dynamic performance. For applications where the DC

## APPLICATIONS INFORMATION

noise gain is one and a large feedback resistor is used,  $C_F$  should be greater than or equal to  $C_{IN}$ . An example would be an I-to-V converter as shown in the Typical Applications section.

### Capacitive Loading

The LT1351 is stable with any capacitive load. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response. Graphs of Frequency Response vs Capacitive Load, Capacitive Load Handling and the transient response photos clearly show these effects.

### Input Considerations

Each of the LT1351 inputs is the base of an NPN and a PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current does not depend on NPN/PNP beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

The inputs can withstand transient differential input voltages up to 10V without damage and need no clamping or source resistance for protection. Differential inputs, however, generate large supply currents (tens of mA) as required for high slew rates. If the device is used with sustained differential inputs, the average supply current will increase, excessive power dissipation will result and the part may be damaged. *The part should not be used as a comparator, peak detector or other open-loop application with large, sustained differential inputs.* Under normal, closed-loop operation, an increase of power dissipation is only noticeable in applications with large slewing outputs and is proportional to the magnitude of the differential input voltage and the percent of the time that the inputs are apart. Measure the average supply current for the application in order to calculate the power dissipation.

### Shutdown

The LT1351 has a Shutdown pin for conserving power. When this pin is open or 2V above the negative supply the part operates normally. When pulled down to  $V^-$  the supply current will drop to about 10 $\mu$ A. The current out of the Shutdown pin is also typically 10 $\mu$ A. In shutdown the amplifier output is not isolated from the inputs so the LT1351 cannot be used in multiplexing applications using the shutdown feature.

A level shift application is shown in the Typical Applications section so that a ground-referenced logic signal can control the Shutdown pin.

### Circuit Operation

The LT1351 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the simplified schematic.

The inputs are buffered by complementary NPN and PNP emitter followers which drive R1, a 1k resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node and compensation capacitor  $C_T$ . Complementary followers form an output stage which buffers the gain node from the load. The output devices Q19 and Q22 are connected to form a composite PNP and composite NPN.

The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step whereas the same output step in unity gain has a 10 times greater input step. The curve of Slew Rate vs Input Level illustrates this relationship.

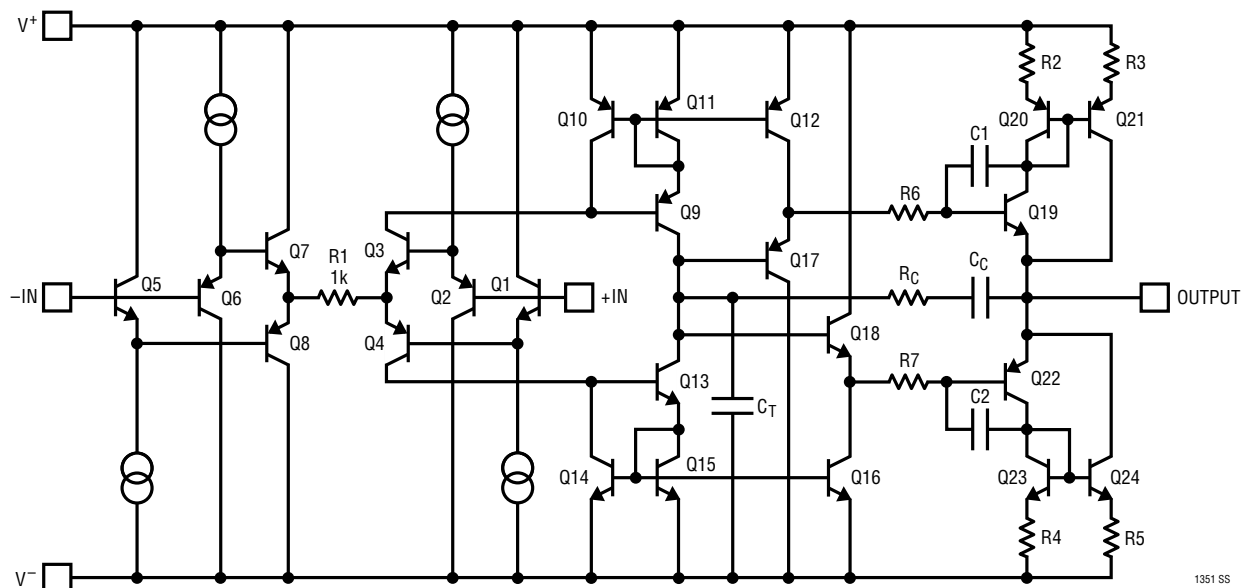
Capacitive load compensation is provided by the  $R_C$ ,  $C_C$  network which is bootstrapped across the output stage. When the amplifier is driving a light load the network has no effect. When driving a capacitive load (or a low value

## APPLICATIONS INFORMATION

resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier and a zero is created by the RC combination, both of

which improve the phase margin. The design ensures that even for very large load capacitances the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

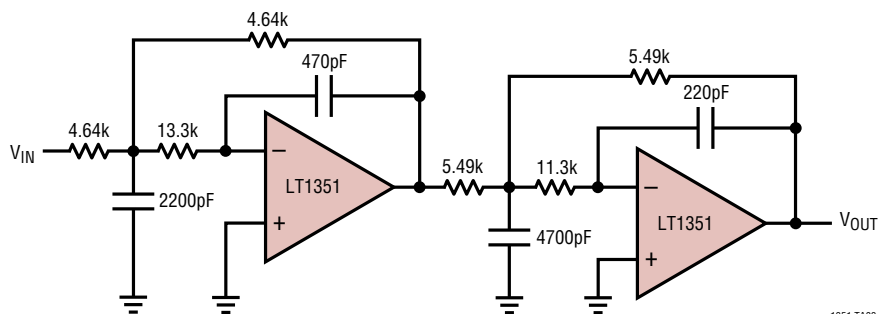
## SIMPLIFIED SCHEMATIC



1351 SS

## TYPICAL APPLICATIONS

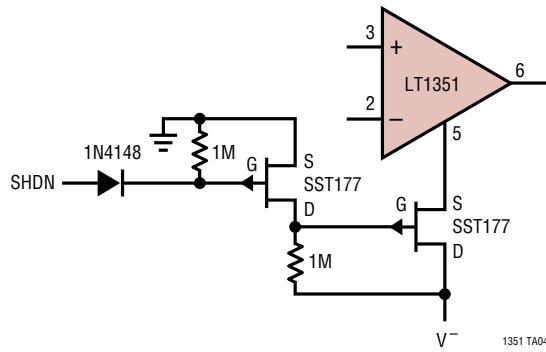
20kHz, 4th Order Butterworth Filter



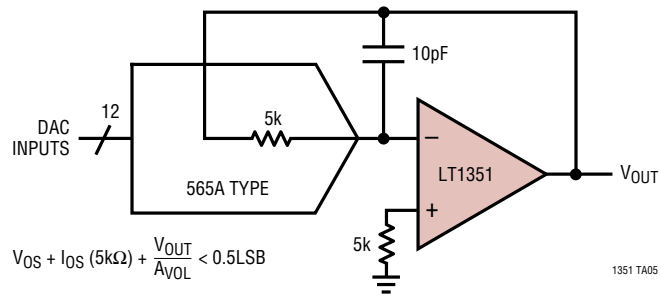
1351 TA03

**TYPICAL APPLICATIONS**

**Shutdown Circuit**

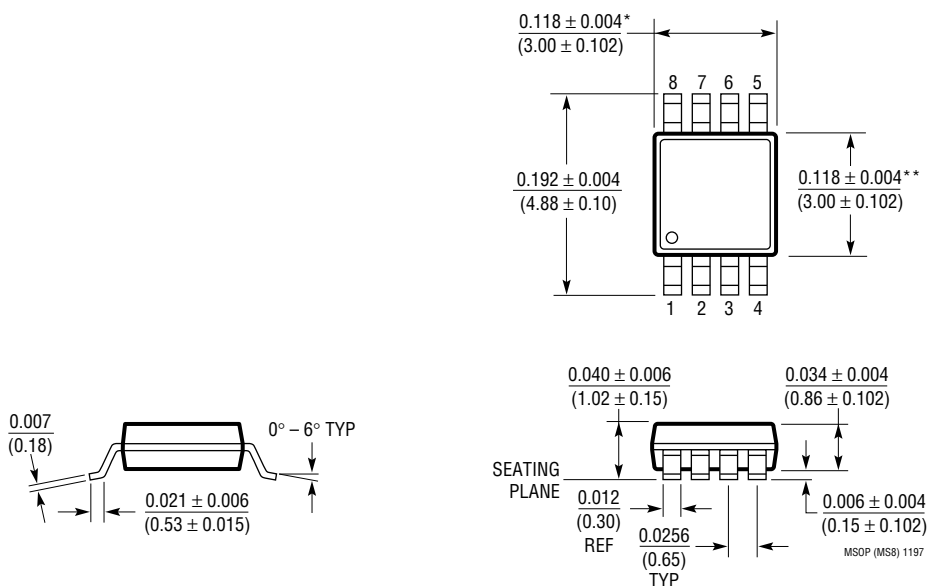


**DAC I-to-V Converter**



**PACKAGE DESCRIPTION** Dimensions in inches (millimeters) unless otherwise noted.

**MS8 Package**  
**8-Lead Plastic MSOP**  
 (LTC DWG # 05-08-1660)

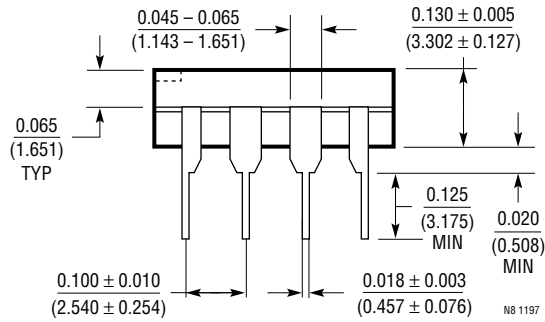
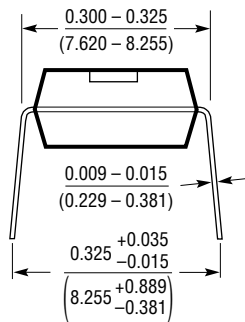
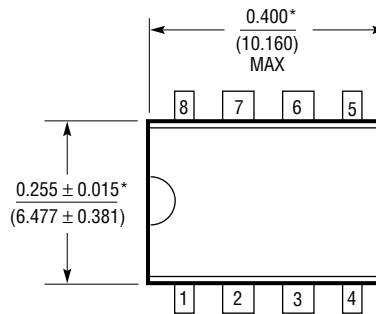


\* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

\*\* DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**PACKAGE DESCRIPTION** Dimensions in inches (millimeters) unless otherwise noted.

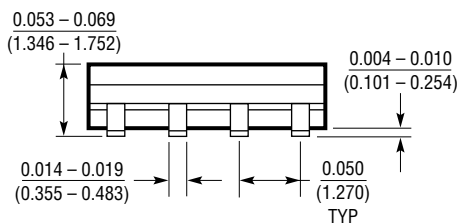
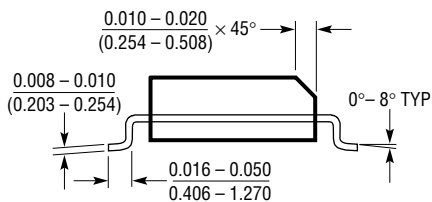
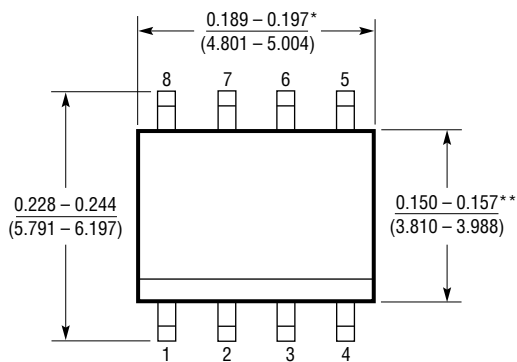
**N8 Package**  
**8-Lead PDIP (Narrow 0.300)**  
 (LTC DWG # 05-08-1510)



\*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

**PACKAGE DESCRIPTION** Dimensions in inches (millimeters) unless otherwise noted.

**S8 Package**  
**8-Lead Plastic Small Outline (Narrow 0.150)**  
 (LTC DWG # 05-08-1610)



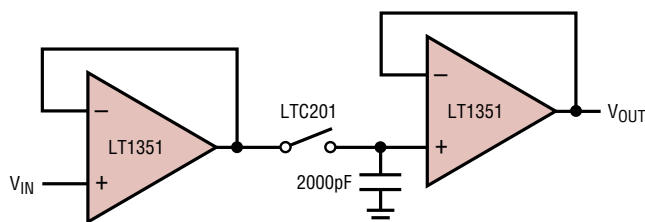
\*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

\*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 0996

## TYPICAL APPLICATION

### Low Power Sample-and-Hold



DROOP:  $20\text{nA}/2000\text{pF} = 10\text{mV/ms}$   
 ACQUISITION TIME:  $10\text{V}, 0.1\% = 2\mu\text{s}$   
 CHARGE INJECTION ERROR:  $8\text{pC}/2000\text{pF} = 4\text{mV}$

1351 TA06

## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1352/LT1353	Dual/Quad $250\mu\text{A}$ , 3MHz, $200\text{V}/\mu\text{s}$ Op Amp	Good DC Precision, Stable with All Capacitive Loads
LT1354	1mA, 12MHz, $400\text{V}/\mu\text{s}$ Op Amp	Good DC Precision, Stable with All Capacitive Loads

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 [Linear Technology](#) Information

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-  Alternative Solution
-  Excess Inventory Management