



**THE DATASHEET OF  
LT1122CCN8#PBF**



## FEATURES

- 100% Tested Settling Time to 1mV at Sum Node, 10V Step Tested with Fixed Feedback Capacitor
 

340ns Typ
540ns Max
- Slew Rate
 

60V/μs Min
14MHz
- Gain-Bandwidth Product
 

1.2 MHz
60°
- Power Bandwidth (20V<sub>P-P</sub>)
- Unity-Gain Stable; Phase Margin
- Input Offset Voltage
 

600μV Max
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- Input Bias Current
 

25°C 75pA Max
70°C 600pA Max
- Input Offset Current
 

25°C 40pA Max
70°C 150pA Max
- Low Distortion

## APPLICATIONS

- Fast 12-Bit D/A Output Amplifiers
- High Speed Buffers
- Fast Sample-and-Hold Amplifiers
- High Speed Integrators
- Voltage to Frequency Converters
- Active Filters
- Log Amplifiers
- Peak Detectors

## DESCRIPTION

The **LT<sup>®</sup>1122** JFET input operational amplifier combines high speed and precision performance.

A unique poly-gate JFET process minimizes gate series resistance and gate-to-drain capacitance, facilitating wide bandwidth performance, without degrading JFET transistor matching.

It slews at 80V/μs and settles in 340ns. The LT1122 is internally compensated to be unity-gain stable, yet it has a bandwidth of 14MHz at a supply current of only 7mA. Its speed makes the LT1122 an ideal choice for fast settling 12-bit data conversion and acquisition systems.

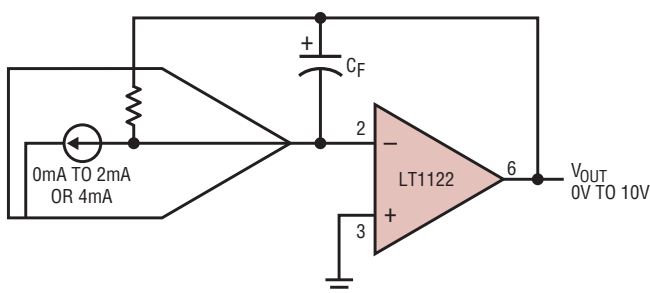
The LT1122 offset voltage of 120μV, and voltage gain of 500,000 also support the 12-bit accurate applications.

The input bias current of 10pA and offset current of 4pA combined with its speed allow the LT1122 to be used in such applications as high speed sample and hold amplifiers, peak detectors, and integrators.

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## TYPICAL APPLICATION

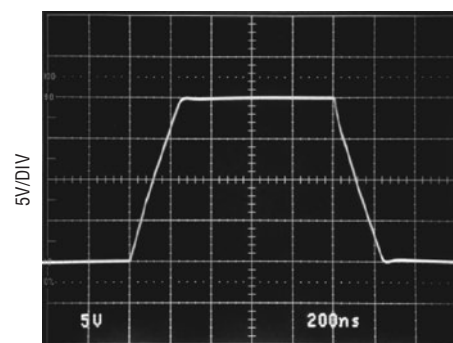
**12-Bit Voltage Output D/A Converter**



12-BIT CURRENT OUTPUT D/A CONVERTER  
 $C_F = 5\text{pF TO } 17\text{pF}$   
 (DEPENDENT ON D/A CONVERTER USED)

LT1122-TA01

**Large-Scale Response**



200ns/DIV  
 $A_v = -1$

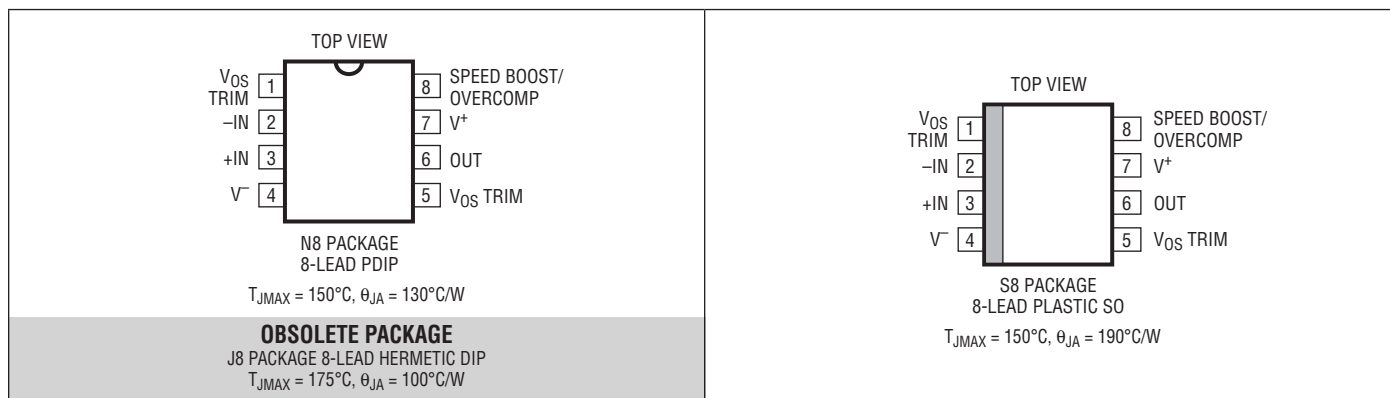
1122 TA07

# LT1122

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage .....	±20V	Operating Temperature Range	
Differential Input Voltage .....	±40V	LT1122AM/BM/CM/DM ( <b>OBSOLETE</b> )..	-55°C to 125°C
Input Voltage.....	±20V	LT1122AC/BC/CC/DC/CS/DS .....	-40°C to 85°C
Output Short Circuit Duration .....	Indefinite	Storage Temperature Range	
Lead Temperature (Soldering, 10 sec.).....	300°C	All Devices .....	-65°C to 150°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1122ACN8#PBF	LT1122ACN8#TRPBF	LT1122ACN8	8-Lead Plastic DIP	-40°C to 85°C
LT1122BCN8#PBF	LT1122BCN8#TRPBF	LT1122BCN8	8-Lead Plastic DIP	-40°C to 85°C
LT1122CCN8#PBF	LT1122CCN8#TRPBF	LT1122CCN8	8-Lead Plastic DIP	-40°C to 85°C
LT1122DCN8#PBF	LT1122DCN8#TRPBF	LT1122DCN8	8-Lead Plastic DIP	-40°C to 85°C
LT1122CS8#PBF	LT1122CS8#TRPBF	1122C	8-Lead Plastic SO	-40°C to 85°C
LT1122DS8#PBF	LT1122DS8#TRPBF	1122D	8-Lead Plastic SO	-40°C to 85°C
OBSOLETE PACKAGE				
LT1122AMJ8#PBF	LT1122AMJ8#TRPBF	LT1122AMJ8	8-Lead Hermetic DIP	-55°C to 125°C
LT1122BMJ8#PBF	LT1122BMJ8#TRPBF	LT1122BMJ8	8-Lead Hermetic DIP	-55°C to 125°C
LT1122CMJ8#PBF	LT1122CMJ8#TRPBF	LT1122CMJ8	8-Lead Hermetic DIP	-55°C to 125°C
LT1122DMJ8#PBF	LT1122DMJ8#TRPBF	LT1122DMJ8	8-Lead Hermetic DIP	-55°C to 125°C
LT1122ACJ8#PBF	LT1122ACJ8#TRPBF	LT1122ACJ8	8-Lead Hermetic DIP	-40°C to 85°C
LT1122BCJ8#PBF	LT1122BCJ8#TRPBF	LT1122BCJ8	8-Lead Hermetic DIP	-40°C to 85°C
LT1122CCJ8#PBF	LT1122CCJ8#TRPBF	LT1122CCJ8	8-Lead Hermetic DIP	-40°C to 85°C
LT1122DCJ8#PBF	LT1122DCJ8#TRPBF	LT1122DCJ8	8-Lead Hermetic DIP	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.  
 Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part markings, go to: <http://www.linear.com/leadfree/>  
 For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_S = \pm 15\text{V}$ ,  $V_{CM} = 0\text{V}$  unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS	LT1122AM/BM LT1122AC/BC			LT1122CM/DM LT1122CC/DC LT1122CS/DS			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
$V_{OS}$	Input Offset Voltage		120	600		130	900		$\mu\text{V}$	
$I_{OS}$	Input Offset Current		4	40		5	50		$\text{pA}$	
$I_B$	Input Bias Current		10	75		12	100		$\text{pA}$	
	Input Resistance Differential		$10^{12}$			$10^{12}$				$\Omega$
	Common Mode	$V_{CM} = -10\text{V to } 8\text{V}$	$10^{12}$			$10^{12}$				$\Omega$
		$V_{CM} = 8\text{V to } 11\text{V}$	$10^{11}$			$10^{11}$				$\Omega$
	Input Capacitance		4			4				$\text{pF}$
SR	Slew Rate	$A_V = -1$	60	80		50	75		$\text{V}/\mu\text{s}$	
	Settling Time (Note 2)	10V to 0V, -10V to 0V 100% Tested: A- and C-Grades to 1mV at Sum Node B- and D-Grades to 1mV at Sum Node All Grades to 0.5mV at Sum Node		340	540		350	590		ns
				350			360			ns
				450			470			ns
GBW	Gain-Bandwidth Product Power Bandwidth	$V_{OUT} = 20V_{P-P}$	14			13				MHz
			1.2			1.1				MHz
$A_{VOL}$	Large-Signal Voltage Gain	$V_{OUT} = \pm 10\text{V}$ , $R_L = 2\text{k}\Omega$ $V_{OUT} = \pm 10\text{V}$ , $R_L = 600\Omega$	180	500		150	450		$\text{V}/\text{mV}$	
			130	250		110	220		$\text{V}/\text{mV}$	
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10\text{V}$	83	99		80	98		dB	
	Input Voltage Range	(Note 4)	$\pm 10.5$	$\pm 11$		$\pm 10.5$	$\pm 11$		V	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10\text{V to } \pm 18\text{V}$	86	103		82	101		dB	
	Input Noise Voltage	0.1Hz to 10Hz	3.0			3.3				$\mu\text{V}_{P-P}$
	Input Noise Voltage Density	$f_0 = 100\text{Hz}$ $f_0 = 10\text{kHz}$	25			27				$\text{nV}/\sqrt{\text{Hz}}$
			14			15				$\text{nV}/\sqrt{\text{Hz}}$
	Input Noise Current Density	$f_0 = 100\text{Hz}$ , $f_0 = 10\text{kHz}$	2			2				$\text{fA}/\sqrt{\text{Hz}}$
$V_{OUT}$	Output Voltage Swing	$R_L = 2\text{k}\Omega$ $R_L = 600\Omega$	$\pm 12$	$\pm 12.5$		$\pm 12$	$\pm 12.5$		V	
			$\pm 11.5$	$\pm 12$		$\pm 11.5$	$\pm 12$		V	
$I_S$	Supply Current		7.5	10		7.8	11		mA	
	Minimum Supply Voltage	(Note 5)	$\pm 5$			$\pm 5$				V
	Offset Adjustment Range	$R_{POT} \geq 10\text{k}$ , Wiper to $V^+$	$\pm 4$	$\pm 10$		$\pm 4$	$\pm 10$		mV	

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ .  $V_S = \pm 15\text{V}$ ,  $V_{CM} = 0\text{V}$ . (Note 2)

SYMBOL	PARAMETER	CONDITIONS	LT1122AC/BC			LT1122CC/DC LT1122CS/DS			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage		●	350	1400		400	2000	$\mu\text{V}$
	Average Temperature Coefficient of Input Offset Voltage		●	5	18		6	25	$\mu\text{V}/^{\circ}\text{C}$
$I_{OS}$	Input Offset Current		●	12	150		15	200	$\text{pA}$
$I_B$	Input Bias Current		●	80	600		90	800	$\text{pA}$
$A_{VOL}$	Large-Signal Voltage Gain	$V_{OUT} = \pm 10\text{V}$ , $R_L \geq 2\text{k}\Omega$	●	120	380		100	340	$\text{V}/\text{mV}$
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10\text{V}$	●	82	98		78	96	$\text{dB}$
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10\text{V}$ to $\pm 17\text{V}$	●	84	101		80	99	$\text{dB}$
	Input Voltage Range		●	$\pm 10$	$\pm 10.8$		$\pm 10$	$\pm 10.8$	$\text{V}$
$V_{OUT}$	Output Voltage Swing	$R_L = 2\text{k}\Omega$	●	$\pm 11.5$	$\pm 12.4$		$\pm 11.5$	$\pm 12.4$	$\text{V}$
SR	Slew Rate	$A_V = -1$	●	50	70		40	65	$\text{V}/\mu\text{s}$

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ .  $V_S = \pm 15\text{V}$ ,  $V_{CM} = 0\text{V}$ . (Note 2)

SYMBOL	PARAMETER	CONDITIONS	LT1122AM/BM			LT1122CS/DS			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage		●	650	2400		800	3400	$\mu\text{V}$
	Average Temperature Coefficient of Input Offset Voltage		●	6	18		7	25	$\mu\text{V}/^{\circ}\text{C}$
$I_{OS}$	Input Offset Current		●	0.5	6		0.6	9	$\text{nA}$
$I_B$	Input Bias Current		●	6	25		7	35	$\text{nA}$
$A_{VOL}$	Large-Signal Voltage Gain	$V_{OUT} = \pm 10\text{V}$ , $R_L \geq 2\text{k}\Omega$	●	70	230		60	200	$\text{V}/\text{mV}$
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10\text{V}$	●	80	97		76	94	$\text{dB}$
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10\text{V}$ to $\pm 17\text{V}$	●	83	100		78	98	$\text{dB}$
	Input Voltage Range		●	$\pm 10$	$\pm 10.5$		$\pm 10$	$\pm 10.5$	$\text{V}$
$V_{OUT}$	Output Voltage Swing	$R_L = 2\text{k}\Omega$	●	$\pm 11.3$	$\pm 12.1$		$\pm 11.3$	$\pm 12.1$	$\text{V}$
SR	Slew Rate	$A_V = -1$	●	45	60		35	55	$\text{V}/\mu\text{s}$

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ .  $V_S = \pm 15\text{V}$ ,  $V_{CM} = 0\text{V}$ . (Note 6)

SYMBOL	PARAMETER	CONDITIONS	LT1122AM/BM			LT1122CS/DS			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage		●	450	1900		500	2700	$\mu\text{V}$
	Average Temperature Coefficient of Input Offset Voltage		●	6	20		7	28	$\mu\text{V}/^{\circ}\text{C}$
$I_{OS}$	Input Offset Current		●	30	600		40	900	$\text{pA}$
$I_B$	Input Bias Current		●	230	2000		260	2700	$\text{pA}$
$A_{VOL}$	Large-Signal Voltage Gain	$V_{OUT} = \pm 10\text{V}$ , $R_L \geq 2\text{k}\Omega$	●	95	340		80	300	$\text{V}/\text{mV}$
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10\text{V}$	●	80	98		76	96	$\text{dB}$
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10\text{V}$ to $\pm 17\text{V}$	●	83	100		78	98	$\text{dB}$
	Input Voltage Range		●	$\pm 10$	$\pm 10.6$		$\pm 10$	$\pm 10.6$	$\text{V}$
$V_{OUT}$	Output Voltage Swing	$R_L = 2\text{k}\Omega$	●	$\pm 11.3$	$\pm 12.2$		$\pm 11.3$	$\pm 12.2$	$\text{V}$
SR	Slew Rate	$A_V = -1$	●	45	60		35	60	$\text{V}/\mu\text{s}$

# ELECTRICAL CHARACTERISTICS

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LT1122 is measured in an automated tester in less than one second after application of power. Depending on the package used, power dissipation, heat sinking, and air flow conditions, the fully warmed up chip temperature can be 10°C to 50°C higher than the ambient temperature.

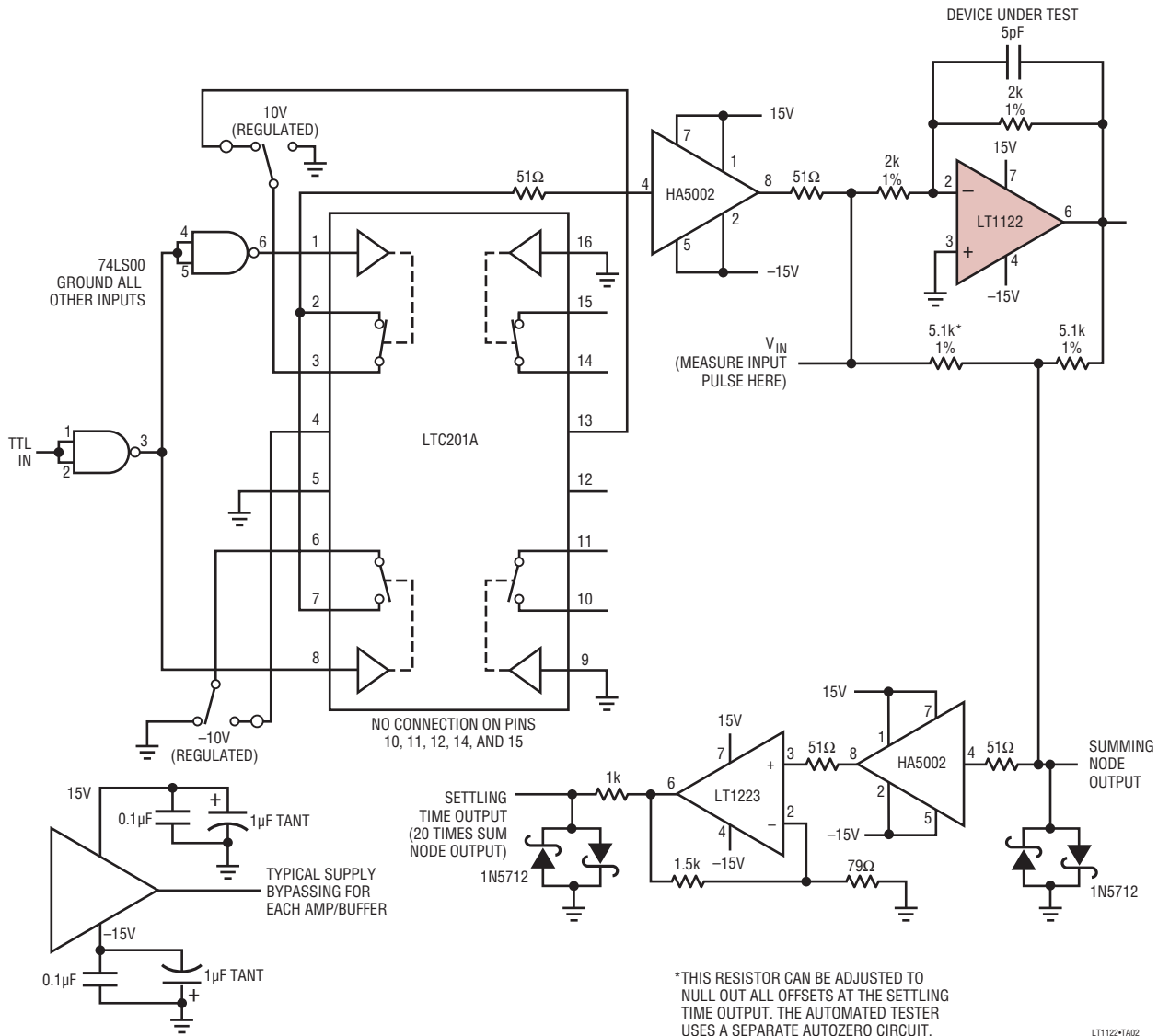
**Note 3:** Settling time is 100% tested for A- and C-grades using the settling time test circuit shown. This test is not included in quality assurance sample testing.

**Note 4:** Input voltage range functionality is assured by testing offset voltage at the input voltage range limits to a maximum of 4mV (A, B grades), to 5.7mV (C, D grades).

**Note 5:** Minimum supply voltage is tested by measuring offset voltage to 7mV maximum at ±5V supplies.

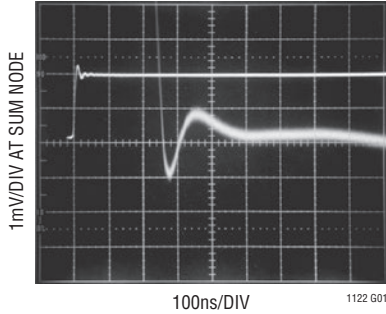
**Note 6:** The LT1122 is not tested and not quality-assurance-sampled at -40°C and at 85°C. These specifications are guaranteed by design, correlation and/or inference from -55°C, 0°C, 25°C, 70°C and/or 125°C tests.

Settling Time Test Fixture

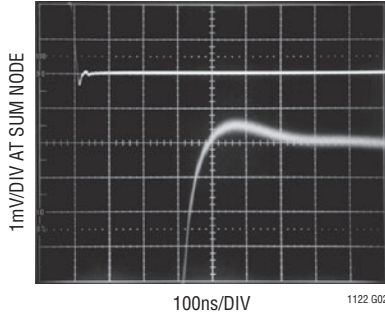


# TYPICAL PERFORMANCE CHARACTERISTICS

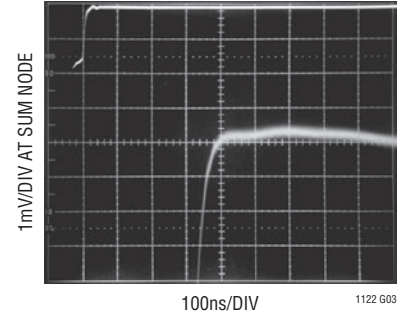
**Settling Time**  
(Input from -10V to 0V)



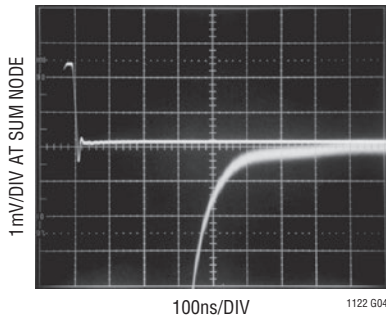
**Settling Time**  
(Input from 10V to 0V)



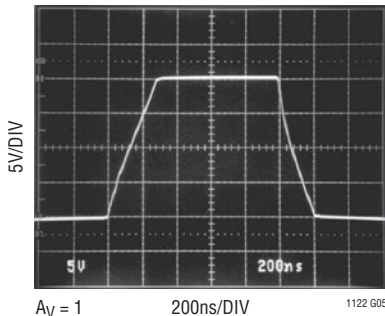
**Settling Time**  
(Input from 0V to 10V)



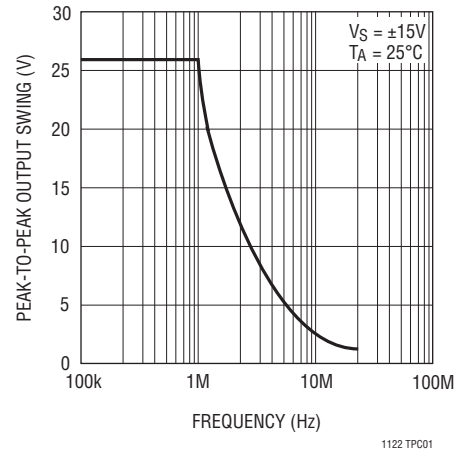
**Settling Time**  
(Input from 0V to -10V)



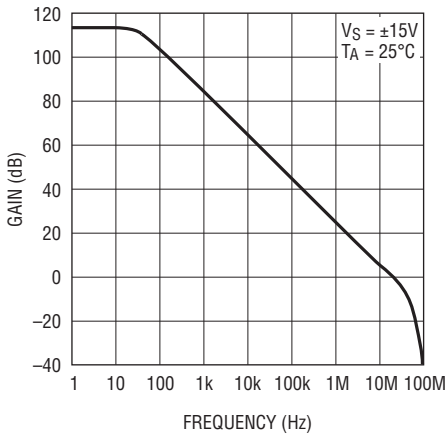
**Large-Signal Response**



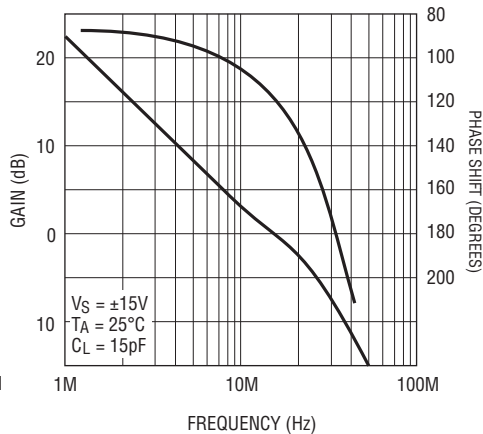
**Undistorted Output Swing vs Frequency**



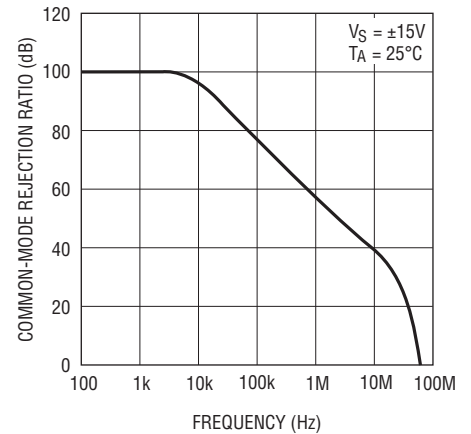
**Voltage Gain vs Frequency**



**Gain, Phase vs Frequency**

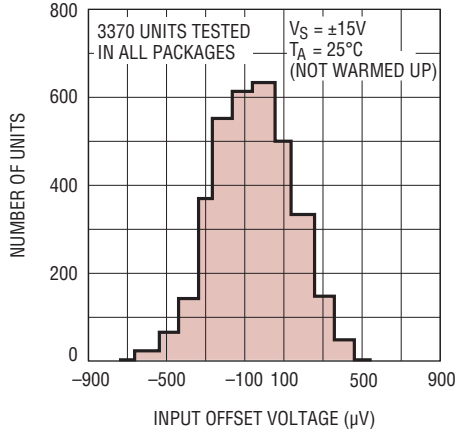


**Common-Mode Rejection vs Frequency**



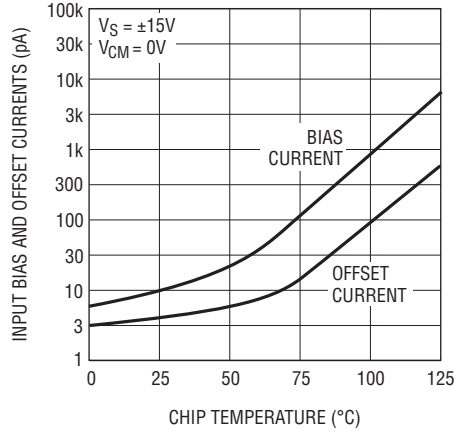
# TYPICAL PERFORMANCE CHARACTERISTICS

**Distribution of Input Offset Voltage**



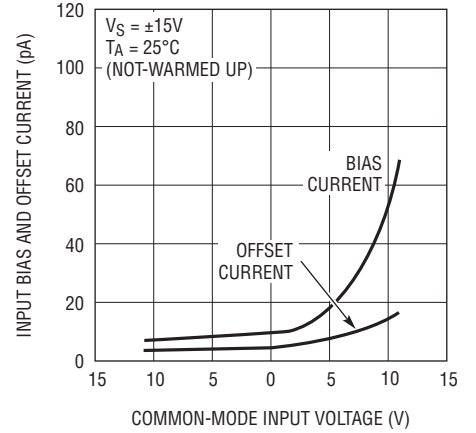
1122 TPC05

**Input Bias and Offset Currents Over Temperature**



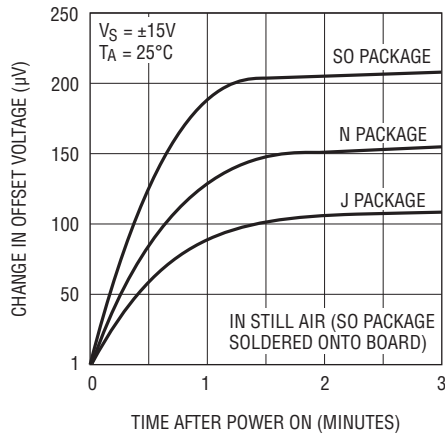
1122 TPC06

**Bias and Offset Currents Over the Common-Mode Range**



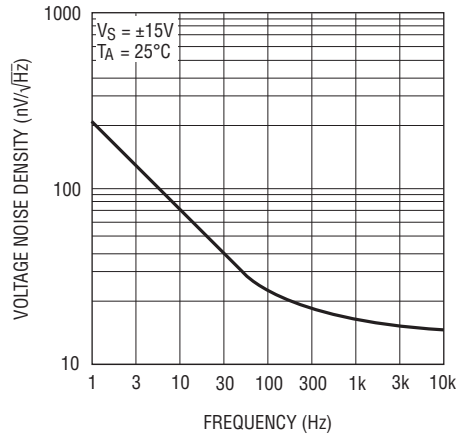
1122 TPC07

**Warm-Up Drift**



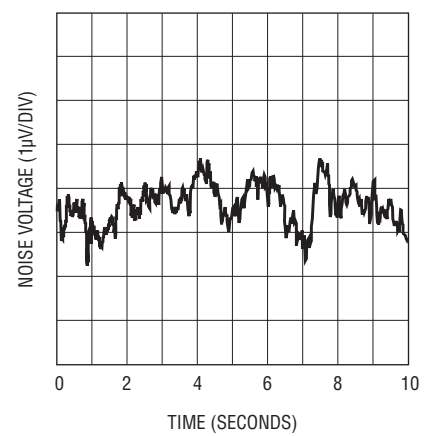
1122 TPC08

**Noise Spectrum**



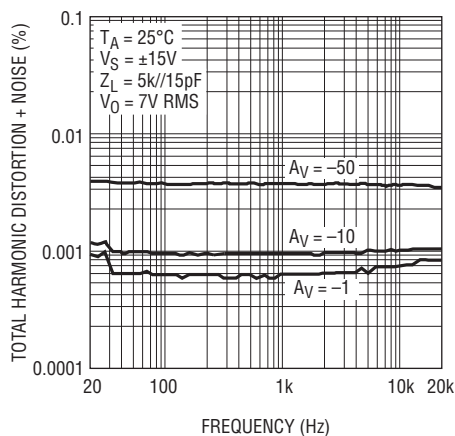
1122 TPC09

**0.1Hz to 10Hz Noise**



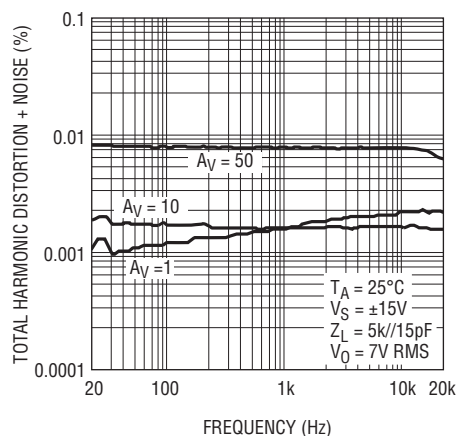
1122 TPC10

**Total Harmonic Distortion + Noise vs Frequency Inverting Gain**



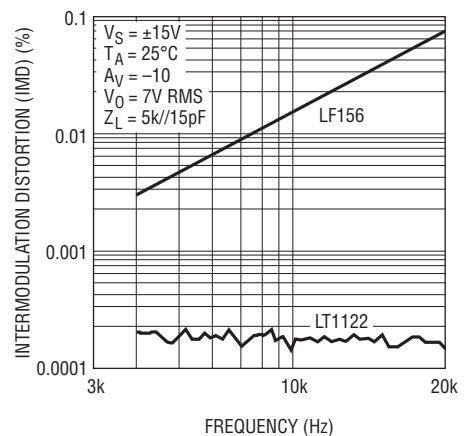
1122 TPC11

**Total Harmonic Distortion + Noise vs Frequency Noninverting Gain**



1122 TPC12

**Intermodulation Distortion (CCIF Method) vs Frequency LT1122 and LF156\***



\*SEE LT1115 DATA SHEET FOR DEFINITION OF CCIF TESTING

1122 TPC13  
1122fb

## APPLICATIONS INFORMATION

### Settling Time Measurements

Settling time test circuits shown on some competitive devices' data sheets require:

1. A "flat top" pulse generator. Unfortunately, flat top pulse generators are not commercially available.
2. A variable feedback capacitor around the device under test. This capacitor varies over a four-to-one range. Presumably, as each op amp is measured for settling time, the capacitor is fine tuned to optimize settling time for that particular device.
3. A small inductor load to optimize settling.

The LT1122's settling time is 100% tested in the test circuit shown. No "flat top" pulse generator is required. The test circuit can be readily constructed, using commercially available ICs. Of course, standard high frequency board construction techniques should be followed. All LT1122s are measured with a constant feedback capacitor. No fine tuning is required.

### Speed Boost/Overcompensation Terminal

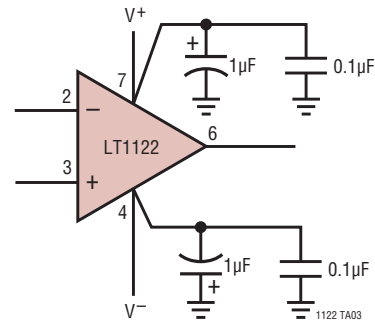
Pin 8 of the LT1122 can be used to change the input stage operating current of the device. Shorting Pin 8 to the positive supply (Pin 7) increases slew rate and bandwidth by about 25%, but at the expense of a reduction in phase margin by approximately 18 degrees. Unity-gain capacitive load handling decreases from typically 500pF to 100pF.

Conversely, connecting a 15k resistor from Pin 8 to ground pulls 1mA out of Pin 8 (with  $V^+ = 15V$ ). This reduces slew rate and bandwidth by 25%. Phase margin and capacitive load handling improve; the latter typically increasing to 800pF.

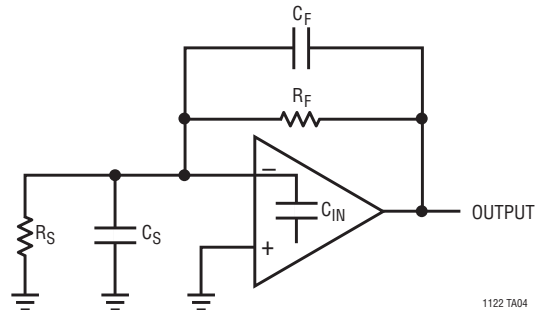
### High Speed Operation

As with most high speed amplifiers, care should be taken with supply decoupling, lead dress and component placement.

The power supply connections to the LT1122 must maintain a low impedance to ground over a bandwidth of 20MHz. This is especially important when driving a significant resistive or capacitive load, since all current delivered to the load comes from the power supplies. Multiple high quality bypass capacitors are recommended for each power supply line in any critical application. A 0.1µF ceramic and a 1µF electrolytic capacitor, as shown, placed as close as possible to the amplifier (with short lead lengths to power supply common) will assure adequate high frequency bypassing, in most applications.

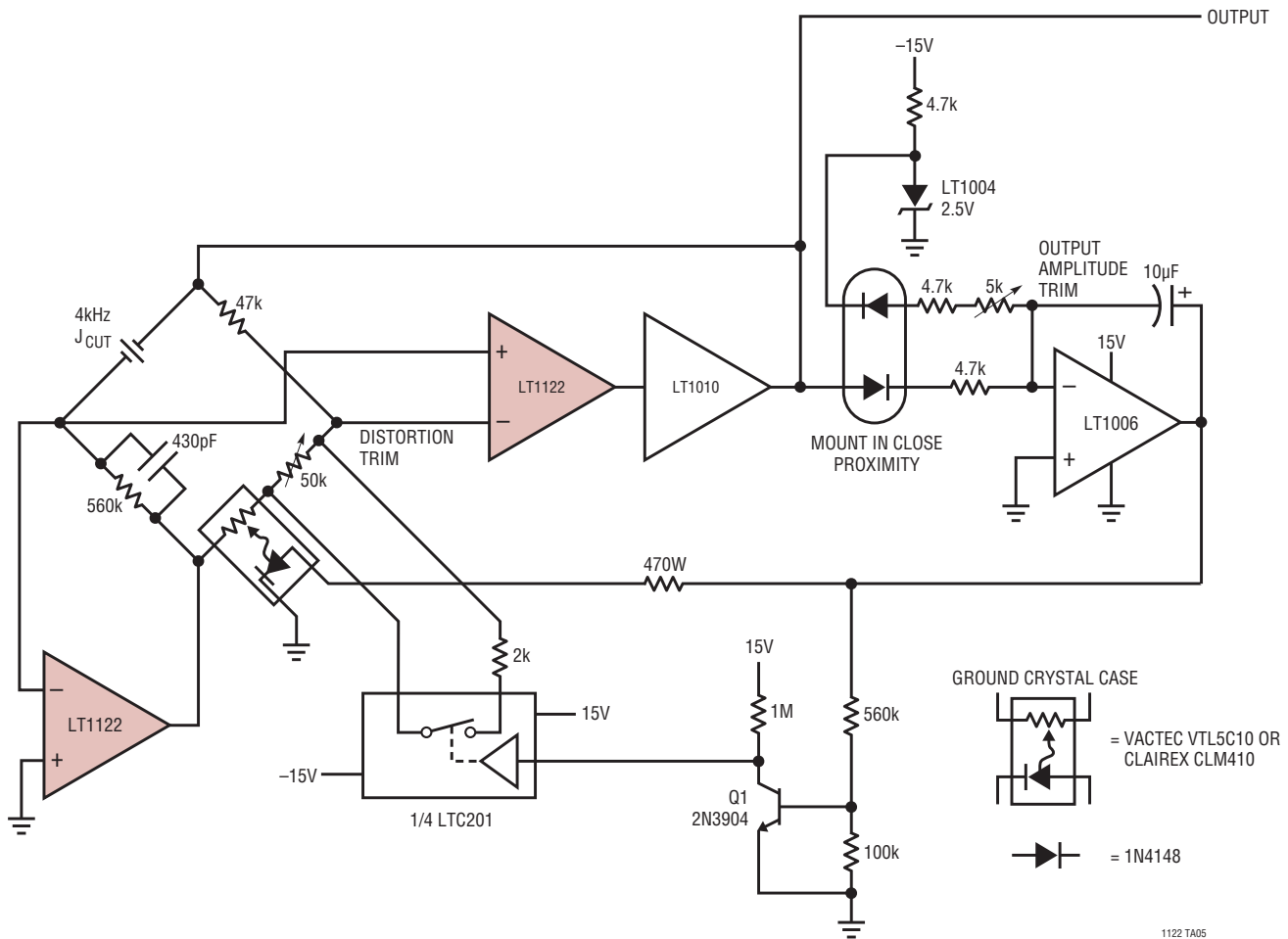


When the feedback around the op amp is resistive ( $R_F$ ), a pole will be created with  $R_F$ , the source resistance and capacitance ( $R_S, C_S$ ), and the amplifier input capacitance ( $C_{IN} \approx 4pF$ ). In low closed-loop gain configurations and with  $R_S$  and  $R_F$  in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor ( $C_F$ ) in parallel with  $R_F$  eliminates this problem. With  $R_S (C_S + C_{IN}) = R_F C_F$ , the effect of the feedback pole is completely removed.



# TYPICAL APPLICATIONS

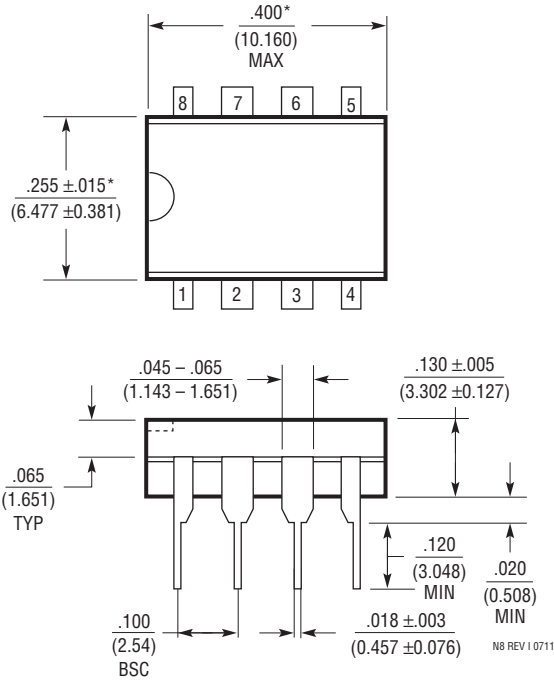
## Quartz Stabilized Oscillator With 9ppm Distortion



# PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

**N Package**  
**8-Lead PDIP (Narrow .300 Inch)**  
 (Reference LTC DWG # 05-08-1510 Rev I)



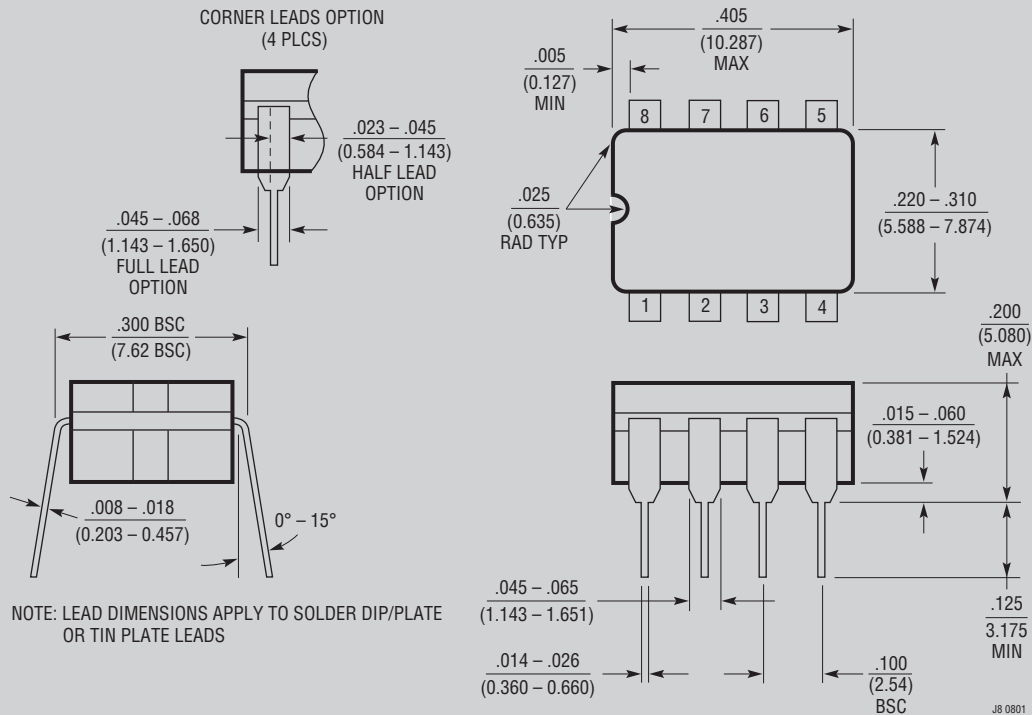
NOTE:  
 1. DIMENSIONS ARE  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$   
 \*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

N8 REV I 0711

# PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

## J8 Package 3-Lead CERDIP (Narrow .300 Inch, Hermetic) (Reference LTC DWG # 05-08-1110)



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS

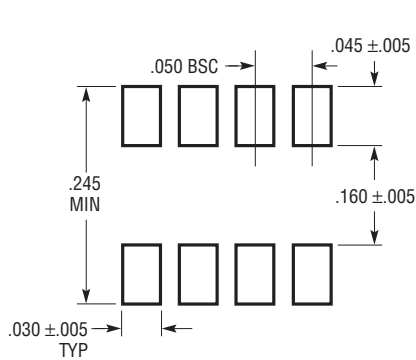
J8 0801

**OBsolete PACKAGE**

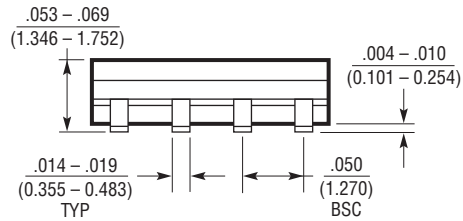
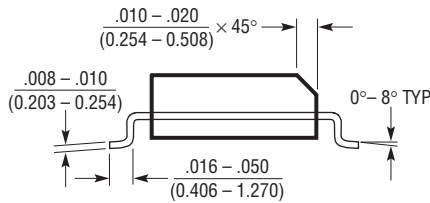
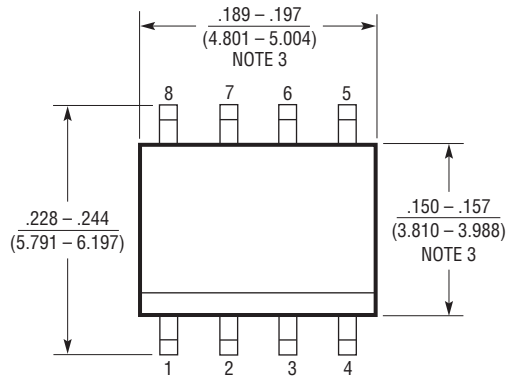
# PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

## S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610 Rev G)



RECOMMENDED SOLDER PAD LAYOUT



- NOTE:  
 1. DIMENSIONS IN  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$   
 2. DRAWING NOT TO SCALE  
 3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)  
 4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

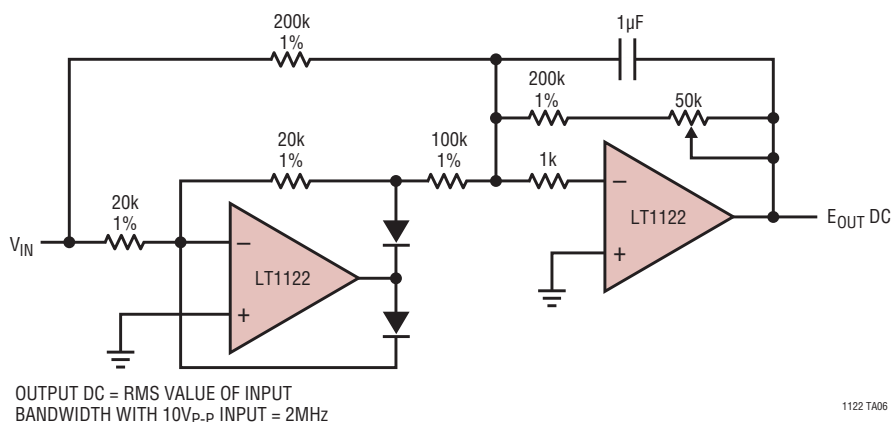
S08 REV G 0212

**REVISION HISTORY** (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	02/14	Updated data sheet to current standards. New Order Information Table, Package Descriptions	2, 10-12

## TYPICAL APPLICATION

### Wide-Band, Filtered, Full Wave Rectifier



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
<a href="#">LT1022</a>	High Speed Precision JFET Op Amp	23V/µs Min Slew Rate, 250µV V <sub>OS</sub>
<a href="#">LT1055/LT1056</a>	Precision High Speed JFET Op Amps	16V/µs Slew Rate, 150µV V <sub>OS</sub>
<a href="#">LT1464</a>	1MHz C-Load™ Stable JFET Op Amp	Capacitive Loads Up to 10nF
<a href="#">LTC®6244</a>	50MHz Low Noise CMOS Op Amp	1pA I <sub>B</sub> , 100µV Max V <sub>OS</sub> , 1.5µV <sub>p-p</sub> , 0.1Hz to 10Hz Noise

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