THE DATASHEET OF

LP5990TM-2.8EV

LP5990 Micropower 200mA CMOS Low Dropout Voltage Regulator

Check for Samples: LP5990

FEATURES

- **Operation from 2.2V to 5.5V Input**
- **±1% Accuracy Over Temp Range**
- **Output Voltage from 0.8V to 3.6V in 50mV Increments**
- **30 µA Quiescent Current (Enabled)**
- **10nA Quiescent Current (Disabled)**
- **160mV Dropout at 200mA Load**
- **60 μV_{RMS} Output Voltage Noise**
- **60 µs Start-Up Time**
- **500µs Shut-Down Time**
- **PSRR 55 dB at 10 kHz**
- **Stable with 0402 1.0µF Ceramic Capacitors**
- **Logic Controlled Enable**
- **Thermal–Overload and Short–Circuit Protection**

APPLICATIONS

- **Cellular Phones**
- **Hand–Held Information Appliances**

PACKAGE

- **4-Bump DSBGA, 0.4 mm Pitch 866 µm x 917 µm (Lead Free)**

DESCRIPTION

The LP5990 regulator is designed to meet the requirements of portable, battery-powered systems providing an accurate output voltage, low noise and low quiescent current.

The LP5990 will provide a 1.8V output from a low input voltage of 2.2V and can provide 200mA to an external load.

When switched into shutdown mode via a logic signal at the enable pin, the power consumption is reduced to virtually

zero.

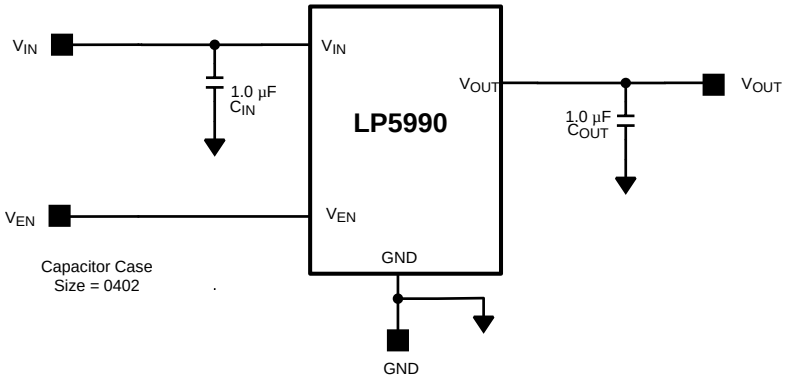
Fast shut-down is achieved by the push pull architecture.

The LP5990 is designed to be stable with space saving 0402 ceramic capacitors as small as 1µF, this gives an overall solution size of < 2.5mm ^{2}.

Performance is specified for a -40°C to 125°C junction temperature range.

The device is available in DSBGA Package (0.4mm pitch) and is available with 1.2V,1.3V,1.8V,2.8V,3.0V,3.3V and 3.6V outputs. Lower voltage options down to 0.8V are available on request. For all other output voltage options please contact your local TI sales office.

TYPICAL APPLICATION CIRCUIT



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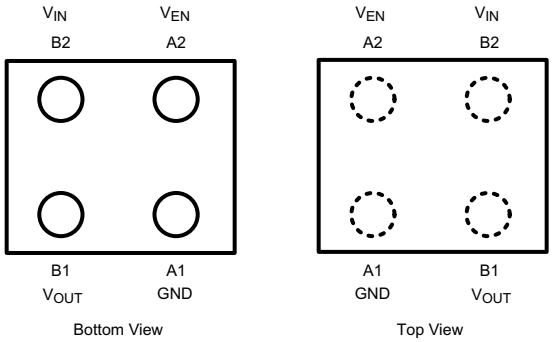
CONNECTION DIAGRAMS

Figure 1. 4-Bump Thin DSBGA Package, 0.4mm pitch
Package Number YFQ0004CEA



The actual physical placement of the package marking will vary from part to part.

PIN DESCRIPTIONS

Pin No. DSBGA	Symbol	Name and Function
A2	V_{EN}	Enable input; disables the regulator when ≤ 0.35V. Enables the regulator when ≥ 1.0V.
A1	GND	Common ground.
B1	V_{OUT}	Output voltage. A 1.0 µF Low ESR capacitor should be connected to this Pin. Connect this output to the load circuit.
B2	V_{IN}	Input voltage supply. A 1.0 µF capacitor should be connected at this input.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)(3)

V_{IN} Pin: Input Voltage		-0.3 to 6.0V
V_{OUT} Pin: Output Voltage		-0.3 to (V_{IN} + 0.3V) to 6.0V (max)
V_{EN} Pin: Enable Input Voltage		-0.3 to 6.0V (max)
Continuous Power Dissipation (4)		Internally Limited
Junction Temperature (T_{JMAX})		150°C
Storage Temperature Range		-65 to 150°C
Maximum Lead Temperature (Soldering, 10 sec.)		260°C
ESD Rating (5)	Human Body Model	2 kV
	Machine Model	200V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage.
(5) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

OPERATING RATINGS (1), (2)

V_{IN}: Input Voltage Range	2.2V to 5.5V
V_{EN}: Enable Voltage Range	0 to 5.5V (max)
Recommended Load Current (3)	0 to 200 mA
Junction Temperature Range (T_J)	-40°C to +125°C
Ambient Temperature Range (T_A) (3)	-40°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$. See applications section.

THERMAL PROPERTIES

Junction to Ambient Thermal Resistance θ_{JA} (1)	JEDEC Board (DSBGA) (2)	100.6°C/W
	4L Cellphone Board (DSBGA)	174.8°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.
(2) Detailed description of the board can be found in JESD51-7

ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for T_A = 25°C. Limits in **boldface** type apply over the full operating junction temperature range (-40°C ≤ T_J ≤ +125°C). Unless otherwise noted, specifications apply to the LP5990 Typical Application Circuit (pg. 1) with: V_{IN} = $V_{OUT\ (NOM)}$ + 1.0V, or 2.2V, whichever is higher. V_{EN} = 1.0V, C_{IN} = C_{OUT} = 1.0 µF, I_{OUT} = 1.0 mA. (1), (2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IN}	Input Voltage			2.2		5.5	V
ΔV_{OUT}	Output Voltage Tolerance	V_{IN} = ($V_{OUT(NOM)}$ + 1.0V) to 5.5V		**−1**		**1**	%
	Line Regulation	V_{IN} = ($V_{OUT(NOM)}$ + 1.0V) to 5.5V, I_{OUT} = 1 mA			1		mV
	Load Regulation	I_{OUT} = 1 mA to 200 mA			5	**15**	mV
I_{LOAD}	Load Current	See (3)		0			mA
	Maximum Output Current			**200**			
I_Q	Quiescent Current (4)	V_{EN} = 1.0V, I_{OUT} = 0 mA			30	**75**	µA
		V_{EN} = 1.0V, I_{OUT} = 200 mA			35		
		V_{EN} = <0.35V (Disabled)			0.01		
V_{DO}	Dropout Voltage (5)	I_{OUT} = 200 mA			160	**250**	mV
I_{SC}	Short Circuit Current Limit	See (6)			600		mA
PSRR	Power Supply Rejection Ratio (7)	f = 10 kHz, I_{OUT} = 200 mA			55		dB
e_n	Output Noise Voltage (7)	BW = 10 Hz to 100 kHz, V_{IN} = 4.2V, I_{OUT} = 1 mA	V_{OUT} = 1.8V		60		μV_{RMS}
			V_{OUT} = 2.8V		85		
$T_{SHUTDOWN}$	Thermal Shutdown	Temperature			160		°C
		Hysteresis			20		
Enable Input Thresholds							
V_{IL}	Low Input Threshold (V_{EN})	V_{IN} = 2.2V to 5.5V				**0.35**	V

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are specified by design, test, or statistical analysis. Typical numbers are not specified, but do represent the most likely norm.
(3) The device maintains a stable, regulated output voltage without a load current.
(4) Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT}.
(5) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value. This parameter only applies to output voltages above 2.8V.
(6) Short Circuit Current is measured with V_{OUT} pulled to 0V.
(7) This specification is ensured by design.

ELECTRICAL CHARACTERISTICS (continued)

Limits in standard typeface are for T_A = 25°C. Limits in **boldface** type apply over the full operating junction temperature range (-40°C ≤ T_J ≤ +125°C). Unless otherwise noted, specifications apply to the LP5990 Typical Application Circuit (pg. 1) with: V_{IN} = $V_{OUT\ (NOM)}$ + 1.0V, or 2.2V, whichever is higher. V_{EN} = 1.0V, C_{IN} = C_{OUT} = 1.0 µF, I_{OUT} = 1.0 mA. (1), (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Input Threshold (V_{EN})	V_{IN} = 2.2V to 5.5V	**1.0**			V
I_{EN}	Input Current at V_{EN} Pin (8)	V_{EN} = 5.5V and V_{IN} = 5.5V		2	**5**	µA
		V_{EN} = 0.0V and V_{IN} = 5.5V		0.001		
Transient Characteristics						
ΔV_{OUT}	Line Transient (7)	T_{rise} = T_{fall} = 30µs. ΔV_{IN} = 600 mV		4		mV
	Load Transient (7)	I_{OUT} = 1 mA to 200 mA in 1 µs		–50		mV
		I_{OUT} = 200 mA to 1 mA in 1 µs		50		
T_{ON}	Turn on Time	To 98% of $V_{OUT(NOM)}$		60		µs
T_{OFF}	Turn off Time from Enable	100mV of $V_{OUT(NOM)}$ I_{OUT}= 0mA		500		µs

(8) There is a 3 MΩ resistor between V_{EN} and ground on the device.

OUTPUT & INPUT CAPACITOR, RECOMMENDED SPECIFICATIONS(1)

Symbol	Parameter	Conditions	Min	Nom	Max	Units
C_{IN}	Input Capacitance	Capacitance for stability	**0.3**	1.0		µF
C_{OUT}	Output Capacitance		**0.3**	1.0	**10**	
ESR	Output/Input Capacitance		5		500	mΩ

(1) The minimum capacitance should be greater than 0.3 µF over the full range of operating conditions. The capacitor tolerance should be 30% or better over the full temperature range. The full range of operating conditions for the capacitor in the application should be considered during device selection to ensure this minimum capacitance specification is met. X7R capacitors are recommended however capacitor types X5R, Y5V and Z5U may be used with consideration of the application and conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, $C_{IN} = C_{OUT} = 1.0\mu F$, $V_{IN} = V_{OUT(NOM)} + 1.0V$, $V_{EN} = 1.0V$, $I_{OUT} = 1mA$, $T_A = 25°C$.

Output Voltage Change vs Temperature

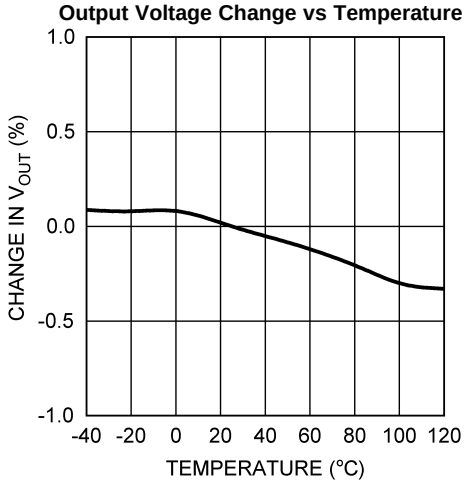


Figure 2.

Ground Current vs Load Current

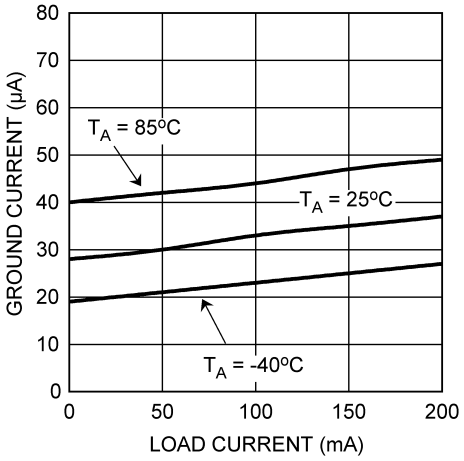


Figure 3.

Ground Current vs V_{IN}. I_{LOAD}= 1mA

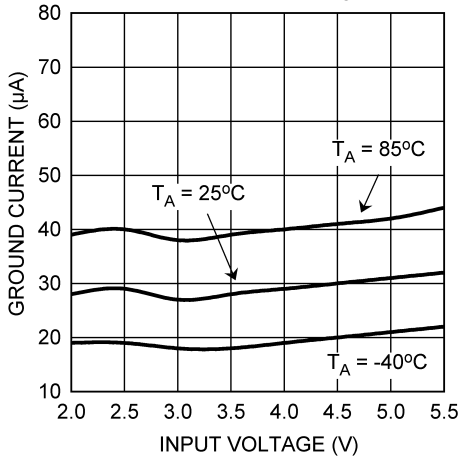


Figure 4.

Ground Current vs V_{IN}. I_{LOAD} = 200mA

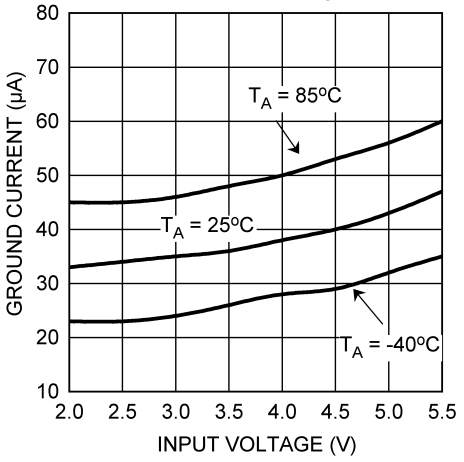


Figure 5.

Dropout Voltage

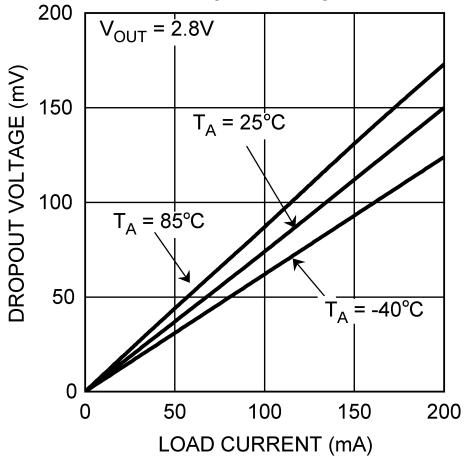


Figure 6.

Load Transient Response V_{OUT} = 2.8V

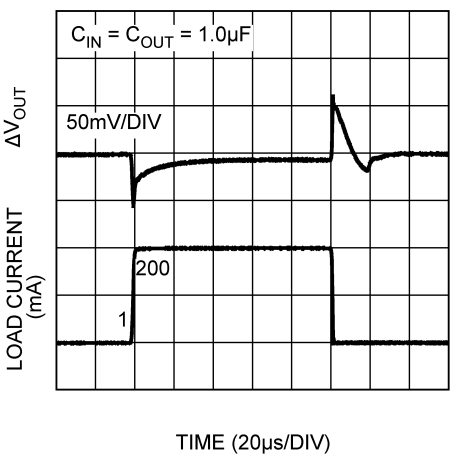


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1.0\mu F$, $V_{IN} = V_{OUT(NOM)} + 1.0V$, $V_{EN} = 1.0V$, $I_{OUT} = 1mA$, $T_A = 25°C$.

Load Transient Response. V_{OUT} = 2.8V

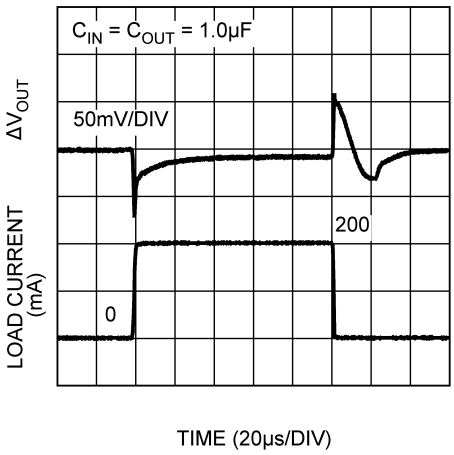


Figure 8.

Short Circuit Current

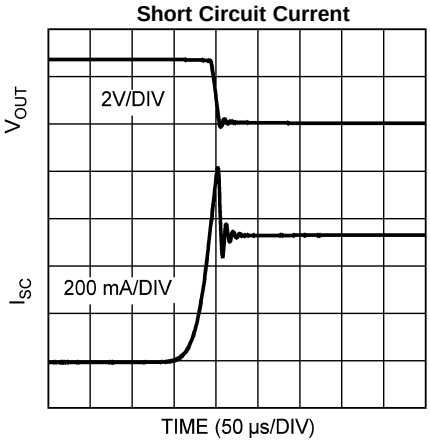


Figure 9.

Line Transient Response

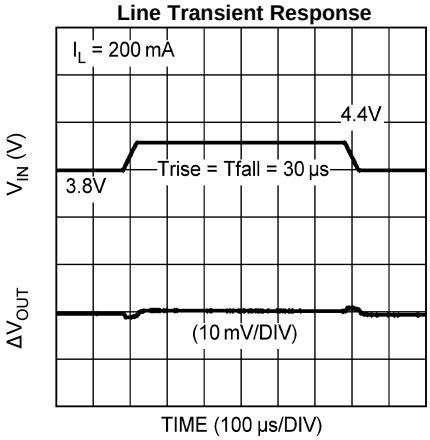


Figure 10.

Line Transient Response

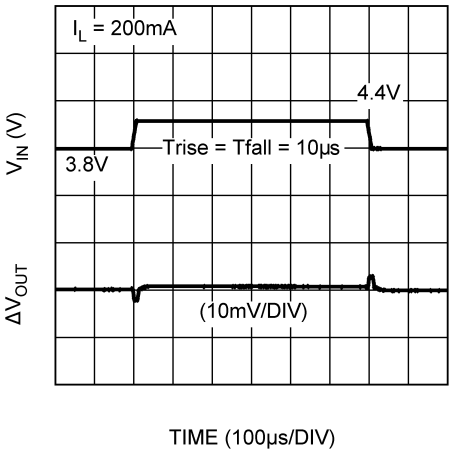


Figure 11.

Start-up Time

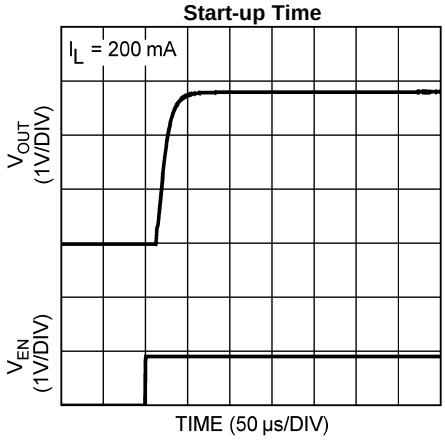


Figure 12.

Shutdown Characteristics

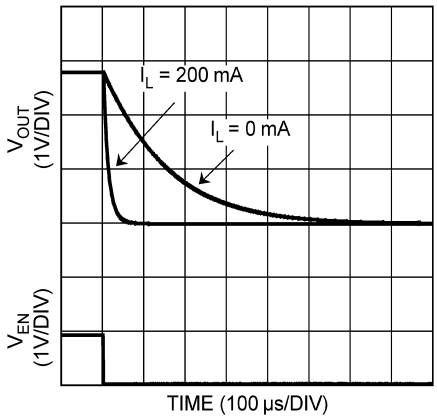


Figure 13.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1.0\mu F$, $V_{IN} = V_{OUT(NOM)} + 1.0V$, $V_{EN} = 1.0V$, $I_{OUT} = 1mA$, $T_A = 25°C$.

Power Supply Rejection ratio

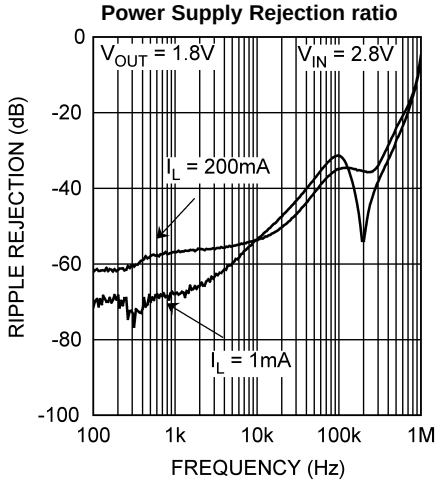


Figure 14.

Output Noise Density

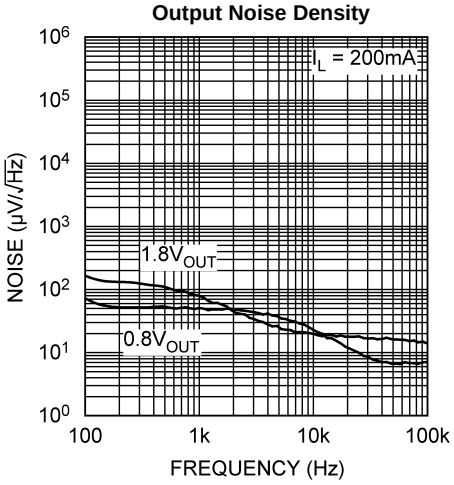


Figure 15.

APPLICATION HINTS

POWER DISSIPATION AND DEVICE OPERATION

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air. As stated in Note 3 of the Operating Ratings table, the allowable power dissipation for the device in a given package can be calculated using the equation:

$$P_D = \frac{(T_{JMAX} - T_A)}{\theta_{JA}}$$

The actual power dissipation across the device can be represented by the following equation:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT}$$

This establishes the relationship between the power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP5990 requires external capacitors for regulator stability. The LP5990 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitor is required for stability. The input capacitor should be at least equal to or greater than the output capacitor. It is recommended that a 1.0 µF capacitor be connected between the LP5990 input pin and ground.

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: To ensure stable operation it is essential that good PCB practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are to be used to connect the battery or other power source to the LP5990, then it is recommended to increase the input capacitor to at least 2.2µF. Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application. There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain 0.3 µF over the entire operating temperature range.

OUTPUT CAPACITOR

The LP5990 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types X5R or X7R) 1.0 µF, and with ESR between 5 mΩ to 500 mΩ, is suitable in the LP5990 application circuit.

Other ceramic capacitors such as Y5V and Z5U are less suitable owing to their inferior temperature characteristics. (See section in Capacitor Characteristics).

For this device the output capacitor should be connected between the V_{OUT} pin and a good ground connection and should be mounted within 1 cm of the device.

It may also be possible to use tantalum or film capacitors at the device output, V_{OUT}, but these are not as attractive for reasons of size and cost (see the section Capacitor Characteristics).

The output capacitor must meet the requirement for the minimum value of capacitance (0.3µF) and have an ESR value that is within the range 5 mΩ to 500 mΩ for stability.

CAPACITOR CHARACTERISTICS

The LP5990 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values in the range of 1.0 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1.0 µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP5990

For both input and output capacitors careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly depending on the conditions of operation and capacitor type.

In particular the output capacitor selection should take account of all the capacitor parameters to ensure that the specification is met within the application.Capacitance value can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on particular case size with smaller sizes giving poorer performance figures in general. As an example Figure 16 shows a typical graph showing a comparison of capacitor case sizes in a Capacitance versus DC Bias plot. As shown in the graph, as a result of the DC Bias condition, the capacitance value may drop below the minimum capacitance value given in the recommended capacitor table (0.3µF in this case). Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommend that the capacitor manufacturer's specifications for the nominal value capacitor are consulted for all conditions as some capacitors may not be suited in the application.

The temperature performance of ceramic capacitors varies by type and manufacturer. Most large value ceramic capacitors (≥2.2 µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47 µF to 4.7 µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

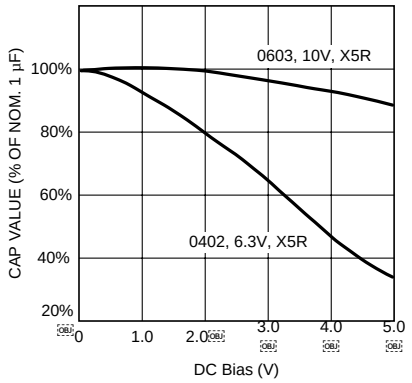


Figure 16.

NO-LOAD STABILITY

The LP5990 will remain stable and in regulation with no external load.

ENABLE CONTROL

The LP5990 may be switched ON or OFF by a logic input at the ENABLE pin, V_{EN} . A high voltage at this pin will turn the device on. When the enable pin is low, the regulator output is off and the device typically consumes 3 nA. If the application does not require the shutdown feature, the V_{EN} pin should be tied to V_{IN} to keep the regulator output permanently on.

The signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

DSBGA MOUNTING

The DSBGA package requires specific mounting techniques, which are detailed in TI Application Note AN-1112 (SNVA009).

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

DSBGA LIGHT SENSITIVITY

Exposing the DSBGA device to direct light may cause incorrect operation of the device. Light sources such as halogen lamps can affect electrical performance if they are situated in proximity to the device.

Light with wavelengths in the red and infra-red part of the spectrum have the most detrimental effect thus the fluorescent lighting used inside most buildings has very little effect on performance.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5990TM-1.2/NOPB	ACTIVE	DSBGA	YFQ	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5990TM-1.8/NOPB	ACTIVE	DSBGA	YFQ	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5990TM-2.8/NOPB	ACTIVE	DSBGA	YFQ	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5990TM-3.0/NOPB	ACTIVE	DSBGA	YFQ	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5990TM-3.6/NOPB	ACTIVE	DSBGA	YFQ	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5990TMX-1.2/NOPB	ACTIVE	DSBGA	YFQ	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5990TMX-1.8/NOPB	ACTIVE	DSBGA	YFQ	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5990TMX-2.8/NOPB	ACTIVE	DSBGA	YFQ	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5990TMX-3.3/NOPB	ACTIVE	DSBGA	YFQ	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5990TMX-3.6/NOPB	ACTIVE	DSBGA	YFQ	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

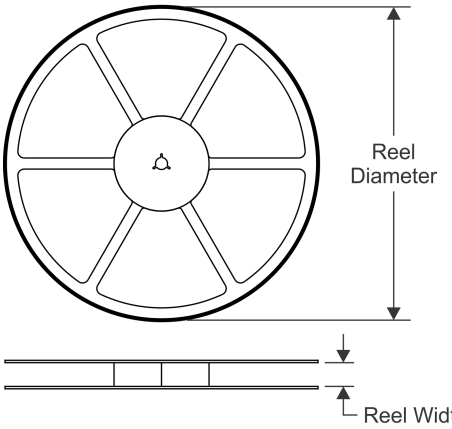
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

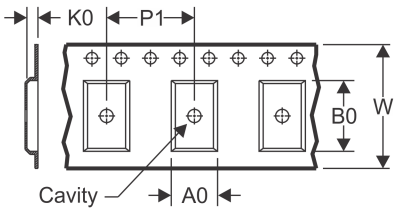
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

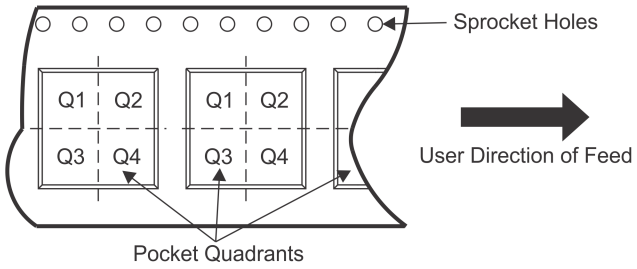


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

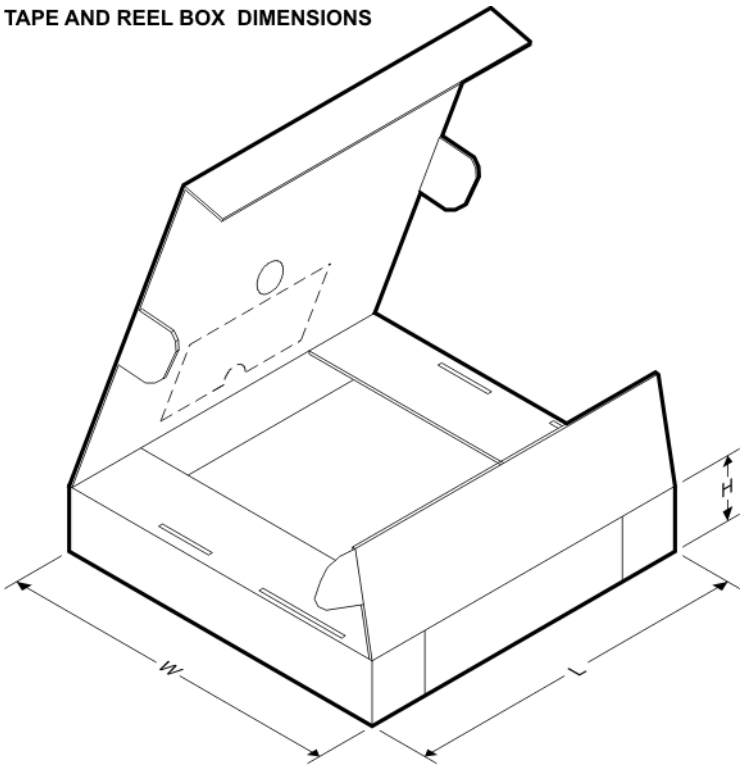
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5990TM-1.2/NOPB	DSBGA	YFQ	4	250	178.0	8.4	0.92	0.99	0.7	4.0	8.0	Q1
LP5990TM-1.8/NOPB	DSBGA	YFQ	4	250	178.0	8.4	0.92	0.99	0.7	4.0	8.0	Q1
LP5990TM-2.8/NOPB	DSBGA	YFQ	4	250	178.0	8.4	0.92	0.99	0.7	4.0	8.0	Q1
LP5990TM-3.0/NOPB	DSBGA	YFQ	4	250	178.0	8.4	0.92	0.99	0.7	4.0	8.0	Q1
LP5990TM-3.6/NOPB	DSBGA	YFQ	4	250	178.0	8.4	0.92	0.99	0.7	4.0	8.0	Q1
LP5990TMX-1.2/NOPB	DSBGA	YFQ	4	3000	178.0	8.4	0.92	0.99	0.7	4.0	8.0	Q1
LP5990TMX-1.8/NOPB	DSBGA	YFQ	4	3000	178.0	8.4	0.92	0.99	0.7	4.0	8.0	Q1
LP5990TMX-2.8/NOPB	DSBGA	YFQ	4	3000	178.0	8.4	0.92	0.99	0.7	4.0	8.0	Q1
LP5990TMX-3.3/NOPB	DSBGA	YFQ	4	3000	178.0	8.4	0.92	0.99	0.7	4.0	8.0	Q1
LP5990TMX-3.6/NOPB	DSBGA	YFQ	4	3000	178.0	8.4	0.92	0.99	0.7	4.0	8.0	Q1

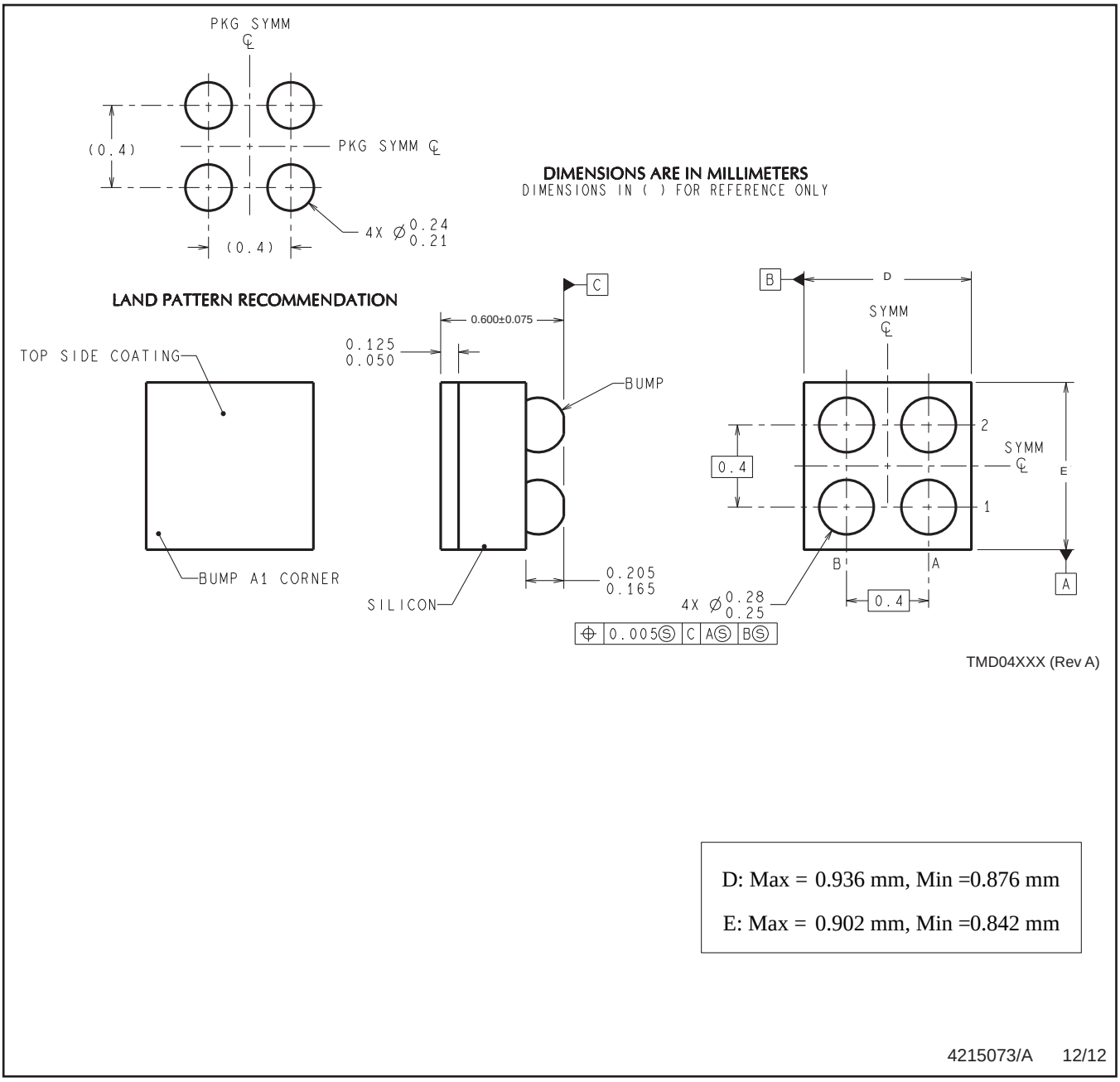
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5990TM-1.2/NOPB	DSBGA	YFQ	4	250	210.0	185.0	35.0
LP5990TM-1.8/NOPB	DSBGA	YFQ	4	250	210.0	185.0	35.0
LP5990TM-2.8/NOPB	DSBGA	YFQ	4	250	210.0	185.0	35.0
LP5990TM-3.0/NOPB	DSBGA	YFQ	4	250	210.0	185.0	35.0
LP5990TM-3.6/NOPB	DSBGA	YFQ	4	250	210.0	185.0	35.0
LP5990TMX-1.2/NOPB	DSBGA	YFQ	4	3000	210.0	185.0	35.0
LP5990TMX-1.8/NOPB	DSBGA	YFQ	4	3000	210.0	185.0	35.0
LP5990TMX-2.8/NOPB	DSBGA	YFQ	4	3000	210.0	185.0	35.0
LP5990TMX-3.3/NOPB	DSBGA	YFQ	4	3000	210.0	185.0	35.0
LP5990TMX-3.6/NOPB	DSBGA	YFQ	4	3000	210.0	185.0	35.0

YFQ0004



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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