THE DATASHEET OF

LNK457DG

LNK454/456-458/460
LinkSwitch™-PL Family

LED Driver IC with TRIAC Dimming, Single-Stage PFC and Constant Current Control for Non-Isolated Applications

Product Highlights

Dramatically Simplifies Off-line LED Drivers
- Flicker-free phase-controlled TRIAC dimming
- Single-stage power factor correction and accurate constant current (CC) output
- Very low component count with small non-electrolytic bulk capacitor for compact replacement lamp designs
- Compact SO8, eSOP, and eDIP packages
- Completely eliminates control loop compensation

Advanced Performance Features
- Optimized for non-isolated flyback designs
- Frequency jitter greatly reduces EMI filter size and costs
- Low dissipation direct sensing of LED current

Advanced Protection and Safety Features
- Cycle skipping regulation for abnormally low output power to clamp peak output current delivered
- 725 V integrated power MOSFET allows small bulk capacitance and maximizes power capability
- Short-circuit, overload, open feedback and output overvoltage protection
- Hysteretic thermal shutdown
- Meets high-voltage creepage between DRAIN and all other pins both on PCB and at package

EcoSmart™ - Energy Efficient
- High power factor optimizes system lumen per input VA
- Control algorithm balances switching and conduction losses over line and load to maintain optimum efficiency

Description

The LinkSwitch-PL family enables a very small and low cost single-stage power factor corrected constant current driver for solid state lighting. Optimized for direct LED current sensing, the LinkSwitch-PL operates over a wide input voltage range delivering an output power of up to 16 W. The LinkSwitch-PL control algorithm provides flicker-free TRIAC dimming with minimal external components.

Each device incorporates a 725 V rated power MOSFET, a novel discontinuous mode variable frequency variable on-time controller, frequency jitter, cycle-by-cycle current limit and hysteretic thermal shutdown in a monolithic 4-pin IC, available in SO-8C, eSOP-12, and eDIP-12 packages.

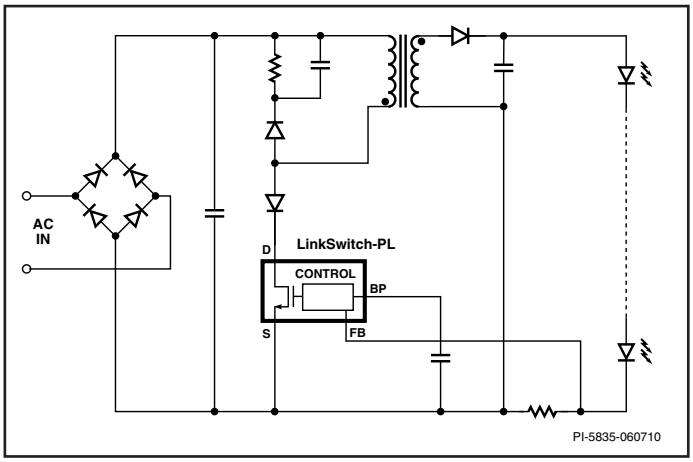


Figure 1. Basic Application Schematic.

Output Power Table

Product[2]	85-265 VAC	
	Minimum Output Power	Maximum Output Power[1]
LNK454D	1.5 W	3 W
LNK456D	3 W	6 W
LNK457D/K/V	4 W	8 W
LNK458K/V	6 W	11.5 W
LNK460K/V	8 W	16 W

Table 1. Output Power Table.

Notes:
1. Maximum practical continuous power in an open frame design with adequate heat sinking, measured at +50 °C ambient (see Key Applications Considerations for more information).
2. Packages: D: SO-8C, K: eSOP-12, V: eDIP-12.

	Output Current			
Number of Serial LEDs	**350 mA**	**500 mA**	**700 mA**	**1000 mA**
1	LNK454	LNK454	LNK454	LNK456
2	LNK454	LNK456	LNK456	LNK457
3	LNK456	LNK456	LNK457	LNK458
4	LNK456	LNK457	LNK458	LNK460
5	LNK457	LNK458	LNK460	
6	LNK457	LNK458	LNK460	
7	LNK458	LNK460		
8	LNK458	LNK460		
9	LNK458	LNK460		
10	LNK460			
11	LNK460			
12	LNK460			

Figure 2. Device Selection Based on Length of Output LED Series String and Current. A Typical Voltage Drop of 3.5 V per LED is Assumed.

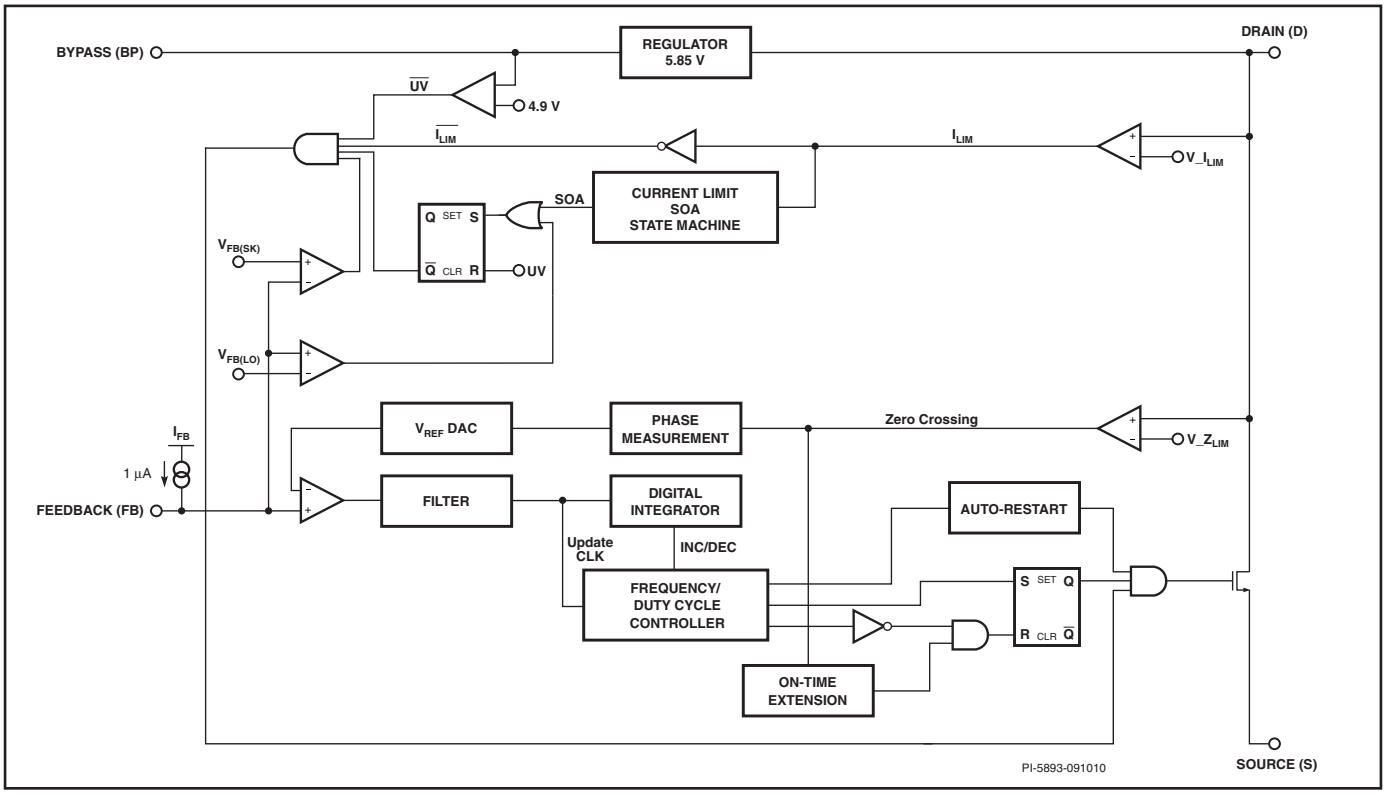


Figure 2. Functional Block Diagram.

Pin Functional Description

DRAIN (D) Pin:
High-voltage power MOSFET drain connection. The internal start-up bias current is drawn from this pin through a switched high-voltage current source. Drain current sensing and associated controller functions are also performed using this pin.

SOURCE (S) Pin:
Power MOSFET source connection. Ground reference for BYPASS and FEEDBACK pins.

BYPASS (BP) Pin:
Connection point for the external bypass capacitor for the internally generated 5.85 V supply.

FEEDBACK (FB) Pin:
LED current sensing pin. During normal operation the 290 mV threshold determines the average value of the current flowing through the load sense resistor.

A second threshold clamps excessive output current ripple.

A third higher threshold is used to protect against output short-circuit and overvoltage conditions (see Figure 5).

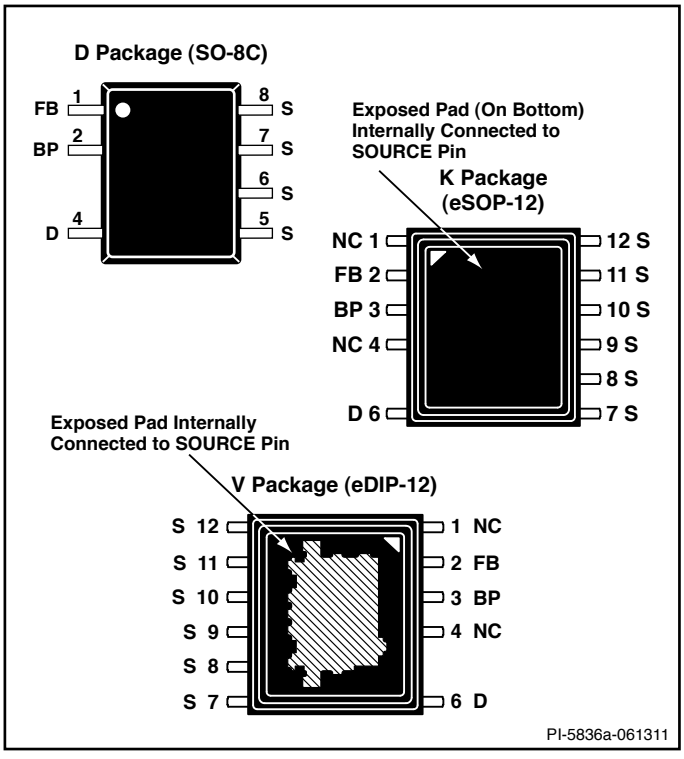


Figure 3. Pin Configuration (Top View).

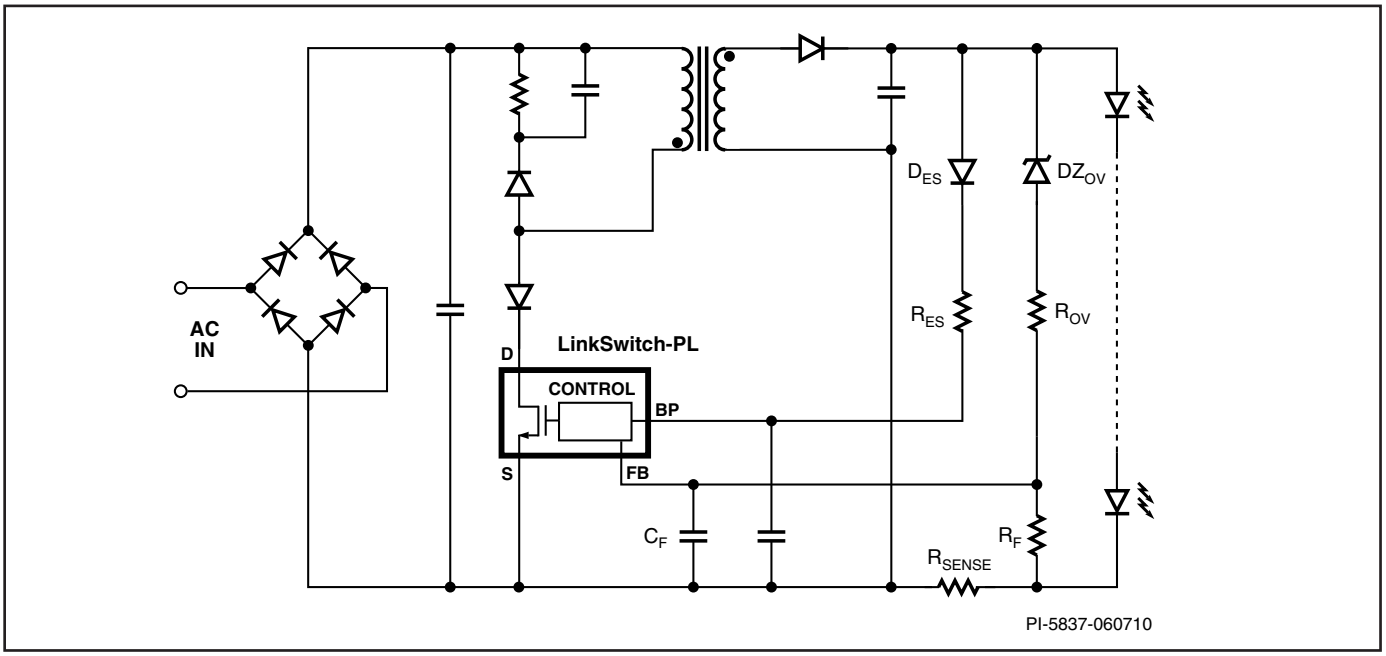


Figure 4. Typical Application Schematic.

Functional Description

The LinkSwitch-PL combines a high-voltage power MOSFET switch with a power supply controller in one device. The IC provides a single-stage power factor correction plus LED current control. The LinkSwitch-PL controller consists of an oscillator, feedback (sense and logic) circuit, 5.85 V regulator, hysteretic over-temperature protection, frequency jittering, cycle-by-cycle current limit, loop compensation circuitry, auto-restart, switching on-time extension, power factor and constant current control.

In a direct LED current sensing configuration, the average FEEDBACK pin voltage is a replica of the LED current, scaled by the sense resistor (R_{SENSE} in Figure 4). A small low-pass filter (R_F and C_F in Figure 4) reduces high frequency noise at the FEEDBACK pin.

Figure 5 illustrates the operating regions of the FEEDBACK pin voltage. The LinkSwitch-PL sets its operating point such that the average FEEDBACK pin voltage in steady-state operation is 290 mV. This threshold is set low to minimize the sensing resistor dissipation. The internal MOSFET switching frequency and on-time are updated once every input AC half-cycle to regulate the output current and maintain high power factor.

If the FEEDBACK pin peak voltage exceeds 550 mV, cycle skipping mode is triggered and the power processed by the integrated power MOSFET is clamped on a cycle-by-cycle basis. Switching frequency may vary during an input voltage half-cycle to reduce thermal stress on the output LEDs.

Auto-restart protection is triggered by a FEEDBACK pin voltage in excess of 2 V. This feature can be used to provide output overvoltage protection (via DZ_{OV} and R_{OV}, in Figure 4), which triggers the IC to enter auto-restart.

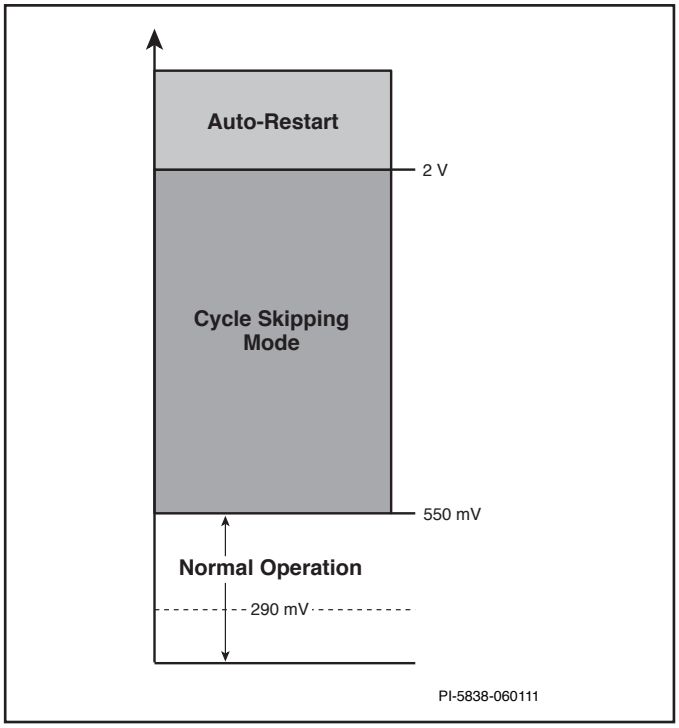


Figure 5. FEEDBACK Pin Operational Voltage Thresholds.

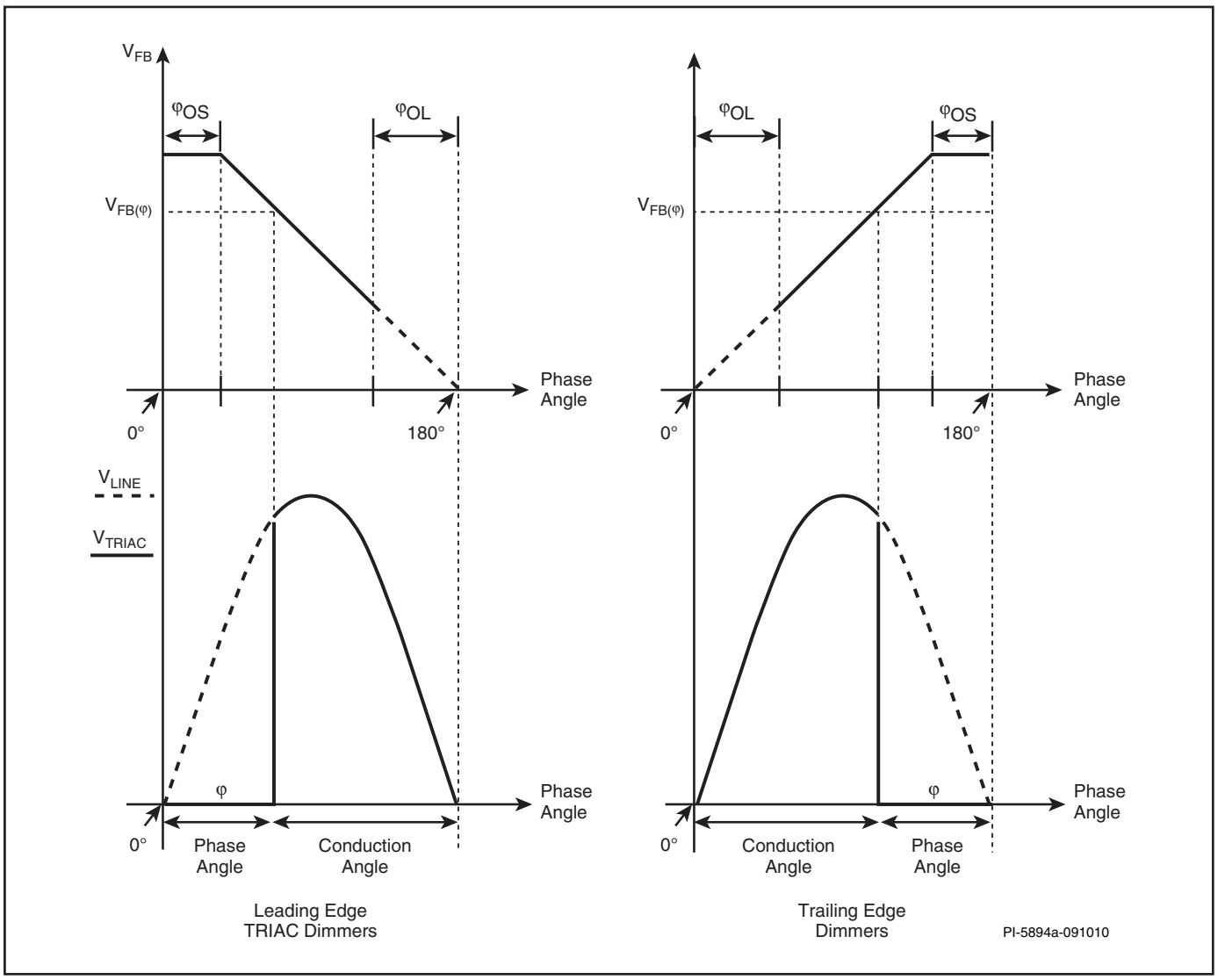


Figure 6. Feedback Voltage vs. Phase Angle Dimming Characteristics.

TRIAC (Phase-Controlled) Dimming

The LinkSwitch-PL integrates several features to improve dimming range and reduce external circuit complexity when using a phase-controlled TRIAC dimmer. The output LED current is controlled by the FEEDBACK pin voltage which changes proportionally to the TRIAC dimmer conduction angle. When the conduction angle decreases, the voltage at the FEEDBACK pin decreases causing the average LED current to decrease.

The FEEDBACK pin reference voltage adjustment is initiated at approximately 25% of the AC line half-cycle duration. When this (φOS) threshold is exceeded, V_{FB} and the output LED current are reduced until a second phase angle threshold is reached. At this point, with the TRIAC conduction angle being very limited, the IC runs open loop at constant frequency and duty cycle (φOL region) and the integrated power MOSFET processes as much power as the heavily chopped input voltage will allow creating a light output that is deeply dimmed.

The 520 mV clamping feedback threshold is also linearly reduced during dimming to control LED current ripple.

IC Supply and BYPASS Pin

The internal 5.85 V regulator charges the bypass capacitor connected to the BYPASS pin to 5.85 V by drawing current from the voltage on the DRAIN pin whenever the power MOSFET is off. The BYPASS pin is the internal supply voltage node. When the power MOSFET is on, the device operates from the energy stored in the bypass capacitor. Extremely low power consumption of the internal circuitry allows LinkSwitch-PL to operate continuously from current it takes from the DRAIN pin. A bypass capacitor value of 1 μF is sufficient for both high frequency decoupling and energy storage. Dimming applications may require a higher bypass capacitor value.

During phase angle dimming when the conduction angle is small the AC input voltage is present for only short periods of time. In that case the IC should not rely on the integrated high-voltage current source, but instead external bias circuitry should be used to supply the IC from the output (D_{ES} and R_{ES} in Figure 4). If the output voltage is less than 7 V, external bias circuitry should be implemented. This is accomplished by adding an auxiliary winding on the transformer, which is then rectified and filtered via a diode (ultrafast) and capacitor. The winding voltage (turns) should be selected such that the maximum IC consumption can be supported at the lowest operating output current.

Start-up, Switching Frequency and On-time Range

At start-up the controller uses an initial switching frequency f_{MIN} and minimum on-time $t_{ON(MIN)}$. The charging of the output capacitor together with the energy delivery to the output LEDs determines a step-by-step increase of the power MOSFET switching frequency and on-time updated every half-cycle of the AC input voltage.

The steady-state switching frequency and on-time are determined by the line voltage, voltage drop across the LEDs and converter efficiency.

At light load when the device reaches the minimum frequency f_{MIN} and on-time $t_{ON(MIN)}$, the controller regulates by skipping cycles. In this mode of operation the input current is not power factor corrected and the average output current is not guaranteed to fall within the normal range. A properly designed supply will not operate in this mode under normal load conditions.
A power supply designed correctly will operate within the switching frequency range [f_{MIN} … f_{MAX}], with an on-time falling between $t_{ON(MIN)}$ and $t_{ON(MAX)}$ when connected to a normal load.

Overload Protection

In case of overload, the system will increase the operating frequency and on-time each AC half-cycle until the maximum frequency and maximum on-time are reached. When this state is reached, the controller enters auto-restart protection, thus inhibiting the gate of the power MOSFET for approximately 1.28 s if the main line frequency is 50 Hz, 1.02 s if it is 60 Hz. After this auto-restart off-time expires, the power MOSFET is re-enabled and a normal start-up is initiated, i.e. at f_{MIN} and $t_{ON(MIN)}$, stepping up until regulation is achieved again. In case of a persistent overload condition, the auto-restart duty cycle DC_{AR} is ~33%.

Overload protection is inhibited during phase dimming when the TRIAC conduction duty cycle is less than 60%.

Output Overvoltage Protection

If a no-load condition is present on the output of the supply, the output overvoltage Zener (DZ_{OV} in Figure 4) will conduct once its threshold is reached. A voltage V_{OV} in excess of $V_{FB(AR)}$ = 2 V will appear across the FEEDBACK pin and the IC will enter auto-restart.

Output Short-Circuit

If the output of the supply (i.e. the LED load) is short-circuited, then a large amount of energy will be delivered to the sense resistor, generating a high-voltage at the FEEDBACK pin. If this condition develops more than 2 V on the FEEDBACK pin, then the IC will interpret this event as an output short-circuit and will enter auto-restart.

Safe Operating Area (SOA) Protection

If 3 consecutive cycles of the power MOSFET are prematurely terminated due to the power MOSFET current exceeding the current limit after the leading edge blanking time, SOA protection mode is triggered and the IC will enter auto-restart.

Hysteretic Thermal Shutdown

The thermal shutdown circuitry senses the die junction temperature. The thermal shutdown threshold is set to 142 °C typical with a 75 °C hysteresis. When the die temperature rises above this threshold (142 °C) the power MOSFET is disabled and remains disabled until the die temperature falls by 75 °C, at which point the power MOSFET is re-enabled.

LinkSwitch-PL Application Example

The circuit shown in Figure 7 provides a single constant current output of 350 mA with an LED string voltage of 15 V. The output current can be reduced using a standard AC mains TRIAC dimmer down to 1% (3 mA) without instability and flickering of the LED load. The board is compatible with both low cost leading edge and more sophisticated trailing edge dimmers.

The board was optimized to operate over the universal AC input voltage range (85 VAC to 265 VAC, 47 Hz to 63 Hz) but suffers no damage over an input range of 0 VAC to 300 VAC. This increases field reliability and lifetime during line sags and swells. LinkSwitch-PL based designs provide high power factor (>0.9 at 115 VAC / 230 VAC) and low THD (<15% at 230 VAC, <10% at 115 VAC) enabling compliance to all current international requirements and enabling a single design to be used worldwide.

The form factor of the board was chosen to meet the requirements for standard pear shaped (A19) LED replacement lamps. The output is non-isolated and requires the mechanical design of the enclosure to isolate both the supply and the LED load from the user.

PI Part Selection

One device size larger than required was selected to increase efficiency and reduce device thermal rise. This typically gives the highest efficiency. Further increasing the device size often results in the same or lower efficiency due to the larger switching losses associated with a larger power MOSFET.

AC Line TRIAC Dimmer Interface Circuits

The requirement to provide output dimming with low cost, TRIAC based, leading edge phase dimmers introduces a number of trade-offs in the design.

Due to the much lower power consumed by LED lighting compared to incandescent lighting, the current drawn by the lamp is below the holding current of the TRIAC dimmer. This causes undesirable behavior such as limited dimming range and/or flickering. Inrush current that flows to charge the input capacitance when the TRIAC turns on causes current ringing. This too can cause similar undesirable behavior as the ringing may cause the TRIAC current to fall to zero and turn off for the remainder of the AC cycle or rapidly turn on and off.

To overcome these issues the design includes three circuit blocks, a passive damper, an active damper and a bleeder. The drawback of these blocks is increased power dissipation and therefore reduced efficiency of the supply. In this design, the values selected allow flicker-free operation with a single lamp connected to a single dimmer at high-line. For flicker-free operation with multiple lamps in parallel or at low line voltages only (100/115 VAC) then the values may be optimized to reduce dissipation and increase efficiency.

As these blocks are only required for dimming applications, for non-dimming designs these components can simply be omitted with jumpers used to replace R7, R8 and R20.

Active and Passive Damper Circuits

Resistor R20 forms a passive damper that together with the active damper limits the peak inrush current when the TRIAC fires on each half-cycle. It should be a flameproof type to safely fail during a single point fault (e.g. failure of a bridge diode).

The active damper circuit connects a series resistance (R7 and R8) with the input rectifier for a period of each AC half-cycle, it is then bypassed for the remainder of the AC cycle by a parallel SCR (Q3). Resistor R3, R4 and C3 determines the delay before the turn-on of Q3 which then shorts out the damper resistors R7 and R8.

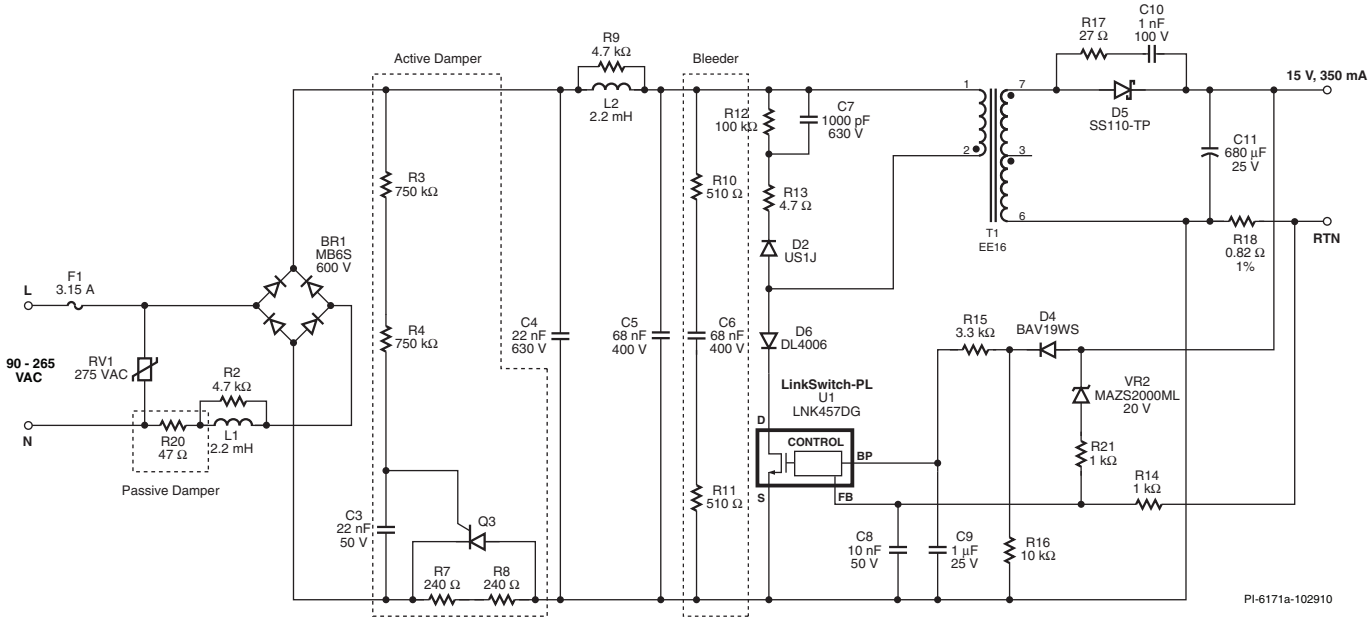


Figure 7. Schematic of a 5 W, 15 V LED Driver for A19 Incandescent Lamp Replacement.

Bleeder Circuit
Resistor R10, R11 and C6 form a bleeder network which ensures the initial input current is high enough meet the TRIAC holding current requirement, especially during small conduction angles. For non-dimming application R10, R11 and C6 may be omitted.

Input Rectifier and EMI Filter
EMI filtering is provided by L1 and a pi (π) filter formed by C4, L2 and C5. Resistors R2 and R9 dampen the self resonances of the filter stages and reduce the resultant peaks in the conducted EMI spectrum. As shown the design meets EN55015 conducted limits with >20 dB margin.

The incoming AC is rectified by BR1 and filtered by C4 and C5. The total effective input capacitance, the sum of C4 and C5, was selected to ensure correct zero crossing detection of the AC input by the LinkSwitch-PL device, necessary for correct dimming operation.

Primary Components
The LNK457DG device (U1) incorporates the power switching device, oscillator, CC control engine, start-up, and protection functions. The integrated 725 V power MOSFET provides extended design margin, improving robustness during line surge events even in high-line applications. The device is powered from the BYPASS pin via the decoupling capacitor C9. At start-up, C9 is charged by U1 from an internal current source via the DRAIN pin and then during normal operation it is supplied by the output via R15 and D4. For non-dimming designs D4 and R15 may be omitted.

The rectified and filtered input voltage is applied to one end of the primary winding of T1. The other side of the transformer's primary winding is driven by the integrated power MOSFET in U1. The leakage inductance drain voltage spike is limited by an RCD-R clamp consisting of D2, R13, R12, and C7.

Diode D6 is used to protect the IC from negative ringing (drain voltage below source voltage) when the power MOSFET is off and the input voltage is below the reflected output voltage (V_{OR}).

Output Rectification
The secondary of the transformer is rectified by D5, a Schottky barrier type for higher efficiency, and filtered by C11. Resistor R17 and C10 damp high frequency ringing and improve conducted and radiated EMI.

Output Feedback
The CC mode set-point is determined by the voltage drop that appears across R18 which is then fed to the FEEDBACK pin of U1. Output overvoltage protection is provided by VR2 and R21.

Application Considerations

Input Capacitor Selection

For correct operation during dimming, the LinkSwitch-PL device must detect line voltage zero crossing. This is sensed internally via the drain node at the point the DC bus falls to <19 V. The requirement for the DC bus to reach this level on each half-cycle limits the maximum capacitance on the DC side of the input bridge rectifier. Typically the maximum capacitance value needed for high power factor also results in meeting the 19 V limit however during development, this should be verified on an oscilloscope.

If a reduction in capacitance is required and this results in increased conducted EMI then capacitance may be added before the input rectifier which effectively isolates it from the bus capacitance.

For applications intended for use with leading edge TRIAC dimmers, film capacitors are recommended as ceramic capacitors typically create audible noise.

Output Capacitor Selection
Output capacitance has a direct effect on the output load (LED) ripple current. The larger the capacitance, the lower the ripple current. Excessive capacitance can prevent the output reaching regulation within the auto-restart time and either cause failure to start or require several start-up attempts (hiccups). Too little capacitance can cause the voltage of the FEEDBACK pin to exceed the cycle skipping mode threshold, degrading PF and causing output flicker while dimming.

Therefore the output capacitance value should be selected such that the ripple voltage across the output current sense resistor (R18 in Figure 7) and fed into the FEEDBACK pin is within the range of 100 mVp-p ≤ $V_{FEEDBACK}$ ≤ 400 mVp-p with a target value of 290 mVp-p.

The output capacitor type is not critical. Non-electrolytic capacitors are attractive in terms of lifetime (ceramics and solid dielectric types do not have an electrolyte that evaporates over time) however electrolytic types offer the best volumetric efficiency vs. cost. If multi-layer ceramics are selected, verify the data sheet curves of capacitance vs. applied voltage and temperature coefficient. The typical capacitance value may be 50% lower across temperature and/or close to rated voltage. For all capacitor types verify the capacitor(s) selected are rated for the output ripple current. For electrolytic types, this requires selecting a low ESR type. A temperature rating of 105 °C or higher is recommended for long lifetime. For typical designs there is minimal self heating of the output capacitor and therefore lifetime is determined by the internal ambient temperature and broadly follows the Arrhenius equation, i.e. lifetime doubles for every 10 °C drop in operating temperature. For example the selection of a capacitor with a rated life of 5,000 hours at 105 °C would have an expected lifetime of 40,000 hours at 75 °C. End of life is typically defined for an electrolytic capacitor as a doubling of the ESR and the capacitance reducing by 20%. This often has little impact to the performance seen by the end user and extends the fit for purpose lifetime.

Feedback Pin Signal
During normal non-dimming (full power) operation, the FEEDBACK pin threshold voltage (the voltage developed across the current sense resistor) is 290 mV. For best output current regulation, between 100 mVp-p to 400 mVp-p of voltage ripple is recommended. This can be achieved through selecting the appropriate value of

output capacitance and the value of the current sense resistor. If the peak of the ripple voltage exceeds 550 mV, the device will enter cycle skipping mode which will reduce PFC performance (lower PF and increase THD).

Transformer Considerations for use with Leading Edge TRIAC Dimmers

Audible noise can be created in the transformer due to the abrupt change in flux when the TRIAC turns on. This can be minimized by selecting cores with higher mechanical resonant frequencies. Cores with long narrow legs should be avoided (e.g. EEL types). RM and other pot core types are good choices and produce less audible noise than EE cores for the same flux density. Reducing the core flux density (BM) also reduces audible noise generation. A value below 1500 Gauss usually eliminates any noise generation but reduces the power capability of a given core size.

Working with TRIAC Dimmers

The requirement to provide output dimming with low cost, TRIAC based, leading edge phase dimmers introduces a number of trade-offs in the design.

For correct operation incandescent phase angle dimmers typically have a specified minimum load, typically ~40 W for a 230 VAC rated unit. This is to ensure that the current through the internal TRIAC stays above its specified holding current threshold.

Due to the much lower power consumed by LED lighting the input current drawn by the lamp is below the holding current of the TRIAC within the dimmer. The input capacitance of the driver allows large inrush currents to flow when the TRIAC fires. This then generates input current ringing with the input stage and line inductance which may cause the current to fall below the TRIAC holding current. Both of these mechanisms cause undesirable behavior such as limited dimming range and/or flickering.

To overcome these issues two circuit blocks, damper and bleeder, are incorporated in dimming applications. The drawback of these circuits is increased dissipation and therefore reduced efficiency of the supply.

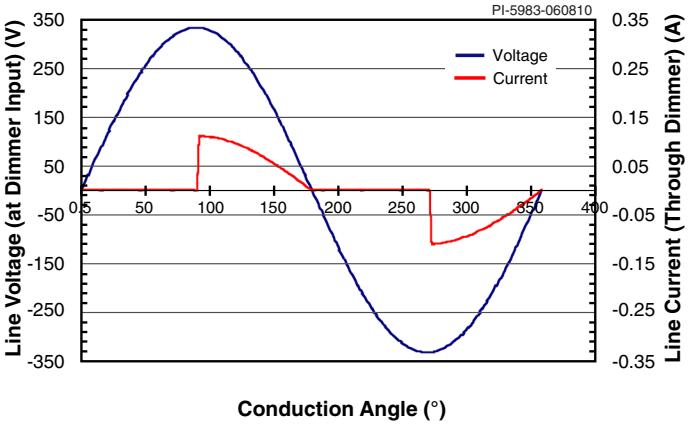


Figure 8. Ideal Input Voltage and Current Waveforms for a Leading Edge TRIAC Dimmer at 90° Conduction Angle.

Figure 8 shows the line voltage and current at the input of a leading edge TRIAC dimmer. In this example, the TRIAC conducts at 90 degrees.

Figure 9 shows the desired rectified bus voltage and current.

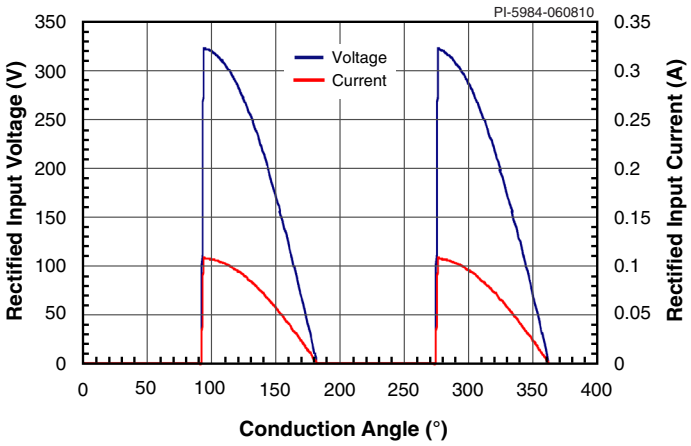


Figure 9. Resultant Waveforms Following Rectification of Ideal TRIAC Dimmer Output.

Figure 10 shows undesired rectified bus voltage and current with the TRIAC turning off prematurely and restarting. On the first half-cycle this is due to the input current ringing below the holding current of the TRIAC, excited by the initial inrush current. The second half-cycle also shows the TRIAC turning off due to the current falling below the holding current towards the end of the conduction angle. This difference in behavior on alternate half-cycles is often seen due to a difference in the holding current of the TRIAC between the two operating quadrants.

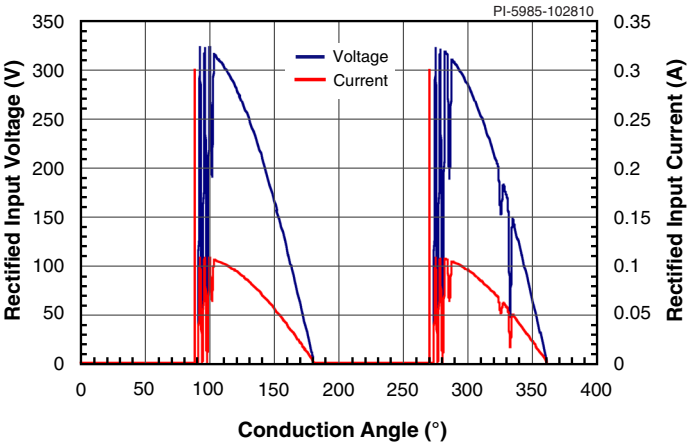


Figure 10. Example of Phase Angle Dimmer Showing Erratic Firing.

If the TRIAC is turning off before the end of the half-cycle or rapidly turning on and off then a bleeder and damper circuit are required.

In general as power dissipated in the bleeder and damper circuits increases, so does dimmer compatibility.

Initially install a bleeder network across the rectified power bus (R10, R11 and C6 in Figure 7) with initial values of 0.1 μF and a total resistance of 1 kΩ and power rating of 2 W.

Reduce the capacitance value to find the minimum acceptable value. Reducing the capacitance value reduces power dissipation and therefore increases efficiency.

If the bleeder circuit does not maintain conduction in the TRIAC, then add a damper. The purpose of the damper is to limit the inrush current (as the input capacitance charges) and associated ringing that occurs when the TRIAC turns on.

Initially add a passive damper which is a simple resistor in series with the AC input (R20 in Figure 7). Values in the range of 10 Ω – 100 Ω are typical with the upper range being limited by the allowed dissipation / temperature rise and reduction in efficiency. Values below 10 Ω may also be used but are less effective especially in high AC line input designs.

If a passive damper is insufficient to prevent incorrect TRIAC operation then an active damper can be added. This is typical in high-line applications due to the much larger inrush current that flows when the TRIAC turns on. A low cost active damper circuit is formed by R3, R4, C3, Q3, R7 and R8 in Figure 7. Resistor R7 and R8 limit the inrush current and can be a much higher value than the passive case as they are in circuit for only a fraction of the line cycle. Silicon controlled rectifier (SCR) Q3 shorts R7 and R8 after a delay defined by R3, R4 and C3. The delay is adjusted to give the shortest time that provides acceptable dimmer performance to minimize the dissipation in the resistors. The SCR is a low current, low cost device available in TO-92 packages with very low gate current requirements. The gate drive requirement of the selected SCR together with the minimum specified line voltage defines the maximum value of R7 and R8.

It's common for different dimmers to behave differently across manufacturers and power ratings. For example a 300 W dimmer requires less dampening and requires less power loss in the bleeder than a 600 W or 1000 W dimmer due to the use of a lower current rating TRIAC which typically have lower holding currents. Line impedance differences can also cause variation in behavior so during development the use of an AC source is recommended for consistency however testing using AC mains power should also be performed.

Electronic Trailing Edge Dimmers

Figure 11 shows the line voltage and current at the input of the power supply with a trailing edge electronic dimmer. In this example, the dimmer conducts at 90 degrees. This type of dimmer typically uses a power MOSFET or IGBT to provide the switching function and therefore no holding current is necessary. Also since the conduction begins at the zero crossing, high current surges and line ringing are not an issue. Use of these types of dimmers typically does not require damper and bleeder circuits.

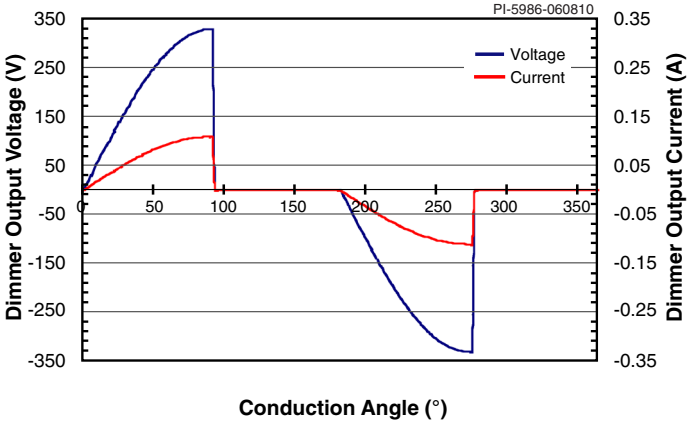


Figure 11. Ideal Dimmer Output Voltage and Current Waveforms for a Trailing Edge Dimmer at 90° Conduction Angle.

Thermal Considerations

Lighting applications present unique thermal challenges for the power supply designer. In many cases the LED load and associated heat sink determine the power supply ambient temperature. Therefore it is important to properly heat sink and verify the operating temperatures of all devices. For the LinkSwitch-PL device a SOURCE pin (D package) or exposed pad (K or V package) temperature of <115 °C is recommended to allow margin for unit to unit variation. Worst case conditions are typically maximum output power, maximum external ambient and either minimum or maximum input voltage.

Layout Considerations

Primary Side Connections

The BYPASS pin capacitor should be located as close to the BYPASS pin and connected as close to the SOURCE pin as possible. The SOURCE pin trace should not be shared with the main power MOSFET switching currents. All FEEDBACK pin components that connect to the SOURCE pin should follow the same guideline as for the BYPASS pin capacitor.

It is critical that the main power MOSFET switching currents return to the bulk capacitor with the shortest path possible. Long high current paths create excessive conducted and radiated noise.

Secondary Side Connections

The output rectifier and output filter capacitor should be as close as possible. The transformer output return pin should have a short trace to the return side of the output filter capacitor. These currents should not flow through the primary side source pin currents. The primary side source pin and secondary side return should be connected with a short trace.

Quick Design Checklist

Maximum Drain Voltage

Verify that the peak V_{DS} does not exceed 700 V under all operating conditions including start-up and fault conditions.

Maximum Drain Current

Measure the peak drain current under all operation conditions including start-up and fault conditions. Look for signs of transformer saturation (usually occurs at high ambient temperatures). Verify that the peak current is less than stated in the Absolute Maximum Ratings section.

Thermal Check

At maximum output power, both minimum and maximum line voltage and ambient temperature; verify that temperature specifications are not exceeded for the LinkSwitch-PL, transformer, output diodes, output capacitors and drain clamp components.

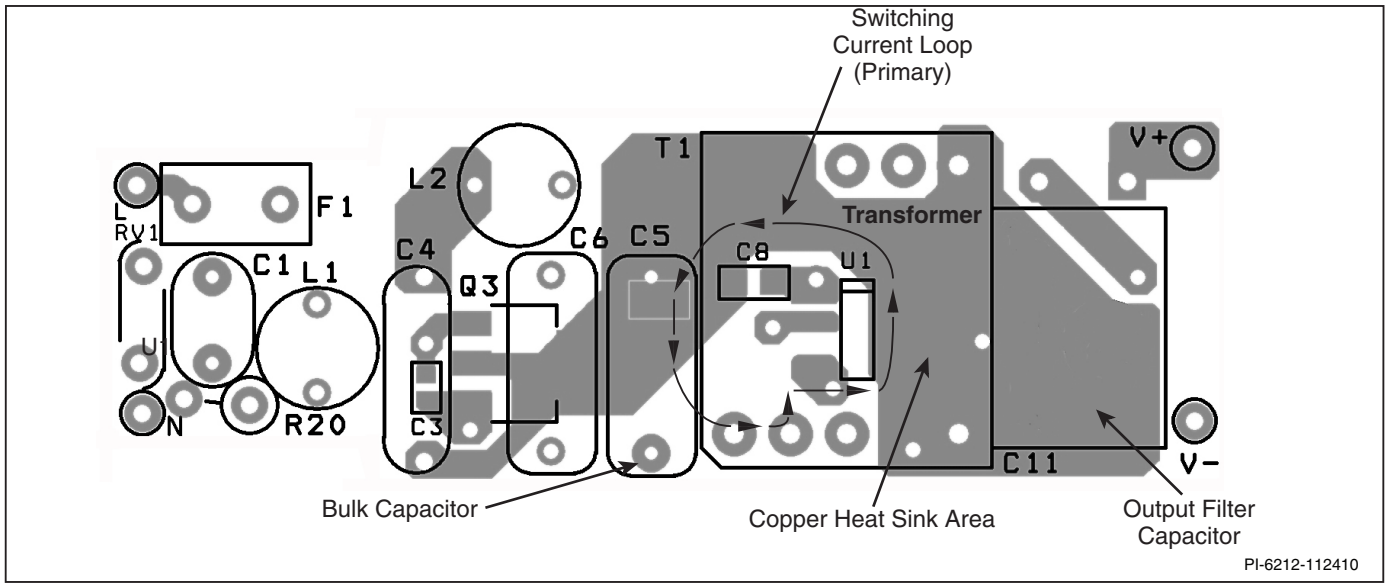


Figure 12. RD-251 PCB Top View.

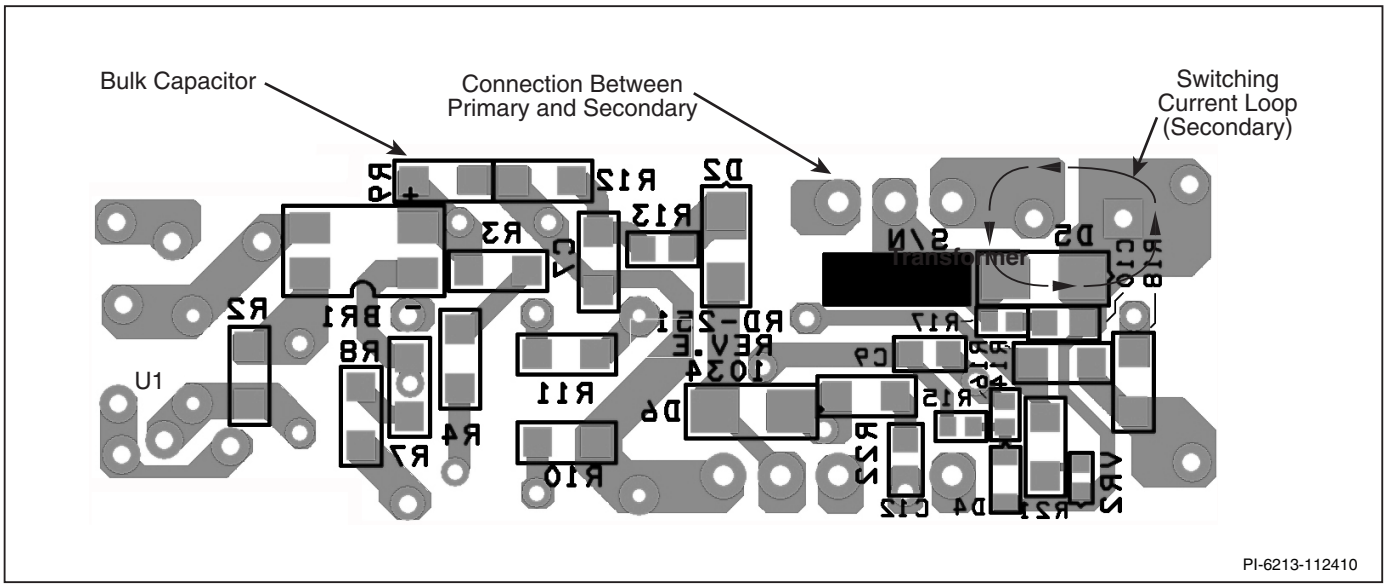


Figure 13. RD-251 PCB Bottom View.

Absolute Maximum Ratings[1,4]

DRAIN Pin Peak Current[5]: LNK454 ..... 400 mA (750 mA)
LNK456 .....850 mA (1450 mA)
LNK457 ..... 1350 mA (2000 mA)
LNK458 .....1750 mA (2650 mA)
LNK460 .....2700 mA (5100 mA)
DRAIN Pin Voltage ……..... -0.3 V to 725 V
FEEDBACK Pin Voltage ……..... -0.3 to 9 V
BYPASS Pin Voltage ……..... -0.3 to 9 V
Lead Temperature[3] .....260 °C
Storage Temperature ……..... -65 to 150 °C
Operating Junction Temperature[2].....-40 to 150 °C

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. Normally limited by internal circuitry.
3. 1/16 in. from case for 5 seconds.
4. The Absolute Maximum Ratings specified may be applied, one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings for extended periods of time may affect product reliability.
5. The higher peak Drain current (in parentheses) is allowed while the Drain voltage is simultaneously less than 400 V.

Thermal Resistance

Thermal Resistance: D (SO-8C) Package:
(θ_{JA}) ..... 100 °C/W[1], 80 °C/W[2]
(θ_{JC}) ..... 30 °C/W[3]
K (eSOP) Package:
(θ_{JA}) ..... 69 °C/W[1], 49 °C/W[2]
(θ_{JC}) .....2 °C/W[4]
V (eDIP) Package:
(θ_{JA}) .....76 °C/W[1], 64 °C/W[2]
(θ_{JC}) .....2 °C/W[4]

Notes:
1. Soldered to 0.36 sq. in. (232 mm^2), 2 oz. (610g/m^2) copper clad, with no external heat sink attached.
2. Soldered to 1 sq. in. (645 mm^2), 2 oz. (610g/m^2) copper clad, with no external heat sink attached.
3. Measured on the SOURCE pin close to plastic interface.
4. Measured at the surface of exposed pad.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to +125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Maximum Output Frequency	f_{MAX}	T_J = 25 °C	Average	110	122	134	kHz
			Peak-Peak Jitter		6		%
Minimum Output Frequency	f_{MIN}	T_J = 25 °C	Average	25.8	29.6	33.4	kHz
			Peak-Peak Jitter		6		%
Maximum Switch ON-Time	$t_{ON(MAX)}$	T_J = 25 °C			5.74		µs
Minimum Switch ON-Time	$t_{ON(MIN)}$	T_J = 25 °C			1.2		µs
Maximum Duty Cycle	DC_{MAX}				70		%
FEEDBACK Pin Voltage	V_{FB}	T_J = 25 °C Non-dimming (full power) operation		280	290	300	mV
FEEDBACK Pin Voltage Triggering Cycle Skipping Mode	$V_{FB(SK)}$				550		mV
FEEDBACK Pin Voltage for IC Auto-Restart	$V_{FB(AR)}$				2		V
Feedback Pull-up Current	I_{FB}			-1.3	-1.0	-0.7	µA

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to +125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Function (cont.)							
DRAIN Supply Current	I_{S1}	$V_{FB} > V_{FB(SK)}$ (MOSFET not switching)			450		µA
	I_{S2}	V_{FB} = 0 V (MOSFET switching at f_{MAX})	LNK454		530		µA
			LNK456		585		
			LNK457		650		
			LNK458		730		
			LNK460		1050		
BYPASS Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C	LNK454	-5.9	-4.2	-2.5	mA
			LNK456/457/458	-8.3	-5.9	-3.5	
			LNK460	-11.9	-8.5	-5.1	
	I_{CH2}	V_{BP} = 4 V, T_J = 25 °C	LNK454	-3.4	-2.4	-1.4	mA
			LNK456/457/458	-5.2	-3.7	-2.2	
			LNK460	-8.0	-5.7	-3.4	
BYPASS Pin Voltage	V_{BP}			5.60	5.85	6.15	V
BYPASS Pin Shunt Voltage	V_{SHUNT}	I_{BP} = 2 mA		5.9	6.2	6.6	V
Circuit Protection							
Current Limit	I_{LIMIT}	di/dt = 160 mA/µs T_J = 25 °C	LNK454	255	290	325	mA
		di/dt = 325 mA/µs T_J = 25 °C	LNK456	510	580	650	
		di/dt = 490 mA/µs T_J = 25 °C	LNK457	800	910	1020	
		di/dt = 650 mA/µs T_J = 25 °C	LNK458	1012	1150	1288	
		di/dt = 980 mA/µs T_J = 25 °C	LNK460	1637	1860	2083	
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C		160	200		ns
Current Limit Delay	t_{ILD}	T_J = 25 °C			150		ns
Thermal Shutdown Temperature	T_{SD}			135	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$				75		°C
BYPASS Pin Power-up Reset Threshold Voltage	$V_{BP(RESET)}$				4.9		V

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to +125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Output							
ON-State Resistance	$R_{DS(ON)}$	LNK454 I_D = 26 mA	T_J = 25 °C		23.1	26.6	Ω
			T_J = 100 °C		34.4	39.8	
		LNK456 I_D = 53 mA	T_J = 25 °C		11.7	13.5	
			T_J = 100 °C		17.5	20.2	
		LNK457 I_D = 85 mA	T_J = 25 °C		6.9	7.9	
			T_J = 100 °C		10.4	11.9	
		LNK458 I_D = 110 mA	T_J = 25 °C		4.4	5.1	
			T_J = 100 °C		6.7	7.6	
		LNK460 I_D = 170 mA	T_J = 25 °C		2.2	2.6	
			T_J = 100 °C		3.3	3.9	
OFF-State Leakage	I_{DSS1}	V_{BP} = 6.2 V, V_{FB} > $V_{FB(SK)}$, V_{DS} = 580 V, T_J = 125 °C				50	µA
Breakdown Voltage	BV_{DSS}	V_{BP} = 6.2 V, V_{FB} > $V_{FB(SK)}$, T_J = 25 °C		725			V
DRAIN Supply Voltage				50			V
Auto-Restart OFF-Time	$t_{AR(OFF)}$	f_{MAIN} = 50 Hz			1.28		s
		f_{MAIN} = 60 Hz			1.02		
Auto-Restart Duty Cycle	DC_{AR}				33		%

Typical Performance Characteristics

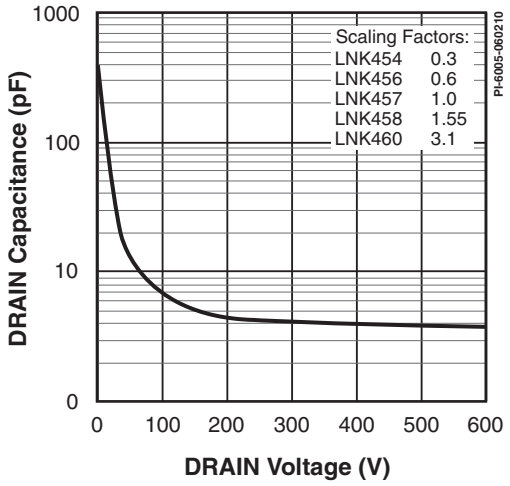


Figure 7. Drain Capacitance vs. Drain Voltage.

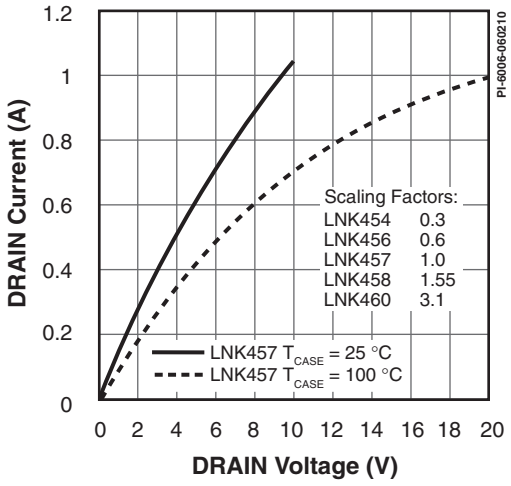


Figure 8. Drain Current vs. Drain Voltage.

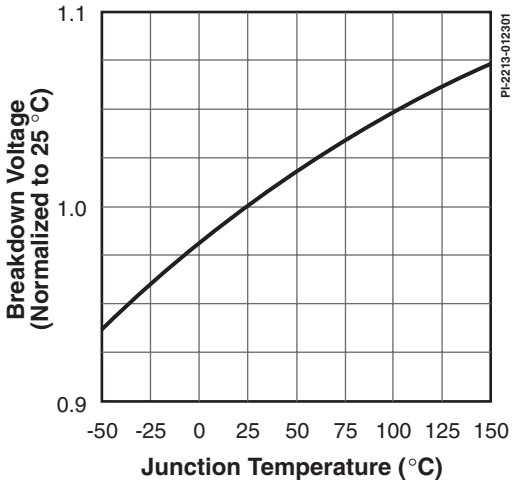


Figure 9. Breakdown vs. Temperature.

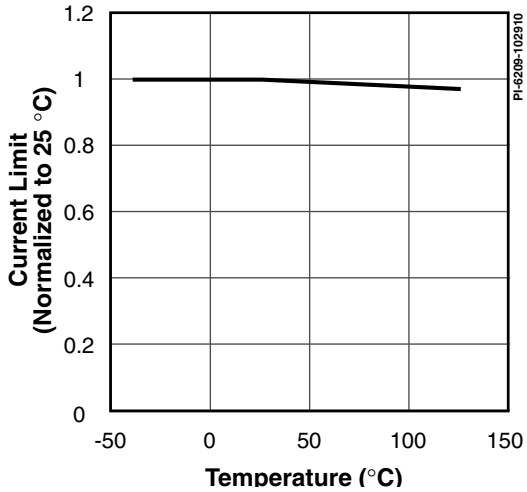
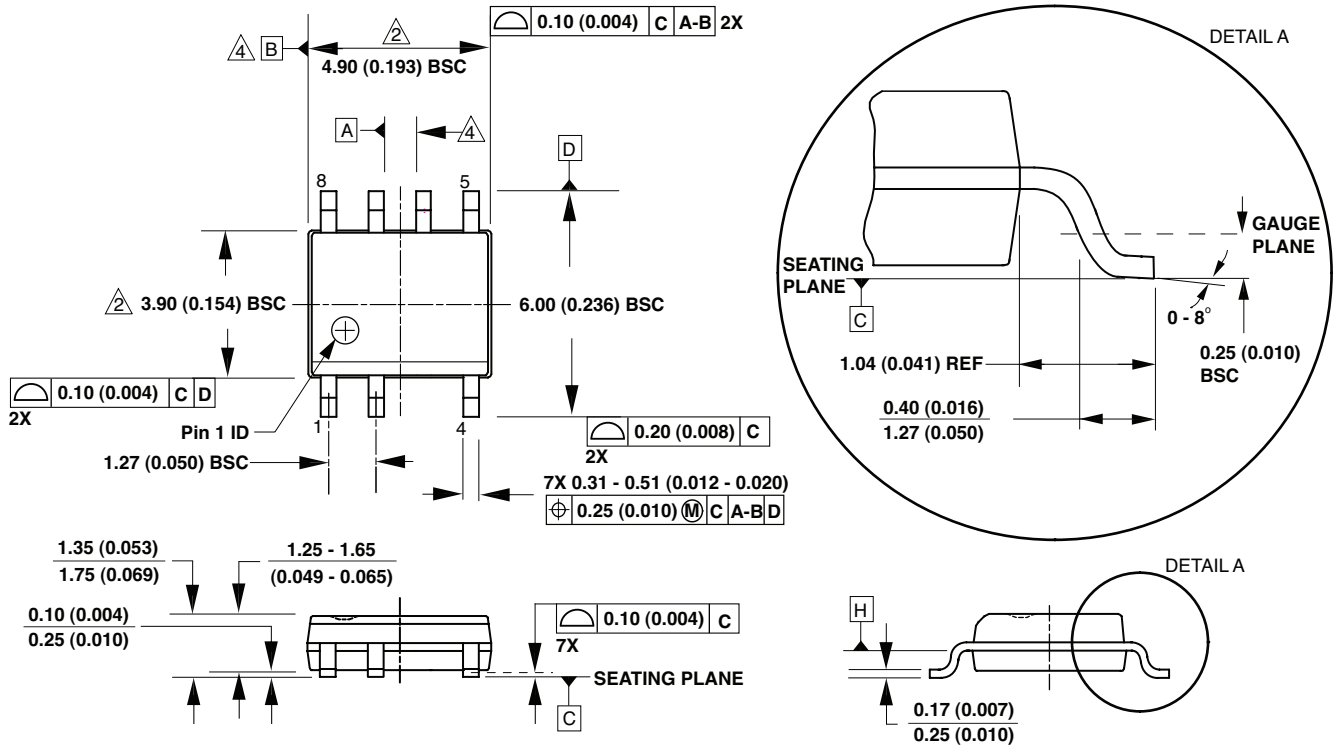


Figure 10. Standard Current Limit vs. Temperature.

SO-8C (D Package)



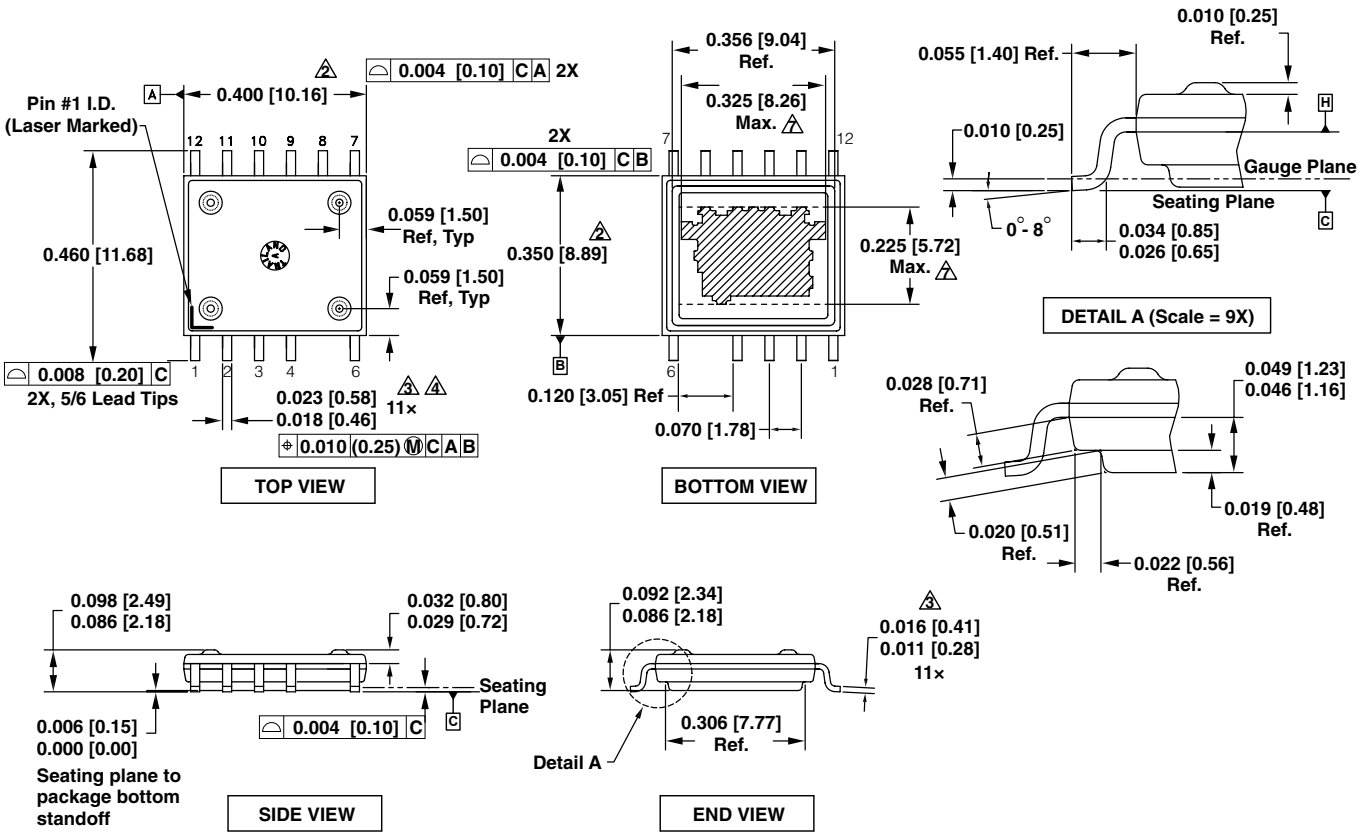
Notes:

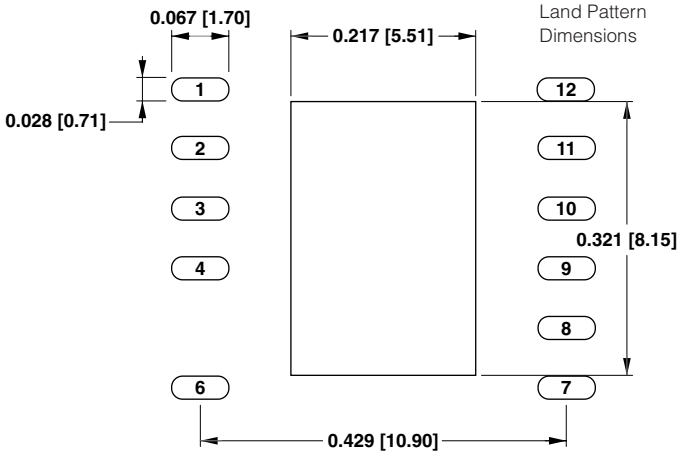
1. JEDEC reference: MS-012.
2. Package outline exclusive of mold flash and metal burr.
3. Package outline inclusive of plating thickness.
4. Datums A and B to be determined at datum plane H.
5. Controlling dimensions are in millimeters. Inch dimensions are shown in parenthesis. Angles in degrees.

D07C

PI-4526-040110

eSOP-12B (K Package)



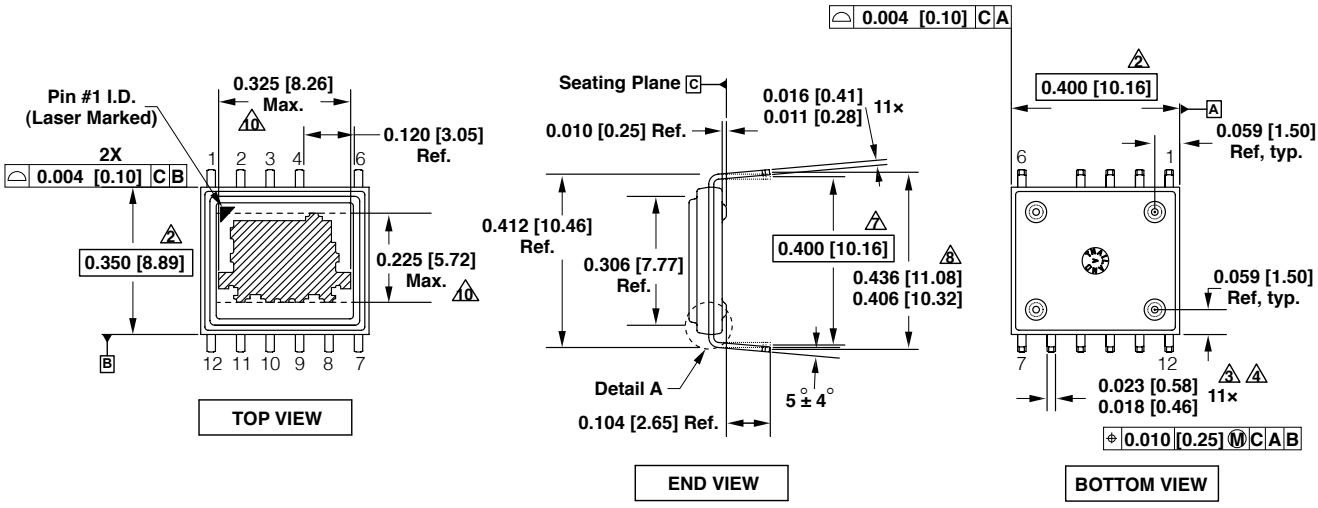


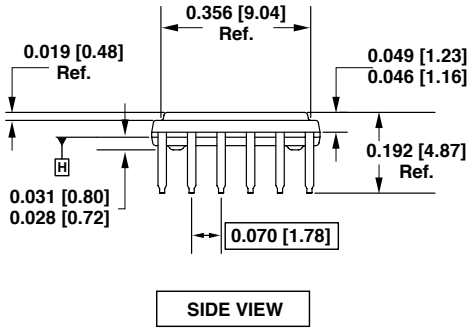
Notes:

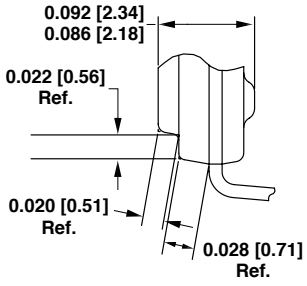
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include interlead flash or protrusions.
5. Controlling dimensions in inches [mm].
6. Datums A and B to be determined at Datum H.
7. Exposed pad is nominally located at the centerline of Datums A and B. "Max" dimensions noted include both size and positional tolerances.

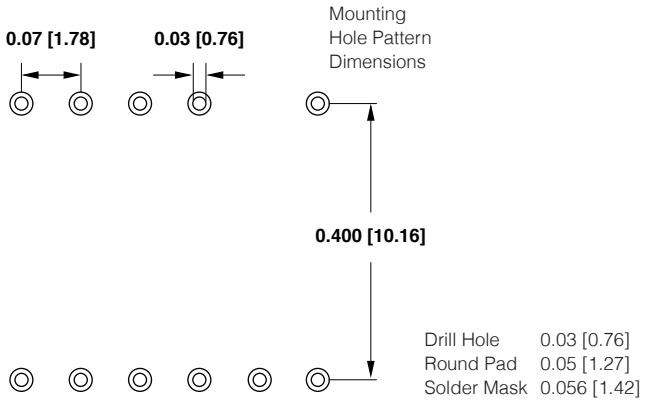
PI-5748a-100311

eDIP-12B (V Package)







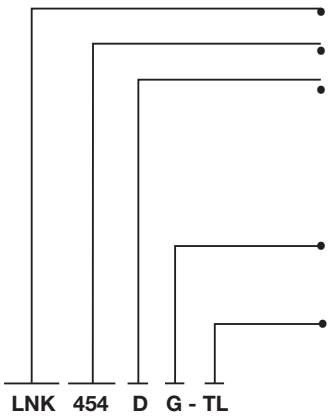


Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches [mm].
6. Datums A and B to be determined at Datum H.
7. Measured with the leads constrained to be perpendicular to Datum C.
8. Measured with the leads unconstrained.
9. Lead numbering per JEDEC SPP-012.
10. Exposed pad is nominally located at the centerline of Datums A and B. “Max” dimensions noted include both size and positional tolerances.

PI-5556a-100311

Part Ordering Information



- **LinkSwitch Product Family**
- **PL Series Number**
- **Package Identifier**

D	SO-8C
K	eSOP-12
V	eDIP-12

- **Package Material**

G	GREEN: Halogen Free and RoHS Compliant

- **Tape & Reel and Other Options**

Blank	Standard Configurations
TL	Tape & Reel, 2.5 k pcs minimum for D package, 1 k pcs minimum for K package.

Revision	Notes	Date
A	Initial Release.	11/01/10
B	Revised K and V Package Drawings.	06/11
C	Added eDIP-12B and eSOP-12B packages. Removed eDIP-12 and eSOP-12 packages.	10/11

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