THE DATASHEET OF

RDK-257

LNK403-410/413-420
LinkSwitch-PH LED Driver IC Family

Single-Stage PFC, Primary-Side Constant Current Control and TRIAC Dimming/Non-Dimming Options

Product Highlights

Dramatically Simplifies Off-line LED Drivers
- Single-stage combination of power factor correction and accurate constant-current (CC) output
  - Enables very long lifetime designs (no electrolytic capacitors)
  - Eliminates optocoupler and all secondary current control circuitry
  - Eliminates control loop compensation circuitry
- Simple primary-side PWM dimming interface
- Universal input voltage range
- LNK403-410 optimized for flicker-free TRIAC dimming

EcoSmart™ – Energy Efficient
- Single-stage PFC combined with output CC control
  - Greatly increases efficiency, >90% achievable
  - Reduces component count
  - No current sense resistors
- Low standby power remote ON/OFF feature (<50 mW at 230 VAC)

Accurate and Consistent Performance
- Compensates for transformer inductance variations
- Compensates for line input voltage variation
- Frequency jittering greatly reduces EMI filter size and cost

Advanced Protection and Safety Features
- Auto-restart for short-circuit protection
- Open circuit fault detection mode
- Automatic thermal shutdown restart with hysteresis
- Meets high voltage creepage requirement between DRAIN and all other signal pins both on PCB and at package

Green Package
- Halogen free and ROHS compliant package

Applications
- Off-line LED driver

Description

The LinkSwitch™-PH dramatically simplifies implementation of LED drivers requiring long lifetime, high efficiency, PF >0.9, and TRIAC dimming capability (LNK403-410). The single-stage combined power factor and constant-current controller eliminates a switching stage and the electrolytic bulk capacitor. The advanced primary-side control used by the LinkSwitch-PH device provides accurate constant current control while eliminating the need for an optocoupler and current sensing circuits.

LinkSwitch-PH incorporates a 725 V power FET, a continuous-mode PWM controller, a high-voltage switched current source for self biasing, frequency jittering, protection circuitry including cycle-by-cycle current limit and hysteretic thermal shutdown.

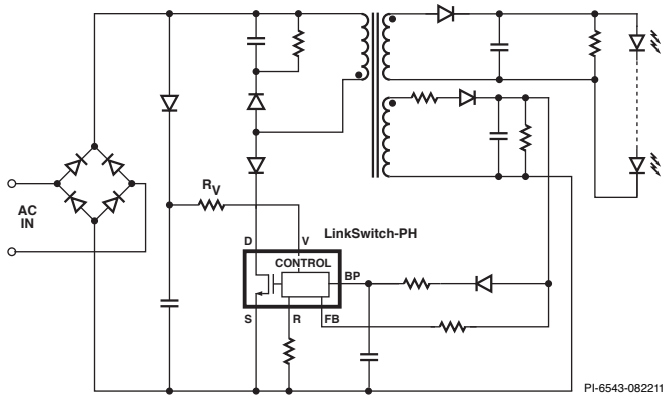


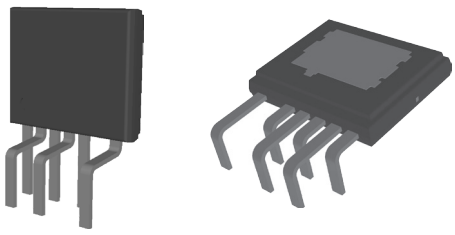
Figure 1. Typical Application Schematic.

Output Power Table[1,2]

Product[5]	R_V = 2 MΩ		R_V = 4 MΩ	
	85-132 VAC		85-308 VAC	
	Minimum Output Power[3]	Maximum Output Power[4]	Minimum Output Power[3]	Maximum Output Power[4]
LNK403/413E/L	2.5 W	4.5 W	6.5 W	12 W
LNK404/414E/L	2.5 W	5.5 W	6.5 W	15 W
LNK405/415E/L	3.8 W	7.0 W	8.5 W	18 W
LNK406/416E/L	4.5 W	8.0 W	10 W	22 W
LNK407/417E/L	5.5 W	10 W	12 W	25 W
LNK408/418E/L	6.8 W	13.5 W	16 W	35 W
LNK409/419E/L	8.0 W	20 W	18 W	50 W
LNK410/420E/L	18 W	31 W	40 W	78 W

Table 1. Output Power Table.

Notes:
1. *Continuous power in an open frame with adequate heat sinking at device local ambient of 70 °C.*
2. *Power level calculated on typical LED string voltage with efficiency >80%.*
3. *Minimum output power with C_{BP} = 10 µF.*
4. *Maximum output power with C_{BP} = 100 µF. LNK4x3EG C_{BP} = 10 µF.*
5. *Package: eSIP-7C, eSIP-7F.*



eSIP-7C (E Package) eSIP-7F (L Package)

Figure 2. Package Options.

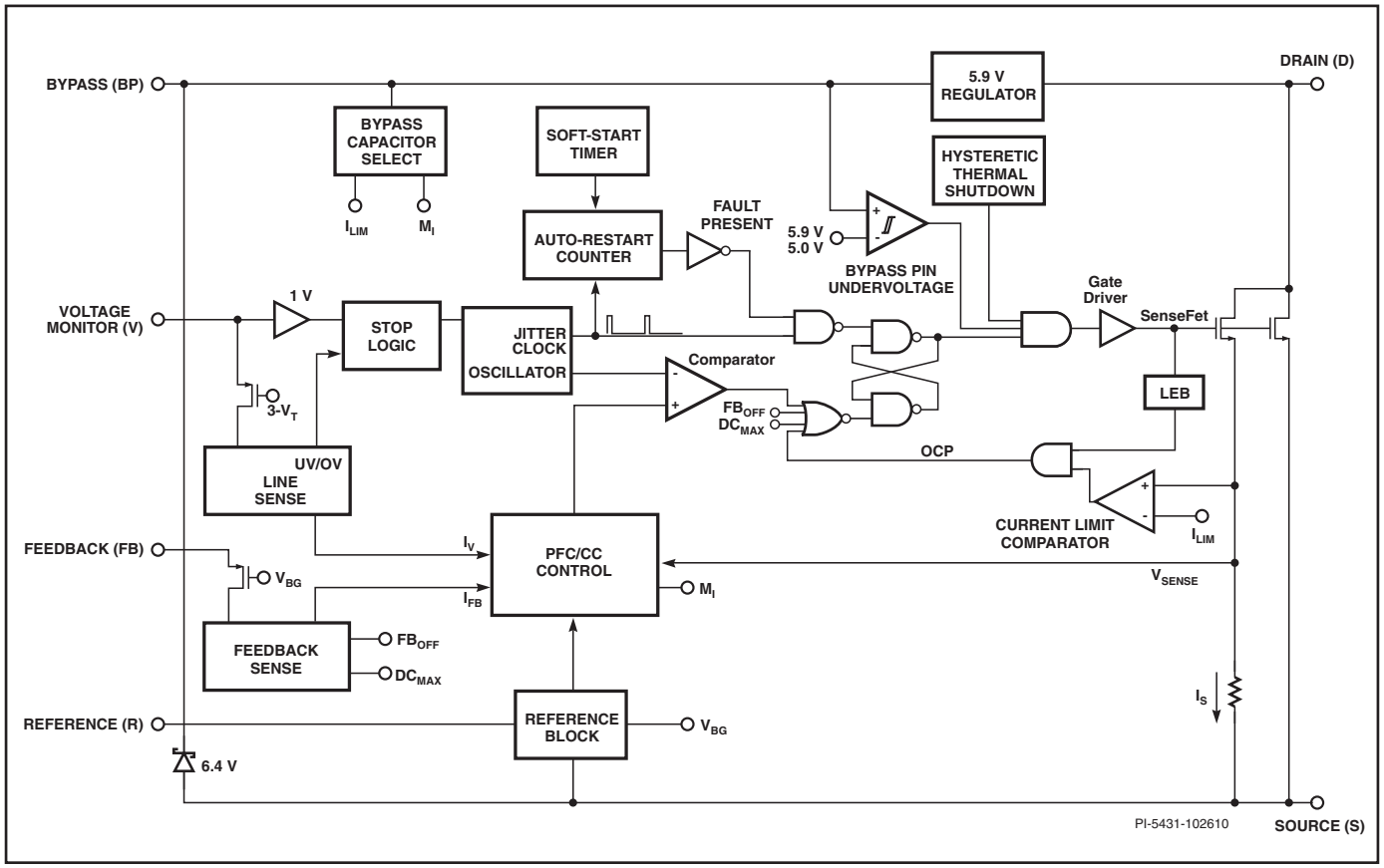


Figure 3. Functional Block Diagram.

Pin Functional Description

DRAIN (D) Pin:
This pin is the power FET drain connection. It also provides internal operating current for both start-up and steady-state operation.

SOURCE (S) Pin:
This pin is the power FET source connection. It is also the ground reference for the BYPASS, FEEDBACK, REFERENCE and VOLTAGE MONITOR pins.

BYPASS (BP) Pin:
This is the connection point for an external bypass capacitor for the internally generated 5.9 V supply. This pin also provides output power selection through choice of the BYPASS pin capacitor value.

FEEDBACK (FB) Pin:
The FEEDBACK pin is used for output voltage feedback. The current into the FEEDBACK pin is directly proportional to the output voltage. The FEEDBACK pin also includes circuitry to protect against open load and overload output conditions.

REFERENCE (R) Pin:
This pin is connected to an external precision resistor and is used to configure for dimming (LNK403-410) and non-TRIAC dimming (LNK413-420) modes of operation.

VOLTAGE MONITOR (V) Pin:
This pin interfaces with an external input line peak detector, consisting of a rectifier, filter capacitor and resistors. The applied current is used to control stop logic for line under-voltage (UV), overvoltage (OV), provide feed-forward to control the output current and the remote ON/OFF function.

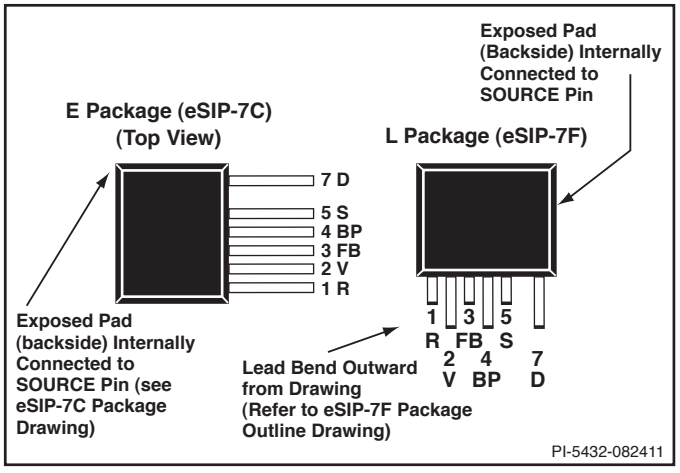


Figure 4. Pin Configuration.

Functional Description

A LinkSwitch-PH device monolithically integrates a controller and high-voltage power FET into one package. The controller implements both high power factor and a constant current output in a single stage. The LinkSwitch-PH controller consists of an oscillator, feedback (sense and logic) circuit, 5.9 V regulator, hysteretic over-temperature protection, frequency jittering, cycle-by-cycle current limit, auto-restart, inductance correction, power factor and constant current control.

FEEDBACK Pin Current Control Characteristics

The figure shown below illustrates the operating boundaries of the FEEDBACK pin current. Above $I_{FB(SKIP)}$ switching is disabled and below $I_{FB(AR)}$ the device enters into auto-restart.

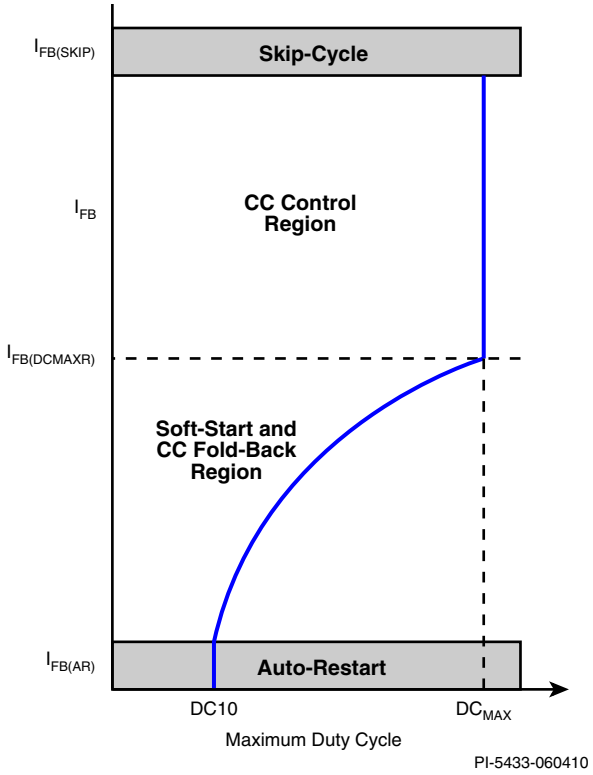


Figure 5. FEEDBACK Pin Current Characteristic.

The FEEDBACK pin current is also used to clamp the maximum duty cycle to limit the available output power for overload and open-loop conditions. This duty cycle reduction characteristic also promotes a monotonic output current start-up characteristic to prevent over-shoot.

REFERENCE Pin

The REFERENCE pin is tied to ground (SOURCE) via an external resistor. The value selected sets the internal references, determining the operating mode for dimming (LNK403-410) and non-dimming (LNK413-420) operation and the line undervoltage and overvoltage thresholds of the VOLTAGE MONITOR pin. For non-dimming or PWM dimming applications with LNK413-420, the external resistor should be a 24.9 kΩ ±1%, for high-line and universal input voltage designs, and 49.9 kΩ ±1% for low-line input voltage designs. For phase angle AC dimming with LNK403-410, the external resistor should be a 49.9 kΩ ±1%. One percent resistors are recommended as the resistor tolerance directly affects the output tolerance. Other resistor values should not be used.

BYPASS Pin Capacitor Power Gain Selection

LinkSwitch-PH devices have the capability to tailor the internal gain to either full or a reduced output power setting. This allows selection of a larger device to minimize dissipation for both thermal and efficiency reasons. The power gain is selected with the value of the BYPASS pin capacitor. The full power setting is selected with a 100 µF capacitor and the reduced power setting (for higher efficiency) is selected with a 10 µF capacitor. The BYPASS pin capacitor sets both the internal power gain as well as the over-current protection (OCP) threshold. Unlike the larger devices, the LNK4x3 power gain is not programmable. Use a 10 µF capacitor for the LNK4x3.

Switching Frequency

The switching frequency is 66 kHz. To further reduce the EMI level, the switching frequency is jittered (frequency modulated) by approximately ±1 kHz.

Soft-Start

The controller includes a soft-start timing feature which inhibits the auto-restart protection feature for the soft-start period (t_{SOFT}) to distinguish start-up into a fault (short-circuit) from a large output capacitor. At start-up the LinkSwitch-PH clamps the maximum duty cycle to reduce the output power. The total soft-start period is t_{SOFT}.

Remote ON/OFF and EcoSmart

The VOLTAGE MONITOR pin has a 1 V threshold comparator connected at its input. This voltage threshold is used for remote ON/OFF control. When a signal is received at the VOLTAGE MONITOR pin to disable the output (VOLTAGE MONITOR pin tied to ground through an optocoupler photo-transistor) the LinkSwitch-PH will complete its current switching cycle before the internal power FET is forced off.

The remote ON/OFF feature can also be used as an eco-mode or power switch to turn off the LinkSwitch-PH and keep it in a very low power consumption state for indefinite long periods. When the LinkSwitch-PH is remotely turned on after entering this mode, it will initiate a normal start-up sequence with soft-start the next time the BYPASS pin reaches 5.9 V. In the worst case, the delay from remote on to start-up can be equal to the full discharge/charge cycle time of the BYPASS pin. This reduced consumption remote off mode can eliminate expensive and unreliable in-line mechanical switches.

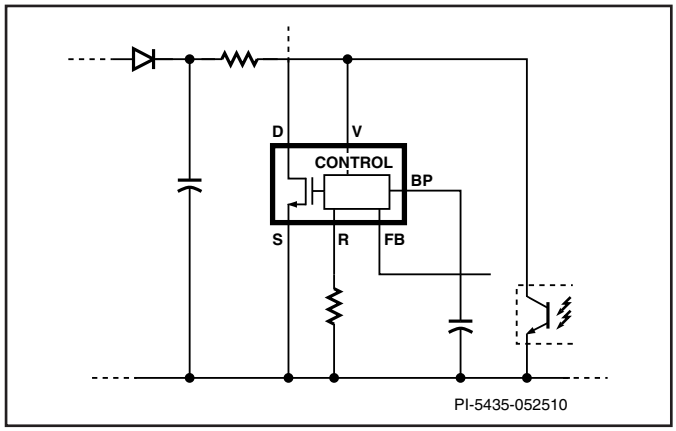


Figure 6. Remote ON/OFF VOLTAGE MONITOR pin Control

5.9 V Regulator/Shunt Voltage Clamp

The internal 5.9 V regulator charges the bypass capacitor connected to the BYPASS pin to 5.9 V by drawing a current from the voltage on the DRAIN pin whenever the power FET is off. The BYPASS pin is the internal supply voltage node. When the power FET is on, the device operates from the energy stored in the bypass capacitor. Extremely low power consumption of the internal circuitry allows LinkSwitch-PH to operate continuously from current it takes from the DRAIN pin. A bypass capacitor value of 10 or 100 µF is sufficient for both high frequency decoupling and energy storage. In addition, there is a 6.4 V shunt regulator clamping the BYPASS pin at 6.4 V when current is provided to the BYPASS pin through an external resistor. This facilitates powering of LinkSwitch-PH externally through a bias winding to increase operating efficiency. It is recommended that the BYPASS pin is supplied current from the bias winding for normal operation.

Auto-Restart

In the event of an open-loop fault (open FEEDBACK pin resistor or broken path to feedback winding), output short-circuits or an overload condition the controller enters into the auto-restart mode. The controller annunciates both short-circuit and open-loop conditions once the FEEDBACK pin current falls below the $I_{FB(AR)}$ threshold after the soft-start period. To minimize the power dissipation under this fault condition the shutdown/auto-restart circuit turns the power supply on (same as the soft-start period) and off at an auto-restart duty cycle of typically DC_{AR} for as long as the fault condition persists. If the fault is removed during the auto-restart off-time, the power supply will remain in auto-restart until the full off-time count is completed. Special consideration must be made to appropriately size the output capacitor to ensure that after the soft-start period (t_{SOFT}) the FEEDBACK pin current is above the $I_{FB(AR)}$ threshold to ensure successful power-supply start-up. After the soft-start time period, auto-restart is activated only when the FEEDBACK pin current falls below $I_{FB(AR)}$.

Over-Current Protection

The current limit circuit senses the current in the power FET. When this current exceeds the internal threshold (I_{LIMIT}), the power FET is turned off for the remainder of that cycle. A leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power FET is turned on. This leading edge blanking time has been set so that current spikes caused by capacitance and rectifier reverse recovery will not cause premature termination of the power FET conduction.

Line Under/Overvoltage Protection

This device includes both line under- and overvoltage detection to limit the minimum start-up and maximum operating voltage detected through the VOLTAGE MONITOR pin. An external peak detector consisting of a diode and capacitor are required to provide input line peak voltage to the VOLTAGE MONITOR pin through a resistor. At power up, I_{UV+} keeps the LinkSwitch-PH off until the input line voltage reaches the undervoltage threshold. At power down, I_{UV-} prevents restart attempts after the output goes out of regulation.

The same resistor used for UV also sets line overvoltage (OV) shutdown threshold which, once exceeded, forces the LinkSwitch-PH to stop switching (after completion of the current switching cycle). Once the line voltage returns to normal, the device resumes normal operation. A small amount of hysteresis is provided on the OV threshold to prevent noise triggering. When the power FET is off, the rectified DC high voltage surge capability is increased to the voltage rating of the power FET (725 V), due to the absence of the reflected voltage and leakage spikes on the drain.

Hysteretic Thermal Shutdown

The thermal shutdown circuitry senses the controller die temperature. The threshold is set at 142 °C typical with a 75 °C hysteresis. When the die temperature rises above this threshold (142 °C) the power FET is disabled and remains disabled until the die temperature falls by 75 °C, at which point the power FET is re-enabled.

Safe Operating Area (SOA) Protection

The device also features a safe operating area (SOA) protection mode which disables FET switching for 40 cycles in the event the peak switch current reaches the I_{LIMIT} threshold and the switch on-time is less than $t_{ON(SOA)}$. This protection mode protects the device under short-circuited LED conditions and at start-up during the soft-start period when auto-restart protection is inhibited. The SOA protection mode remains active in normal operation.

Application Example

14 W TRIAC Dimmable High Power Factor LED Driver Design Example

The circuit schematic in Figure 7 shows a TRIAC dimmable high power-factor LED driver based on LNK406EG from the LinkSwitch-PH family of devices. It was optimized to drive an LED string at a voltage of 28 V with a constant current of 0.5 A (±5%) ideal for PAR lamp retro-fit applications. The design operates over a universal input voltage range of 90 VAC to 265 VAC but provides the specified output current tolerance over a line voltage range of 90 VAC to 132 VAC (this is configurable for high-line only applications by simple component value changes).

The key goals of this design were compatibility with standard leading edge TRIAC AC dimmers, very wide dimming range (1000:1, 500 mA:0.5 mA), high efficiency (>85%) and high power factor (>0.9). The design is fully protected from faults such as no-load, overload and output short-circuit conditions and over temperature.

Circuit Description

The LinkSwitch-PH device (U1) integrates the power FET, controller and start-up functions into a single package reducing the component count versus typical implementations. Configured as part of an isolated continuous conduction mode flyback converter, U1 provides high power factor via its internal control algorithm together with the small input capacitance of the design. Continuous conduction mode operation results in reduced primary peak and RMS current. This both reduces EMI noise, allowing simpler, smaller EMI filtering components and improves efficiency. Output current regulation is maintained without the need for secondary-side sensing which eliminates current sense resistors and improves efficiency.

Input Stage

Fuse F1 provides protection from component failures while RV1 provides a clamp during differential line surges, keeping the peak drain voltage of U1 below the 725 V rating of the internal power FET. Bridge rectifier BR1 rectifies the AC line voltage. EMI filtering is provided by L1-L3, C1, R16 and R17 together with the safety rated Y class capacitor (C7) that bridges the safety isolation barrier between primary and secondary. Resistor R16 and R17 act to damp any resonances formed between L1, L2, C1 and the AC line impedance. A small bulk capacitor (C2) is required to provide a low impedance source for the primary switching current. The maximum value of C1 and C2 is limited in order to maintain a power factor of greater than 0.9.

LinkSwitch-PH Primary

To provide peak line voltage information to U1 the incoming rectified AC peak charges C3 via D2. This is then fed into the VOLTAGE MONITOR pin of U1 as a current via R2 and R3. This sensed current is also used by the device to set the line input overvoltage and undervoltage protection thresholds. Resistor R1 provides a discharge path for C3 with a time constant much longer than that of the rectified AC to prevent generation of line frequency ripple.

The VOLTAGE MONITOR pin current and the FEEDBACK pin current are used internally to control the average output LED current. For TRIAC phase-dimming applications a 49.9 kΩ resistor (R4) is used on the REFERENCE pin and 4 MΩ (R2+R3) on the VOLTAGE MONITOR pin to provide a linear relationship between input voltage and the output current and maximizing the dimming range. Resistor R4 also sets the internal line input undervoltage and overvoltage protection thresholds.

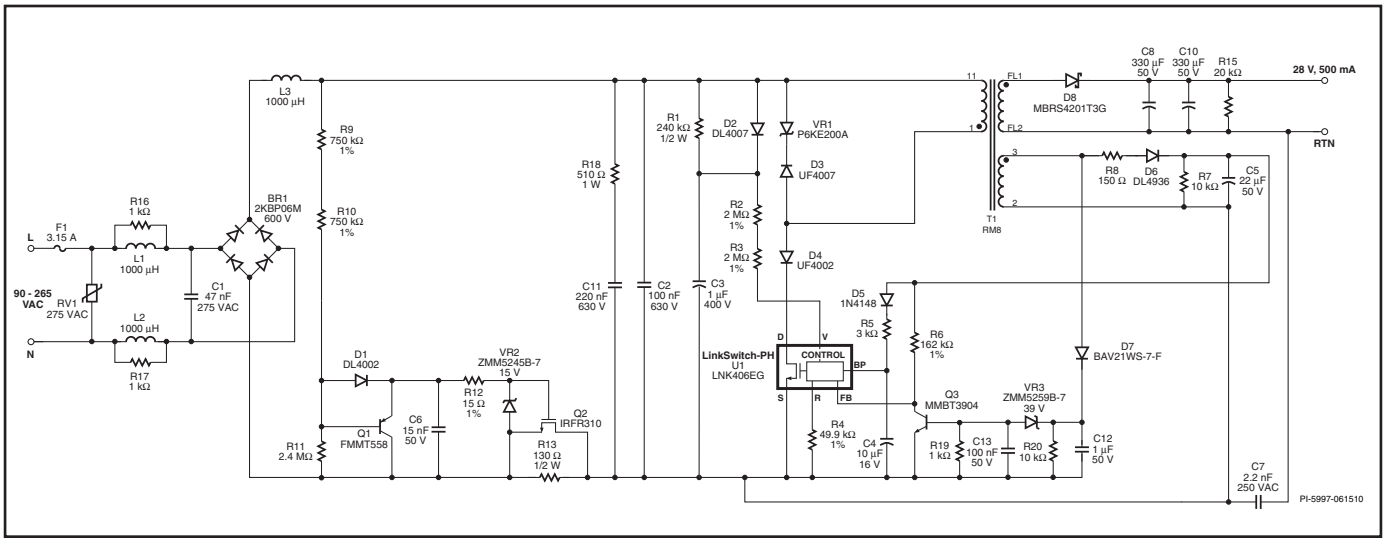


Figure 7. Schematic of an Isolated, TRIAC Dimmable, High Power Factor, Universal Input, 14 W LED Driver.

Diode D3 and VR1 clamp the drain voltage to a safe level due to the effects of leakage inductance. Diode D4 is necessary to prevent reverse current from flowing through U1 for the period of the rectified AC input voltage that the voltage across C2 falls to below the reflected output voltage (V_{OR}).

Diode D6, C5, R7 and R8 create the primary bias supply from an auxiliary winding on the transformer. Capacitor C4 provides local decoupling for the BYPASS pin of U1 which is the supply pin for the internal controller. During start-up C4 is charged to ~6 V from an internal high-voltage current source tied to the device DRAIN pin. This allows the part to start switching at which point the operating supply current is provided from the bias supply via R5. Capacitor C4 also selects the output power mode (10 μF for reduced power was selected to reduce dissipation in U1 and increase efficiency).

Feedback

The bias winding voltage is proportional to the output voltage (set by the turns ratio between the bias and secondary windings). This allows the output voltage to be monitored without secondary-side feedback components. Resistor R6 converts the bias voltage into a current which is fed into the FEEDBACK pin of U1. The internal engine within U1 combines the FEEDBACK pin current, VOLTAGE MONITOR pin current and drain current information to provide a constant output current over a 1.5:1 output voltage variation (LED string voltage variation of ±25%) at a fixed line input voltage.

To limit the output voltage at no-load an output overvoltage protection circuit is set by D7, C12, R20, VR3, C13, Q3 and R19. Should the output load be disconnected then the bias voltage will increase until VR3 conducts, turning on Q3 and reducing the current into the FEEDBACK pin. When this current drops below 20 μA the part enters auto-restart and switching is disabled for 1500 ms allowing time for the output and bias voltages to fall.

Output Rectification

The transformer secondary winding is rectified by D8 and filtered by C8 and C10. A Schottky barrier diode was selected for efficiency and the combined value of C8 and C10 were selected to give peak-to-peak and LED ripple current equal to 40% of the mean value. For designs where lower ripple is desirable the output capacitance value can be increased. A small pre-load is provided by R15 which limits the output voltage under no-load conditions.

TRIAC Phase Dimming Control Compatibility

The requirement to provide output dimming with low cost, TRIAC-based, leading edge phase dimmers introduces a number of trade-offs in the design.

Due to the much lower power consumed by LED based lighting the current drawn by the overall lamp is below the holding current of the TRIAC within the dimmer. This can cause undesirable behaviors such as limited dimming range and/or flickering as the TRIAC fires inconsistently. The relatively large impedance the LED lamp presents to the line allows significant ringing to occur due to the inrush current charging the input capacitance when the TRIAC turns on. This too can cause similar undesirable behavior as the ringing may cause the TRIAC current to fall to zero and turn off.

To overcome these issues two circuits, the Active Damper and Passive Bleeder, are incorporated. The drawback of these circuits is increased dissipation and therefore reduced efficiency of the supply. For non-dimming applications these components can simply be omitted.

The Active Damper consists of components R9, R10, R11, R12, D1, Q1, C6, VR2, Q2 in conjunction with R13. This circuit limits the inrush current that flows to charge C2 when the TRIAC turns on by placing R13 in series for the first 1 ms of the TRIAC conduction. After approximately 1 ms, Q2 turns on and shorts R13. This keeps the power dissipation on R13 low and allows a larger value during current limiting. Resistor R9, R10, R11 and C6 provide the 1 ms delay after the TRIAC conducts. Transistor Q1 discharges C6 when the TRIAC is not conducting and VR2 clamps the gate voltage of Q2 to 15 V.

The Passive Bleeder circuit is comprised of C11 and R18. This helps to keep the input current above the TRIAC holding current while the input current corresponding to the effective driver resistance increases during each AC half-cycle.

7 W High Power Factor Non-Dimmable LED Driver Design Example with Enhanced Line Regulation

The circuit schematic in Figure 8 shows a high power-factor LED driver based on a LNK413EG from the LinkSwitch-PH family of devices. It was optimized to drive an LED string at a voltage of 21 V with a constant current of 0.33 A, ideal for PAR20/PAR30 lamp retro-fit applications. The design operates over the universal input voltage range of 90 VAC to 265 VAC and is a non-dimming application. A non-dimming application has tighter output current variation with changes in the line voltage than a dimming application. It's key to note that, although not specified for dimming, no circuit damage will result if the end user does operate the design with a phase controlled dimmer.

Circuit Description

Input Stage

Fuse F1 provides protection from component failures while RV1 provides a clamp during differential line surges, keeping the peak drain voltage of U1 below the 725 V rating of the internal power FET. Bridge rectifier BR1 rectifies the AC line voltage. EMI filtering is provided by L1-L3, C2 together with the safety rated Y class capacitor (C7) that bridges the safety isolation barrier between primary and secondary. Resistor R2 and R3 act to damp any resonances formed between L1, L2, C2 and the AC line impedance. A small bulk capacitor (C3) is required to provide a low impedance source for the primary switching current. The maximum value of C2 and C3 is limited in order to maintain a power factor of greater than 0.9.

LinkSwitch-PH Primary

To provide peak line voltage information to U1 the incoming rectified AC peak charges C8 via D6. This is then fed into the VOLTAGE MONITOR pin of U1 as a current via R4, R7 and R8. The VOLTAGE MONITOR pin current and the FEEDBACK pin current are used internally to control the average output LED current. The combined value of R4, R7 and R8 (3.909 MΩ) and R11, R12 (1.402 MΩ) connected to the VOLTAGE MONITOR pin provides excellent line regulation over the entire 90 VAC to 265 VAC input range.

The VOLTAGE MONITOR pin current is also used by the device to set the line input overvoltage and undervoltage protection thresholds.

Diode D1 and VR1 clamp the drain voltage to a safe level due to the effects of leakage inductance. A Zener clamp was selected for lowest component count and highest efficiency. Diode D5 is necessary to prevent reverse current from flowing through U1 during the period when the AC input voltage is lower than the reflected output voltage (V_{OR}). A space efficient RM6 core was selected for this design. The RM core geometry helps minimizes audible noise but requires the use of flying leads to meet safety spacing requirements.

Diode D3, C6, R5, R9 and R18 create the primary bias supply from an auxiliary winding on the transformer. Resistor R5 provides filtering of leakage inductance generated voltage spikes to improve tracking of the bias and output voltages. It also forms a pole with C6 at ~100 Hz. Resistors R9 and R18 act as a small load to ensure that the bias voltage collapses during output short-circuit when U1 enters auto-restart operation to protect the supply.

Output overvoltage and load disconnection protection is provided by D8, C14, R24, VR3, C15, R23 and Q2. Should the output LED load become disconnected the output voltage will rise causing an associated rise in the bias winding voltage across C14. Once this exceeds the voltage rating of VR3, Q2 turns on pulling down the FEEDBACK pin of U1 and initiating auto-restart operation. Once in auto-restart the low duty cycle of operation (~3%) together with the small pre-load on the output prevents the output voltage rising to a high level. Once the output load is reconnected normal operation resumes.

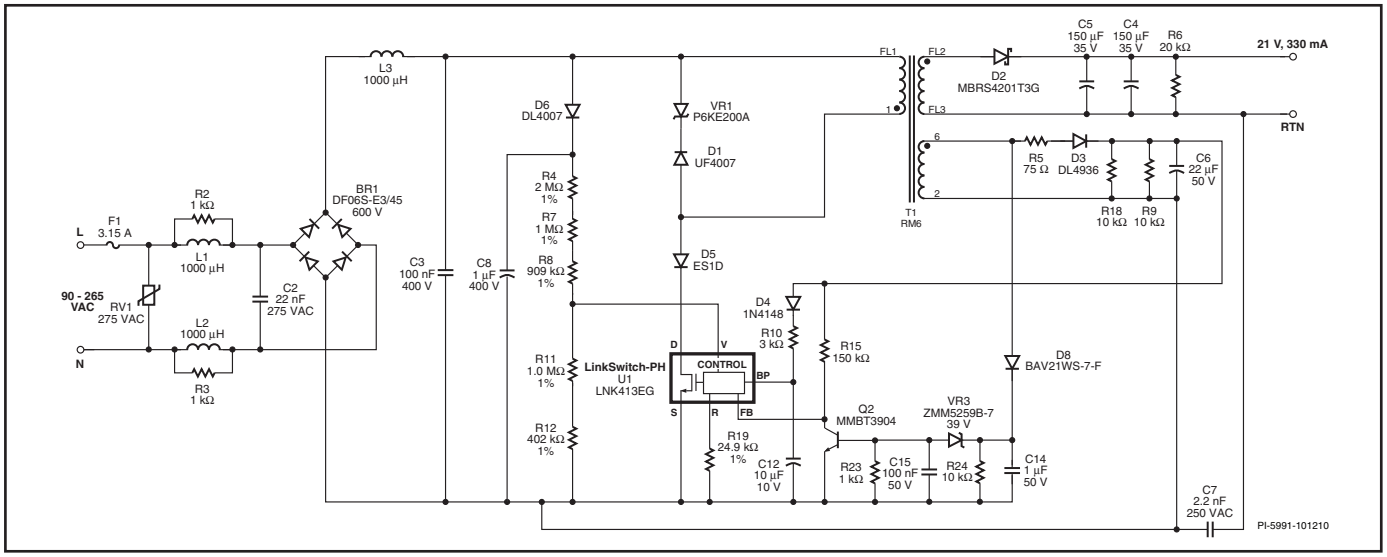


Figure 8. Schematic of an Isolated, Non-Dimmable, High Power Factor, Universal Input, 7 W LED Driver.

Capacitor C12 provides local decoupling for the BYPASS pin of U1 which is the supply pin for the internal controller. During start-up C4 is charged to ~6 V from an internal high-voltage current source tied to the device DRAIN pin. Once the bias voltage has risen into regulation the operating supply current is provided via R10. Diode D4 prevents U1 from charging C6 during start-up which would increase the start-up delay time.

Feedback

The bias winding voltage is proportional to the output voltage (set by the turns ratio between the bias and secondary windings). This allows the output voltage to be monitored without secondary-side feedback components. Resistor R15 converts the bias voltage into a current which is fed into the FEEDBACK pin of U1. The internal engine within U1 combines the FEEDBACK pin current, VOLTAGE MONITOR pin current and drain current information to provide a constant output current over a 2:1 output voltage range.

Output Rectification

The transformer secondary winding is rectified by D2 and filtered by C4 and C5. A Schottky barrier diode was selected for efficiency and the combined value of C4 and C5 were selected to give an acceptable LED ripple current. For designs where lower ripple is desirable the output capacitance value can be increased. A small pre-load is provided by R6 which limits the output voltage under no-load conditions.

Key Application Considerations

Power Table

The data sheet power table (Table 1) represents the minimum and maximum practical continuous output power based on the following conditions:

1. Efficiency of 80%
2. Device local ambient of 70 °C
3. Sufficient heat sinking to keep the device temperature below 100 °C
4. For minimum output power column
   - Reflected output voltage (V_{OR}) of 120 V
   - FEEDBACK pin current of 135 µA
   - BYPASS pin capacitor value of 10 µF
5. For maximum output power column
   - Reflected output voltage (V_{OR}) of 65 V
   - FEEDBACK pin current of 165 µA
   - BYPASS pin capacitor value of 100 µF (LNK4x3EG = 10 µF)

Note that input line voltages above 85 VAC do not change the power delivery capability of LinkSwitch-PH devices.

Device Selection

Select the device size by comparing the required output power to the values in Table 1. For thermally challenging designs, e.g., incandescent lamp replacement, where either the ambient temperature local to the LinkSwitch-PH device is high and/or there is minimal space for heat sinking use the minimum output power column. This is selected by using a 10 µF BYPASS pin capacitor and results in a lower device current limit and therefore lower conduction losses. For open frame design or designs where space is available for heat sinking then refer to the maximum output power column. This is selected by using a 100 µF BYPASS pin capacitor for all but the LNK4x3 which has only one power setting. In all cases in order to obtain the best output current tolerance maintain the device temperature below 100 °C

Maximum Input Capacitance

To achieve high power factor, the capacitance used in both the EMI filter and for decoupling the rectified AC (bulk capacitor) must be limited in value. The maximum value is a function of the output power of the design and reduces as the output power reduces. For the majority of designs limit the total capacitance to less than 200 nF with a bulk capacitor value of 100 nF. Film capacitors are recommended compared to ceramic types as they minimize audible noise with operating with leading edge phase dimmers. Start with a value of 10 nF for the capacitance in the EMI filter and increase in value until there is sufficient EMI margin.

REFERENCE Pin Resistance Value Selection

The LinkSwitch-PH family contains phase dimming devices, LNK403-410, and non-dimming devices, LNK413-420. The non-dimmable devices use a 24.9 kΩ ±1% REFERENCE pin resistor in high-line and universal input voltage designs and 49.9 kΩ ±1% in low-line input voltage designs, for best output current tolerance (over AC input voltage changes). The dimmable devices use 49.9 kΩ ±1% to achieve the widest dimming range.

VOLTAGE MONITOR Pin Resistance Network Selection

For widest AC phase angle dimming range with LNK403-410, use a 4 MΩ resistor connected to the line voltage peak detector circuit. Make sure that the resistor's voltage rating is sufficient for the peak line voltage. If necessary use multiple series connected resistors.

For best line regulation, use a series combination of resistors that equals 3.909 MΩ connected to the line voltage peak detector. In addition, connect a 1 MΩ in series with a 402 kΩ resistor (1.402 MΩ total) from the VOLTAGE MONITOR pin to SOURCE pin. Use 1% tolerance resistors for good accuracy. Line regulation can be further improved by using the PIXIs spreadsheet's fine tuning section. See the LinkSwitch-PH Application Note for more information.

Primary Clamp and Output Reflected Voltage V_{OR}

A primary clamp is necessary to limit the peak drain to source voltage. A Zener clamp requires the fewest components and board space and gives the highest efficiency. RCD clamps are also acceptable however the peak drain voltage should be carefully verified during start-up and output short-circuit as the clamping voltage varies with significantly with the peak drain current.

For the highest efficiency, the clamping voltage should be selected to be at least 1.5 times the output reflected voltage, V_{OR}, as this keeps the leakage spike conduction time short. When using a Zener clamp in a universal input or high-line only application, a V_{OR} of less than 135 V is recommended to allow

for the absolute tolerances and temperature variations of the Zener. This will ensure efficient operation of the clamp circuit and will also keep the maximum drain voltage below the rated breakdown voltage of the FET. An RCD (or RCDZ) clamp provides tighter clamp voltage tolerance than a Zener clamp. The RCD clamp is more cost effective than the Zener clamp but requires more careful design to ensure that the maximum drain voltage does not exceed the power FET breakdown voltage. These V_{OR} limits are based on the BV_{DSS} rating of the internal FET, a V_{OR} of 60 V to 100 V is typical for most designs, giving the best PFC and regulation performance.

Series Drain Diode

An ultra-fast or Schottky diode in series with the drain is necessary to prevent reverse current flowing through the device. The voltage rating must exceed the output reflected voltage, V_{OR}. The current rating should exceed two times the average primary current and have a peak rating equal to the maximum drain current of the selected LinkSwitch-PH device.

Line Voltage Peak Detector Circuit

LinkSwitch-PH devices use the peak line voltage to regulate the power delivery to the output. A capacitor value of 1 µF to 4.7 µF is recommended to minimize line ripple and give the highest power factor (>0.9), smaller values are acceptable but result in lower PF and higher line current distortion.

Operation with Phase Controlled Dimmers

Dimmer switches control incandescent lamp brightness by not conducting (blanking) for a portion of the AC voltage sine wave. This reduces the RMS voltage applied to the lamp thus reducing the brightness. This is called natural dimming and the LinkSwitch-PH LNK403-410 devices when configured for dimming utilize natural dimming by reducing the LED current as the RMS line voltage decreases. By this nature, line regulation performance is purposely decreased to increase the dimming range and more closely mimic the operation of an incandescent lamp. Using a 49.9 kΩ REFERENCE pin resistance selects natural dimming mode operation.

Leading Edge Phase Controlled Dimmers

The requirement to provide flicker-free output dimming with low cost, TRIAC-based, leading edge phase dimmers introduces a number of trade-offs in the design.

Due to the much lower power consumed by LED based lighting the current drawn by the overall lamp is below the holding current of the TRIAC within the dimmer. This causes undesirable behaviors such as limited dimming range and/or flickering. The relatively large impedance the LED lamp presents to the line allows significant ringing to occur due to the inrush current charging the input capacitance when the TRIAC turns on. This too can cause similar undesirable behavior as the ringing may cause the TRIAC current to fall to zero and turn off.

To overcome these issues two circuits, the Active Damper and Passive Bleeder, are incorporated. The drawback of these circuits is increased dissipation and therefore reduced efficiency of the supply so for non-dimming applications these components can simply be omitted.

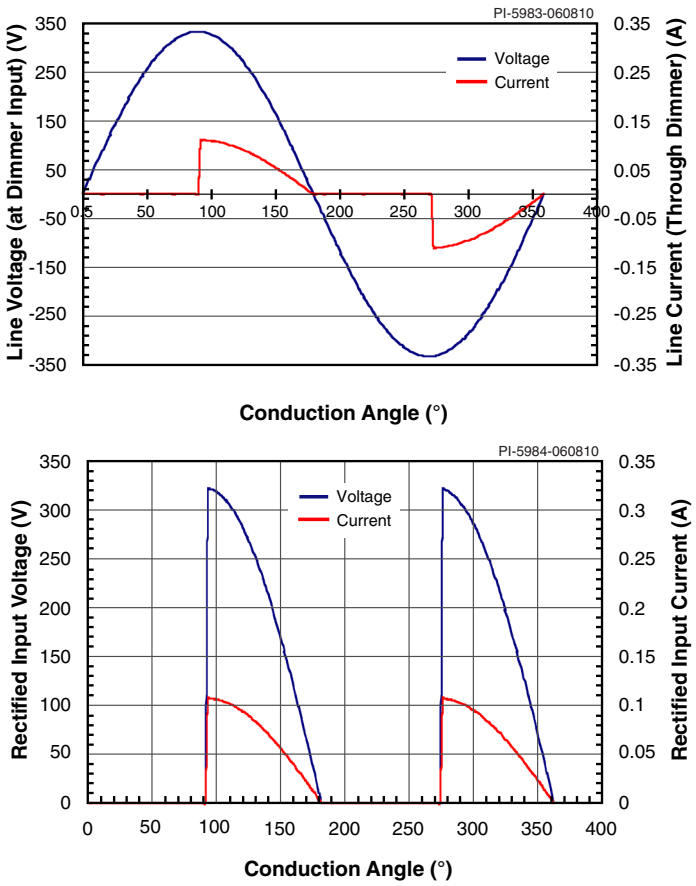


Figure 9. (a) Ideal Input Voltage and Current Waveforms for a Leading Edge TRIAC Dimmer at 90° Conduction Angle. (b) Resultant Waveforms Following Rectification of TRIAC Dimmer Output.

Figure 9(a) shows the line voltage and current at the input of a leading edge TRIAC dimmer with Figure 9(b) showing the resultant rectified bus voltage. In this example, the TRIAC conducts at 90 degrees.

Figure 10 shows undesired rectified bus voltage and current with the TRIAC turning off prematurely and restarting.

If the TRIAC is turning off before the end of the half-cycle erratically or alternate half AC cycles have different conduction angles then flicker will be observed in the LED light due to variations in the output current. This can be solved by including a bleeder and damper circuit.

Dimmers will behave differently based on manufacturer and power rating, for example a 300 W dimmer requires less dampening and requires less power loss in the bleeder than a 600 W or 1000 W dimmer due to different drive circuits and TRIAC holding current specifications. Line voltage also has a significant impact as at high-line for a given output power the input current and therefore TRIAC current is lower but the peak inrush current when the input capacitance charges is higher creating more ringing. Finally multiple lamps in parallel driven from the same dimmer can introduce more ringing due to the

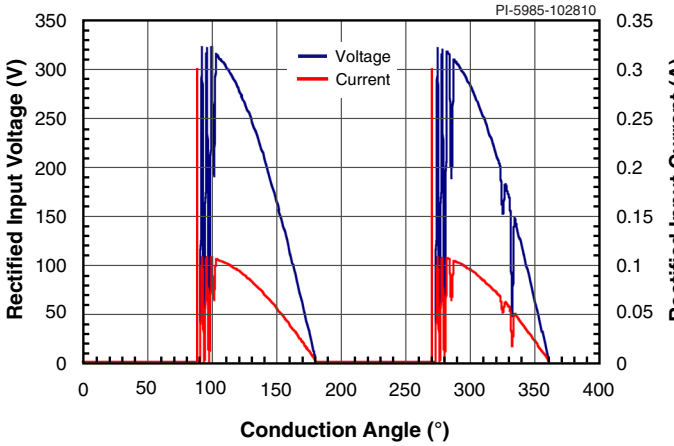


Figure 10. Example of Phase Angle Dimmer Showing Erratic Firing.

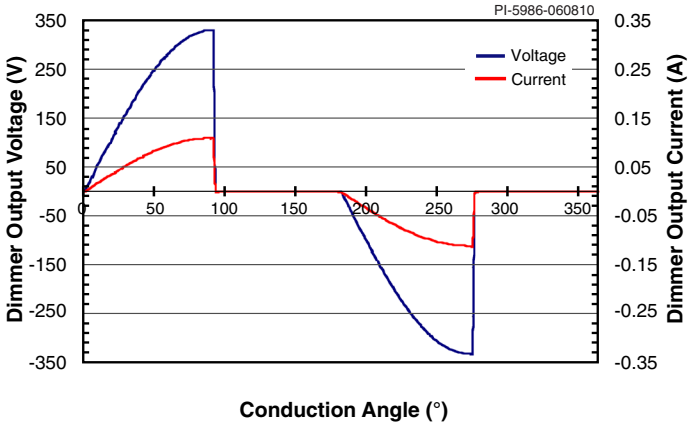


Figure 11. Ideal Dimmer Output Voltage and Current Waveforms for a Trailing Edge Dimmer at 90° Conduction Angle.

increased capacitance of parallel units. Therefore when testing dimmer operation verify on a number of models, different line voltages and with both a single driver and multiple drivers in parallel.

Start by adding a bleeder circuit. Add a 0.44 µF capacitor and 510 Ω 1 W resistor (components in series) across the rectified bus (C11 and R18 in Figure 7). If this results in satisfactory operation reduce the capacitor value to the smallest that results in acceptable performance to reduce losses and increase efficiency.

If the bleeder circuit does not maintain conduction in the TRIAC, then add an active damper as shown in Figure 7. This consists of components R9, R10, R11, R12, D1, Q1, C6, VR2, Q2 in conjunction with R13. This circuit limits the inrush current that flows to charge C2 when the TRIAC turns on by placing R13 in series for the first 1 ms of the TRIAC conduction. After approximately 1 ms, Q2 turns on and shorts R13. This keeps the power dissipation on R13 low and allows a larger value to be used during current limiting. Increasing the delay before Q2 turns on by increasing the values of resistors R9 and R10 will improve dimmer compatibility but cause more power to be dissipated across R13. Monitor the AC line current and voltage at the input of the power supply as you make the adjustments. Increase the delay until the TRIAC operates properly but keep the delay as short as possible for efficiency.

As a general rule the greater the power dissipated in the bleeder and damper circuits, the more dimmer types will work with the driver.

Trailing Edge Phase Controlled Dimmers

Figure 11 shows the line voltage and current at the input of the power supply with a trailing edge dimmer. In this example, the dimmer conducts at 90 degrees. Many of these dimmers use back-to-back connected power FETs rather than a TRIAC to control the load. This eliminates the holding current issue of TRIACs and since the conduction begins at the zero crossing, high current surges and line ringing are minimized. Typically these types of dimmers do not require damping and bleeder circuits.

Audible Noise Considerations for Use with Leading Edge Dimmers

Noise created when dimming is typically created by the input capacitors, EMI filter inductors and the transformer. The input capacitors and inductors experience high di/dt and dv/dt every AC half-cycle as the TRIAC fires and an inrush current flows to charge the input capacitance. Noise can be minimized by selecting film vs ceramic capacitors, minimizing the capacitor value and selecting inductors that are physically short and wide.

The transformer may also create noise which can be minimized by avoiding cores with long narrow legs (high mechanical resonant frequency). For example, RM cores produce less audible noise than EE cores for the same flux density. Reducing the core flux density will also reduce the noise. Reducing the maximum flux density (BM) to 1500 Gauss usually eliminates any audible noise but must be balanced with the increased core size needed for a given output power.

Thermal and Lifetime Considerations

Lighting applications present thermal challenges to the driver. In many cases the LED load dissipation determines the working ambient temperature experienced by the drive so thermal evaluation should be performed with the driver inside the final enclosure. Temperature has a direct impact on driver and LED lifetime. For every 10 °C rise in temperature, component life is reduced by a factor of 2. Therefore it is important to properly heat sink and verify the operating temperatures of all devices.

Layout Considerations

Primary-Side Connections

Use a single point (Kelvin) connection at the negative terminal of the input filter capacitor for the SOURCE pin and bias returns. This improves surge capabilities by returning surge currents from the bias winding directly to the input filter capacitor. The BYPASS pin capacitor should be located as close to the BYPASS pin and connected as close to the SOURCE pin as possible. The SOURCE pin trace should not be shared with the main power FET switching currents. All FEEDBACK pin components that connect to the SOURCE pin should follow the same rules as the BYPASS pin capacitor. It is critical that the main power FET switching currents return to the bulk capacitor with the shortest path as possible. Long high current paths create excessive conducted and radiated noise.

Secondary-Side Connections

The output rectifier and output filter capacitor should be as close as possible. The transformer's output return pin should have a short trace to the return side of the output filter capacitor.

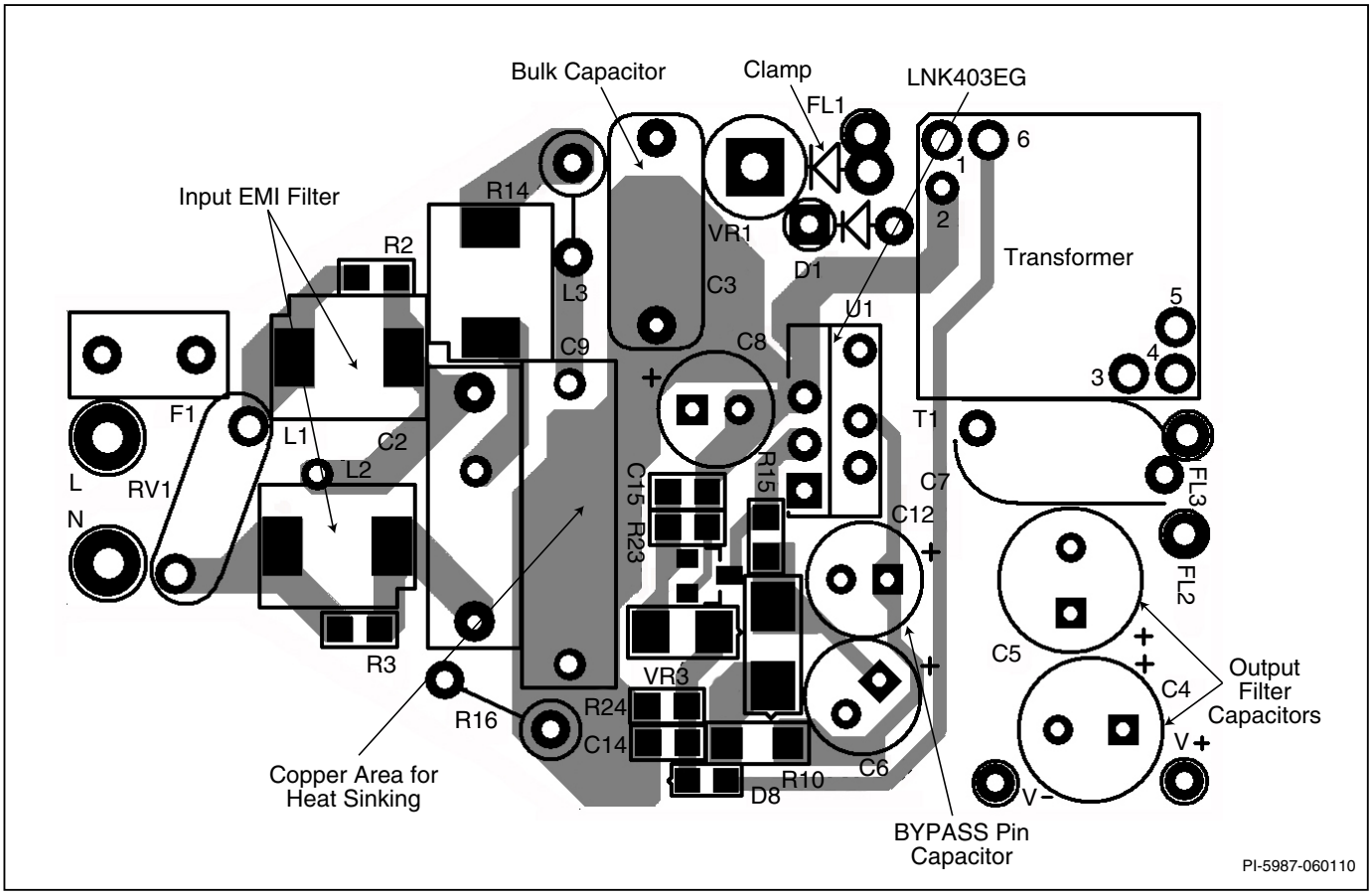


Figure 12. RD-193 7 W Layout Example, Top Layer.

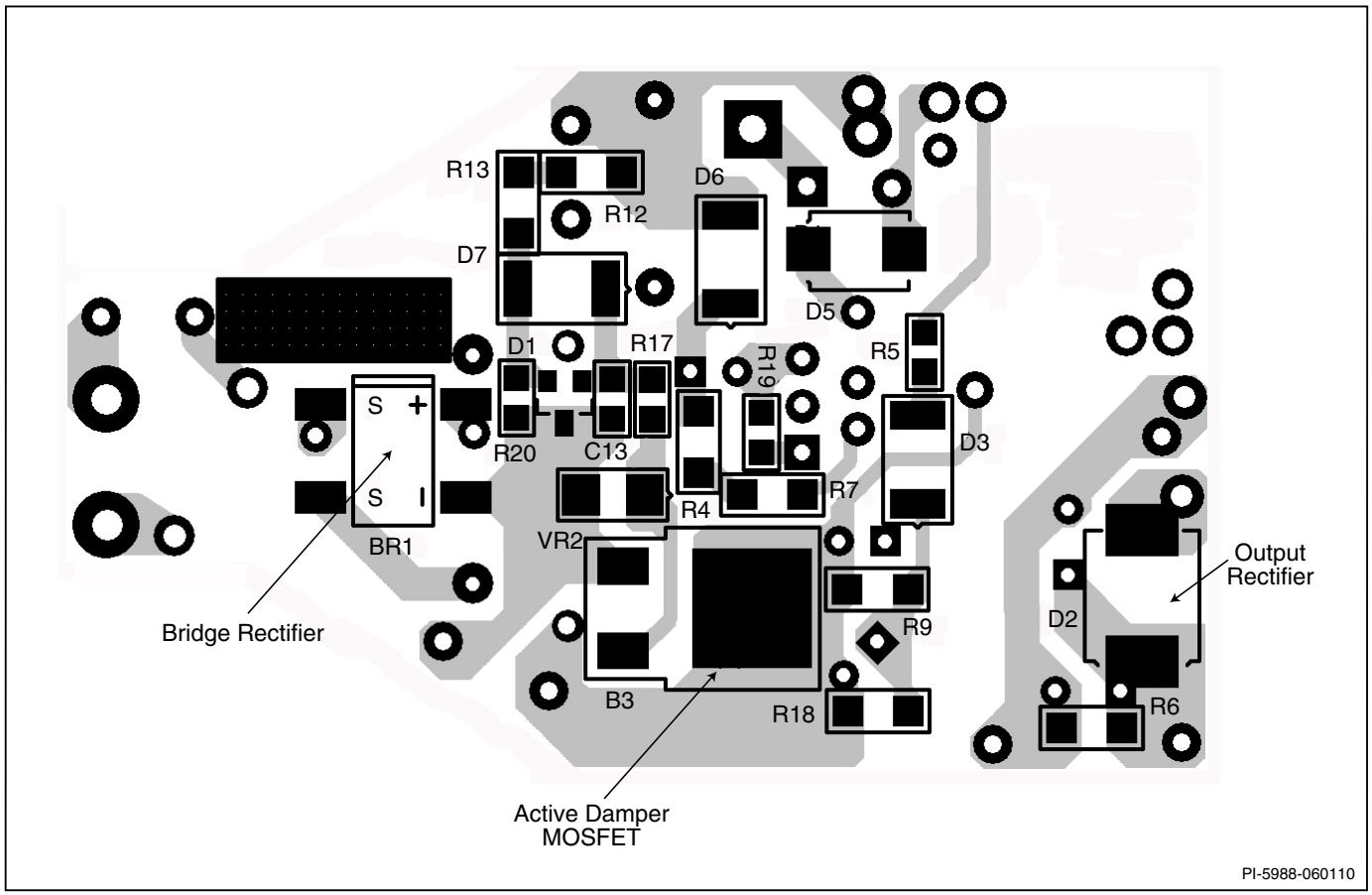


Figure 13. RD-193 7 W Layout Example, Bottom Layer.

Quick Design Checklist

Maximum Drain Voltage

Verify that the peak V_{DS} does not exceed 725 V under all operating conditions including start up and fault conditions.

Maximum Drain Current

Measure the peak drain current under all operation conditions including start up and fault conditions. Look for signs of transformer saturation (usually occurs at highest operating ambient temperatures). Verify that the peak current is less that stated for the Absolute Maximum Rating in the data sheet.

Thermal Check

At maximum output power, both minimum and maximum line voltage and ambient temperature; verify that temperature specifications are not exceeded for the LinkSwitch-PH, transformer, output diodes, output capacitors and drain clamp components.

Absolute Maximum Ratings[1,4]

DRAIN Pin Peak Current[5]: LNK403, LNK413 ..... 1.37 A
LNK404, LNK414 ..... 2.08 A
LNK405, LNK415 ..... 2.72 A
LNK406, LNK416 ..... 4.08 A
LNK407, LNK417 ..... 5.44 A
LNK408, LNK418 ..... 6.88 A
LNK409, LNK419 ..... 7.73 A
LNK410, LNK420 ..... 9.00 A
DRAIN Pin Voltage ..... -0.3 to 725 V
BYPASS Pin Voltage ..... -0.3 to 9 V
BYPASS Pin Current ..... 100 mA
VOLTAGE MONITOR Pin Voltage ..... -0.3 to 9 V[6]
FEEDBACK Pin Voltage ..... -0.3 to 9 V
REFERENCE Pin Voltage ..... -0.3 to 9 V
Lead Temperature[3] ..... 260 °C
Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature[2] ..... -40 to 150 °C

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. Normally limited by internal circuitry.
3. 1/16 in. from case for 5 seconds.
4. Absolute Maximum Ratings specified may be applied, one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings for extended periods of time may affect product reliability.
5. Peak DRAIN current is allowed while the DRAIN voltage is simultaneously less than 400 V. See also Figure 17.
6. During start-up (the period before the BYPASS pin begins powering the IC) the VOLTAGE MONITOR pin voltage can safely rise to 15 V without damage.

Thermal Resistance

Thermal Resistance: eSIP Package:
(θ_{JA}) ..... 105 °C/W[1]
(θ_{JC}) ..... 2 °C/W[2]

Notes:
1. Free Standing with no heat sink.
2. Measured at back surface tab.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -20 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Switching Frequency	f_{OSC}	T_J = 25 °C	Average	62	66	70	kHz
			Peak-Peak Jitter		9		
Frequency Jitter Modulation Rate	f_M	T_J = 25 °C See Note B			1		kHz
BYPASS Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C	LNK403, LNK413	-5.0	-4.2	-3.4	mA
			LNK404, LNK414	-9.6	-8.0	-6.4	
			LNK405-410, LNK415-420	-17	-12	-8.8	
	I_{CH2}	V_{BP} = 5 V, T_J = 25 °C	LNK403, LNK413	-1.6	-1.2	-0.6	
			LNK404, LNK414	-4.2	-3.5	-2.8	
			LNK405-410, LNK415-420	-9	-6.8	-4.6	
Charging Current Temperature Drift		See Note A			0.5		%/°C
BYPASS Pin Voltage	V_{BP}	0 °C < T_J < 100 °C		5.7	5.9	6.1	V
BYPASS Pin Voltage Hysteresis	$V_{BP(H)}$	0 °C < T_J < 100 °C			0.85		V
BYPASS Pin Shunt Voltage	$V_{BP(SHUNT)}$	I_{BP} = 2 mA 0 °C < T_J < 100 °C		6.0	6.4	6.7	V
Soft-Start Time	t_{SOFT}	T_J = 25 °C V_{BP} = 5.9 V		40			ms

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -20 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
Drain Supply Current	I_{CD2}	0 °C < T_J < 100 °C FET Not Switching		0.5	0.85	1.2	mA
	I_{CD1}	0 °C < T_J < 100 °C FET Switching at f_{OSC}		0.9	1.5	2.25	
VOLTAGE MONITOR Pin							
Line Brown-In Threshold Current	I_{UV+}	T_J = 25 °C	R_R = 24.9 kΩ	21.0	22.5	24.0	µA
			R_R = 49.9 kΩ	22.8	24.5	26.2	
Line Brown-Out Threshold Current	I_{UV-}	T_J = 25 °C	R_R = 24.9 kΩ		18.5		µA
			R_R = 49.9 kΩ		15.0		
Line Brown-In/Out Hysteresis	$I_{UV(H)}$	T_J = 25 °C	R_R = 24.9 kΩ	1	4		µA
			R_R = 49.9 kΩ	5	9.4		
Line Overvoltage Threshold	I_{OV}	T_J = 25 °C R_R = 24.9 kΩ R_R = 49.9 kΩ	Threshold	107	112	117	µA
			Hysteresis		4		
VOLTAGE MONITOR Pin Voltage	V_V	0 °C < T_J < 100 °C I_{UV-} < I_V < I_{OV}		2.75	3.0	3.25	V
VOLTAGE MONITOR Pin Short-Circuit Current	$I_{V(SC)}$	V_V = 5 V T_J = 25 °C		170	190	210	µA
Remote ON/OFF Threshold	$V_{V(REM)}$	T_J = 25 °C		0.5			V
FEEDBACK Pin							
FEEDBACK Pin Current at Onset of Maximum Duty Cycle	$I_{FB(DCMAXR)}$	0 °C < T_J < 100 °C				85	µA
FEEDBACK Pin Current Skip Cycle Threshold	$I_{FB(SKIP)}$	0 °C < T_J < 100 °C		220			µA
Maximum Duty Cycle	DC_{MAX}	$I_{FB(DCMAXR)}$ < I_{FB} < $I_{FB(SKIP)}$ 0 °C < T_J < 100 °C		90		99.9	%
FEEDBACK Pin Voltage	V_{FB}	I_{FB} = 150 µA 0 °C < T_J < 100 °C		2.08	2.40	2.62	V
FEEDBACK Pin Short-Circuit Current	$I_{FB(SC)}$	V_{FB} = 5 V T_J = 25 °C		320	400	480	µA
Duty Cycle Reduction	DC10	I_{FB} = $I_{FB(AR)}$, T_J = 25 °C, See Note B		10			%
	DC40	I_{FB} = 40 µA, T_J = 25 °C			20		
	DC60	I_{FB} = 60 µA, T_J = 25 °C			36		
Auto-Restart							
Auto-Restart ON-Time	t_{AR}	T_J = 25 °C V_{BP} = 5.9 V		40			ms
Auto-Restart Duty Cycle	DC_{AR}	T_J = 25 °C			3		%

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -20 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Auto-Restart (cont.)							
SOA Minimum Switch ON-Time	$t_{ON(SOA)}$	T_J = 25 °C See Note B				1.75	µs
FEEDBACK Pin Current During Auto-Restart	$I_{FB(AR)}$	0 °C < T_J < 100 °C				17.5	µA
REFERENCE Pin							
REFERENCE Pin Voltage	V_R	R_R = 24.9 kΩ 0 °C < T_J < 100 °C		1.215	1.245	1.275	V
REFERENCE Pin Current	I_R			48.45	49.70	50.95	µA
Current Limit/Circuit Protection							
Full Power Current Limit (C_{BP} = 100 µF)	$I_{LIMIT(F)}$ T_J = 25 °C	di/dt = 174 mA/µs	LNK404, LNK414	1.02		1.18	A
		di/dt = 174 mA/µs	LNK405, LNK415	1.24		1.44	
		di/dt = 225 mA/µs	LNK406, LNK416	1.50		1.74	
		di/dt = 320 mA/µs	LNK407, LNK417	1.77		2.06	
		di/dt = 350 mA/µs	LNK408, LNK418	2.39		2.77	
		di/dt = 426 mA/µs	LNK409, LNK419	3.26		3.79	
		di/dt = 1060 mA/µs	LNK410, LNK420	4.90		5.70	
Reduced Power Current Limit (C_{BP} = 10 µF)	$I_{LIMIT(R)}$ T_J = 25 °C	di/dt = 133 mA/µs	LNK403, LNK413	0.75		0.85	A
		di/dt = 195 mA/µs	LNK404, LNK414	0.81		0.94	
		di/dt = 192 mA/µs	LNK405, LNK415	1.00		1.16	
		di/dt = 240 mA/µs	LNK406, LNK416	1.19		1.38	
		di/dt = 335 mA/µs	LNK407, LNK417	1.42		1.66	
		di/dt = 380 mA/µs	LNK408, LNK418	1.73		2.01	
		di/dt = 466 mA/µs	LNK409, LNK419	2.35		2.73	
		di/dt = 1060 mA/µs	LNK410, LNK420	4.90		5.70	
Minimum ON-Time Pulse	$t_{LEB} + t_{IL(D)}$	T_J = 25 °C		300	500	700	ns
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C See Note B		150		500	ns
Current Limit Delay	$t_{IL(D)}$	T_J = 25 °C See Note B			150		ns
Thermal Shutdown Temperature				135	142	150	°C
Thermal Shutdown Hysteresis					75		°C
BYPASS Pin Power-Up Reset Threshold Voltage	$V_{BP(RESET)}$	0 °C < T_J < 100 °C		2.25	3.5	4.25	V

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -20 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Output							
ON-State Resistance	$R_{DS(ON)}$	LNK403, LNK413 I_D = 100 mA	T_J = 25 °C		9.00	10.35	Ω
			T_J = 100 °C		13.50	15.5	
		LNK404, LNK414 I_D = 100 mA	T_J = 25 °C		5.40	6.25	
			T_J = 100 °C		8.35	9.7	
		LNK405, LNK415 I_D = 150 mA	T_J = 25 °C		4.10	4.7	
			T_J = 100 °C		6.30	7.3	
		LNK406, LNK416 I_D = 150 mA	T_J = 25 °C		2.80	3.2	
			T_J = 100 °C		4.10	4.75	
		LNK407, LNK417 I_D = 200 mA	T_J = 25 °C		2.00	2.3	
			T_J = 100 °C		3.10	3.6	
		LNK408, LNK418 I_D = 250 mA	T_J = 25 °C		1.60	1.85	
			T_J = 100 °C		2.40	2.8	
		LNK409, LNK419 I_D = 350 mA	T_J = 25 °C		1.40	1.6	
			T_J = 100 °C		2.10	2.45	
		LNK410, LNK420 I_D = 550 mA	T_J = 25 °C		1.05	1.2	
			T_J = 100 °C		1.6	1.85	
OFF-State Drain Leakage Current	I_{DSS}	V_{BP} = 6.4 V, V_{DS} = 560 V, T_J = 100 °C				50	µA
Breakdown Voltage	BV_{DSS}	V_{BP} = 6.4 V, T_J = 25 °C		725			V
Minimum Drain Supply Voltage		T_J < 100 °C		36			V
Rise Time	t_R	Measured in a Typical Flyback			100		ns
Fall Time	t_F				50		ns

NOTES:

A. For specifications with negative values, a negative temperature coefficient corresponds to an increase in magnitude with increasing temperature and a positive temperature coefficient corresponds to a decrease in magnitude with increasing temperature.

B. Guaranteed by characterization. Not tested in production.

Typical Performance Characteristics

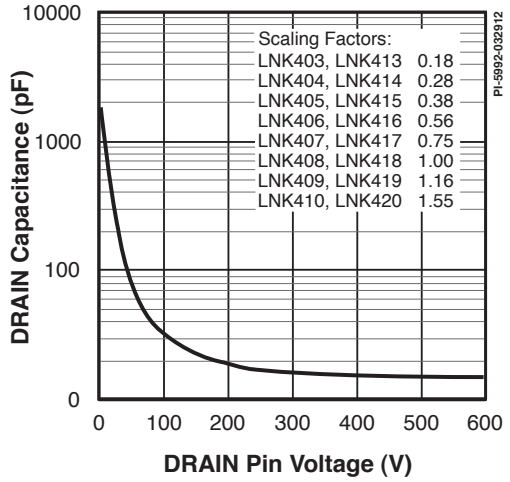


Figure 14. Drain Capacitance vs. Drain Pin Voltage.

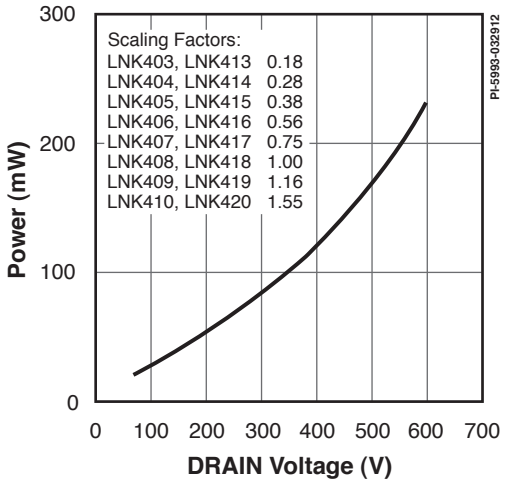


Figure 15. Power vs. Drain Voltage.

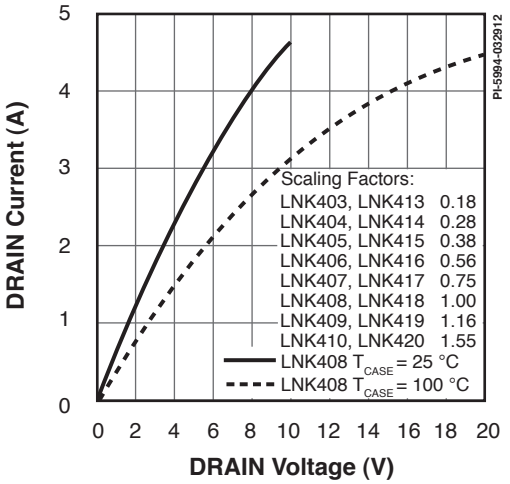


Figure 16. Drain Current vs. Drain Voltage.

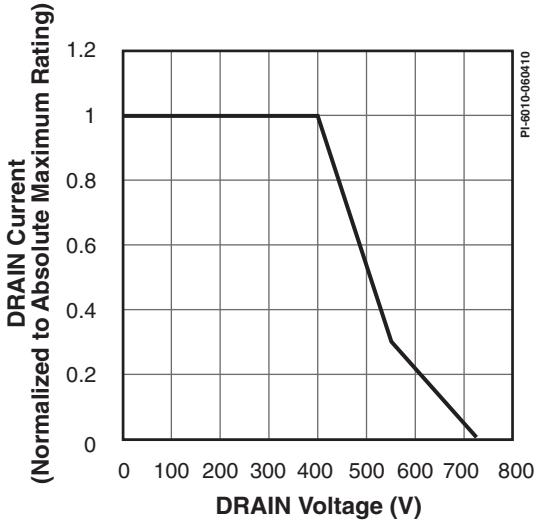
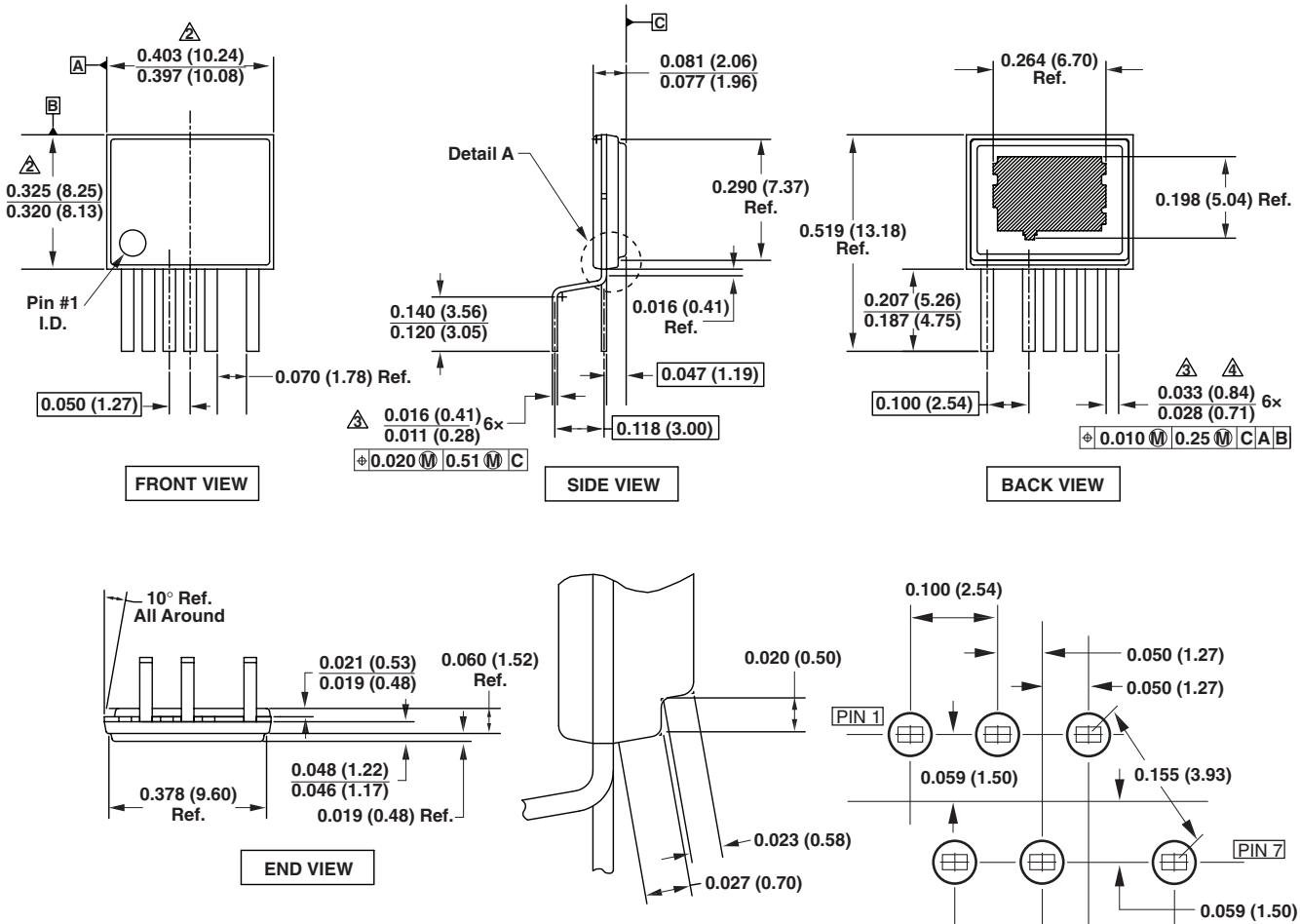


Figure 17. Maximum Allowable Drain Current vs. Drain Voltage.

eSIP-7C (E Package)



Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches (mm).

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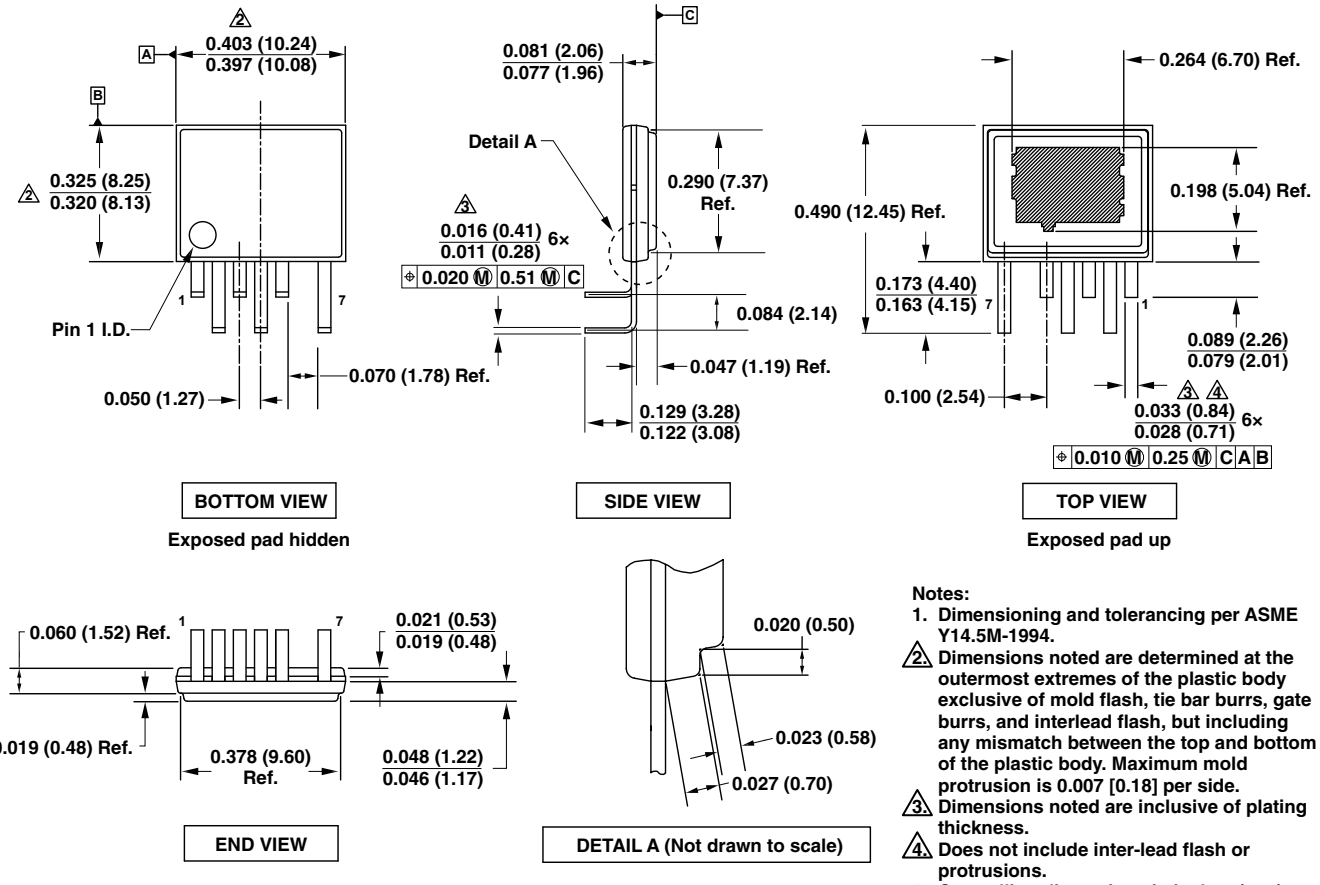
eSIP-7F (L Package)



Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches (mm).

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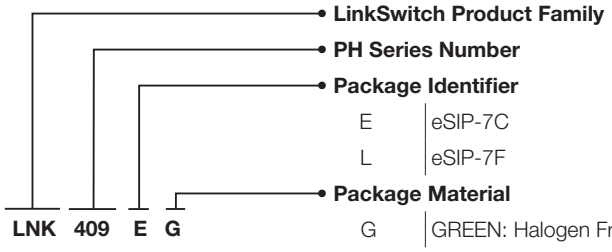
Part Ordering Information



Revision	Notes	Date
A	Initial Release.	06/09/10
B	Updated Power Table.	08/06/10
C	Added Non-Dimming parts and related text.	11/10
D	Added L Package.	08/11
E	Added new LNK410 and LNK420 parts.	12/11
E	Updated Output Power Table values for LNK410/420. Updated Parameter Table values for LNK410/420.	05/12
F	Added Note 6 to Absolute Maximum Ratings section.	06/21/13
G	Updated with new Brand Style Logo.	06/15

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