THE DATASHEET OF

LMV7231SQX/NOPB

LMV7231 Hex Window Comparator With 1.5% Precision and 400-mV Reference

1 Features

- (For V_S = 3.3 V ±10%, Typical Unless Otherwise Noted)
- Undervoltage and Overvoltage Detection
- High Accuracy Voltage Reference: 400 mV
- Threshold Accuracy: ±1.5% (Maximum)
- Wide Supply Voltage Range 2.2 V to 5.5 V
- Input and Output Voltage Range Above V+
- Internal Hysteresis: 6 mV
- Propagation Delay: 2.6 µs to 5.6 µs
- Supply Current 7.7 µA Per Channel
- 24-Lead WQFN Package
- Temperature Range: –40°C to +125°C

2 Applications

- Power Supply Voltage Monitoring
- Battery Monitoring
- Handheld Instruments
- Relay Driving
- Industrial Control Systems

3 Description

The LMV7231 device is a 1.5% accurate Hex Window Comparator which can be used to monitor power supply voltages or any other analog output, such as an analog temperature sensor or current-sense amplifier. The device uses an internal 400-mV reference for the comparator trip value. The comparator set points can be set through external resistor dividers. The LMV7231 has 6 outputs (CO1 to CO6) that signal an undervoltage or overvoltage event for each power supply input. An output (AO) is also provided to signal when any of the power supply inputs have an overvoltage or undervoltage event. This ability to signal an undervoltage or overvoltage event for the individual power supply inputs, in addition to an output to signal such an event on any of the power supply inputs, adds unparalleled system protection capability.

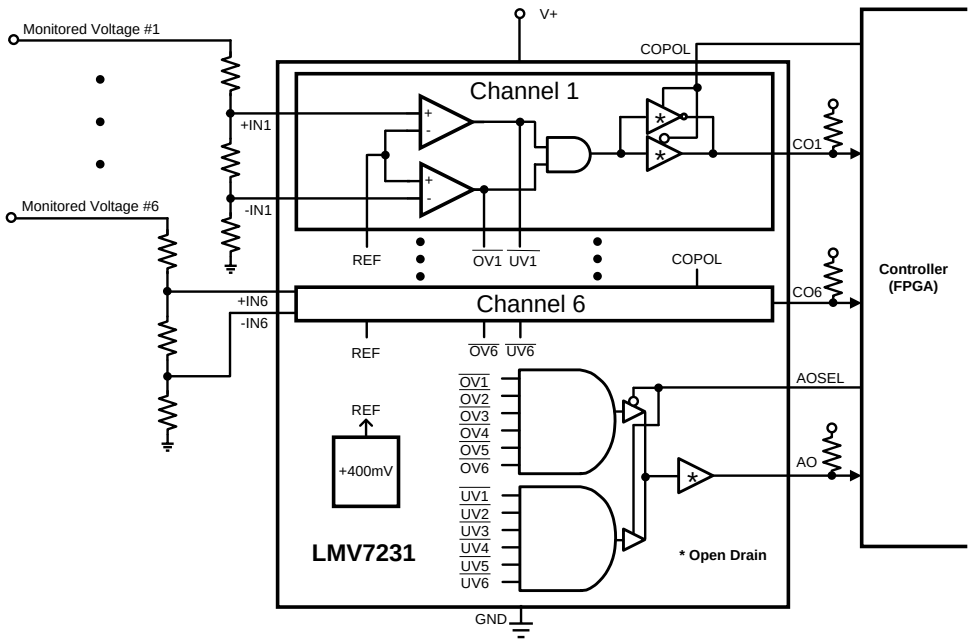
The 2.2-V to 5.5-V power supply voltage range, low supply current, and input or output voltage range above V+ make the LMV7231 ideal for a wide range of power supply monitoring applications. Operation is ensured over the –40°C to +125°C temperature range. The device is available in a 24-pin WQFN package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV7231	WQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (March 2013) to Revision F **Page**

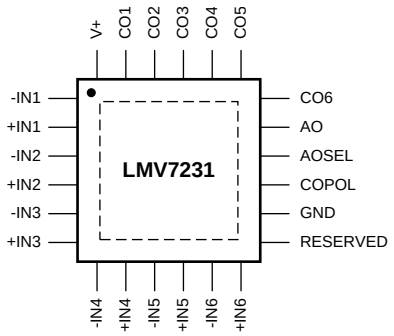
- Added *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* and *Thermal Information* tables, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision D (March 2013) to Revision E **Page**

- Changed layout of National Data Sheet to TI format ... 17

5 Pin Configuration and Functions

RTW Package
24-Pin WQFN
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	–IN1	Analog Input	Negative input for window comparator 1
2	+IN1	Analog Input	Positive input for window comparator 1
3	–IN2	Analog Input	Negative input for window comparator 2
4	+IN2	Analog Input	Positive input for window comparator 2
5	–IN3	Analog Input	Negative input for window comparator 3
6	+IN3	Analog Input	Positive input for window comparator 3
7	–IN4	Analog Input	Negative input for window comparator 4
8	+IN4	Analog Input	Positive input for window comparator 4
9	–IN5	Analog Input	Negative input for window comparator 5
10	+IN5	Analog Input	Positive input for window comparator 5
11	–IN6	Analog Input	Negative input for window comparator 6
12	+IN6	Analog Input	Positive input for window comparator 6
13	RESERVED	Digital Input	Connect to GND
14	GND	Power	Ground reference pin for the power supply voltage
15	COPOL	Digital Input	The state of this pin determines whether the CO1-CO6 pins are active “HIGH” or “LOW”. When tied LOW the CO1-CO6 outputs go LOW to indicate an out-of-window comparison.
16	AOSEL	Digital Input	The state of this pin determines whether the AO pin is active on an overvoltage or undervoltage event. When tied LOW the AO output is active upon an overvoltage event.
17	AO	Open-Drain NMOS Digital Output	This output is the ANDED combination of either the overvoltage comparator outputs or the undervoltage comparator outputs and is controlled by the state of the AOSEL. AO pin is active-low.
18	CO6	Open-Drain NMOS Digital Output	Window comparator 6 NMOS open-drain output
19	CO5	Open-Drain NMOS Digital Output	Window comparator 5 NMOS open-drain output
20	CO4	Open-Drain NMOS Digital Output	Window comparator 4 NMOS open-drain output
21	CO3	Open-Drain NMOS Digital Output	Window comparator 3 NMOS open-drain output
22	CO2	Open-Drain NMOS Digital Output	Window comparator 2 NMOS open-drain output
23	CO1	Open-Drain NMOS Digital Output	Window comparator 1 NMOS open-drain output
24	V+	Power	Power supply pin
DAP	DAP	Thermal Pad	Die Attach Paddle (DAP). Connect to GND.

6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2)(3).

	MIN	MAX	UNIT
Supply voltage		6	V
Voltage at input / output pin	GND − 0.3	6	V
Output current		10	mA
Total package current		50	mA
Junction temperature(4)		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) For soldering specifications, see *Absolute Maximum Ratings for Soldering* (SNOA549).
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±2000	V
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply voltage	2.2	5.5	V
Junction temperature(1)	–40	125	°C

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

6.4 Thermal Information

THERMAL METRIC[1]		LMV7231 RTW (WQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 3.3-V Electrical Characteristics

Unless otherwise specified, all limits ensured for T_A = 25°C, V+ = 3.3 V ±10%, GND = 0 V, and R_L > 1 MΩ.

PARAMETER		TEST CONDITION		MIN[1]	TYP[2]	MAX[1]	UNIT
V_{THR}	Threshold: input rising	R_L = 10 kΩ		394	400	406	mV
			T_A = –10°C to +70°C	391.4		408.6	
V_{THF}	Threshold: input falling	R_L = 10 kΩ		386	394	401	mV
			T_A = –10°C to +70°C	383.8		403.2	
V_{HYST}	Hysteresis (V_{THR} − V_{THF})	R_L = 10 kΩ		3.9	6.0	8.8	mV
I_{BIAS}	Input bias current	V_{IN} = V+, GND, and 5.5 V		–5	0.05	5	nA
			T_A = –10°C to +70°C	–15		15	
V_{OL}	Output low voltage	I_L = 5 mA			160	200	mV
			T_A = –10°C to +70°C			250	
I_{OFF}	Output leakage current	V_{OUT} = V+, 5.5 V and 40 mV of overdrive				0.4	µA
			T_A = –10°C to +70°C			1	
t_{PDHL1}	High-to-low propagation delay (+IN falling)	10 mV of overdrive			2.6	6	µs
t_{PDHL2}	High-to-low propagation delay (-IN rising)	10 mV of overdrive			5.4	10	µs
t_{PDLH1}	Low-to-high propagation delay (+IN rising)	10 mV of overdrive			5.6	10	µs
t_{PDLH2}	Low-to-high propagation delay (-IN falling)	10 mV of overdrive			2.8	6	µs
t_r	Output rise time	C_L= 10 pF, R_L= 10 kΩ			0.5		µs
t_f	Output fall time	C_L = 100 pF, R_L = 10 kΩ				0.25	µs
			T_A = –10°C to +70°C			0.3	
$I_{IN(1)}$	Digital input logic 1 leakage current					0.2	µA
		T_A = –10°C to +70°C				1	
$I_{IN(0)}$	Digital input logic 0 leakage current					0.2	µA
		T_A = –10°C to +70°C				1	
V_{IH}	Digital input logic 1 voltage	T_A = –10°C to +70°C		0.7 × V+			V
V_{IL}	Digital input logic 0 voltage	T_A = –10°C to +70°C				0.3 × V+	V
I_S	Power supply current	No loading (outputs high)			46	60	µA
			T_A = –10°C to +70°C			84	
V_{TH}PSS	V_{TH} power supply sensitivity[3]	V+ ramp rate = 1.1 ms V+ step = 2.5 V to 4.5 V				400	µV
		V+ ramp rate = 1.1 ms V+ step = 4.5 V to 2.5 V		–400			µV

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depends on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) V_{TH} power supply sensitivity is defined as the temporary shift in the internal voltage reference due to a step on the V+ pin.

6.6 Typical Characteristics

V^+ = 3.3 V and T_A =25°C unless otherwise noted.

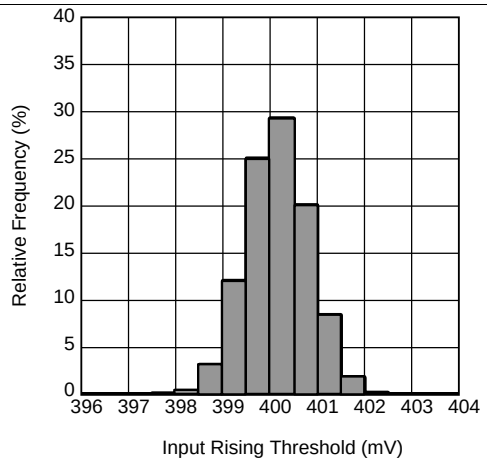


Figure 1. +IN Input Rising Threshold Distribution

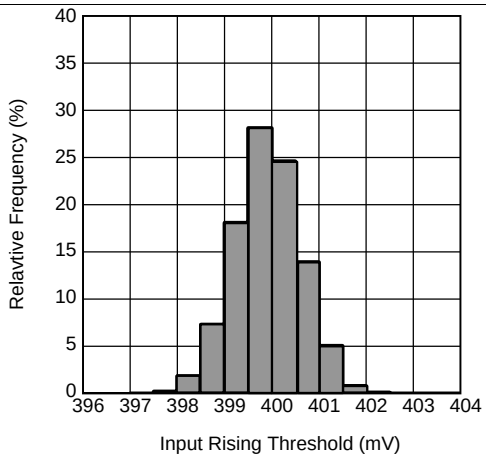


Figure 2. −IN Input Rising Threshold Distribution

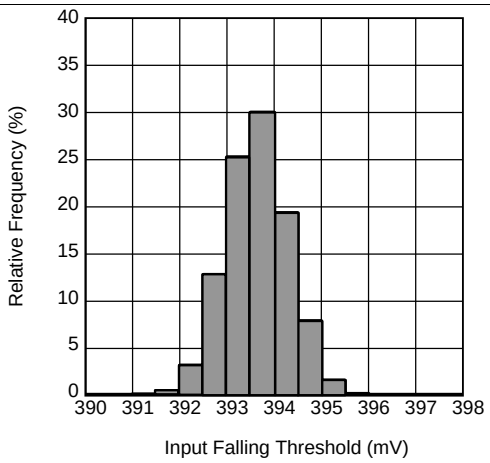


Figure 3. +IN Input Falling Threshold Distribution

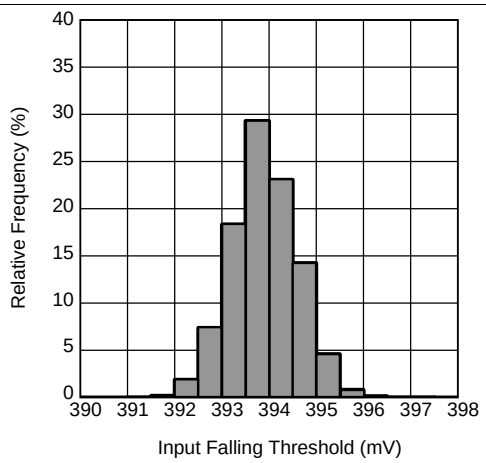


Figure 4. −IN Input Falling Threshold Distribution

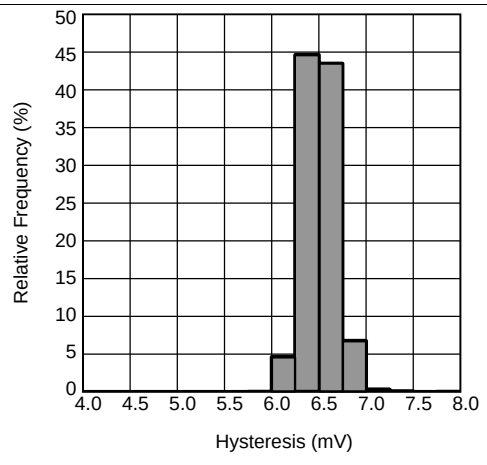


Figure 5. +IN Hysteresis Distribution

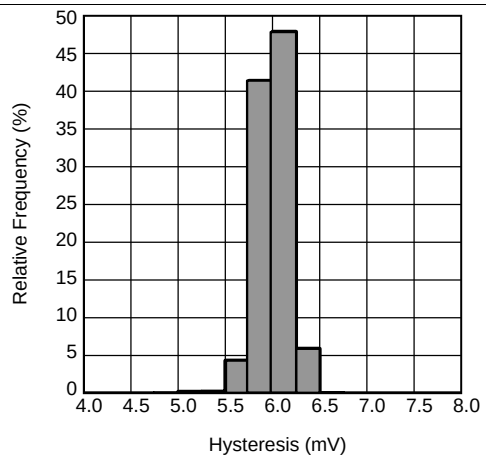


Figure 6. −IN Hysteresis Distribution

Typical Characteristics (continued)

V^+ = 3.3 V and T_A =25°C unless otherwise noted.

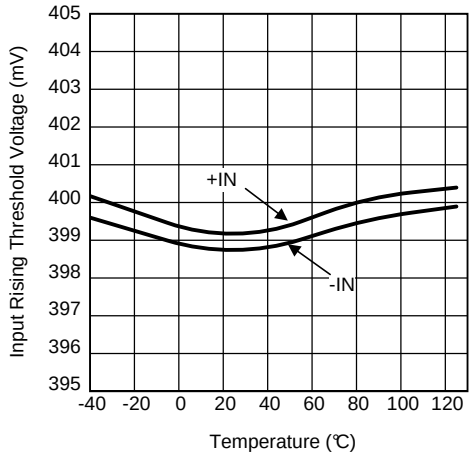


Figure 7. Input Rising Threshold Voltage vs Temperature

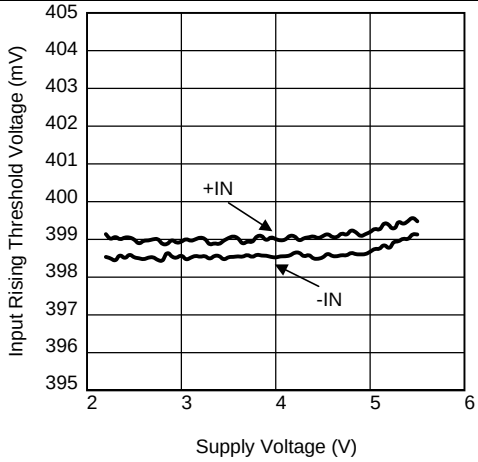


Figure 8. Input Rising Threshold Voltage vs Supply Voltage

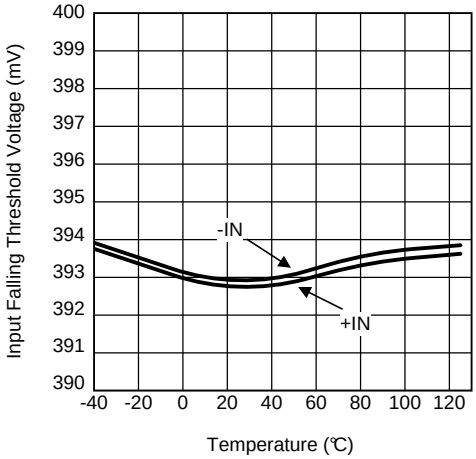


Figure 9. Input Falling Threshold Voltage vs Temperature

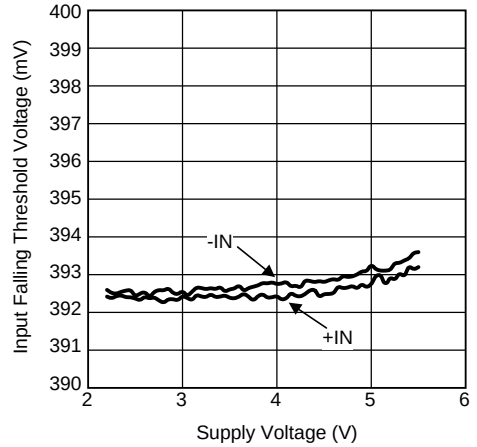


Figure 10. Input Falling Threshold Voltage vs Supply Voltage

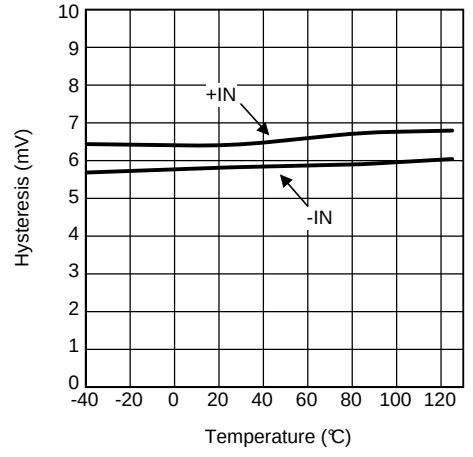


Figure 11. Hysteresis vs Temperature

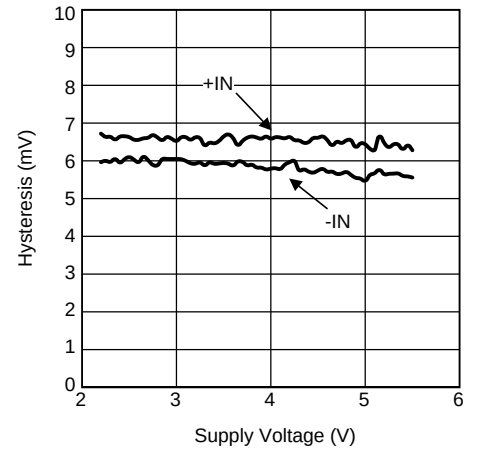


Figure 12. Hysteresis vs Supply Voltage

Typical Characteristics (continued)

V^+ = 3.3 V and T_A =25°C unless otherwise noted.

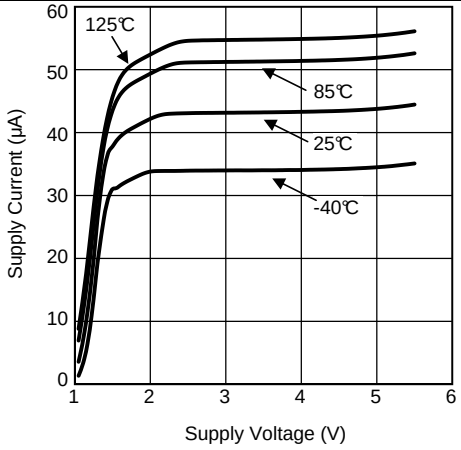


Figure 13. Supply Current vs Supply Voltage and Temperature

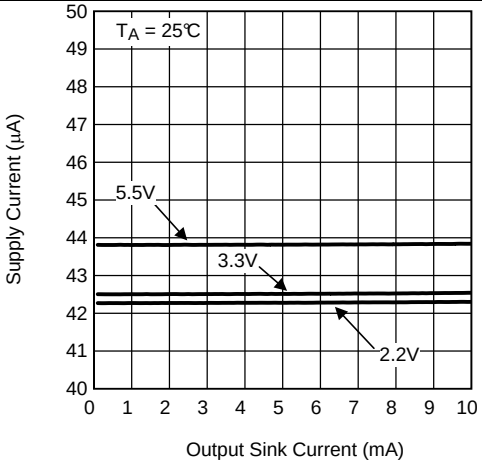


Figure 14. Supply Current vs Output Sink Current

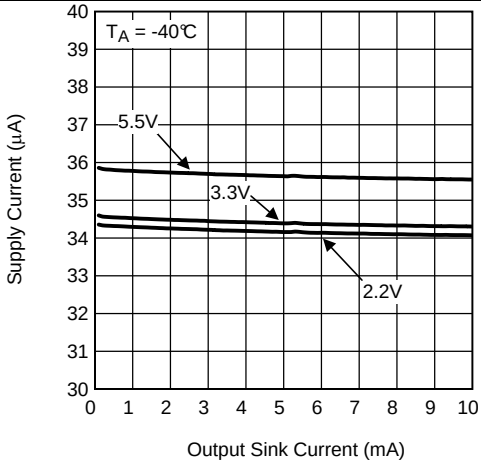


Figure 15. Supply Current vs Output Sink Current

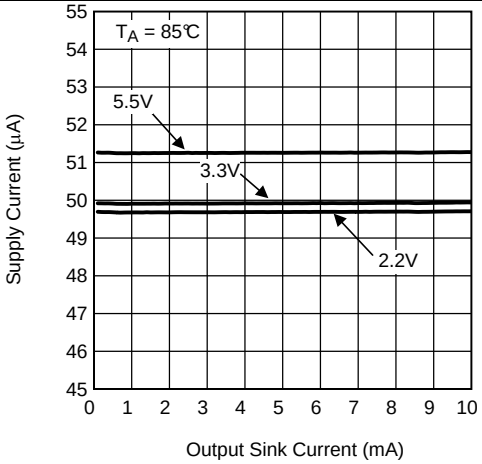


Figure 16. Supply Current vs Output Sink Current

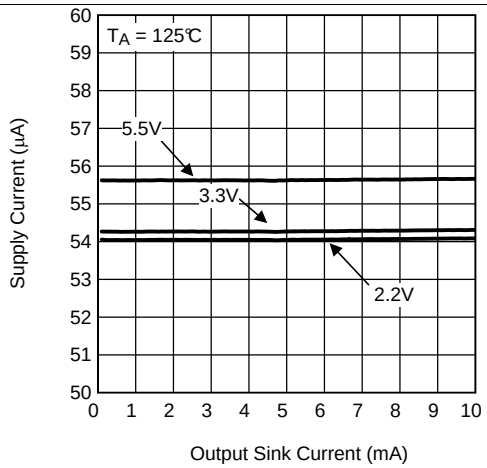


Figure 17. Supply Current vs Output Sink Current

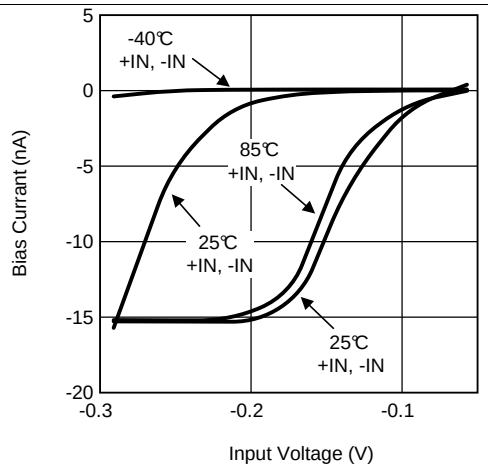


Figure 18. Bias Current vs Input Voltage

Typical Characteristics (continued)

V^+ = 3.3 V and T_A =25°C unless otherwise noted.

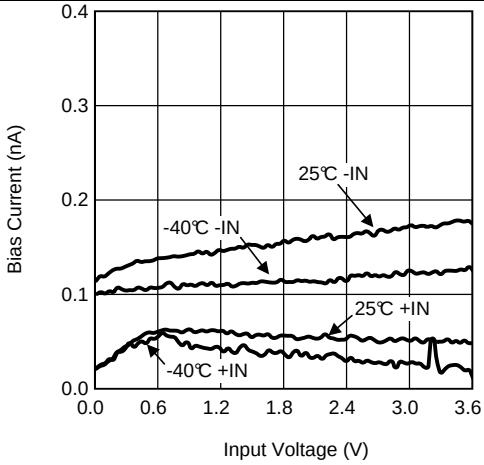


Figure 19. Bias Current vs Input Voltage

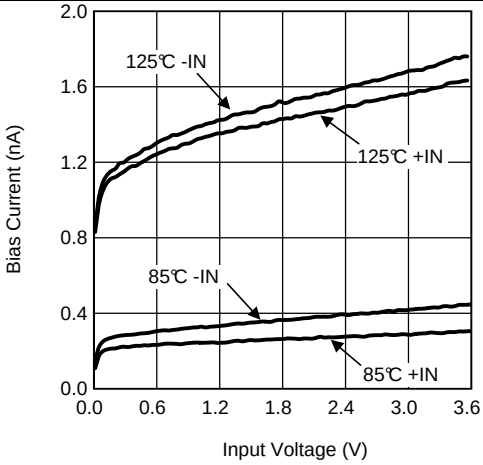


Figure 20. Bias Current vs Input Voltage

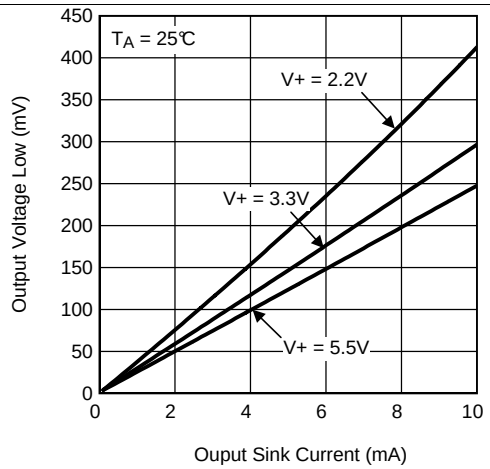


Figure 21. Output Voltage Low vs Output Sink Current

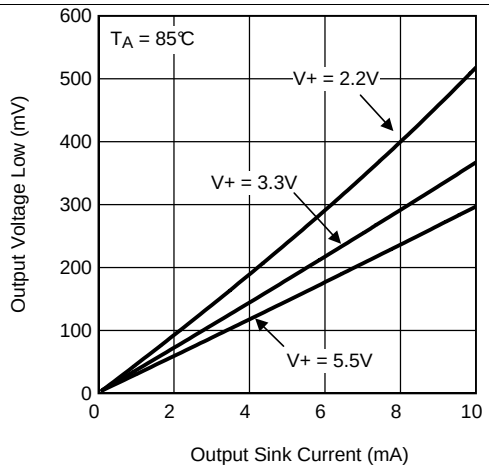


Figure 22. Output Voltage Low vs Output Sink Current

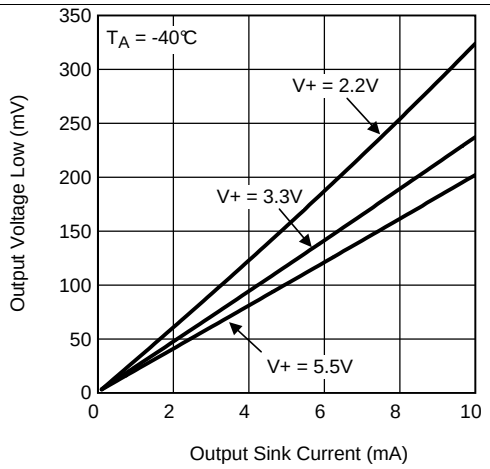


Figure 23. Output Voltage Low vs Output Sink Current

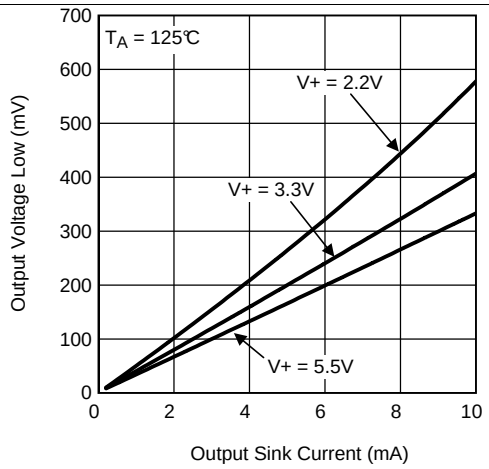


Figure 24. Output Voltage Low vs Output Sink Current

Typical Characteristics (continued)

V^+ = 3.3 V and T_A =25°C unless otherwise noted.

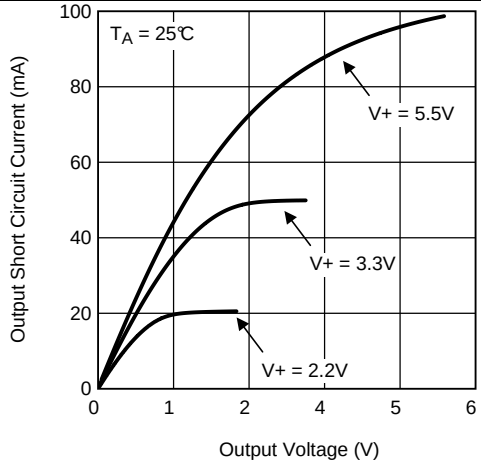


Figure 25. Output Short Circuit Current vs Output Voltage

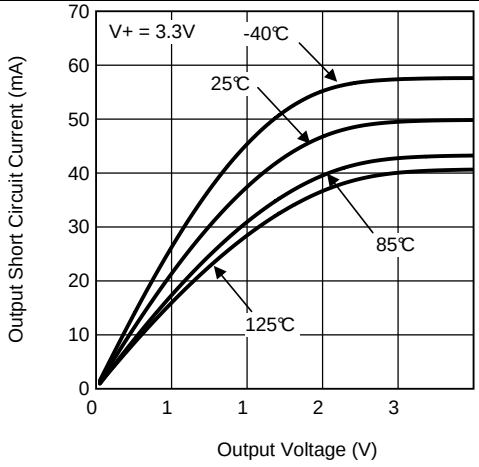


Figure 26. Output Short Circuit Current vs Output Voltage

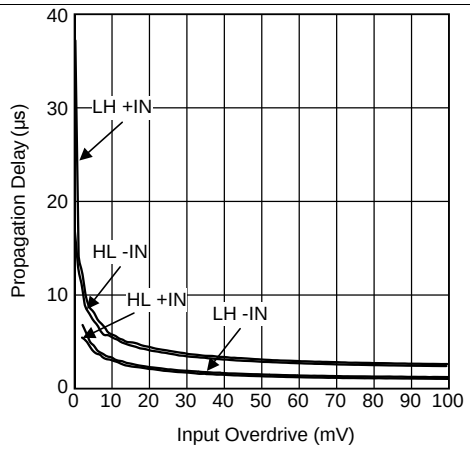


Figure 27. Propagation Delay vs Input Overdrive

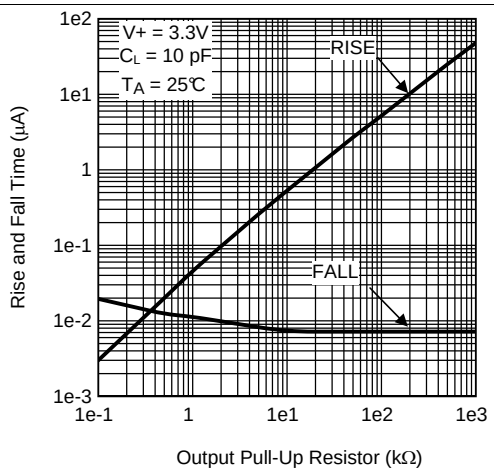


Figure 28. Rise and Fall Times vs Output Pullup Resistor

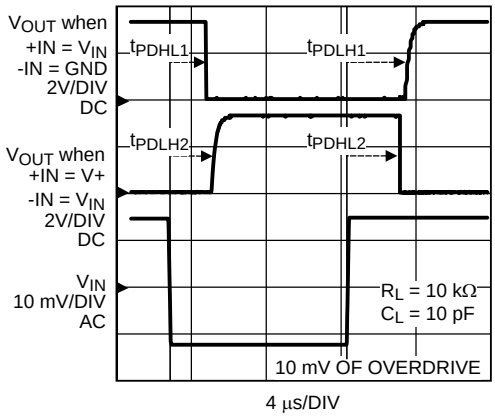


Figure 29. Propagation Delay

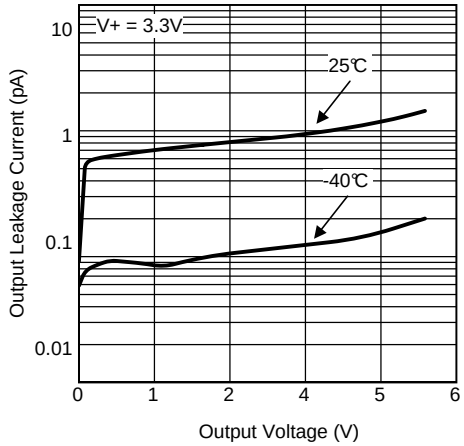


Figure 30. Output Leakage Current vs Output Voltage

Typical Characteristics (continued)

V^+ = 3.3 V and T_A =25°C unless otherwise noted.

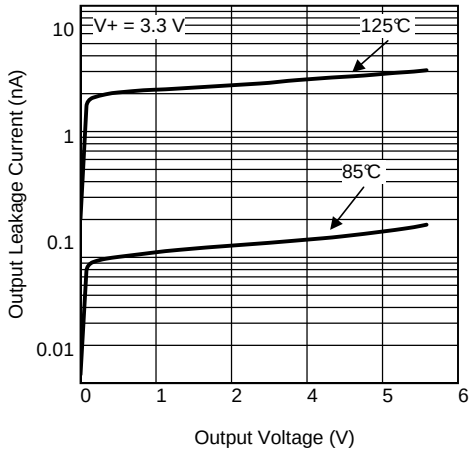


Figure 31. Output Leakage Current vs Output Voltage

7 Detailed Description

7.1 Overview

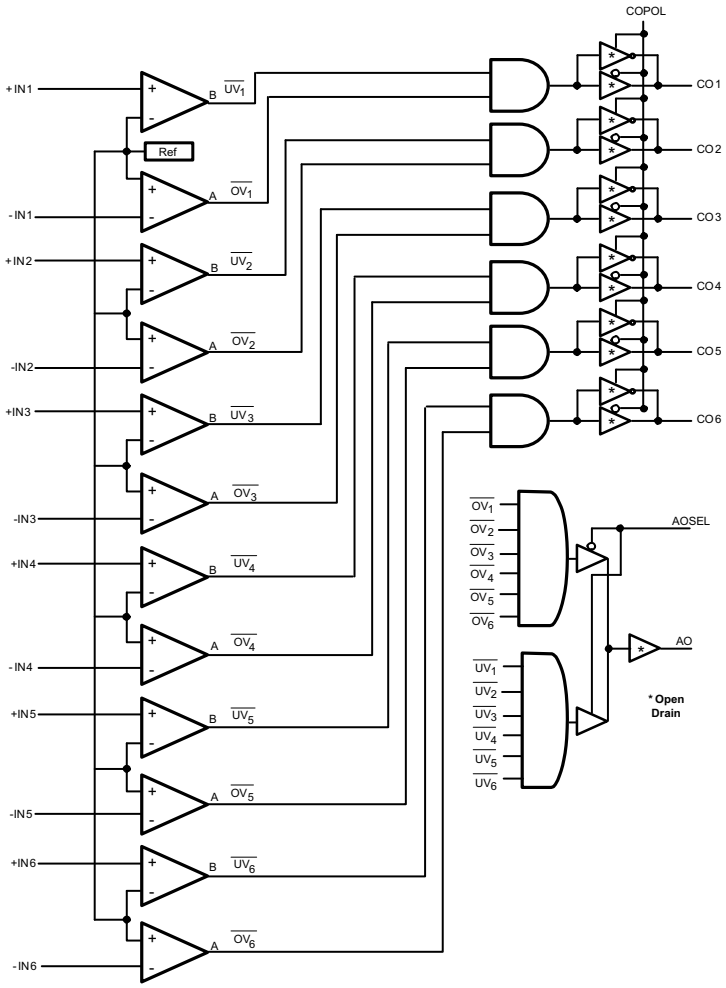
The LMV7231 is Hex Window Comparator which can be used to monitor power supply voltages and other critical system voltage levels.

The LMV7231 contains 6 identical window comparators where the upper and lower trip points are set through external resistor dividers. Each input of the comparator is compared to a internal 1.5% accurate 400-mV reference voltage (V_{REF}).

The 6 window comparator outputs (CO1-CO6) signal an undervoltage or overvoltage event for each power supply input. The COPOL pin sets the *inside* or *outside* of the window indication.

A combined OR'ed output (AO) is also provided to signal when any of the power supply inputs have an overvoltage or undervoltage event. AOSEL sets the logic polarity to create a power-good or error signal.

7.2 Functional Block Diagram



7.3 Feature Description

The LMV7231 Hex Window Comparator with 1.5% precision can accurately monitor up to 6 power rails or batteries at one time. The input and output voltages of the device can exceed the supply voltage, V+, of the comparator, and can be up to the maximum ratings listed in the *Absolute Maximum Ratings* without causing damage or performance degradation. The typical microcontroller input pin with crowbar diode ESD protection circuitry does not allow the input to go above V+, and thus its usefulness is limited in power supply supervision applications.

7.3.1 Input and Output Voltage Range Above V+

The supply independent inputs of the window comparator blocks allow the LMV7231 to be tolerant of system faults. For example, if the power is suddenly removed from the LMV7231 due to a system malfunction while a voltage still exists on the input, it is not an issue as long as the monitored input voltage does not exceed the absolute maximum ratings. Another example where this feature comes in handy is a battery-sense application such as the one in Figure 32. The boards may be sitting on the shelf unbiased with V+ grounded, and yet have a fully charged battery onboard. If the comparator measuring the battery had crowbar diodes, the diode from –IN to V+ would turn on, sourcing current from the battery, eventually draining the battery. However, when using the LMV7231 no current, except the low input bias current of the device, flows into the chip, and the battery charge is preserved.

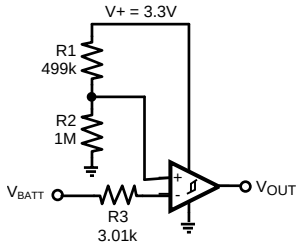


Figure 32. Battery-Sense Application

The output pin voltages of the device can also exceed the supply voltage, V+, of the comparator. This provides extra flexibility and enables designs which pull up the outputs to higher voltage levels to meet system requirements. For example, it is possible to run the LMV7231 at its minimum operating voltage, V+ = 2.2 V, but to bias a blue LED, pull up the output listed in the *Absolute Maximum Ratings*, with a forward voltage of V_F = 4 V.

In a power supply supervision application, the hardwired LMV7231 is a sound solution compared to the microcontroller with software alternative for several reasons. First, start-up is faster. During start-up, code loading time, oscillator ramp time, and reset time do not need to be accounted for. Second, operation is quick. The LMV7231 has a maximum propagation delay and is not affected by sampling and conversion delays related to reading data, calculating data, and setting flags. Third, the device has less overhead. The LMV7231 does not require an expensive power-consuming microcontroller nor is it dependent on controller code which could get damaged or crash.

7.4 Device Functional Modes

7.4.1 +IN1 through +IN6 Input Pins

These inputs set the upper threshold voltage of the channel window comparator. The input voltage is compared to the internal 400-mV reference. These inputs are capable of input voltages up to the *Absolute Maximum Ratings* (6 V), independent of the V+ supply voltage.

7.4.2 –IN1 through –IN6 Input Pins

These inputs set the lower threshold voltage of the channel window comparator. The input voltage is compared to the internal 400-mV reference. These inputs are capable of input voltages up to the *Absolute Maximum Ratings* (6 V), independent of the V+ supply voltage.

Device Functional Modes (continued)

7.4.3 CO1 through C06 Output Pins

These are the open-drain outputs of the individual comparators. A pullup resistor is required or several outputs may be logic OR'ed together with a common pullup resistor. The polarity is determined by the COPOL input pin setting.

7.4.4 COPOL Input Pin

The state of this comparator output polarity select input pin determines whether the CO1-CO6 pins are active-high or active-low. When tied LOW, the CO1-CO6 outputs go LOW to indicate an out-of-window comparison. When tied HIGH, the outputs go LOW to indicate a within-window comparison.

7.4.5 AO Output Pin

This output is the AND'ed combination of either the overvoltage comparator outputs or the undervoltage comparator outputs and is controlled by the state of the AOSEL. The AO pin is active-low.

7.4.6 AOSEL Input Pin

The state of this AND output level select pin determines whether the AO pin is active on an overvoltage or undervoltage event. When tied LOW the AO output is active upon an overvoltage event.

7.4.7 Three-Resistor Voltage Divider Selection

The LMV7231 trip points can be set by external resistor dividers as shown in Figure 33.

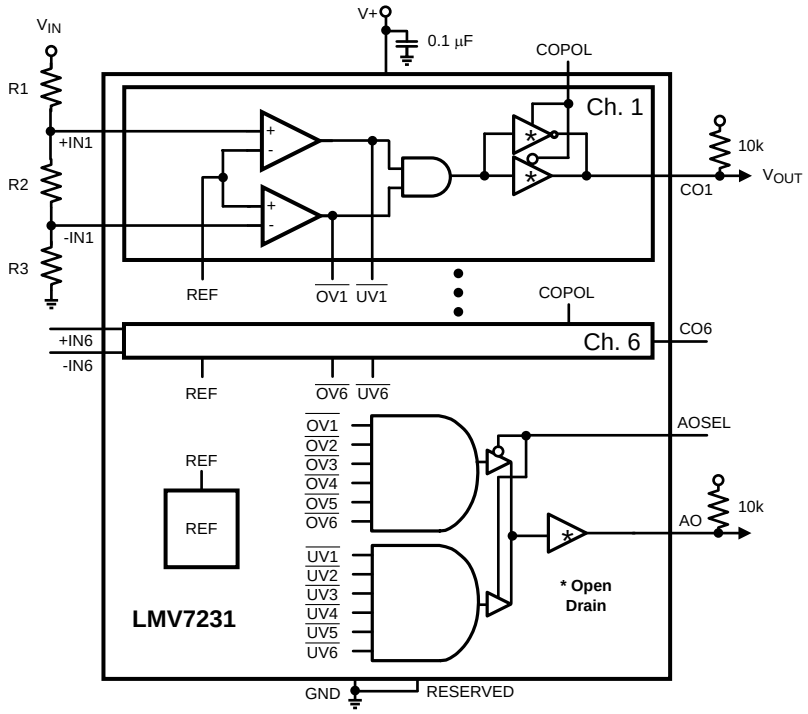


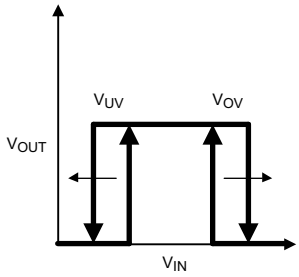
Figure 33. External Resistor Dividers

Each trip point, overvoltage (V_{OV}) and undervoltage (V_{UV}), can be optimized for a falling supply (V_{THF}), or a rising supply (V_{THR}).

Device Functional Modes (continued)

Therefore, there are 2^2 = 4 different optimization cases:

1. Exiting the voltage detection window (Figure 34)
2. Rising into and out of the window (Figure 35)
3. Entering the window (Figure 36)
4. Falling into and out of the window (Figure 37)



R3 set

$R2 = R3((V_{THF}/V_{THR})V_{OV}/V_{UV} \pm 1)$

$R1 = R3((1/V_{THR})V_{OV} - (V_{THF}/V_{THR})V_{OV}/V_{UV})$

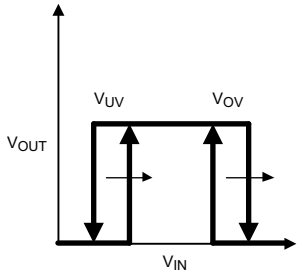
Ex. V_{OV} = 3.465 V, V_{UV} = 3.135 V, that is, V_{RANGE} = 3.3 V ± 5%

R3 set to 10 kΩ

R2 = 10k((0.394/0.4)3.465/3.135 ± 1) ≈ 887 Ω

R1 = 10k((1/0.4)3.465 - (0.394/0.4)3.465/3.135) ≈ 75 kΩ

Figure 34. Exiting the Voltage Detection Window



R3 set

$R2 = R3(V_{OV}/V_{UV} \pm 1)$

$R1 = R3((1/V_{THR})V_{OV} - V_{OV}/V_{UV})$

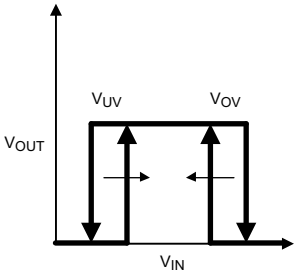
Ex. V_{OV} = 3.465 V, V_{UV} = 3.135 V, that is, V_{RANGE} = 3.3 V ± 5%

R3 set to 10 kΩ

R2 = 10k((3.465/3.135) ± 1) ≈ 1.05 kΩ

R1 = 10k((1/0.4)3.465 ± 3.465/3.135) ≈ 75 kΩ

Figure 35. Rising into and out of the Voltage Detection Window



R3 set

$R2 = R3((V_{THR}/V_{THF})V_{OV}/V_{UV} \pm 1)$

$R1 = R3((1/V_{THF})V_{OV} - (V_{THR}/V_{THF})V_{OV}/V_{UV})$

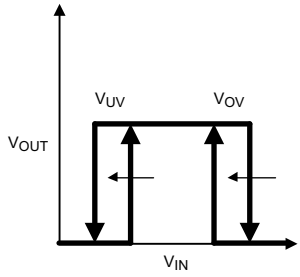
Ex. V_{OV} = 3.465 V, V_{UV} = 3.135 V, that is, V_{RANGE} = 3.3 V ± 5%

R3 set to 10 kΩ

R2 = 10k((0.4/0.394)3.465/3.135 ± 1) ≈ 1.21 kΩ

R1 = 10k((1/0.394)3.465 - (0.4/0.394)3.465/3.135) ≈ 76.8 kΩ

Figure 36. Entering the Voltage Detection Window



R3 set

$R2 = R3(V_{OV}/V_{UV} \pm 1)$

$R1 = R3((1/V_{THF})V_{OV} - V_{OV}/V_{UV})$

Ex. V_{OV} = 3.465 V, V_{UV} = 3.135 V, that is, V_{RANGE} = 3.3 V ± 5%

R3 set to 10 kΩ

R2 = 10k((3.465/3.135) ± 1) ≈ 1.05 kΩ

R1 = 10k((1/0.394)3.465 ± 3.465/3.135) ≈ 76.8 kΩ

Figure 37. Falling into and out of the Voltage Detection Window

NOTE

For each case, each trip point can be optimized for either a rising or falling signal, but not both.

Device Functional Modes (continued)

The governing equations make it such that if the same resistor, R3, and overvoltage-to-undervoltage ratio, V_{OV}/V_{UV}, is used across the channels, the same nominal current travels through the resistor ladder. As a result, R2 is also the same across all channels, and only R1 needs to change to set voltage detection window maximizing reuse of resistor values and minimizing design complexity.

Select the R3 resistor value to be below 100 kΩ so the resistor current through the divider ladder is much greater than the LMV7231 bias current (15 nA worst case, 50 pA typical). If the current traveling through the resistor divider is on the same magnitude of the LMV7231 I_{BIAS}, the I_{BIAS} current creates an error in the circuit and causes trip voltage shifts. The greatest error due to I_{BIAS} is caused when that current passes through the greatest equivalent resistance, REQ = R1∥(R2+R3), which is detected by the positive input of the window comparator, +IN.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMV7231 is specified for operation from 2.2 V to 5.5 V. Some of the specifications apply from –10°C to +70°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* and the *3.3-V Electrical Characteristics*.

8.2 Typical Application

Figure 38 shows a typical power supply supervision circuit using the LMV7231 and the efficient, easy to use LM25007 step-down switching regulator.

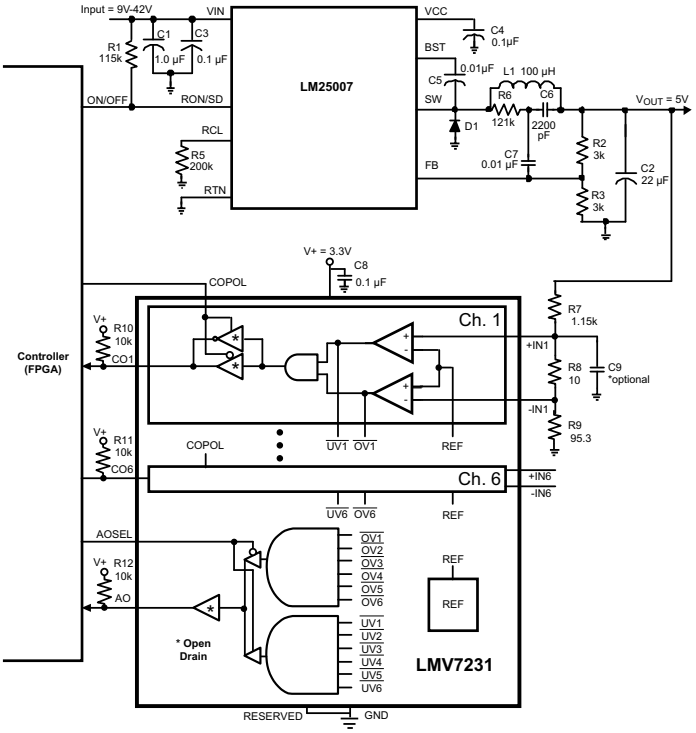


Figure 38. Power Supply Supervision

8.2.1 Design Requirements

Table 1 describes the requested design parameters.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Logic Supply Voltage	3.3 V
Monitored Voltage	5 V
Monitored Voltage Tolerance Window	±5% (4.75 V to 5.25 V)

8.2.2 Detailed Design Procedure

The regulators output voltage is set to 5 V, according to the LM25007 data sheet, SNVS401.

$$V_{OUT} = 2.5 \times (R2 + R3) / R3 \quad (1)$$

$$V_{OUT} = 2.5 \times (3\ k\Omega + 3\ k\Omega) / 3\ k\Omega = 5\ V \quad (2)$$

Resistor R6 and capacitors C6, C7 are utilized to minimize output ripple voltage per the *AN-1453 LM25007 Evaluation Board*, (SNVA152).

The comparator voltage window is set to 5 V ±5%. This requires input voltages of 420 mV and 380 mV, which calculates to R7 = 1.15 kΩ , R8 = 10 Ω, R9 = 95.3 Ω. See the *Three-Resistor Voltage Divider Selection* section for details on how to set the comparator voltage window.

With the components selected, the output ripple voltage on the LM25007 is approximately 30 to 35 mV and is reduced to about 4 mV at the comparator input, +IN1, by the resistor divider. This ripple voltage can be reduced multiple ways. First, user can operate the device in continuous conduction mode rather than discontinuous conduction mode. To do this increase the load current of the device (see SNVS401 for more details). However, the power rating of the resistors in the resistor ladder must not be exceeded. Second, ripple can be reduced further with a bypass capacitor, C9, at the resistor divider. If desired, select a 1-µF capacitor to achieve less than 3-mV ripple at +IN1. However, there is a trade-off that adding capacitance at this node lowers the system response time.

8.2.3 Application Curve

Figure 39 shows the results of sweeping the regulator output voltage through the undervoltage and overvoltage thresholds. COPOL is set LOW so that the output goes LOW while the regulator voltage is within the ±5% thresholds.

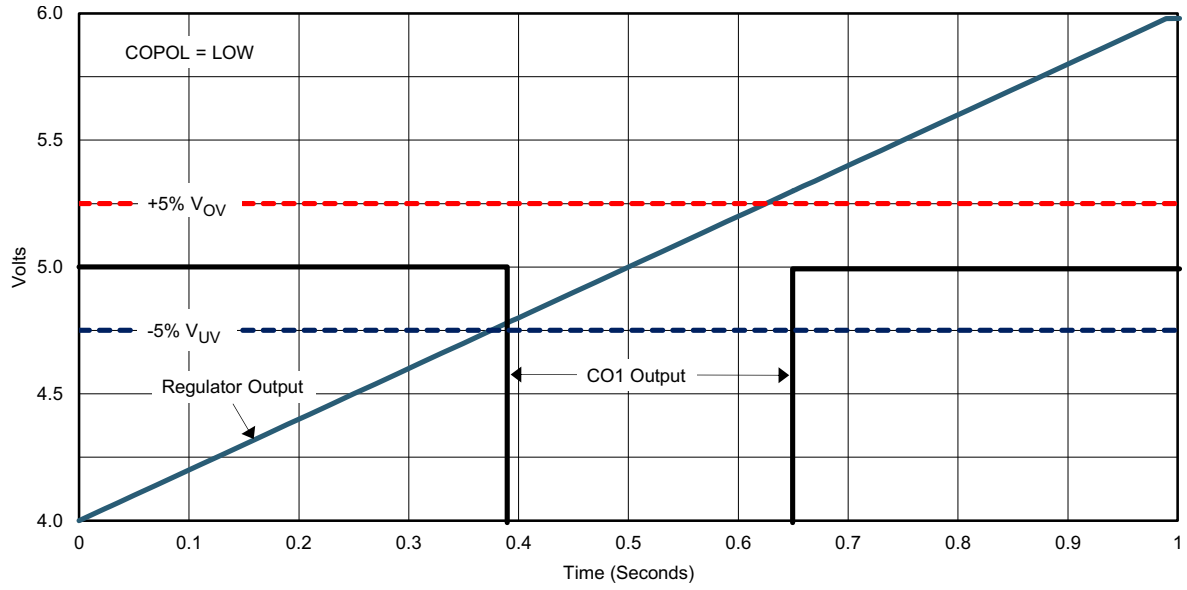


Figure 39. Power Supply Supervisor Thresholds

9 Power Supply Recommendations

Bypass the supply pin, V+, with a 0.1-µF ceramic capacitor placed close to the V+ pin. If transients with rise or fall times of hundreds of µs and magnitudes of hundreds of mV are expected on the power supply line, an RC lowpass filter network as shown in Figure 40 is recommended for additional bypassing. If no such bypass network is used power supply transients can cause the internal voltage reference of the comparator to temporarily shift potentially resulting in a brief incorrect comparator output. For example, if an RC network with 100-Ω resistance and 10-µF capacitance (1.1-ms rise time) is used the voltage reference temporarily shifts the amount, V_{TH} power supply sensitivity (V_{TH}PSS), specified in the *3.3-V Electrical Characteristics* table.

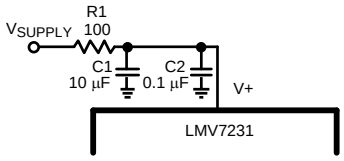


Figure 40. Power Supply Bypassing

10 Layout

10.1 Layout Guidelines

Proper grounding and the use of a ground plane helps to ensure the specified performance of the LMV7231. Minimizing trace lengths, reducing unwanted parasitic capacitance, and using surface-mount components also helps. Comparators are very sensitive to input noise.

1. Use a printed-circuit-board with a good, unbroken low-inductance ground plane.
2. Place a decoupling capacitor (0.1-µF ceramic surface mount capacitor) as close to V+ pin as possible.
3. On the inputs and the outputs, keep lead lengths and the divider resistors as short possible to avoid noise pick-up.

The DAP pad is connected to the bottom of the die and is not designed to carry current. The DAP thermal pad must be connected directly to the GND pin to avoid noise and possible voltage gradients. The primary grounding pin is the GND pin.

10.2 Layout Example

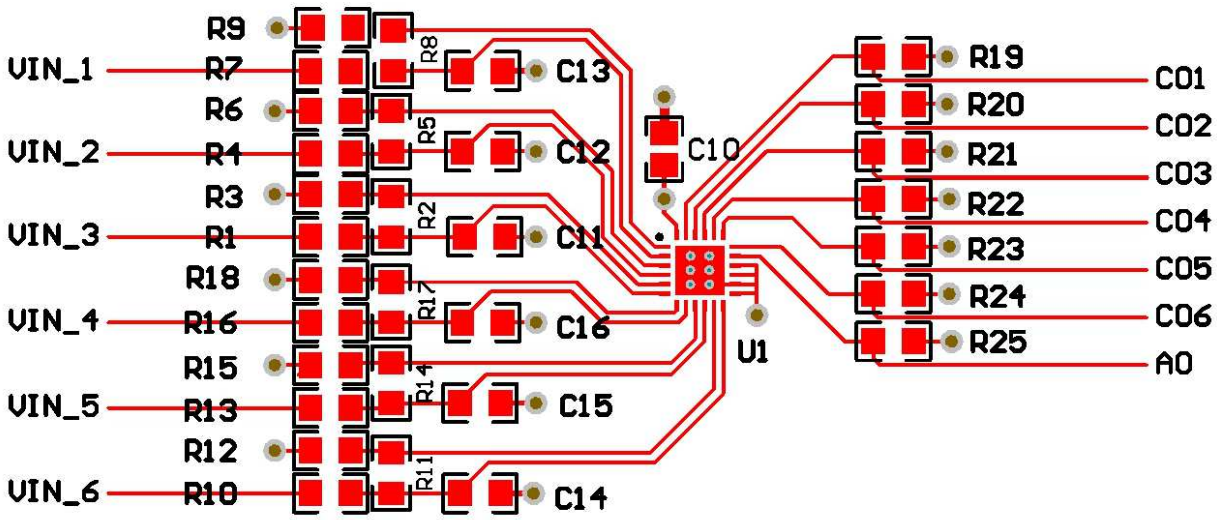


Figure 41. Example Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

LMV7231 Evaluation Board, http://www.ti.com/tool/lmv7231eval

11.2 Documentation Support

11.2.1 Related Documentation

- *LMV7231 Evaluation Board Manual*, SNOU008
- *LM25007 42-V, 0.5-A Step-Down Switching Regulator*, SNVS401
- *AN-1453 LM25007 Evaluation Board*, SNVA152

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV7231SQ/NOPB	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L7231SQ	Samples
LMV7231SQE/NOPB	ACTIVE	WQFN	RTW	24	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L7231SQ	Samples
LMV7231SQX/NOPB	ACTIVE	WQFN	RTW	24	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L7231SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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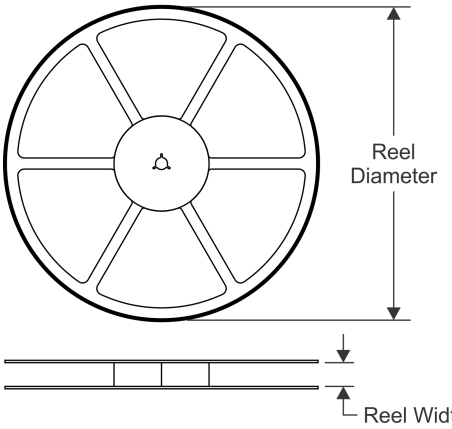
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

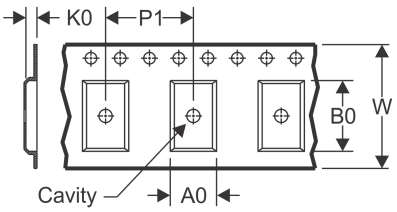
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

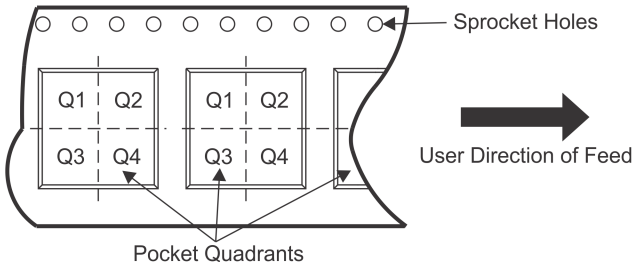


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

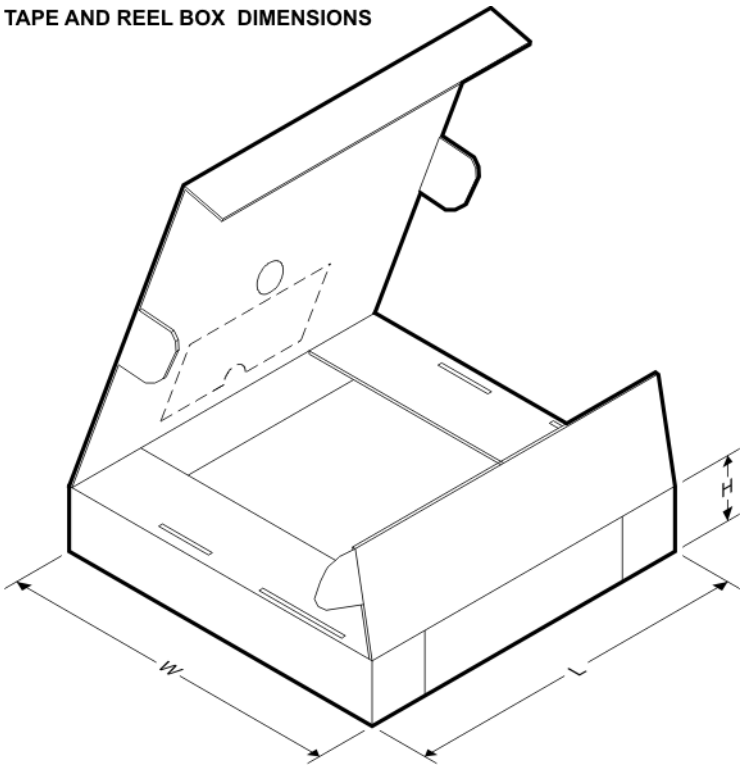
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV7231SQ/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMV7231SQE/NOPB	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMV7231SQX/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

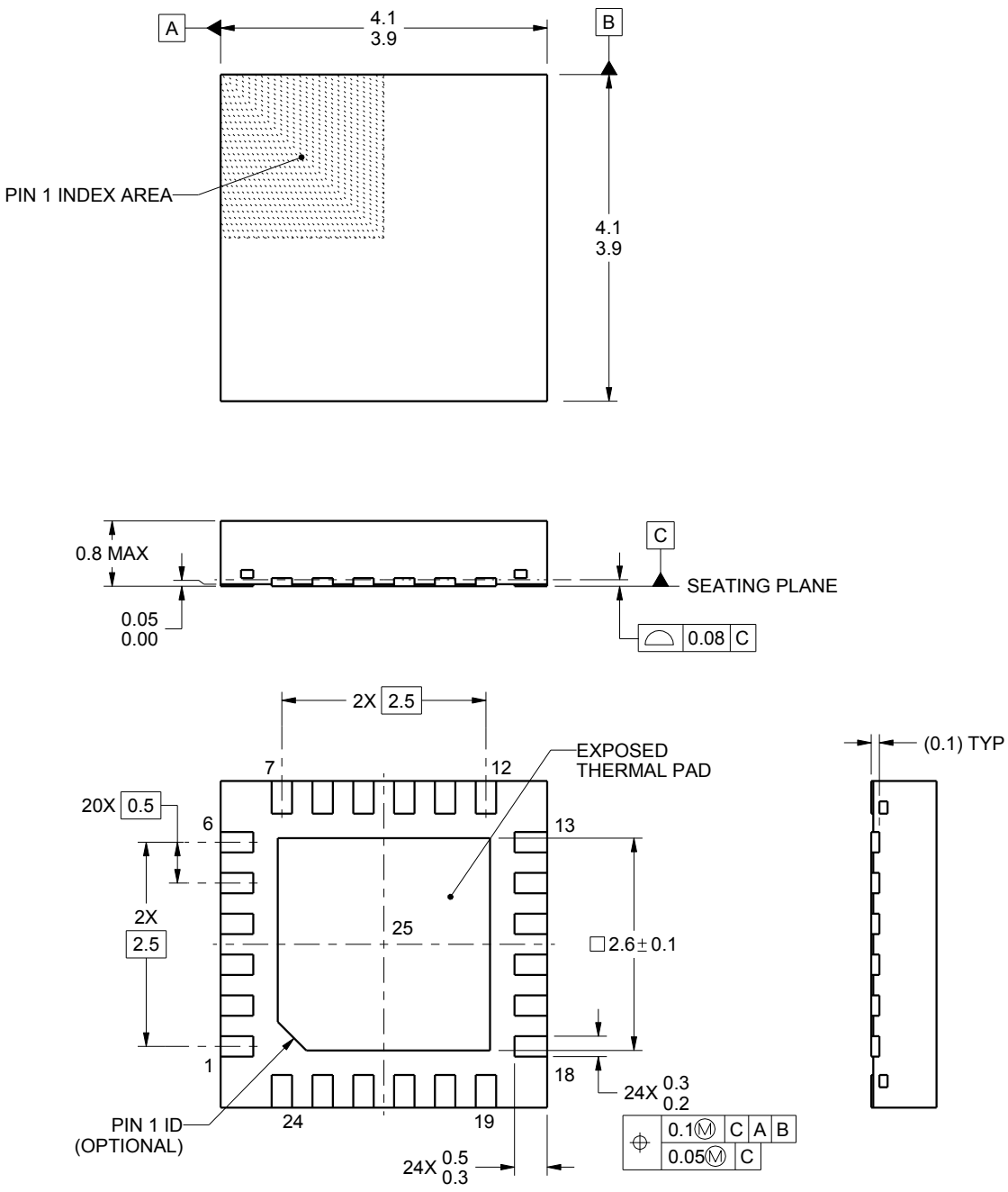
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV7231SQ/NOPB	WQFN	RTW	24	1000	210.0	185.0	35.0
LMV7231SQE/NOPB	WQFN	RTW	24	250	210.0	185.0	35.0
LMV7231SQX/NOPB	WQFN	RTW	24	4500	367.0	367.0	35.0

PACKAGE OUTLINE

RTW0024A

WQFN - 0.8 mm max height

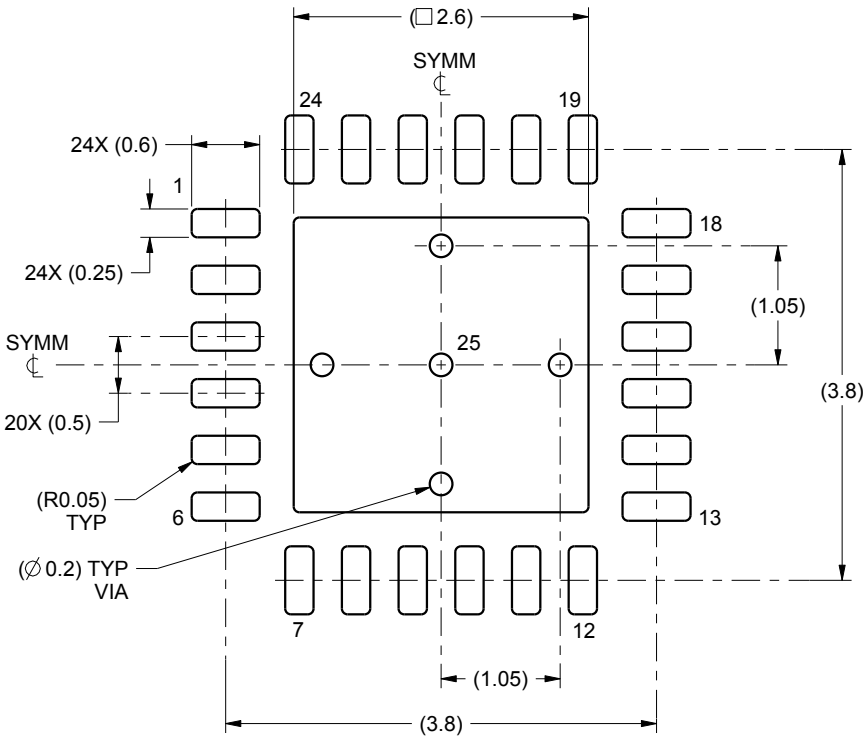
PLASTIC QUAD FLATPACK - NO LEAD



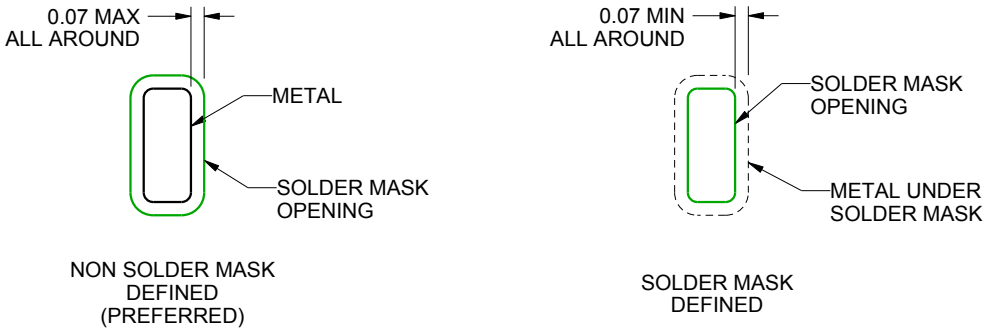
4222815/A 03/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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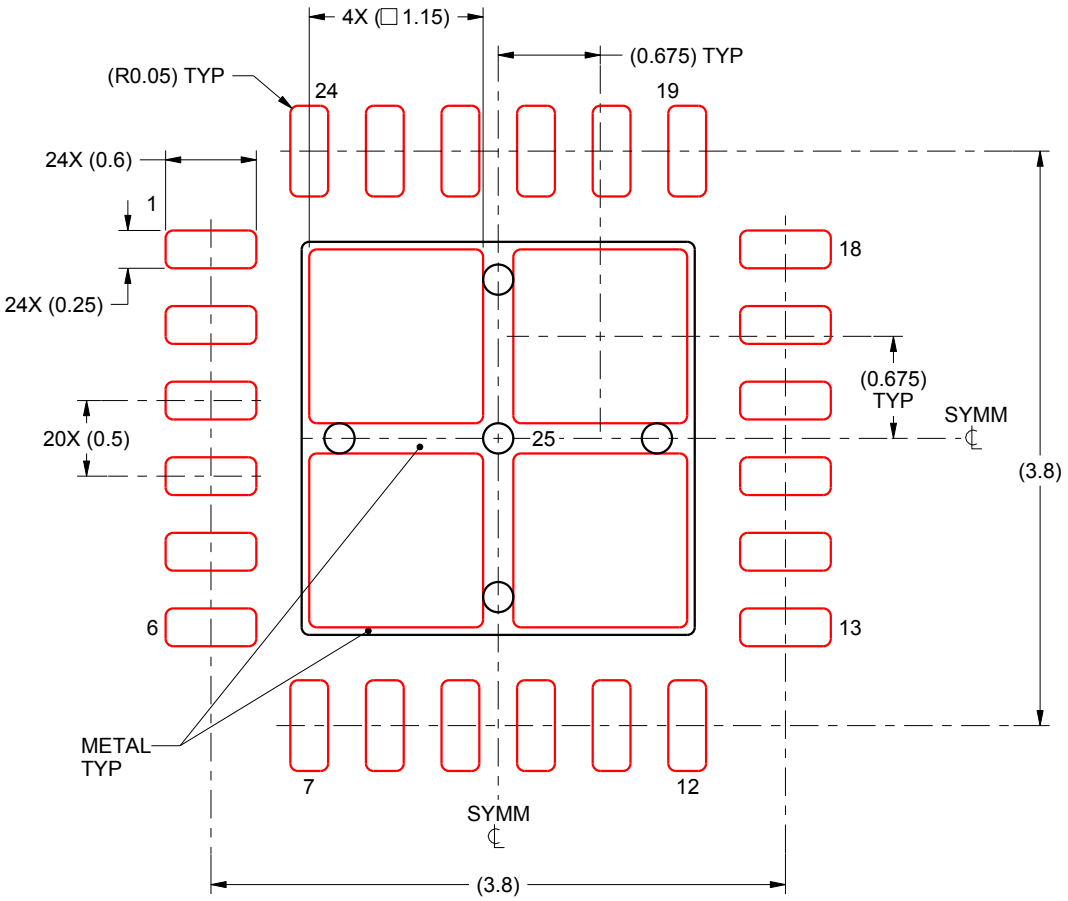
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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