



# THE DATASHEET OF LM8335EVM



## LM8335 General Purpose Output Expander with MIPI® RFFE Host Interface

Check for Samples: [LM8335](#)

### FEATURES

- MIPI RFFE Interface Version 1.10 Compliant
- Supports Output Expansion
- Host Interface Address Select Pin:
  - ADR=GND, USID[3:0]=0001
  - ADR=VDD, USID[3:0]=1001
- Pin-Configurable Initial State: VIO
  - CFG=GND, GPO High-z, with Weak Internal Pull-Down Resistor Enabled; GPO\_OUT\_DATA is Unmasked
  - CFG=VDD, GPO High-z, with Weak Internal Pull-Down Resistor Enabled; GPO\_OUT\_DATA is Masked
- Three Sources for Chip Reset:
  - VIO Input Pin
  - POR
  - Software-Commanded Reset

### APPLICATIONS:

- Smart Handheld Devices
- RF Transceiver Applications

### KEY SPECIFICATIONS

- $1.8 \pm 0.15\text{V}$  MIPI RFFE Operation (VIO)
- $1.8 \pm 0.15\text{V}$  Core Supply (V<sub>DD</sub>)
- 1.65 to 3.6V GPO Supply (V<sub>DDIO</sub>)
- Low Standby and Active Current
- On-Chip Power-On Reset (POR)
- –30 to +85°C Ambient Temperature Range
- 16-Bump DSBGA Package
  - 1.965 mm x 1.965 mm x 0.6 mm, 0.5 mm Pitch (Nominal)

### DESCRIPTION

The LM8335 General Purpose Output Expander is a dedicated device to provide flexible and general purpose, host programmable output expansion functions. This device communicates with a host processor through a MIPI® RFFE Interface (Mobile Industry Processor Interface RF Front-End).

Eight general purpose outputs (GPO) can be configured by the host controller as drive high/low/high-z. Weak pull-ups (PU) or weak pull-downs (PD) can be enabled.

Upon power-on, the LM8335 default configuration is for all GPO to be set based on the state of the CFG pin.

After startup, any changes to the default configuration must be sent from the host via the MIPI RFFE host interface..

The LM8335 is available in a 16-bump lead-free DSBGA package of size 1.965 mm x 1.965 mm x 0.6 mm (0.5 mm pitch).



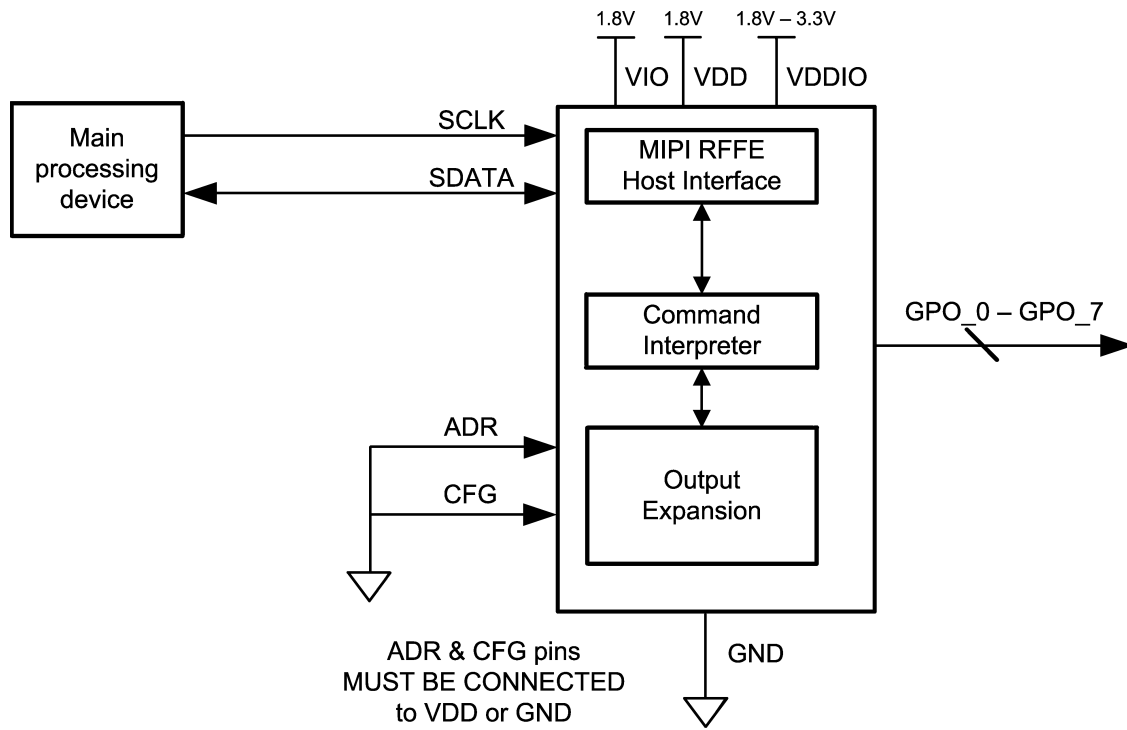
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

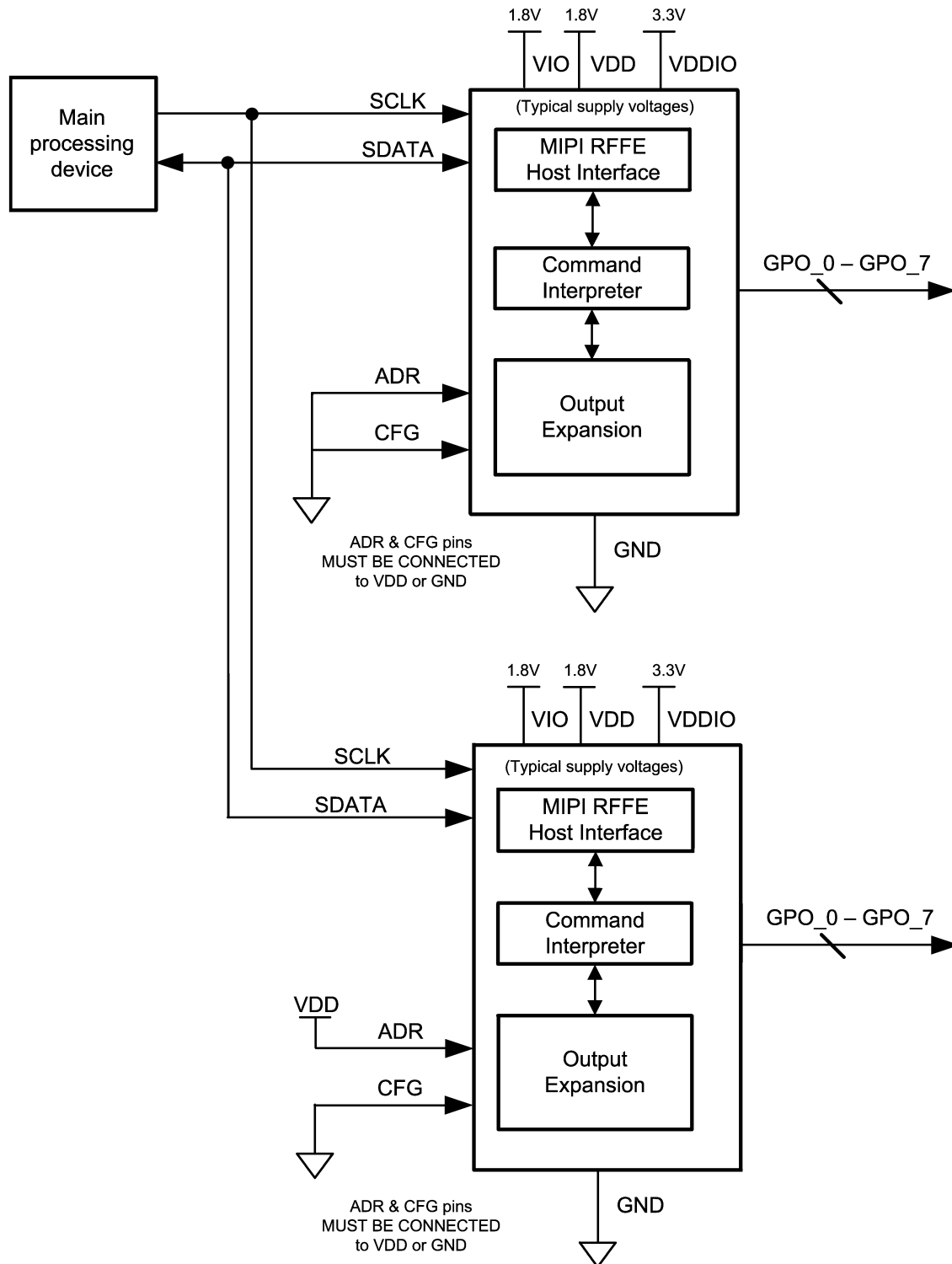
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2012–2013, Texas Instruments Incorporated

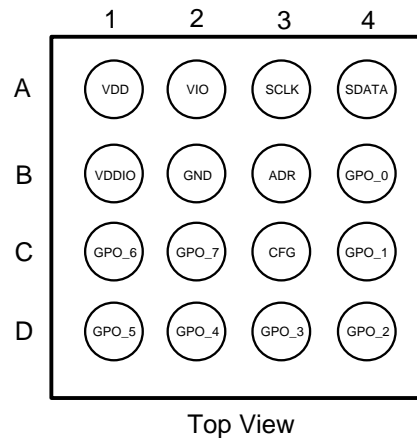
**Single RFFE Slave Application Block Diagram**



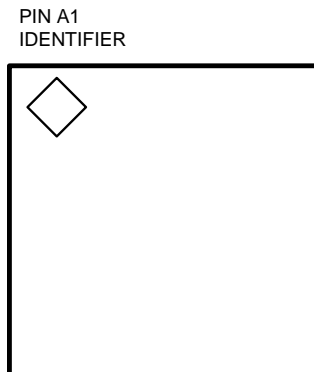
Dual RFFE Slave Application Block Diagram



## Connection Diagram and Package Mark Information



**Figure 1. 16-Bump DSBGA Pinout**  
**1.965mm x 1.965mm x 0.6mm (nom), 0.5mm pitch**  
**See Package Number YZR0016**



**Figure 2. A1 Pin Identifier**

### PIN DESCRIPTIONS

Pin Number	Name	Description
8	GPO_0 through GPO_7	General purpose outputs
1	SCLK	RFFE clock input
1	SDATA	RFFE data input
1	ADR	RFFE chip address input ADR = VDD: USID[3:0] = b1001 ADR = GND: USID[3:0] = b0001
1	CFG	Initial configuration select CFG = VDD: GPO high-z with weak internal pull-down resistor enabled, GPO_OUT_DATA masked CFG = GND: GPO high-z, with weak internal pull-down resistor enabled, GPO_OUT_DATA unmasked
1	VIO	MIPI RFFE VIO (1.8V ± 0.15V)
1	VDD	Core supply VDD (1.8V ± 0.15V)
1	VDDIO	GPO supply VDDIO (1.65V to 3.6V)
1	GND	Ground

## ADR INPUT PIN

The state of the ADR pin determines the MIPI RFFE USID as described in the table above. This enables two devices to be used on the same RFFE bus thereby doubling the number of GPOs available in the system (see [Dual RFFE Slave Application Block Diagram](#)).

## DEFAULT GPO\_x PIN CONFIGURATION

Upon power-on all GPOs will default based on the state of the CFG pin.

### CFG INPUT PIN = GND

The CFG0 mode is an automatic initialization mode. It allows the host to not have to first configure any registers before writing the GPO\_OUT\_DATA register to set the GPOs high or low. In this mode, the GPOs will default as high-z with weak pull-down resistors enabled and the GPO\_OUT\_DATA will be unmasked. When the host writes the GPO\_OUT\_DATA register, the weak pull-down resistor will be disabled. The output driver will immediately be enabled and will drive high or low based on the value written to the GPO\_OUT\_DATA register. In configuration mode CFG0 the GPO data mask function is available but the GPO pull resistor, and high-z functions cannot be changed. Writing to the GPO\_PULL\_DIR, GPO\_PULL\_ENABLE, and GPO\_OUT\_HIGH\_CFG registers will have no effect. If control of the GPO pull resistor or output configuration is required then the CFG1 mode must be used.

### CFG INPUT PIN = VDD

The CFG1 mode is a more general purpose mode where the outputs must be configured during initialization prior to use. In this mode, the GPOs will default as high-z with internal pull-down resistors enabled and GPO\_OUT\_DATA will be masked. During initialization, the host must first write to the GPO\_OUT\_DATA register (Note: this will transition all of the GPOs from high-z with internal pull-down to Full-Buffer driven low with internal pull-down regardless of the value written to the GPO\_OUT\_DATA register). The host must then write to the GPO\_PULL\_DIR, GPO\_PULL\_ENABLE, & GPO\_OUT\_HIGH\_CFG registers to configure each GPO into the desired output configuration. Once that is complete, the host then writes the GPO\_DATA\_MASK and GPO\_OUT\_DATA registers to set the GPO outputs in the desired state. Refer to [Figure 8](#).



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### ABSOLUTE MAXIMUM RATINGS <sup>(1)(2)</sup>

RFFE Supply Voltage (VIO)	-0.3V to 2.2V
Core Supply Voltage (VDD)	-0.3V to 2.2V
GPO Supply Voltage (VDDIO)	-0.3V to 4.0V
DC Input Voltage for SCLK & SDATA pins	-0.3V to (VIO+0.3V)
DC Input Voltage for ADR & CFG pins	-0.3V to (VDD+0.3V)
DC Output Voltage for GPO pins	-0.3V to (VDDIO+0.3V)
Storage Temperature Range	-40°C to +125°C
Operating Ambient Temperature (TA)	-0°C to +85°C
Lead Temperature (TL) (Soldering, 10 sec.)	260°C
ESD Rating (CZAP=120 pF, RZAP=1500Ω)	
Human Body Model <sup>(3)</sup>	1000V
Charge Device Model:	250V

- Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

### OPERATING RATINGS

	Min	Max	Unit
RFFE Supply Voltage (VIO)	1.65	1.95	V
RFFE Supply Noise (VIO)		25	mVpp
Core Supply Voltage (VDD)	1.65	1.95	V
Core Supply Noise (VDD)		25	mVpp
GPO Supply Voltage (VDDIO)	1.65	3.60	V
GPO Supply Noise (VDDIO)		50	mVpp

### DC ELECTRICAL CHARACTERISTICS: GENERAL (ADR, CFG)<sup>(1)(2)</sup>

T<sub>A</sub>: -30°C to +85°C, VIO = 1.8V ± 0.15V, VDD = 1.8V ± 0.15V, VDDIO = 3.3V ± 0.3V (unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V <sub>IH</sub>	Minimum high-level input voltage (ADR, CFG)		0.7 * V <sub>DD</sub>		V <sub>DD</sub> + 0.2	V
V <sub>IL</sub>	Maximum low-level input voltage (ADR, CFG)		-0.2		0.3 * V <sub>DD</sub>	
I <sub>IH</sub>	Logic high-level input current (ADR, CFG)	V <sub>IN</sub> = V <sub>DD</sub>			2	μA
I <sub>IL</sub>	Logic low-level input current (ADR, CFG)	V <sub>IN</sub> = GND	-2			

- All voltages are with respect to the GND pin.
- Min and Max Limits are verified by design, test, or statistical analysis. Typical (Typ.) numbers are not specified, but do represent the most likely norm. Unless otherwise specified conditions for typical specifications are: V<sub>DD</sub> = 1.8V, V<sub>DDIO</sub> = 3.3V, VIO = 1.8V, T<sub>A</sub> = +25°C.

**DC ELECTRICAL CHARACTERISTICS: GPO (GPO\_X, VDD, VDDIO)<sup>(1)(2)</sup>**

T<sub>A</sub>: -30°C to +85°C, V<sub>IO</sub> = 1.8V ± 0.15V, V<sub>DD</sub> = 1.8V ± 0.15V; V<sub>DDIO</sub> = 3.3V ± 0.3V (unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V <sub>OH</sub>	Minimum high-level output voltage	I <sub>OH</sub> = -12 mA (V <sub>DDIO</sub> = 3.3V ± 0.3V)	0.7 * V <sub>DDIO</sub>			V
		I <sub>OH</sub> = -4 mA (V <sub>DDIO</sub> = 1.8V ± 0.15V)				
		I <sub>OH</sub> = -10 μA	V <sub>DDIO</sub> - 0.2			
V <sub>OL</sub>	Maximum low-level output voltage	I <sub>OL</sub> = 12 mA (V <sub>DDIO</sub> = 3.3V ± 0.3V)			0.4	V
		I <sub>OL</sub> = 4 mA (V <sub>DDIO</sub> = 1.8V ± 0.15V)			0.4	
		I <sub>OL</sub> = 10 μA			0.2	
I <sub>OH</sub>	Logic high-level output current	(V <sub>DDIO</sub> = 3.3V ± 0.3V)	-12			mA
		(V <sub>DDIO</sub> = 1.8V ± 0.15V)	-4			
I <sub>OL</sub>	Logic low-level output current	(V <sub>DDIO</sub> = 3.3V ± 0.3V)			12	mA
		(V <sub>DDIO</sub> = 1.8V ± 0.15V)			4	
I <sub>OZ</sub>	High-Z leakage current	0 < V <sub>FIN</sub> < V <sub>DDIO</sub>	-2		2	μA
I <sub>PU</sub>	Pull-Up current	(V <sub>DDIO</sub> = 3.3V ± 0.3V)	-60		-200	μA
		(V <sub>DDIO</sub> = 1.8V ± 0.15V)	-9		-60	
I <sub>PD</sub>	Pull-Down current	(V <sub>DDIO</sub> = 3.3V ± 0.3V)	60		200	μA
		(V <sub>DDIO</sub> = 1.8V ± 0.15V)	9		60	
I <sub>STBY</sub>	V <sub>DD</sub> supply standby current	T <sub>A</sub> = 25°C, V <sub>IO</sub> = 1.8V, V <sub>DD</sub> = 1.8V, V <sub>DDIO</sub> = 3.3V, GPO_X = high-z, PU & PD disabled SCLK = Low			2.5	μA
I <sub>STBYIO</sub>	V <sub>DDIO</sub> supply standby current				2.5	
I <sub>VDD</sub>	V <sub>DD</sub> supply current	T <sub>A</sub> = 25°C, V <sub>DD</sub> = 1.8V		225	400	μA
I <sub>VDDIO</sub>	V <sub>DDIO</sub> supply current	T <sub>A</sub> = 25°C V <sub>DDIO</sub> = 3.3V		200	450	

(1) All voltages are with respect to the GND pin.

(2) Min and Max Limits are verified by design, test, or statistical analysis. Typical (Typ.) numbers are not specified, but do represent the most likely norm. Unless otherwise specified conditions for typical specifications are: V<sub>DD</sub> = 1.8V, V<sub>DDIO</sub> = 3.3V, V<sub>IO</sub> = 1.8V, T<sub>A</sub> = +25°C.

**DC ELECTRICAL CHARACTERISTICS: RFFE (SCLK, SDATA, VIO)<sup>(1)(2)</sup>**

T<sub>A</sub>: -30°C to +85°C, V<sub>IO</sub> = 1.8V ± 0.15V, V<sub>DD</sub> = 1.8V ± 0.15V; V<sub>DDIO</sub> = 3.3V ± 0.3V (unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C <sub>IN</sub>	Input pin capacitance (SCLK, SDATA) <sup>(2)</sup>				2.5	pF
V <sub>TP</sub>	Positive edge threshold voltage (SCLK, SDATA)		0.4 * V <sub>IO</sub>		0.7 * V <sub>IO</sub>	V
V <sub>TN</sub>	Negative edge threshold voltage (SCLK, SDATA)		0.3 * V <sub>IO</sub>		0.6 * V <sub>IO</sub>	
V <sub>HYST</sub>	Input hysteresis voltage (SDATA)		0.1 * V <sub>IO</sub>		0.4 * V <sub>IO</sub>	
V <sub>IORST</sub>	RFFE I/O voltage reset voltage level	V <sub>IO</sub> toggled low			0.2	μA
I <sub>INVIO</sub>	Input current (VIO)	0 < V <sub>IO</sub> < 0.2V	-1		1	
I <sub>IN</sub>	Input current (SCLK, SDATA)	V <sub>IO</sub> = Max, 0.2 * V <sub>IO</sub> < V <sub>IN</sub> < 0.8 * V <sub>IO</sub>	-1		1	
I <sub>VIO</sub>	VIO supply input current	V <sub>IO</sub> = 1.8, RFFE write only mode			100	

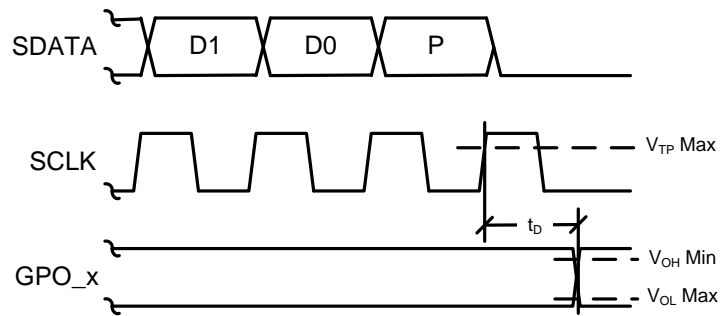
(1) All voltages are with respect to the GND pin.

(2) Min and Max Limits are verified by design, test, or statistical analysis. Typical (Typ.) numbers are not specified, but do represent the most likely norm. Unless otherwise specified conditions for typical specifications are: V<sub>DD</sub> = 1.8V, V<sub>DDIO</sub> = 3.3V, V<sub>IO</sub> = 1.8V, T<sub>A</sub> = +25°C.

**AC ELECTRICAL CHARACTERISTICS: INTERNAL POR, VIO, GPO\_X, SCLK<sup>(1)(2)</sup>**
 $T_A$ : -30°C to +85°C,  $V_{IO} = 1.8V \pm 0.15V$ ,  $V_{DD} = 1.8V \pm 0.15V$ ;  $V_{DDIO} = 3.3V \pm 0.3V$  (unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PORC1}$	VDD POR reset complete	$V_{DD}$ ramp rate = 100 $\mu$ S			1	mS
$t_{PORC2}$	VDDIO POR reset complete	$V_{DDIO}$ ramp rate = 100 $\mu$ S			1	
$t_{READY}$	VIO input signal reset delay time	$V_{IO} = 1.65V$ , SCLK, SDATA = Low, $t_{PORC1}$ , $t_{PORC2}$ = complete			120	nS
$f_{SCLK}$	SCLK frequency		0.032		26	MHz
$t_D$	GPO_x output delay time	$V_{DDIO} = 1.8V \pm 0.15V$ , $C_{LOAD} = 10$ pf			25	nS

- (1) All voltages are with respect to the GND pin.  
 (2) Min and Max Limits are verified by design, test, or statistical analysis. Typical (Typ.) numbers are not specified, but do represent the most likely norm. Unless otherwise specified conditions for typical specifications are:  $V_{DD} = 1.8V$ ,  $V_{DDIO} = 3.3V$ ,  $V_{IO} = 1.8V$ ,  $T_A = +25^\circ C$ .


**Figure 3. GPO Delay Timing**

### MIPI RFFE INTERFACE

The LM8335 provides RFFE compatible slave access to the device specific and RFFE defined registers on a single master bidirectional serial bus interface. The LM8335 uses the three interface signals SCLK, SDATA, and VIO as defined in MIPI RFFE Version 1.10 – 26 July 2011. The VIO voltage supply provides power to the LM8335 RFFE Interface and doubles as an asynchronous enable and reset. Whenever VIO is low the SCLK and SDATA lines must be held low. When the VIO voltage is applied, the LM8335 enables the slave interface and resets the user defined slave registers to the default settings. The LM8335 enters the power down mode via the asynchronous VIO signal. The LM8335 does not support read access.

The LM8335 contains fewer than 28 user defined registers but supports the Extended Register Write Command to allow a burst write of configuration registers during initialization. Any write outside of the range from 0x00 to 0x1F will have no effect on device operation.

The LM8335 recognizes the broadcast Slave Identifier (SID) of 0000b and is configured internally with a Unique Slave Identifier (USID) and a Group Slave Identifier (GSID). The USID is set based on the state of the ADR pin and the GSID is set to 0000b. The USID may be reprogrammed via the RFFE Interface by performing the Register Write USID Command Sequence.

The LM8335 supports only the 1.8V VIO supply levels. The LM8335 utilizes a power-detect reset circuit that resets the RFFE interface and internal registers when VIO is removed.

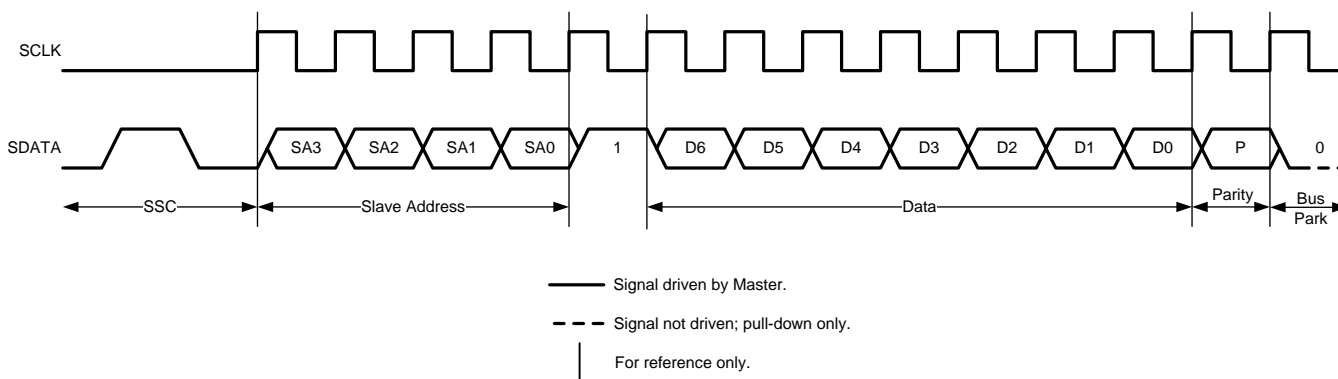


Figure 4. Register 0 Write Command Sequence

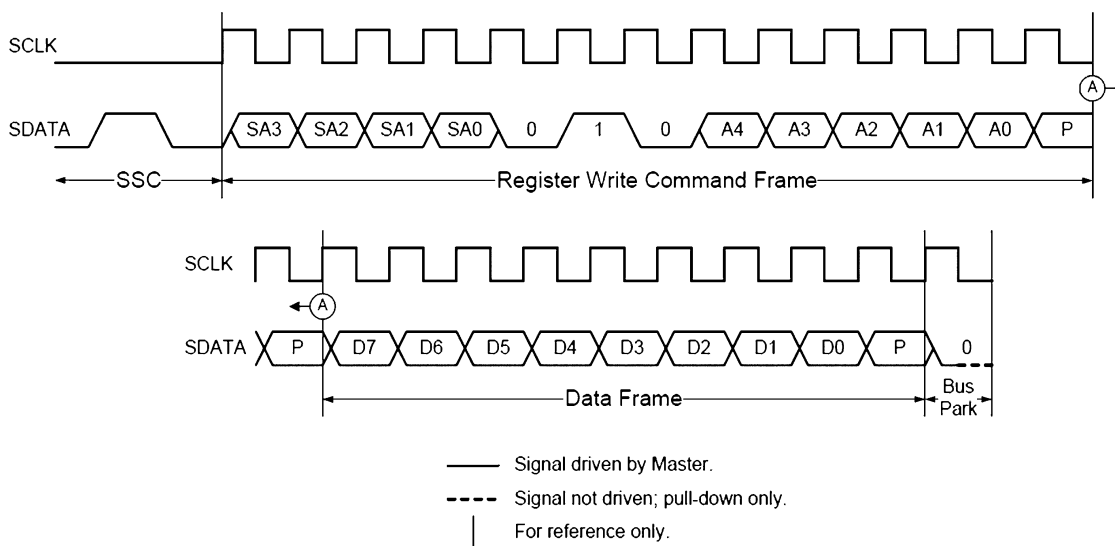


Figure 5. Register Write Command Sequence

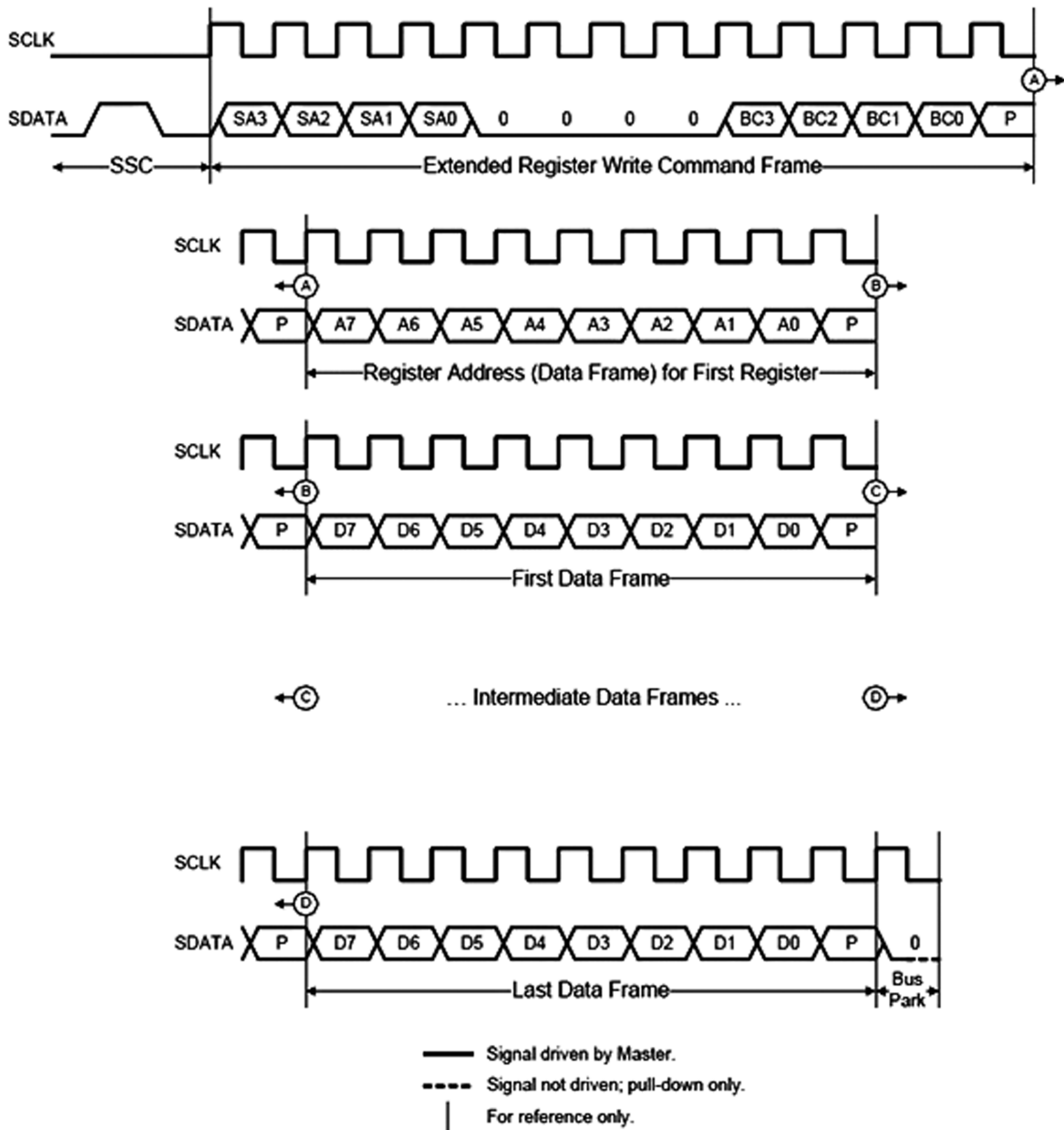


Figure 6. Extended Register Write Command Sequence

**INTERNAL POR OPERATION**

There are two internal POR circuits: one on the VDD supply and one on the VDDIO supply that initialize the LM8335 when power is applied. The duration of the reset is an RC delay which is based on the ramp rate and not a threshold voltage of the VDD/VDDIO supply. VIO can be activated as soon as VDD and VDDIO have reached their minimum respective voltage levels however the LM8335 may still be in reset due to the internal POR timing. When VIO is asserted after VDD and VDDIO  $t_{PORC}$  Max, the device reset will be released based on the VIO  $t_{READY}$  timing.

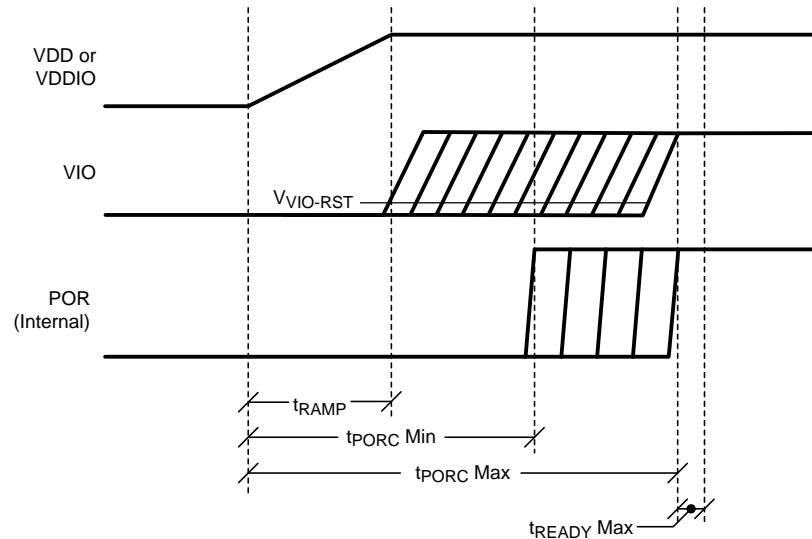


Figure 7. Internal VDD or VDDIO POR Timing

Register Information

Table 1. Register Listing

Register Name	Addr	Bit	Default	Description
CNTL_REG	0x00	7:0	0x00	Software reset register Bit 0 = 0, no effect Bit 0 = 1, reset registers to default values (self-clearing)
GPO_PULL_DIR	0x01	7:0	0x00	GPO pin pull resistor direction 0 = pull-down 1 = pull-up Note: When CFG = GND, writing to this register has no effect. The pull-down resistor will be disabled after the first write to the GPO_OUT_DATA register.
GPO_PULL_ENABLE	0x02	0xFF	0xFF	GPO pin internal pull resistor enable 0 = disabled 1 = enabled Note: GPO_PULL_DIR register selects if the resistor is a pull-up or a pull-down. When CFG = GND, writing to this register has no effect. The pull-down resistor will be disabled after the first write to the GPO_OUT_DATA register.
GPO_OUT_HIGH_CFG	0x03	7:0	0xFF	GPO output high state (full buffer or high-z). 0 = full buffer 1 = high-z (open-drain behavior) Note: When CFG = GND, writing to this register has no effect. The pull-down resistor will be disabled, and all GPO outputs will be in the actively driven state (not high-z) after the first write to the GPO_OUT_DATA register.

**Table 1. Register Listing (continued)**

Register Name	Addr	Bit	Default	Description
GPO_OUT_MASK	0x04	7:0	0xFF (CFG=0) or 0x00 (CFG=1)	GPO output data mask 0 = GPO_OUT_DATA masked 1 = GPO_OUT_DATA unmasked  Note: Only the GPO_OUT_DATA register write is affected by the GPO_OUT_MASK register. When the GPO_OUT_MASK bit is set low (masked), writing to GPO_OUT_DATA register will leave the pin state unchanged. When the GPO_OUT_MASK bit is set high (unmasked), the GPO output will be updated when the GPO_OUT_DATA is written (only GPOs that are unmasked will be changed).
GPO_OUT_DATA	0x05	7:0	0x00	GPO output data 0 = pin set low 1 = pin set high  Note: GPO_OUT_HIGH_CFG register selects if the pin is driven or high-z. The pin state will follow GPO_OUT_DATA only if the corresponding bit is unmasked in the GPO_OUT_MASK register.
PM_TRIG	0x1C	7:0	0x00	MIPI RFFE power mode and trigger register Bits 7:6 = PWR_MODE Bits 5:0 = TRIG_REG
PROD_ID	0x1D	7:0	0xC4	This is a MIPI RFFE reserved read only register and can not be read since readback is not supported on this device. Bits 7:0 = PRODUCT_ID [7:0]  The product ID is provided as information only to support the RFFE USID programming feature.
MAN_ID	0x1E	7:0	0x02	This is a MIPI RFFE reserved read-only register and can not be read since readback is not supported on this device. Bits 7:0 = MANUFACTURER_ID [7:0]  The manufacturer ID is provided as information only to support the RFFE USID programming feature.
USID_REG	0x1F	7:0	0x11 (ADR=0) or 0x19 (ADR=1)	This MIPI RFFE reserved register Bits 7:6 = SPARE Bits 5:4 = MANUFACTURER_ID [9:8] = 1 Bits 3:0 = Programmable Unique Slave Identifier — ADR=Low, USID[3:0]=0001 — ADR=High, USID[3:0]=1001  Note: The USID is initially set based on the state of the ADR pin (default value when ADR=Low shown). This register can not be read since readback is not supported on this device. USID_REG[5:4] are provided as information only to support the RFFE USID programming feature.

**Table 2. General Bit Field Layout for GPO\_x Registers**

7	6	5	4	3	2	1	0
GPO_7	GPO_6	GPO_5	GPO_4	GPO_3	GPO_2	GPO_1	GPO_0

**Table 3. CNTL\_REG Register Bit Fields**

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	rsvd	rsvd	rsvd	SW_RESET

LM8335 CFG Input Pin = VDD  
INITIALIZATION SEQUENCE

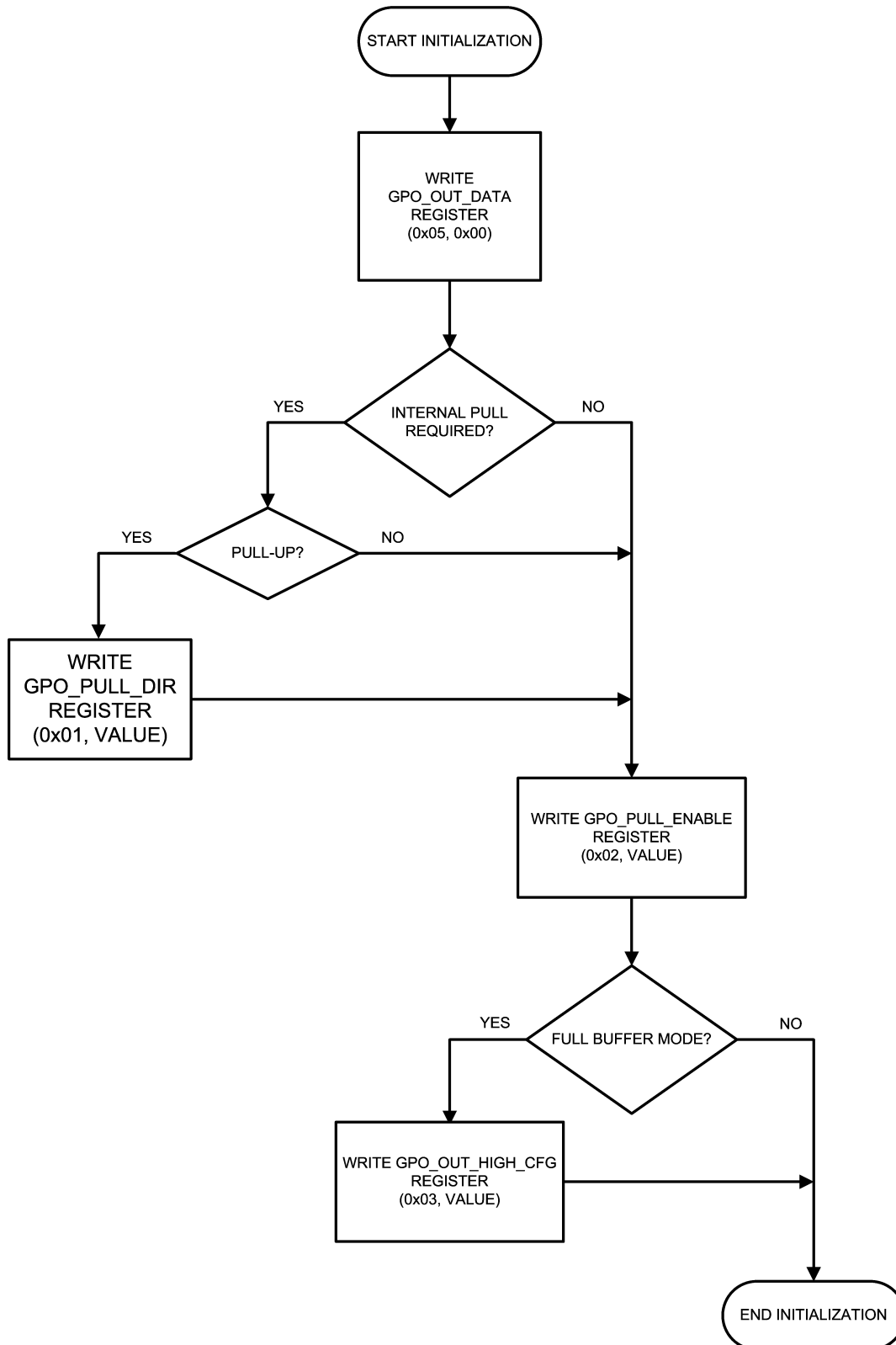


Figure 8. CFG1 MODE Recommended Initialization Sequence

## LM8335 UPDATE GPO PIN STATE

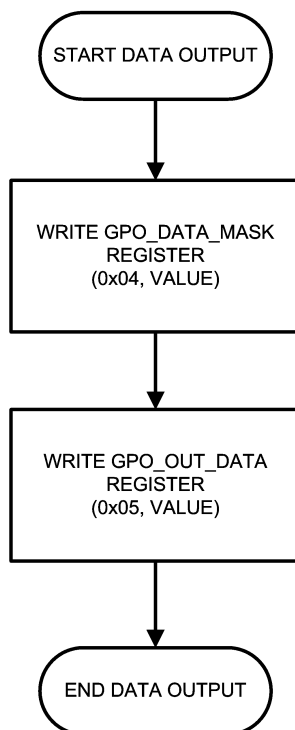


Figure 9. Update GPO Pin State Sequence

---

**REVISION HISTORY**

<b>Changes from Revision A (May 2013) to Revision B</b>	<b>Page</b>
<hr/> <ul style="list-style-type: none"><li>• Changed layout of National Data Sheet to TI format .....</li></ul>	<hr/> <b>14</b>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM8335TLE/NOPB	ACTIVE	DSBGA	YZR	16	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	8335	<a href="#">Samples</a>
LM8335TLX/NOPB	ACTIVE	DSBGA	YZR	16	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	8335	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

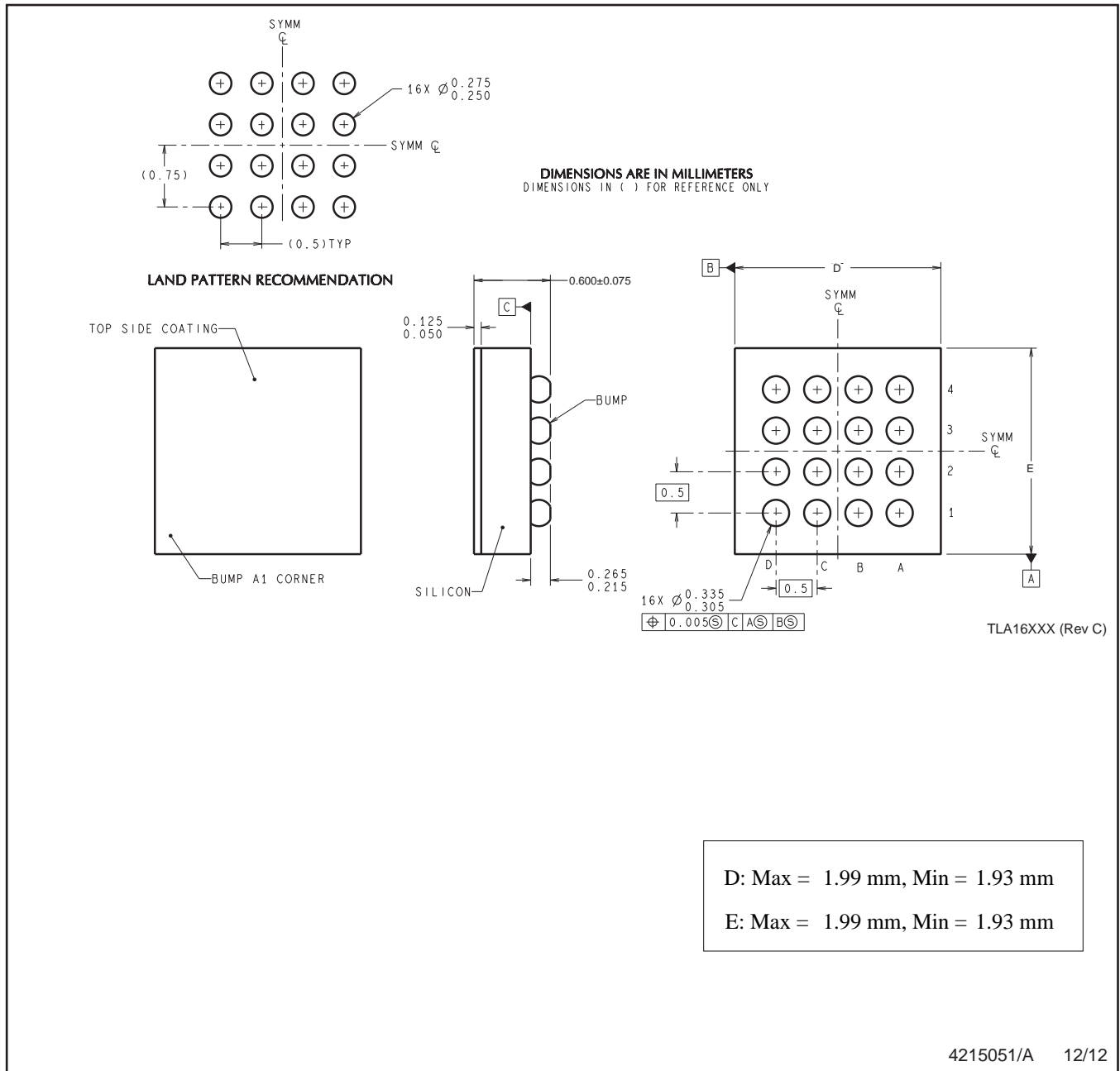
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM8335TLE/NOPB	DSBGA	YZR	16	250	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1
LM8335TLX/NOPB	DSBGA	YZR	16	3000	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM8335TLE/NOPB	DSBGA	YZR	16	250	210.0	185.0	35.0
LM8335TLX/NOPB	DSBGA	YZR	16	3000	210.0	185.0	35.0

YZR0016



D: Max = 1.99 mm, Min = 1.93 mm  
 E: Max = 1.99 mm, Min = 1.93 mm

4215051/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
 B. This drawing is subject to change without notice.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View LM8335EVM](#) on WIN SOURCE

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management