THE DATASHEET OF

LM4930ITLX/NOPB

LM4930 Boomer™ Audio Power Amplifier Series Audio Subsystem with Stereo Headphone & Mono Speaker Amplifiers

Check for Samples: LM4930

FEATURES

- **16-bit Resolution 48kHz Stereo DAC**
- **16-bit Resolution 8kHz Voice Codec**
- **I^2S Digital Audio Data Serial Interface**
- **Two-wire Serial Control Interface**
- **PCM Voice Audio Data Serial Interface**
- **25mW/channel Stereo Headphone Amplifier**
- **330mW Mono 8Ω Amplifier (at AV_{DD} = 3.0V)**
- **32-step Volume Control for Audio Output Amplifiers**
- **No Snubber Networks or Bootstrap Capacitors are Required by the Headphone or Hands-free Amplifiers**
- **Digital Sidetone Generation with Adjustable Attenuation**
- **Gain Controllable Headphone Amp, Mono BTL Amp, Mic Preamp**
- **Available in the 36–bump DSBGA and 44–lead WQFN Packages**

APPLICATIONS

- **Mobile Phones**
- **Mobile/low Power Audio Appliances**
- **PDAs**

KEY SPECIFICATIONS

- **PLS OUT at AV_{DD} = 5.0V, 8Ω 1% THD+N 1W (typ)**
- **PLS OUT at AV_{DD} = 3.0V, 8Ω 1% THD+N 330mW (typ)**
- **PH/P OUT at AV_{DD} = 3.0V, 32Ω 0.5% THD+N 25mW (typ)**
- **Supply Voltage Range**
  - **DV_{DD}(1) 2.6V to 4.5V**
  - **AV_{DD}(1) 2.6V to 5.5V**
- **Total Shutdown Current 2µA (typ)**
- **PSRR at 217Hz, AV_{DD} = 3V 50dB (typ)**

(1) Best operation is achieved by maintaining 3.0V ≤ AV_{DD} ≤ 5.0 and 3.0V ≤ DV_{DD} ≤ 3.6V. AV_{DD} must be equal to or greater than DV_{DD}. for proper operation.

DESCRIPTION

The LM4930 is an integrated audio subsystem that supports voice and digital audio functions. The LM4930 includes a high quality I^2S input stereo DAC, a voice band codec, a stereo headphone amplifier and a high-power mono speaker amplifier. It is primarily designed for demanding applications in mobile phones and other portable devices.

The LM4930 features an I^2S serial interface for full range audio, a 16-bit PCM bi-directional serial interface for the voice band codec and an two-wire interface for control. The full range music path features an SNR of 86dB with a 16-bit 48kHz input. The stereo DAC can also be used while the voice codec is in use. The headphone amplifier delivers $25mW_{RMS}$ to a 32Ω single-ended stereo load with less than 0.5% distortion (THD+N) when AV_{DD} = 3V. The mono speaker amplifier delivers up to 330mW into an 8Ω load with less than 1% distortion when AV_{DD} = 3V.

The LM4930 employs advanced techniques to reduce power consumption, to reduce controller overhead and to eliminate click and pop. Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. It is, therefore, ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

Typical Application

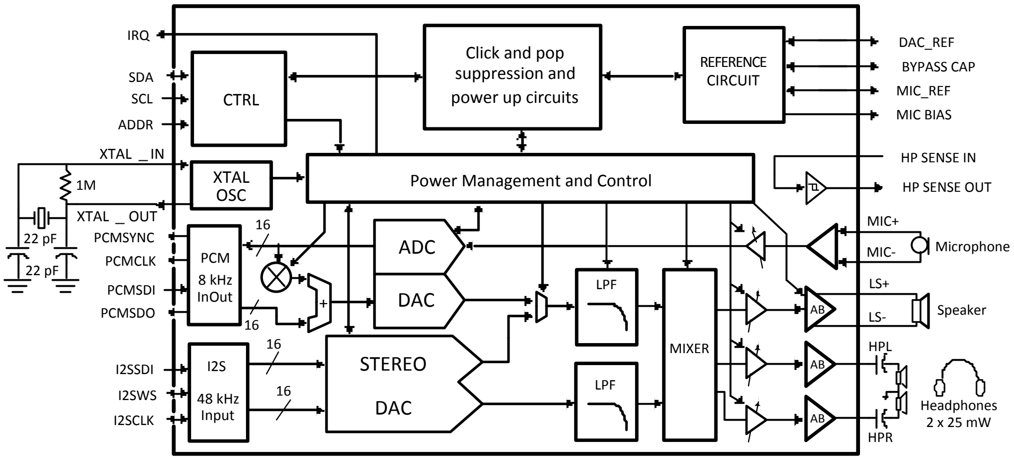

Figure 1. Typical I^{2}S + Voice Codec Application Circuit for Mobile Phones

Connection Diagrams

Top View

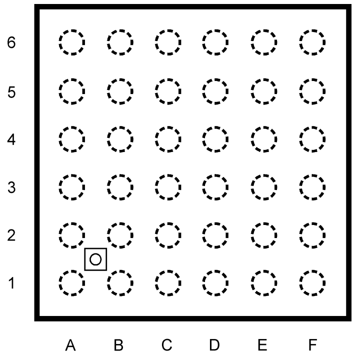

Figure 2. 36 - Bump DSBGA Package
See Package Number YZR0036KRA

Top View

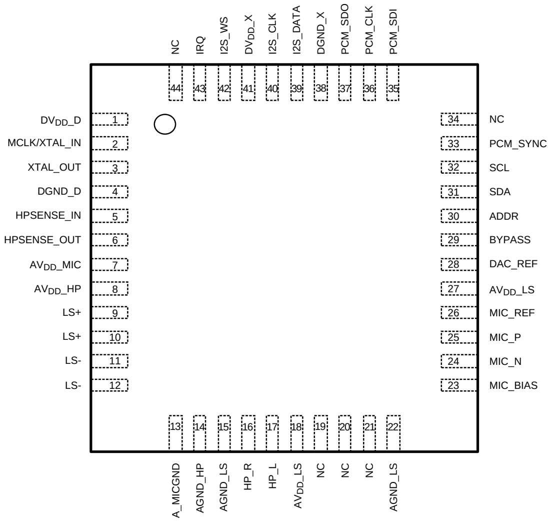

Figure 3. 44 - Lead WQFN Package
See Package Number NJN0044A

Pin Descriptions

Pin No.	Pin Name	Description
A1	MIC_P	Microphone positive differential input
A2	MIC_N	Microphone negative differential input
A3	AVDD_MIC	Analog V_{dd} for microphone preamp
A4	DAC_REF	D/A converter reference voltage
A5	SDA	Two-wire control interface serial data pin
A6	SCL	Two-wire control interface serial clock pin
B1	AGND_MIC	Analog ground for microphone preamp
B2	MIC_BIAS	Microphone bias supply output (2V)
B3	MIC_REF	Internal fixed-reference bypass capacitor decoupling pin
B4	ADDR	Control bus address select pin
B5	PCM_SDI	PCM serial data in
B6	PCM_CLK	PCM Serial clock pin
C1	AVDD_HP	Analog V_{dd} for headphone amplifier
C2	NC	No Connect
C3	BYPASS	Half-supply bypass capacitor decoupling pin
C4	PCM_SYNC	PCM Frame sync pin
C5	I2S_DATA	I^2S serial data input
C6	DGND_D	Digital ground
D1	HP_L	Headphone amplifier connection (Left)
D2	HP_R	Headphone amplifier connection (Right)
D3	HPSENSE_IN	Connection for sense pin of headphone jack
D4	PCM_SDO	PCM serial data out
D5	I2S_CLK	I^2S serial bit clock
D6	DVDD_D	Digital V_{dd}
E1	AGND_HP	Analog ground for headphone amplifier
E2	LS-	Loudspeaker amplifier BTL negative out (-)
E3	HPSENSE_OUT	Logic output pin to indicate headphone connection status. Outputs logic high when HPSENSE_IN is high and outputs logic low when HPSENSE_IN is low. See Figure 50 for suggested application circuit
E4	IRQ	LM4930 mode status indicator pin
E5	I2S_WS	I^2S word select
E6	XTAL_OUT	Negative feedback source for external crystal MCLK
F1	AGND_LS	Analog ground for loudspeaker amplifier
F2	LS+	Loudspeaker amplifier BTL positive out (+)
F3	AVDD_LS	Analog V_{DD} for loudspeaker amplifier
F4	DGND_X	Digital ground
F5	DVDD_X	Digital V_{DD}
F6	MCLK/XTAL_IN	12.288MHz or 24.576MHz Master Clock from crystal (via XTAL OUT) or external source

System Control Registers

The LM4930 is controlled with a two-wire serial interface. This interface is used to configure the operating mode, digital interfaces, and delta-sigma modulators. The LM4930 is controlled by writing information into a series of write-only registers, each with its own unique 7 bit address. The following registers are programmable:

Table 1. BASIC CONFIGURATION Registers(1)

<table>
<tr><td colspan="17">BASIC CONFIGURATION (XX1000). (Set = logic 1, Clear = logic 0)</td></tr>
<tr><td>BIT</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESET</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>

<table>
<tr><th>Address</th><th>Register</th><th colspan="5">Description</th></tr>
<tr><td rowspan="13">3:0</td><td rowspan="13">MODE</td><td colspan="5">The LM4930 can be placed in one of several modes that dictate the basic operation. When a new mode is selected the LM4930 will change operation silently and will re-configure the power management profile automatically. The modes are described as follows:(2)</td></tr>
<tr><td>Mode</td><td>Mono Speaker Amplifier Source</td><td>Headphone Left Source</td><td>Headphone Right Source</td><td>Comment</td></tr>
<tr><td>0000</td><td>None</td><td>None</td><td>None</td><td>Powerdown mode</td></tr>
<tr><td>0001</td><td>None</td><td>None</td><td>None</td><td>Standby mode</td></tr>
<tr><td>0010</td><td>Voice</td><td>None</td><td>None</td><td>Mono speaker mode</td></tr>
<tr><td>0011</td><td>None</td><td>Voice</td><td>Voice</td><td>Headphone call mode</td></tr>
<tr><td>0100</td><td>Voice</td><td>Voice</td><td>Voice</td><td>Conference call mode</td></tr>
<tr><td>0101</td><td>Audio (L+R)</td><td>None</td><td>None</td><td>L+R mixed to mono speaker</td></tr>
<tr><td>0110</td><td>None</td><td>Audio (Left)</td><td>Audio (Right)</td><td>Headphone stereo audio</td></tr>
<tr><td>0111</td><td>Audio (L+R)</td><td>Audio (Left)</td><td>Audio (Right)</td><td>L+R mixed to mono speaker + stereo headphone audio</td></tr>
<tr><td>1000</td><td>Audio (Left)</td><td>Voice</td><td>Voice</td><td>Mixed Mode</td></tr>
<tr><td>1001</td><td>Voice + Audio (Left)</td><td>Voice</td><td>Voice</td><td>Mixed mode</td></tr>
<tr><td>1010</td><td>Voice</td><td>Audio (Left)</td><td>Audio (Left)</td><td>Mixed Mode</td></tr>
<tr><td>4</td><td>SOFT_RESET</td><td colspan="5">Resets the LM4930, excluding the control registers</td></tr>
<tr><td>5</td><td>PCM_LONG</td><td colspan="5">If set the PCM interface uses a long frame sync.(3)</td></tr>
<tr><td>6</td><td>PCM_COMPANDED</td><td colspan="5">If set the 8 MSBs are presumed to be companded data and the 8 LSBs are ignored.(3)</td></tr>
<tr><td>7</td><td>PCM_LAW</td><td colspan="5">If set, the companded G711 data is set to be A-law, else µ-law is assumed(3)</td></tr>
<tr><td>8:9</td><td>PCM_SYNC_MODE</td><td colspan="5">Sets 1 (00h), 2 (01h) or 4(10h) 16 bit frames per sync. The PCM_SDO pin is tri-stated during the latter frames.(3)</td></tr>
<tr><td>10</td><td>PCM_ALWAYS_ON</td><td colspan="5">This bit should be set if another codec is using the PCM bus. When set, the LM4930 will drive the clock and sync signals in all modes except Powerdown(3)</td></tr>
<tr><td>11</td><td>I2S_M/S</td><td colspan="5">I2S master or slave select. If set then I2S = master. Cleared = slave</td></tr>
<tr><td>12</td><td>I2S_RES</td><td colspan="5">I2S resolution select. If set then 32 bits per frame. If cleared then 16 bits per frame</td></tr>
<tr><td>13</td><td>RSVD</td><td colspan="5">RESERVED(4)</td></tr>
<tr><td>14</td><td>RSVD</td><td colspan="5">RESERVED(4)</td></tr>
<tr><td>15</td><td>RSVD</td><td colspan="5">RESERVED(4)</td></tr>
</table>

(1) This register is used to configure the I2S and PCM interfaces as well as the 48kHz DAC module. The 7 bit address for the BASICCONFIG register is XX10000.
(X = 0 if ADDR is set to logic 0)
(X = 1 if ADDR is set to logic 1)

(2) With the exception of Standby Mode, rapid switching between modes should be avoided. Rapid switching between modes will not ensure that the desired mode will be activated.

(3) It is recommended to alter this bit only while the part is in Powerdown Mode.

(4) Reserved bits should be set to zero when programming the associated register.

Table 2. VOICE/TEST CONFIG Registers[1]

VOICETESTCONFIG (XX10001). (Set = logic 1, Clear = logic 0)																
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<table>
<tr><th>Address</th><th>Register</th><th>Description</th></tr>
<tr><td>0</td><td>CLASS</td><td>If set, configures the chip for use with an external class D or linear amplifier and turns the BTL speaker output into a buffer.[2]</td></tr>
<tr><td>4:1</td><td>SIDESTONE_ATTEN</td><td>Programs the attenuation of the digital sidetone. Attenuation is set as follows:
<table>
<tr><th>4:1</th><th>Sidetone Attenuation</th><th>4:1</th><th>Sidetone Attenuation</th></tr>
<tr><td>0000</td><td>Mute</td><td>1000</td><td>-9dB</td></tr>
<tr><td>0001</td><td>-30dB</td><td>1001</td><td>-6dB</td></tr>
<tr><td>0010</td><td>-27dB</td><td>1010</td><td>-3dB</td></tr>
<tr><td>0011</td><td>-24dB</td><td>1011</td><td>0dB</td></tr>
<tr><td>0100</td><td>-21dB</td><td>1100</td><td>Mute</td></tr>
<tr><td>0101</td><td>-18dB</td><td>1101</td><td>Mute</td></tr>
<tr><td>0110</td><td>-15dB</td><td>1110</td><td>Mute</td></tr>
<tr><td>0111</td><td>-12dB</td><td>1111</td><td>Mute</td></tr>
</table></td></tr>
<tr><td>5</td><td>AUTOSIDE</td><td>This feature is included for use with the mono speaker in hands-free applications where sidetones may not be desirable. If set, the sidetone is always muted in modes when voice is played on the mono speaker (0010, 0100, 1001, and 1010), otherwise the sidetone is present at whatever level is set in the attenuation conrol register</td></tr>
<tr><td>6</td><td>CLOCK_DIV</td><td>If set, allows for the use of a 24.576MHz crystal. Default setting is for 12.288MHz crystal.[2]</td></tr>
<tr><td>7</td><td>ZXD_DISABLE</td><td>Disables the zero crossing detect in the stereo DAC to ensure immediate mode changes rather than waiting for a zero cross.[3]</td></tr>
<tr><td>8:9</td><td>RSVD</td><td>RESERVED[4]</td></tr>
<tr><td>10:11</td><td>CAP_SIZE</td><td>Set to accomodate different bypass capacitor values to give correct turn-off delay and click/pop performance. Value is set as follows:[2]
<table>
<tr><th>10:11</th><th>Delay</th><th>Bypass Capacitor Size</th></tr>
<tr><td>00</td><td>25ms</td><td>0.1µF</td></tr>
<tr><td>01</td><td>50ms</td><td>0.39µF</td></tr>
<tr><td>10</td><td>85ms</td><td>1µF</td></tr>
<tr><td>11</td><td>RESERVED</td><td>RESERVED</td></tr>
</table></td></tr>
<tr><td>12</td><td>ZXDS_SLOW</td><td>If set, this forces the stereo DAC outputs to wait for a zero crossing before powering down</td></tr>
<tr><td>13</td><td>MUTE_LS</td><td>If set, mutes the loudspeaker amplifier in any mode where it is not already muted</td></tr>
<tr><td>14</td><td>MUTE_HP</td><td>If set, mutes the headphone amplifier in any mode where it is not already muted</td></tr>
<tr><td>15</td><td>MUTE_MIC</td><td>If set, mutes the microphone preamp</td></tr>
</table>

(1) This register configures the voiceband codec, sidetone attenuation, and selected control functions. The 7 bit address for the VOICE TESTCONFIG register is XX10001.
(X = 0 if ADDR is set to logic 0)
(X = 1 if ADDR is set to logic 1)
(2) It is recommended to alter this bit only while the part is in Powerdown Mode.
(3) To ensure a successful transistion into Powerdown Mode, ZXD_DISABLE must be set whenever there is no audio input signal present.
(4) Reserved bits should be set to zero when programming the associated register.

Table 3. GAIN CONFIG Registers(1)

GAINCONFIG (XX10010). (Set = logic 1, Clear = logic 0)																
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address	**Register**	**Description**			
4:0	LOUDSPKR_GAIN	Programs the gain of the loudspeaker amplifier. Gain is set as follows:			
		4:0	**Loudspeaker Gain**	**4:0**	**Loudspeaker Gain**
		00000	-34.5dB	10000	-10.5dB
		00001	-33dB	10001	-9dB
		00010	-31.5dB	10010	-7.5dB
		00011	-30dB	10011	-6dB
		00100	-28.5dB	10100	-4.5dB
		00101	-27dB	10101	-3dB
		00110	-25.5dB	10110	-1.5dB
		00111	-24dB	10111	0dB
		01000	-22.5dB	11000	1.5dB
		01001	-21dB	11001	3dB
		01010	-19.5dB	11010	4.5dB
		01011	-18dB	11011	6dB
		01100	-16.5dB	11100	7.5dB
		01101	-15dB	11101	9dB
		01110	-13.5dB	11110	10.5dB
		01111	-12dB	11111	12dB
9:5	HP_GAIN	Programs the gain of the headphone amplifier. Gain is set as follows:			
		9:5	**Headphone Gain**	**9:5**	**Headphone Gain**
		00000	-46dB	10000	-22.5dB
		00001	-45dB	10001	-21dB
		00010	-43.5dB	10010	-19.5dB
		00011	-42db	10011	-18dB
		00100	-40.5dB	10100	-16.5dB
		00101	-39dB	10101	-15dB
		00110	-37.5dB	10110	-13.5dB
		00111	-36dB	10111	-12dB
		01000	-34.5dB	11000	-10.5dB
		01001	-33dB	11001	-9dB
		01010	-31.5dB	11010	-7.5dB
		01011	-30dB	11011	-6dB
		01100	-28.5dB	11100	-4.5dB
		01101	-27dB	11101	-3dB
		01110	-25.5dB	11110	-1.5dB
		01111	-24dB	11111	0dB
13:10	MIC_GAIN	Programs the gain of the microphone amplifier. Gain is set as follows:			

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(1) This register is used to control the gain of the headphone amplifier, the loudspeaker amplifier, and the microphone preamplifier. The 7 bit address for the GAINCONFIG register is XX10010.
(X = 0 if ADDR is set to logic 0)
(X = 1 if ADDR is set to logic 1)

Table 3. GAIN CONFIG Registers[1] (continued)

		13:10	**Mic Preamp Gain**
		0000	17dB
		0001	19dB
		0010	21dB
		0011	23dB
		0100	25dB
		0101	27dB
		0110	29dB
		0111	31dB
		1000	33dB
		1001	35dB
		1010	37dB
		1011	39dB
		1100	41dB
		1101	43dB
		1110	45dB
		1111	47dB
15:14	RSVD	RESERVED[2]	

(2) Reserved bits should be set to zero when programming the associated register.

Timing Diagrams

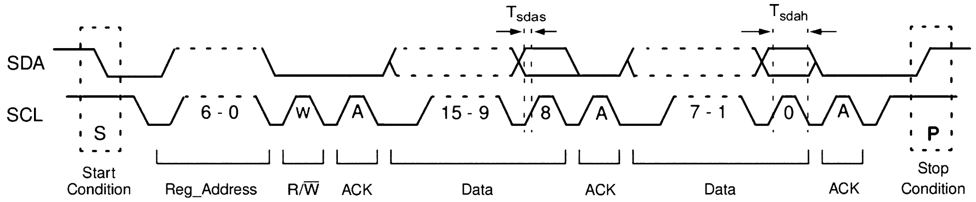

Figure 4. Two-Wire Control Interface Timing Diagram

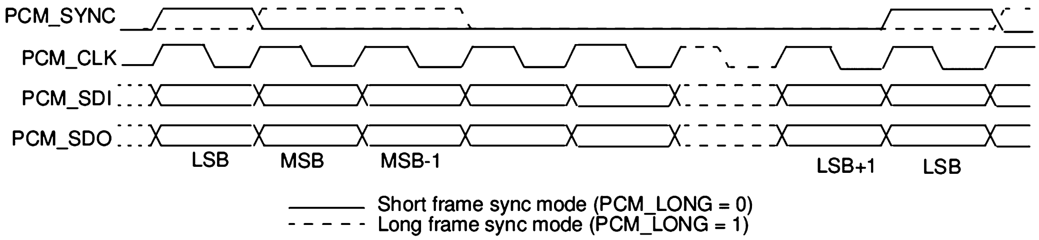

Figure 5. PCM Receive Timing Diagram

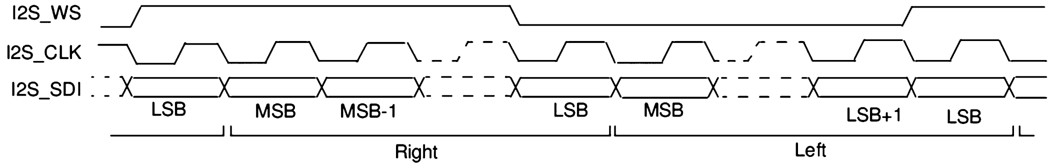

Figure 6. I²S Transmit Timing Diagram

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

Analog Supply Voltage		6.0V
Digital Storage Supply Voltage		6.0V
Storage temperature		-65°C to +150°C
Power Dissipation(4)		Internally Limited
ESD Susceptibility	Human Body Model(5)	2000V
	Machine Model(6)	200V
Junction temperature		150°C
Thermal Resistance	θ_{JA} - YZR0036KRA	105°C/W
	θ_{JA} - NJN0044A(7)	27°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which specifies specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.

(2) All voltages are measured with respect to the relevant GND pin unless otherwise specified.

(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} ,θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} – T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4930, see power derating currents for more information.

(5) Human body model: 100pF discharged through a 1.5kΩ resistor.

(6) Machine model: 220pF - 240pF discharged through all pins.

(7) The given θ_A is for an LM4930 packaged in an NJN0044A with the Exposed-DAP soldered to an exposed 2in^2 area of 1oz printed circuit board copper with 16 thermal vias as described in AN-1187.

Operating Ratings(1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	$-30°C \le T_A \le +85°C$
Supply Voltage	DV_{DD}(2)	2.6V - 4.5V
	AV_{DD}(2)	2.6V - 5.5V

(1) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} ,θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} – T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4930, see power derating currents for more information.

(2) Best operation is achieved by maintaining $3.0V \le AV_{DD} \le 5.0$ and $3.0V \le DV_{DD} \le 3.6V$. AV_{DD} must be equal to or greater than DV_{DD}. for proper operation.

Electrical Characteristics DV_{DD} = 3.3V, AV_{DD} = 5V, R_{LHP} = 32Ω, R_{LHF} = 8Ω(1)(2)(3)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A= 25°C.

Parameter		Test Conditions	LM4930		Units (Limits)
			Typ(4)	Limits(5)(6)	
DI_{DD}	Digital Power Supply Current	f_{MCLK} = 12.288MHz			
		Output Mode = "0010" Output Mode = "0011" Output Mode = "0100"	2		
		Output Mode = "0101" Output Mode = "0110" Output Mode = "0111"	4.4		
		Output Mode = "1000" Output Mode = "1001" Output Mode = "1010"	4.9	8	mA (max)
AI_{DD}	Analog Power Supply Quiescent Current	f_{MCLK} = 12.288MHz; No Load			
		Output Mode = "0010"	7.0		
		Output Mode = "0011"	6.3		
		Output Mode = "0100"	8.0		
		Output Mode = "0101"	8.2		
		Output Mode = "0110"	7.4		
		Output Mode = "0111"	8.7		
		Output Mode = "1000" Output Mode = "1001" Output Mode = "1010"	9.5	14	mA (max)
DI_{SD}	Digital Powerdown Current	f_{MCLK} = 12.288MHz Output Mode = "0000" Powerdown Mode	1	7	µA (max)
AI_{SD}	Analog Powerdown Current	f_{MCLK} = 12.288MHz Output Mode = "0000" Powerdown Mode	1	2	µA (max)
DI_{ST}	Digital Standby Current	f_{MCLK} = 12.288MHz Output Mode = "0001" Standby Mode	1.4	2	mA (max)
AI_{ST}	Analog Standby Current	f_{MCLK} = 12.288MHz Output Mode = "0001" Standby Mode	230	1000	µA (max)
V_{FS_LS}	Full-Scale Output Voltage (Mono speaker amplifier)	CLASS = 0; 0dB gain setting; 8Ω BTL load(7)	2.5		V_{P-P}
V_{FS_HP}	Full-Scale Output Voltage (Headphone amplifier)	0dB gain setting; 32Ω Stereo Load(7)	2.5		V_{P-P}
V_{MIC_BIAS}	Mic Bias Voltage		2.0		V
THD+N	Headphone Amplifier Total Harmonic Motion Distortion + Noise	f_{IN} = 1 kHz, P_{OUT} = 7.5mW; 32Ω Stereo Load	0.07		%
P_{OHP}	Headphone Amplifier Output Power	THD+N = 0.5%, f_{OUT} = 1kHz	27	20	mW (min)
P_{OLS}	Mono Speaker Amplifier Output Power	THD+N = 1%, f_{OUT} = 1kHz	1		W
PSRR	Power Supply Rejection Ratio	C_{BYPASS} = 1.0µF C_{DAC_REF} = 1.0µF V_{RIPPLE} = 200mV_{P-P} @ 217Hz, MIC_P, MIC_N terminated with 10Ω to ground	55	45	dB (min)

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(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which specifies specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.

(2) All voltages are measured with respect to the relevant GND pin unless otherwise specified.

(3) Best operation is achieved by maintaining 3.0V ≤ AV_{DD} ≤ 5.0 and 3.0V ≤ DV_{DD} ≤ 3.6V. AV_{DD} must be equal to or greater than DV_{DD}. for proper operation.

(4) Typicals are measured at 25°C and represent the parametric norm.

(5) Limits are specified to Texas Instrument's AOQL (Average Outgoing Quality Level).

(6) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.

(7) This value represents the 0dB output level of the given amplifier for the given analog supply voltage. Gain values given in the GAINCONFIG register are relative to these full-scale values for each output amplifier.

Electrical Characteristics DV_{DD} = 3.3V, AV_{DD} = 5V, R_{LHP} = 32Ω, R_{LHF} = 8Ω[1][2][3] (continued)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A= 25°C.

Parameter		Test Conditions	LM4930		Units (Limits)
			Typ[4]	Limits[5][6]	
SNR (Voice)	Signal-to-Noise Ratio (Voice DAC Path)	Signal = Vo at f = 1kHz @1% THD+N, 32Ω Stereo Load; Noise = digital zero, A-weighted, 0dB gain setting	72		dB
SNR (Music)	Signal-to-Noise Ratio (Music Audio Path)	Signal = Vo at f = 1kHz @1% THD+N, 32Ω Stereo Load; Noise = digital zero, A-weighted; 0dB gain setting	86		dB
DR (Voice)	Dynamic Range (Voice DAC Path)	Signal = Vo at f = 1kHz @1% THD+N, 32Ω Stereo Load; Noise for -60dBFS digital input; A-weighted; 0dB gain setting	72		dB
DR (Music)	Dynamic Range (Music Audio Path)	Signal = Vo at f=1kHz @1% THD+N, 32Ω Stereo Load; Noise for -60dBFS digital input; A-weighted, 0dB gain setting	86		dB
SNR_{ADC}	Signal-to-Noise Ratio (Voice ADC Path)	Reference signal = 0dBFS MIC_P, MIC_N terminated with 10Ω to ground; A-weighted; 47dB MIC preamp gain setting	75		dB
DR_{ADC}	Dynamic Range (Voice ADC Path)	Reference signal = 0dBFS Noise for -60dBFS digital input; A-weighted; 47dB MIC preamp gain setting	75		dB
X_{TALK}	Stereo Channel-to-Channel Crosstalk	f_S = 48kHz, f_{IN} = 1kHz sinewave at -3dB_{FS}	75		dB
V_{MIC-IN}	Maximum Differential MIC Input Voltage	17dB MIC Preamp gain setting	570		mV_{P-P}
R_{VDAC}	Voice DAC Ripple	300Hz - 3.3kHz through head-phone output.	+/-0.15	+/-0.2	dB (max)
R_{VADC}	Voice ADC Ripple	300Hz - 3.3kHz through head-phone output.	+/-0.25	+/-0.3	dB (max)
PB_{VDAC}	Voice DAC Passband	-3dB Point	3.46		kHz
SBA_{VDAC}	Voice DAC Stopband Attenuation	Above 4kHz	72		dB
UPB_{VADC}	Voice ADC Upper Passband Cutoff Frequency.	Upper -3dB Point	3.47		kHz
LPB_{VADC}	Voice ADC Lower Passband Cutoff Frequency.	Lower -3dB Point	0.230		kHz
SBA_{VADC}	Voice ADC Stopband Attenuation	Above 4kHz	65		dB
SBA_{NOTCH}	Voice ADC Notch Attenuation	Centered on 55Hz, figure gives worst case attenuation for 50Hz & 60Hz.	58		dB
R_{DAC}	Audio DAC Ripple	20Hz - 20kHz through head-phone output.	+/-0.1	+/-0.2	dB (max)
PB_{DAC}	Audio DAC Passband Width	-3dB point	22.7		kHz
SBA_{DAC}	Audio DAC Stopband Attenuation	Above 24kHz	76		dB
DR_{DAC}	Audio DAC Dynamic Range Digital Filter Section	Signal = VO at f = 1kHz @ 1% THD+N; f = 1kHz; Noise for -60dBFS digital input; 0dB gain; A-weighted	97		dB
SNR_{DAC}	Audio DAC SNR Digital Filter Section	Signal = VO at f = 1kHz @ 1% THD+N; f = 1kHz; Noise for -60dBFS digital input; 0dB gain; A-weighted	97		dB
ΔA_{CH-CH}	Stereo Channel-to-Channel Gain Mismatch		0.3		dB
V_{IL}	Digital Input: Logic Low Voltage Level		0.4		V
V_{IH}	Digital Input: Logic High Voltage Level		1.4		V
	Volume Control Range (Headphone amplifiers)	Maximum Attenuation Minimum Attenuation	-46.5 0		dB dB
	Volume Control Range (Mono speaker amplifier)	Minimum Gain Maximum Gain	-34.5 12		dB dB

Electrical Characteristics DV_{DD} = 3.3V, AV_{DD} = 5V, R_{LHP} = 32Ω, R_{LHF} = 8Ω(1)(2)(3) (continued)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A= 25°C.

Parameter		Test Conditions	LM4930		Units (Limits)
			Typ[4]	Limits[5][6]	
	Volume Control Step Size (Output amplifiers)		1.5		dB
	Volume Control Range (Microphone Preamp)	Minimum Gain Maximum Gain	17 47		dB dB
	Volume Control Step Size (Microphone Preamp)		2		dB
	Side Tone Attenuation Range	Maximum Attenuation Minimum Attenuation	-30 0		dB dB
	Side Tone Attenuation Step Size		3		dB
f_{MCLK}	MCLK frequency	CLOCK_DIV = 0 CLOCK_DIV = 1	12.288 24.576		MHz MHz
	MCLK Duty Cycle		50	40 60	% (min) % (max)
f_{CONV}	Sampling Clock Frequency[8]		48		kHz
f_{CLKSCL}	SCL_CLK Frequency		400		kHz
$t_{RISESCL}$	SCL_CLK, SCL_DATA Rise Time		300		ns
$t_{FALLSCL}$	SCL_CLK, SDA_DATA Fall Time		300		ns
t_{SDAH}	SDA_DATA Hold Time		500		ns
t_{SDAS}	SDA_DATA Setup Time		500		ns
f_{CLKPCM}	PCM_CLK Frequency	PCM_SYNC_MODE = 00 PCM_SYNC_MODE = 01 PCM_SYNC_MODE = 10	128 256 512		kHz
	PCM_CLK Duty Cycle		50	40 60	% (min) % (max)
f_{CLKI2S}	I2S_CLK Frequency	I2S_RES = 0 I2S_RES = 1	1.536 3.072		MHz
	I2S_CLK Duty Cycle		50	40 60	% (min) % (max)

(8) The sampling clock frequency is equal to the master clock frequency divided by 256. (f_{conv} = f_{MCLK}/256)

Electrical Characteristics DV_{DD} = 3V, AV_{DD} = 3V, R_{LHP} = 32Ω, R_{LHF} = 8Ω(1)(2)(3)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A= 25°C.

Parameter		Test Conditions	LM4930		Units (Limits)
			Typ(4)	Limits(5)(6)	
DI_{DD}	Digital Power Supply Current	f_{MCLK} = 12.288MHz			
		Output Mode = "0010" Output Mode = "0011" Output Mode = "0100"	1.6		
		Output Mode = "0101" Output Mode = "0110" Output Mode = "0111"	3.8		
		Output Mode = "1000" Output Mode = "1001" Output Mode = "1010"	4.2	7	mA (max)
AI_{DD}	Analog Power Supply Quiescent Current	f_{MCLK} = 12.288MHz; No Load			
		Output Mode = "0010"	5.8		
		Output Mode = "0011"	5.1		
		Output Mode = "0100"	6.5		
		Output Mode = "0101"	6.4		
		Output Mode = "0110"	5.8		
		Output Mode = "0111"	7.0		
		Output Mode = "1000" Output Mode = "1001" Output Mode = "1010"	7.5	12	mA (max)
DI_{SD}	Digital Powerdown Current	f_{MCLK} = 12.288MHz Output Mode = "0000" Powerdown Mode	1	7	µA (max)
AI_{SD}	Analog Powerdown Current	f_{MCLK} = 12.288MHz Output Mode = "0000" Powerdown Mode	0.6	1.5	µA (max)
DI_{ST}	Digital Standby Current	f_{MCLK} = 12.288MHz Output Mode = "0001" Standby Mode	1.1	1.7	mA (max)
AI_{ST}	Analog Standby Current	f_{MCLK} = 12.288MHz Output Mode = "0001" Standby Mode	100	300	µA (max)
V_{FS_LS}	Full-Scale Output Voltage (Mono speaker amplifier)	CLASS = 0; 0dB gain setting; 8Ω BTL load(7)	2.5		V_{P-P}
V_{FS_HP}	Full-Scale Output Voltage (Headphone amplifier)	0dB gain setting; 32Ω Stereo Load(7)	2.5		V_{P-P}
V_{MIC_BIAS}	Mic Bias Voltage		2		V
THD+N	Headphone Amplifier Total Harmonic Distortion + Noise	f_{IN} = 1kHz, P_{OUT} = 7.5mW	0.07		%
P_{OHP}	Headphone Amplifier Output Power	THD+N = 0.5%, f_{OUT} = 1kHz	25	15	mW (min)
P_{OLS}	Mono Speaker Amplifier Output Power	THD+N = 1%, f_{OUT} = 1kHz	330	270	mW (min)
PSRR	Power Supply Rejection Ratio	C_{BYPASS} = 1.0µF C_{DAC_REF} = 1.0µF V_{RIPPLE} = 200mV_{P-P} @ 217Hz	50	42	dB (min)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which specifies specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the relevant GND pin unless otherwise specified.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} ,θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4930, see power derating currents for more information.
(4) Typicals are measured at 25°C and represent the parametric norm.
(5) Limits are specified to Texas Instrument’s AOQL (Average Outgoing Quality Level).
(6) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.
(7) This value represents the 0dB output level of the given amplifier for the given analog supply voltage. Gain values given in the GAINCONFIG register are relative to these full-scale values for each output amplifier.

Electrical Characteristics DV_{DD} = 3V, AV_{DD} = 3V, R_{LHP} = 32Ω, R_{LHF} = 8Ω[1][2][3] (continued)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A= 25°C.

Parameter		Test Conditions	LM4930		Units (Limits)
			Typ[4]	Limits[5][6]	
SNR (Voice)	Signal-to-Noise Ratio (Voice DAC Path)	Signal = Vo at f = 1kHz @1% THD+N, 32Ω Stereo Load; Noise = digital zero, A-weighted; 0dB gain setting	72		dB
SNR (Music)	Signal-to-Noise Ratio (Music Audio Path)	Signal = Vo at f = 1kHz @1% THD+N, 32Ω Stereo Load; Noise = digital zero, A-weighted; 0dB gain setting	86		dB
DR (Voice)	Dynamic Range (Voice DAC Path)	Signal = Vo at f = 1kHz @1% THD+N, 32Ω Stereo Load; Noise for -60dBFS digital input; A-weighted, 0dB gain setting	72		dB
DR (Music)	Dynamic Range (Music Audio Path)	Signal = Vo at f=1kHz @1% THD+N, 32Ω Stereo Load; Noise for -60dBFS digital input; A-weighted, 0dB gain setting	86		dB
SNR$_{ADC}$	Signal-to-Noise Ratio (Voice ADC Path)	Reference signal = 0dBFS MIC_P, MIC_N terminated with 10Ω to ground; A-weighted; 47dB MIC preamp gain setting	75		dB
DR$_{ADC}$	Dynamic Range (Voice ADC Path)	Reference signal = 0dBFS Noise for -60dBFS digital input; A-weighted; 47dB MIC preamp gain setting	75		dB
X$_{TALK}$	Stereo Channel-to-Channel Crosstalk	f_S = 48kHz, f_{IN} = 1kHz sinewave at -3dB$_{FS}$	73		dB
V$_{MIC-IN}$	Maximum Differential MIC Input Voltage	17dB MIC Preamp gain setting	570		mV$_{P-P}$
R$_{VDAC}$	Voice DAC Ripple	300Hz - 3.3kHz through head-phone output.	+/-0.15	+/-0.2	dB (max)
R$_{VADC}$	Voice ADC Ripple	300Hz - 3.3kHz through head-phone output.	+/-0.25	+/-0.3	dB (max)
PB$_{VDAC}$	Voice DAC Passband	-3dB Point	3.46		kHz
SBA$_{VDAC}$	Voice DAC Stopband Attenuation	Above 4kHz	72		dB
UPB$_{VADC}$	Voice ADC Upper Passband Cutoff Frequency.	Upper -3dB Point	3.47		kHz
LPB$_{VADC}$	Voice ADC Lower Passband Cutoff Frequency.	Lower -3dB Point	0.230		kHz
SBA$_{VADC}$	Voice ADC Stopband Attenuation	Above 4kHz	65		dB
SBA$_{NOTCH}$	Voice ADC Notch Attenuation	Centered on 55Hz, figure gives worst case attenuation for 50Hz & 60Hz.	58		dB
R$_{DAC}$	Audio DAC Ripple	20Hz - 20kHz through head-phone output.	+/-0.1	+/-0.2	dB (max)
PB$_{DAC}$	Audio DAC Passband Width	-3dB point	22.7		kHz
SBA$_{DAC}$	Audio DAC Stopband Attenuation	Above 24kHz	76		dB
DR$_{DAC}$	Audio DAC Dynamic Range Digital Filter Section	Signal = VO at f = 1kHz @ 1% THD+N; f = 1kHz; Noise for -60dBFS digital input; 0dB gain; A-weighted	97		dB
SNR$_{DAC}$	Audio DAC SNR Digital Filter Section	Signal = VO at f = 1kHz @ 1% THD+N; f = 1kHz; Noise for -60dBFS digital input; 0dB gain; A-weighted	97		dB
ΔA$_{CH-CH}$	Stereo Channel-to-Channel Gain Mismatch		0.3		dB
V$_{IL}$	Digital Input: Logic Low Voltage Level		0.4		V
V$_{IH}$	Digital Input: Logic High Voltage Level		1.4		V
	Volume Control Range (Headphone amplifiers)	Maximum Attenuation Minimum Attenuation	-46.5 0		dB dB
	Volume Control Range (Mono speaker amplifier)	Minimum Gain Maximum Gain	-34.5 12		dB dB

Electrical Characteristics DV_{DD} = 3V, AV_{DD} = 3V, R_{LHP} = 32Ω, R_{LHF} = 8Ω(1)(2)(3) (continued)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A= 25°C.

Parameter		Test Conditions	LM4930		Units (Limits)
			Typ(4)	Limits(5)(6)	
	Volume Control Step Size (Output amplifiers)		1.5		dB
	Volume Control Range (Microphone Preamp)	Minimum Gain Maximum Gain	17 47		dB
	Volume Control Step Size (Microphone Preamp)		2		dB
	Side Tone Attenuation Range	Maximum Attenuation Minimum Attenuation	-30 0		dB dB
	Side Tone Attenuation Step Size		3		dB
f_{MCLK}	MCLK frequency	CLOCK_DIV = 0 CLOCK_DIV = 1	12.288 24.576		MHz MHz
	MCLK Duty Cycle		50	40 60	% (min) % (max)
f_{CONV}	Sampling Clock Frequency	See(8)	48		kHz
f_{CLKSCL}	SCL_CLK Frequency		400		kHz
$t_{RISESCL}$	SCL_CLK, SCL_DATA Rise Time		300		ns
$t_{FALLSCL}$	SCL_CLK, SDA_DATA Fall Time		300		ns
t_{SDAH}	SDA_DATA Hold Time		500		ns
t_{SDAS}	SDA_DATA Setup Time		500		ns
f_{CLKPCM}	PCM_CLK Frequency	PCM_SYNC_MODE = 00 PCM_SYNC_MODE = 01 PCM_SYNC_MODE = 10	128 256 512		kHz kHz kHz
	PCM_CLK Duty Cycle		50	40 60	% (min) % (max)
f_{CLKI2S}	I2S_CLK Frequency	I2S_RES = 0 I2S_RES = 1	1.536 3.072		MHz MHz
	I2S_CLK Duty Cycle		50	40 60	% (min) % (max)

(8) The sampling clock frequency is equal to the master clock frequency divided by 256. (f_{conv} = f_{MCLK}/256)

Typical Performance Characteristics (1)

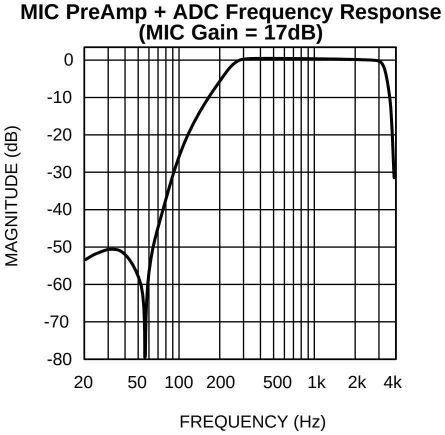
MIC PreAmp + ADC Frequency Response (MIC Gain = 17dB)

Figure 7.

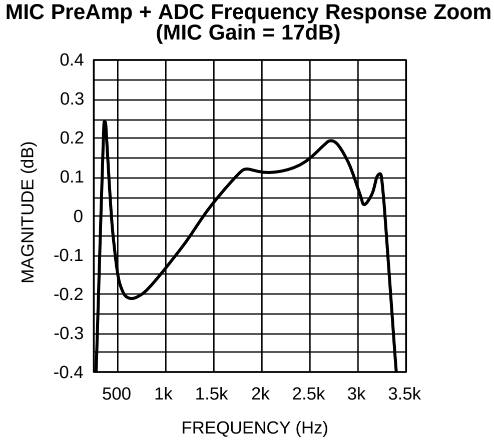
MIC PreAmp + ADC Frequency Response Zoom (MIC Gain = 17dB)

Figure 8.

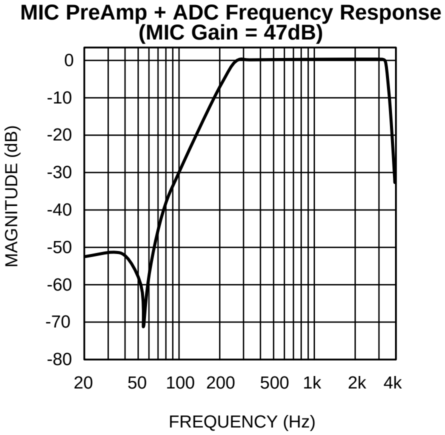
MIC PreAmp + ADC Frequency Response (MIC Gain = 47dB)

Figure 9.

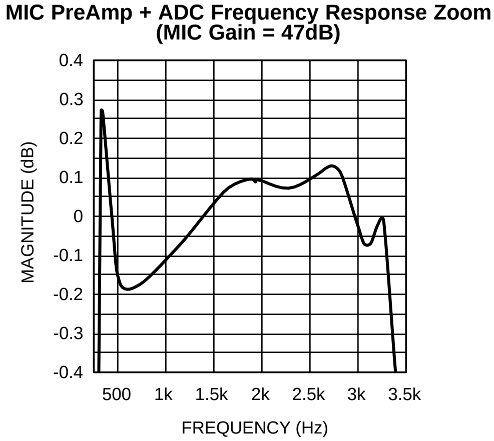
MIC PreAmp + ADC Frequency Response Zoom (MIC Gain = 47dB)

Figure 10.

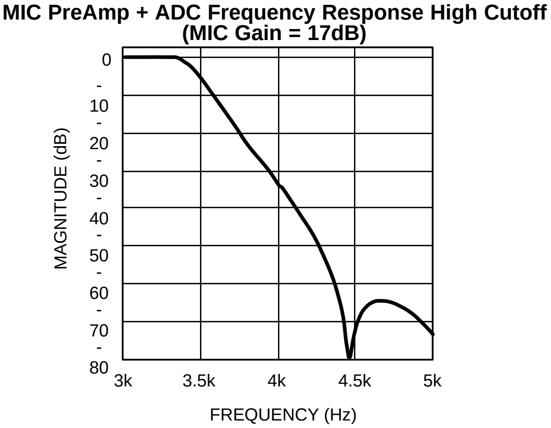
MIC PreAmp + ADC Frequency Response High Cutoff (MIC Gain = 17dB)

Figure 11.

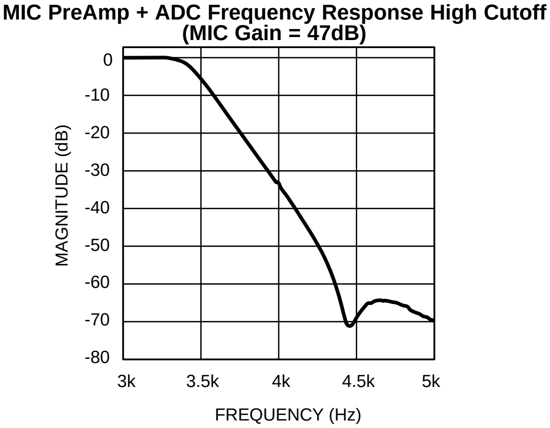
MIC PreAmp + ADC Frequency Response High Cutoff (MIC Gain = 47dB)

Figure 12.

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(1) 0dBm0 = -3dBFS for the PCM voice codec and 0dBm0 = -1dBFS for the I^2S DAC, unless otherwise specified.

Typical Performance Characteristics [(1)] (continued)

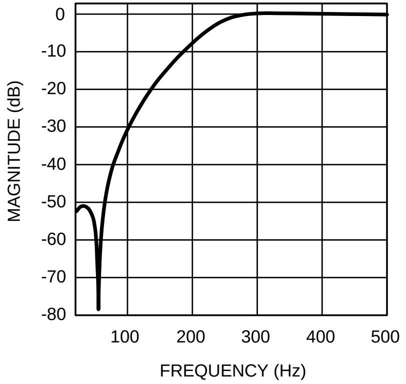
MIC PreAmp + ADC Frequency Response Low Cutoff (MIC Gain = 17dB)

Figure 13.

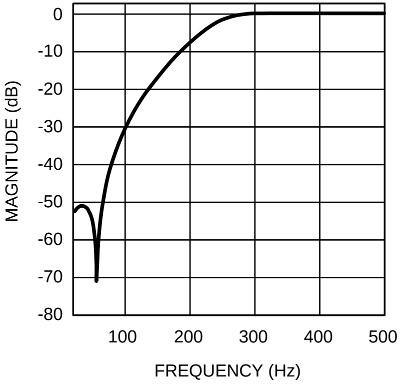
MIC PreAmp + ADC Frequency Response Low Cutoff (MIC Gain = 47dB)

Figure 14.

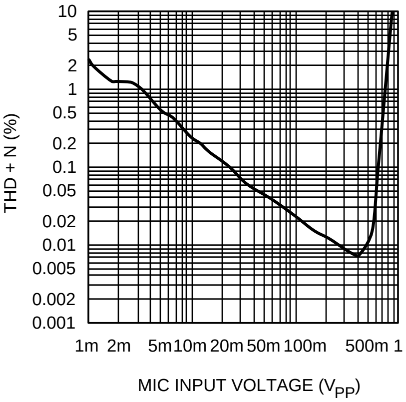
ADC THD+N vs MIC Input Voltage (MIC Gain = 17dB)

Figure 15.

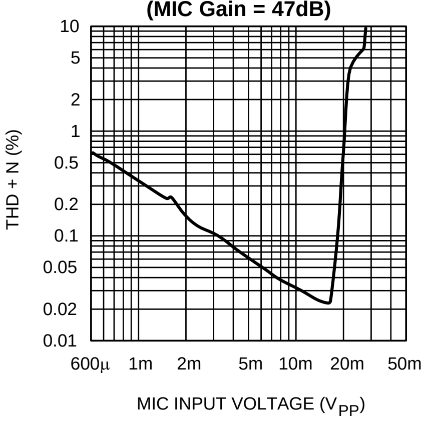
ADC THD+N vs MIC Input Voltage (MIC Gain = 47dB)

Figure 16.

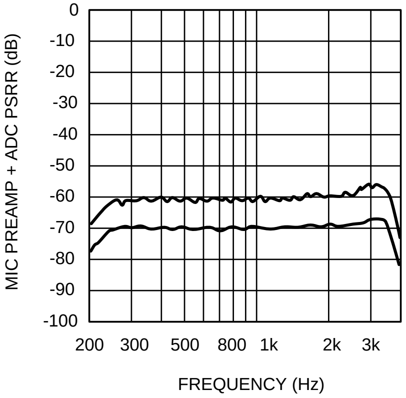
MIC PreAmp + ADC PSRR vs Frequency Top Trace = 47dB MIC Gain, Bottom Trace = 17dB MIC Gain

Figure 17.

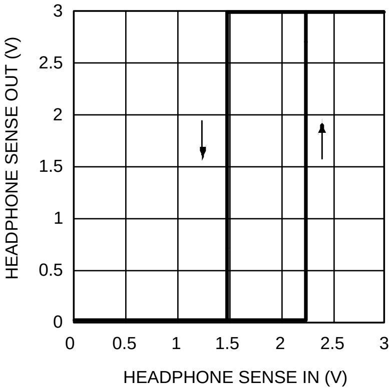
Headphone Sense In Hysteresis Loop (AV_{DD} = 3V)

Figure 18.

Typical Performance Characteristics (1) (continued)

**Headphone Sense In Hysteresis Loop
(AV_{DD} = 5V)**

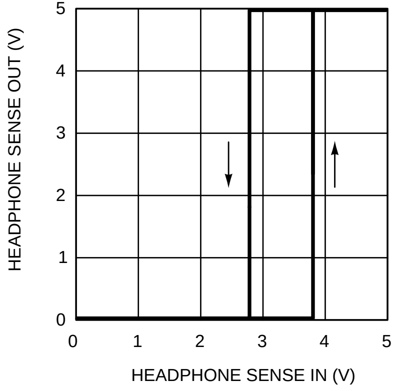

Figure 19.

**I^2S DAC Frequency Response
(Handsfree Output)**

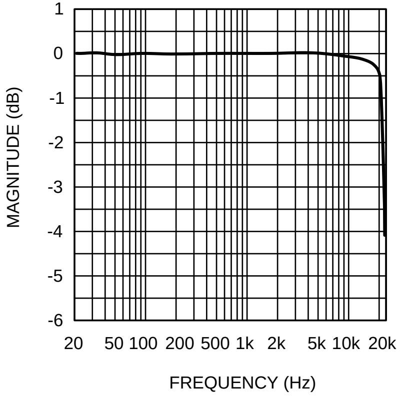

Figure 20.

**I^2S DAC Frequency Response Zoom
(Handsfree Output)**

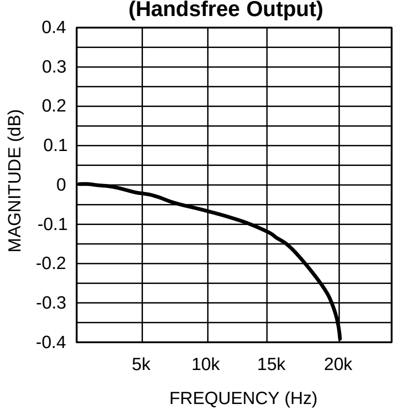

Figure 21.

**I^2S DAC Frequency Response Zoom
(Headphone Output)**

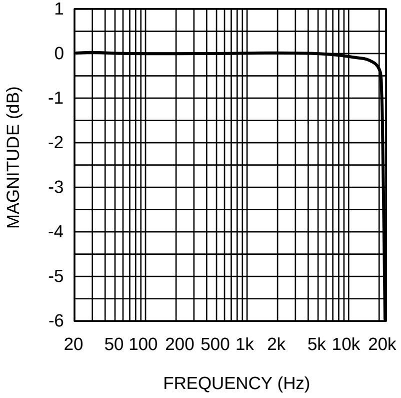

Figure 22.

**I^2S DAC Frequency Response Zoom
(Headphone Output)**

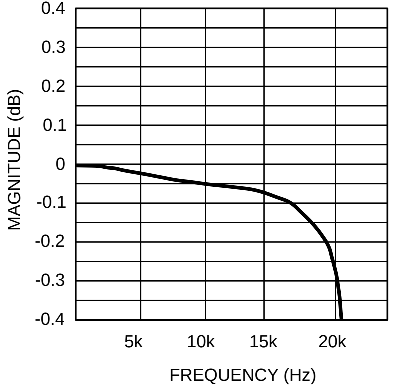

Figure 23.

**THD+N
vs
I^2S Input Voltage
(Handsfree Output, 0dB Handsfree Gain)**

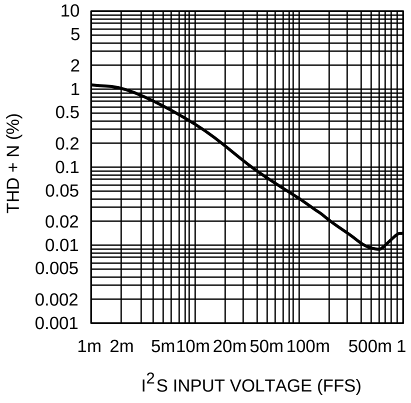

Figure 24.

Typical Performance Characteristics (1) (continued)

THD+N
vs
I^2S Input Voltage
(Headphone Output, 0dB Headphone Gain)

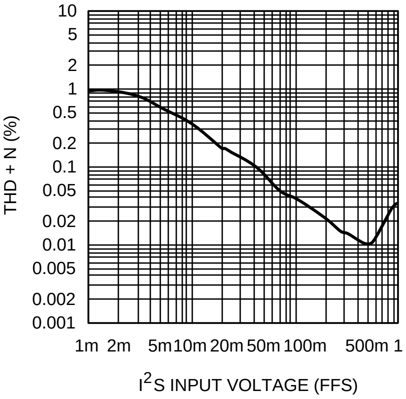

Figure 25.

I^2S DAC Crosstalk
(Top Trace = Left to Right, Bottom Trace = Right to Left)

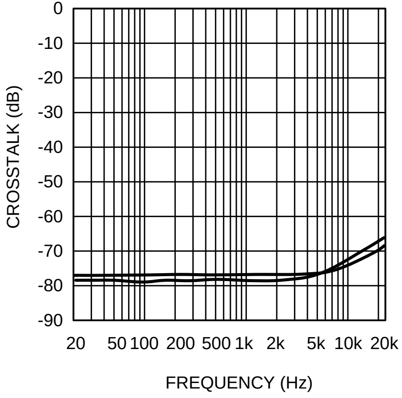

Figure 26.

MIC Bias Dropout Voltage vs
MIC Bias Current

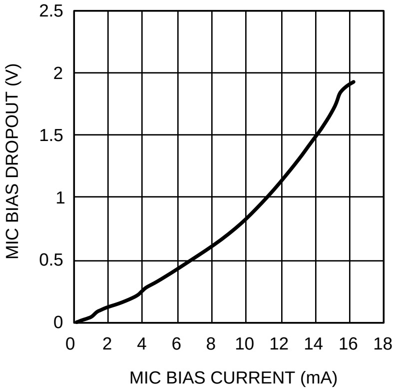

Figure 27.

PCM DAC Frequency Response
(Handsfree Output)

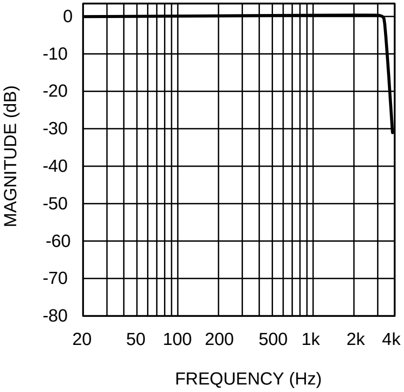

Figure 28.

PCM DAC Frequency Response Zoom
(Handsfree Output)

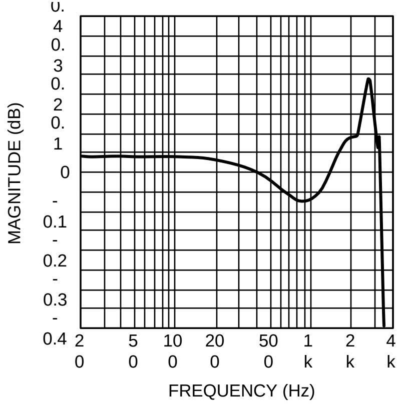

Figure 29.

PCM DAC Frequency Response
(Headphone Output)

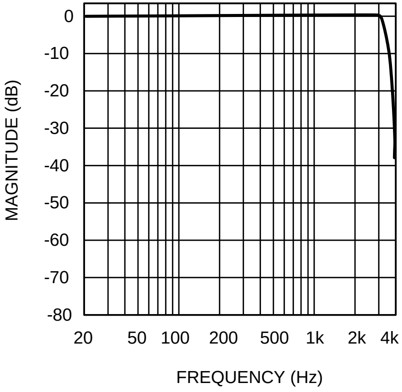

Figure 30.

Typical Performance Characteristics [(1)] (continued)

PCM DAC Frequency Response Zoom (Headphone Output)

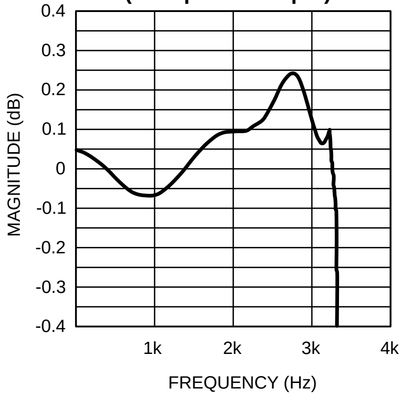

Figure 31.

THD+N vs PCM Input Voltage (Handsfree Output, 0dB Handsfree Gain)

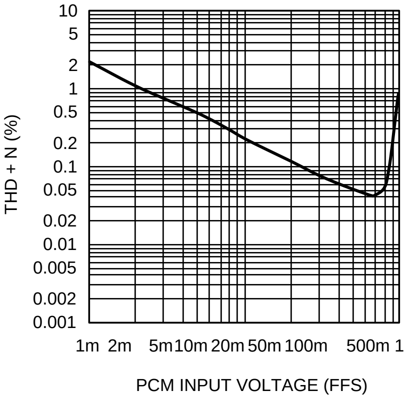

Figure 32.

THD+N vs PCM Input Voltage (Headphone Output, 0dB Headphone Gain)

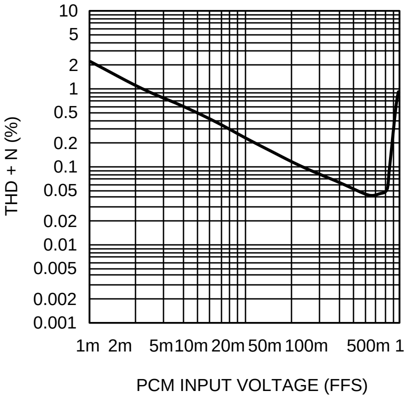

Figure 33.

Crosstalk (AV_{DD} = 5V and AV_{DD} = 3V, Headphone Output)

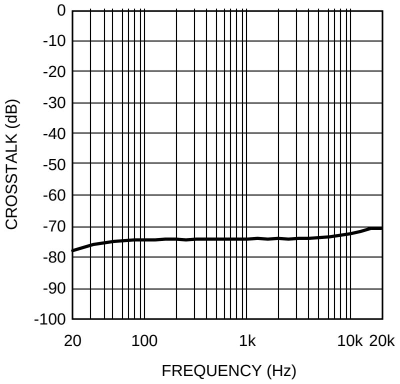

Figure 34.

PSRR vs Frequency (AV_{DD} = 3V, R_L = 16Ω, Headphone Output)

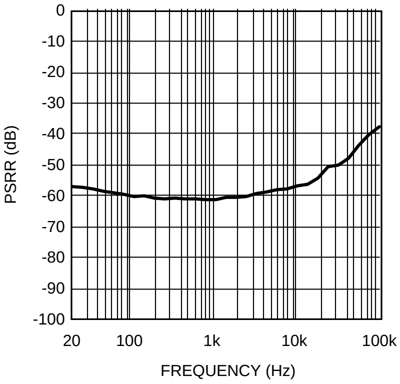

Figure 35.

PSRR vs Frequency (AV_{DD} = 3V, R_L = 32Ω, Headphone Output)

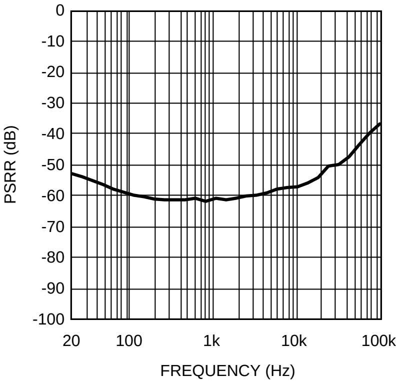

Figure 36.

Typical Performance Characteristics [(1)] (continued)

PSRR vs Frequency (AV_{DD} = 3V, R_L = 8Ω, Handsfree Output)

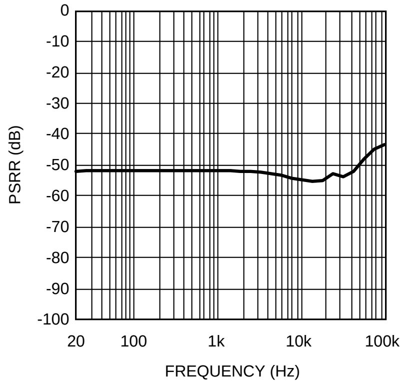

Figure 37.

PSRR vs Frequency (AV_{DD} = 5V, R_L = 16Ω, Headphone Output)

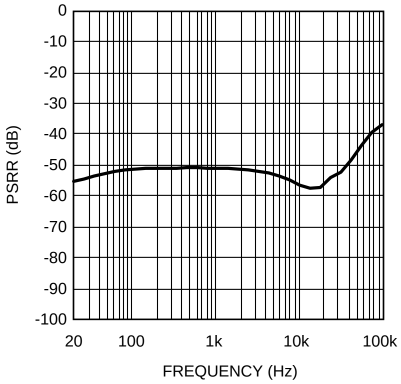

Figure 38.

PSRR vs Frequency (AV_{DD} = 5V, R_L = 32Ω, Headphone Output)

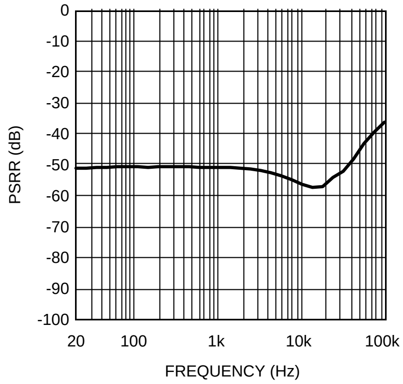

Figure 39.

PSRR vs Frequency (AV_{DD} = 5V, R_L = 8Ω, Handsfree Output)

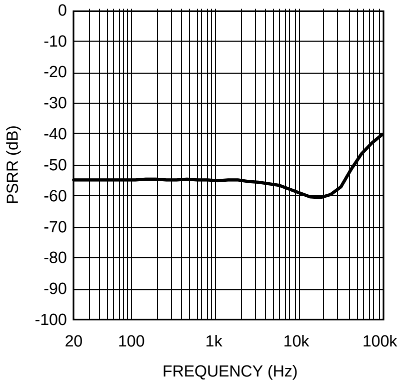

Figure 40.

THD+N vs Frequency (AV_{DD} = 3V, R_L = 8Ω, P_O = 150mW, Handsfree Output)

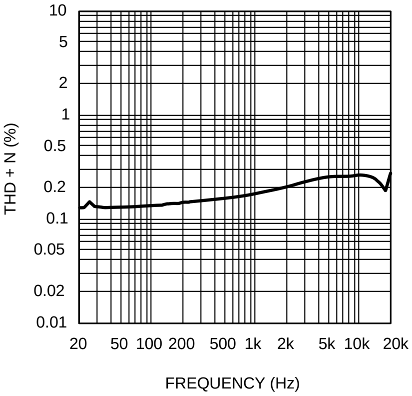

Figure 41.

THD+N vs Frequency (AV_{DD} = 5V and AV_{DD} = 3V, R_L = 16Ω, P_O = 15mW, Headphone Output)

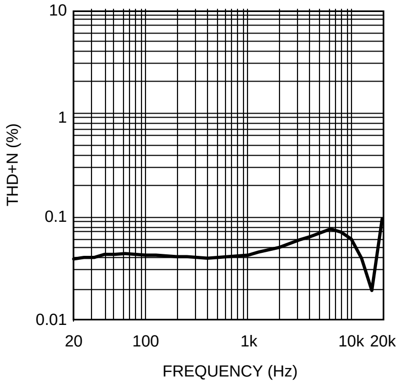

Figure 42.

Typical Performance Characteristics (1) (continued)

THD+N
vs
Frequency
(AV_{DD} = 5V and AV_{DD} = 3V, R_L = 32Ω, P_O = 7.5mW, Headphone Output)

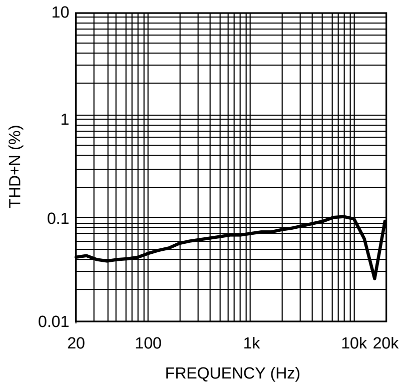

Figure 43.

THD+N
vs
Frequency
(AV_{DD} = 5V, R_L = 8Ω, P_O = 250mW, Handsfree Output)

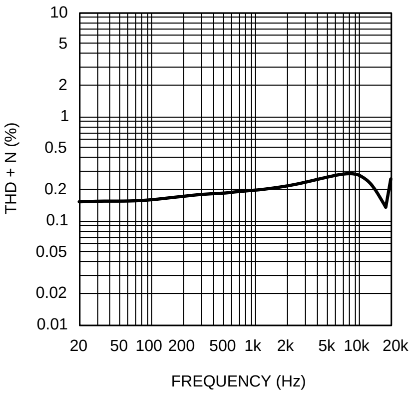

Figure 44.

THD+N
vs
Output Power
AV_{DD} = 3V, R_L = 16Ω, f = 1kHz, Headphone Output)

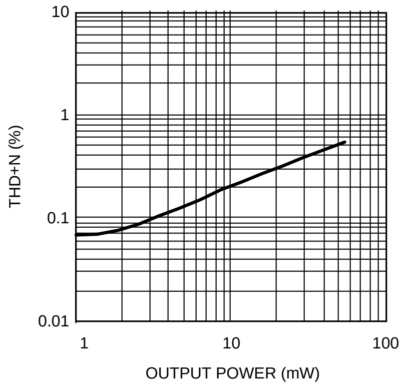

Figure 45.

THD+N
vs
Output Power
(AV_{DD} = 3V, R_L = 8Ω, f = 1kHz, Handsfree Output)

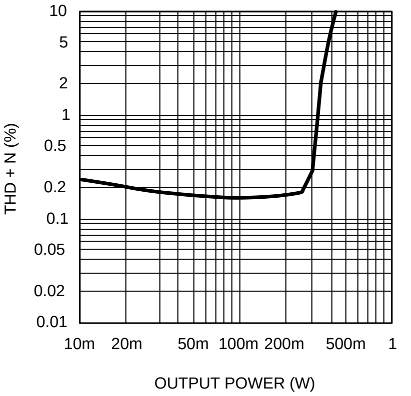

Figure 46.

THD+N
vs
Output Power
(AV_{DD} = 5V and AV_{DD} = 3V, R_L = 32Ω, f = 1kHz, Headphone Output)

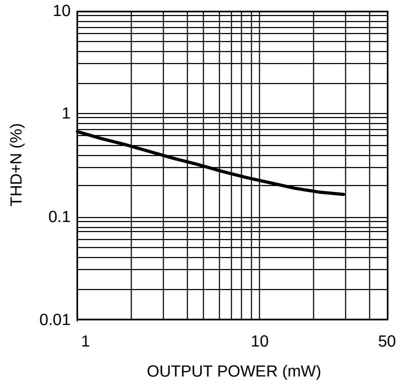

Figure 47.

THD+N
vs
Output Power
(AV_{DD} = 5V and AV_{DD} = 3V, R_L = 16Ω, f = 1kHz, Headphone Output)

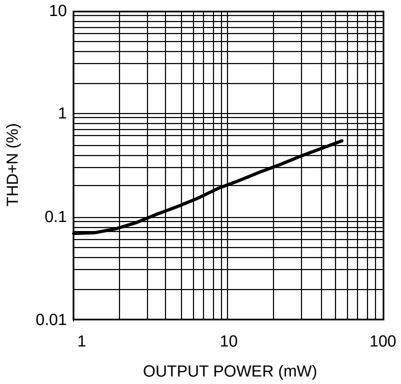

Figure 48.

Typical Performance Characteristics [(1)] (continued)

THD+N
vs
Output Power
(AV_{DD} = 5V, R_L = 8Ω, f = 1kHz, Handsfree Output)

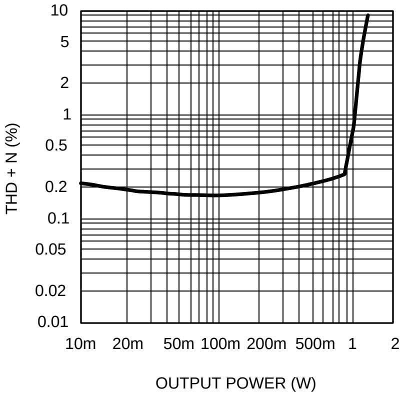

Figure 49.

APPLICATION INFORMATION

REFERENCE DESIGN BOARD AND LAYOUT

LM4930ITL Board Layout

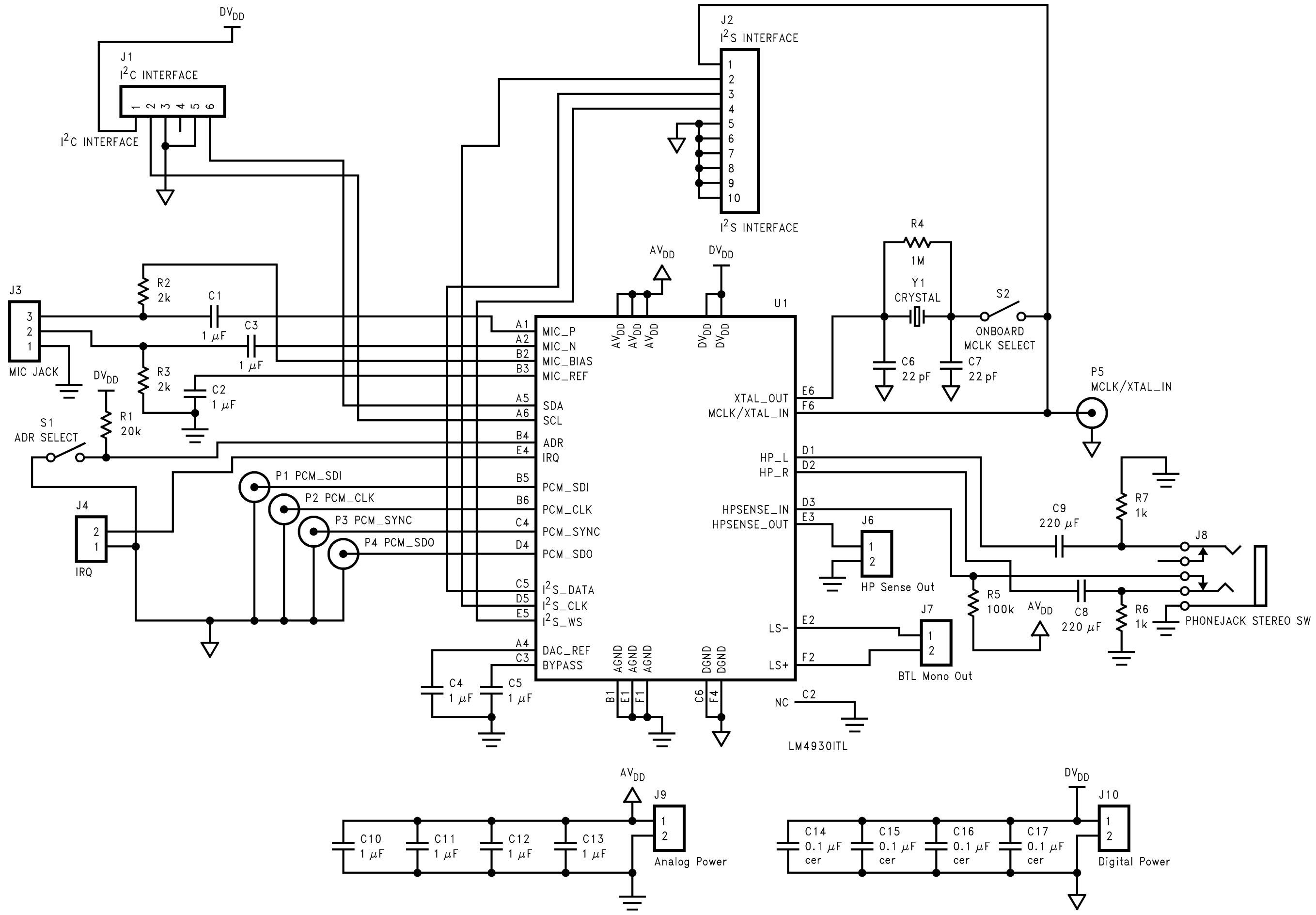

Figure 50. LM4930ITL Demo Board Schematic

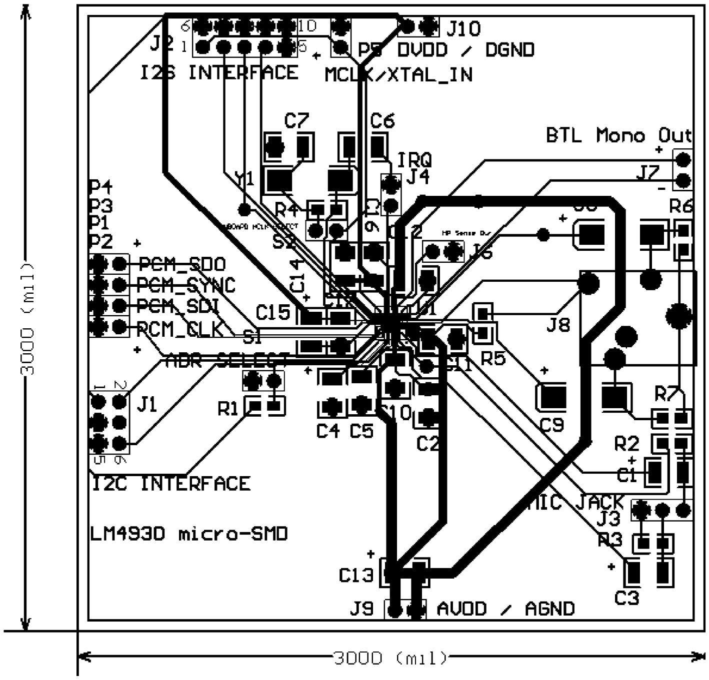

Figure 51. LM4930ITL Demo Board Composite View

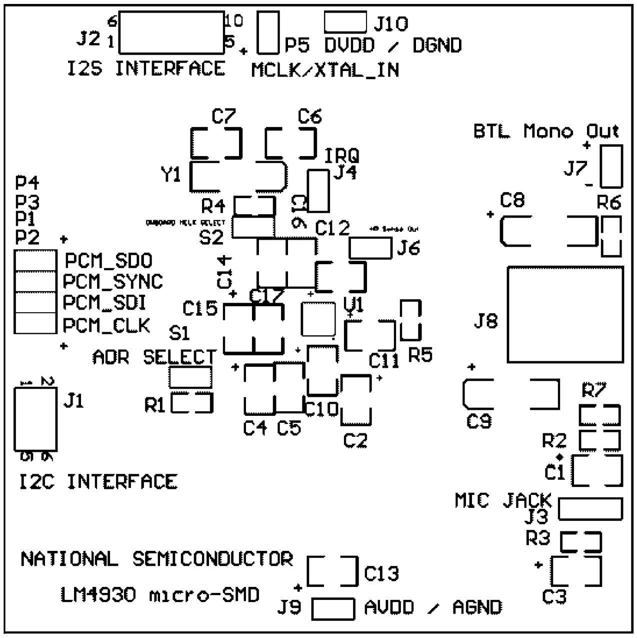

Figure 52. LM4930ITL Demo Board Silkscreen

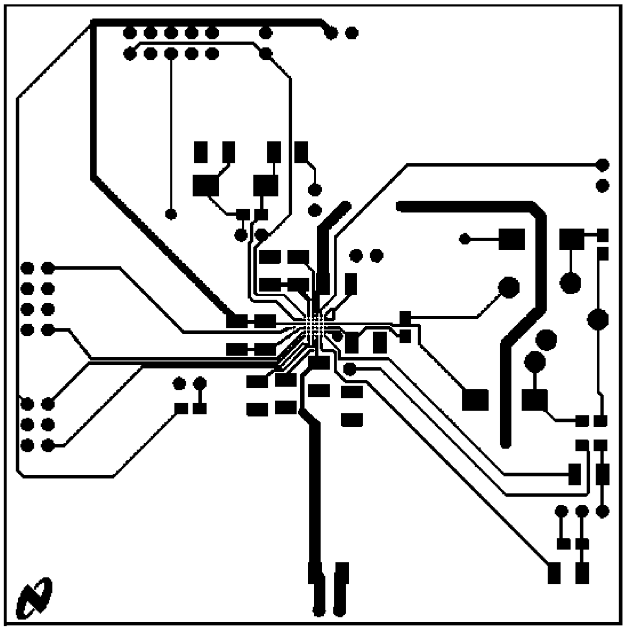

Figure 53. LM4930ITL Demo Board Top Layer

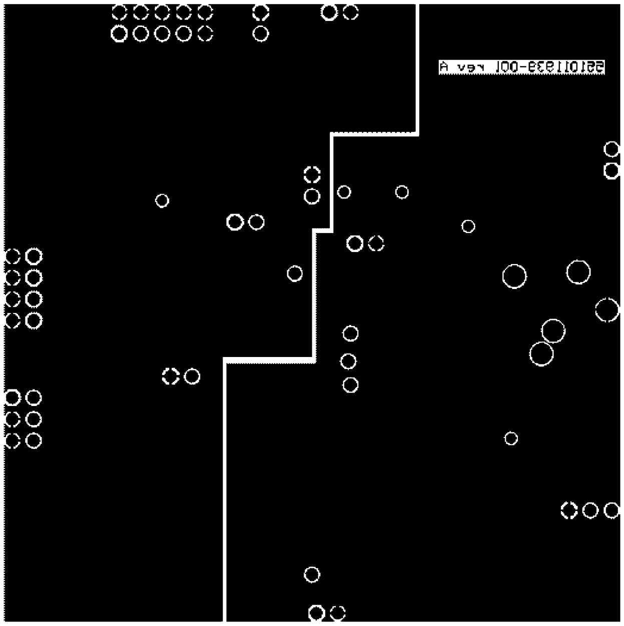

Figure 54. LM4930ITL Demo Board Bottom Layer

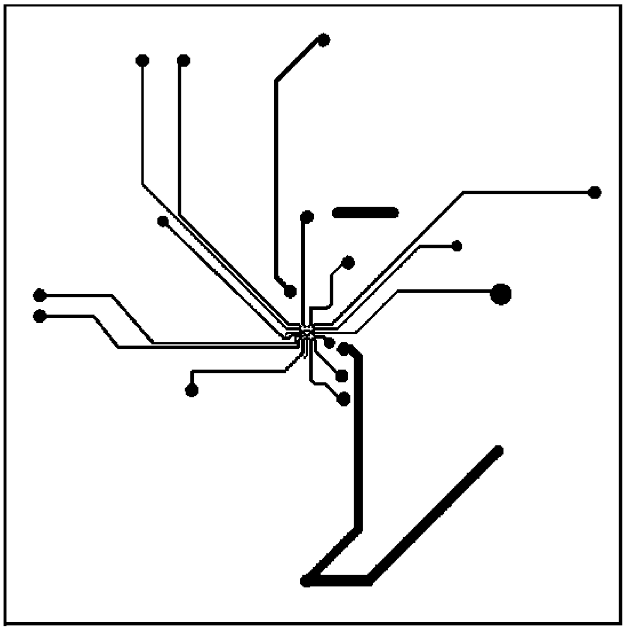

Figure 55. LM4930ITL Demo Board Inner Layer 1

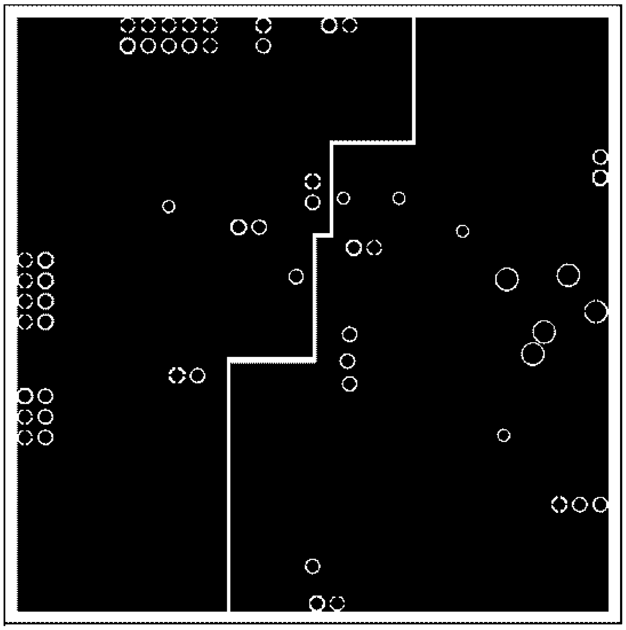

Figure 56. LM4930ITL Demo Board Inner Layer 2

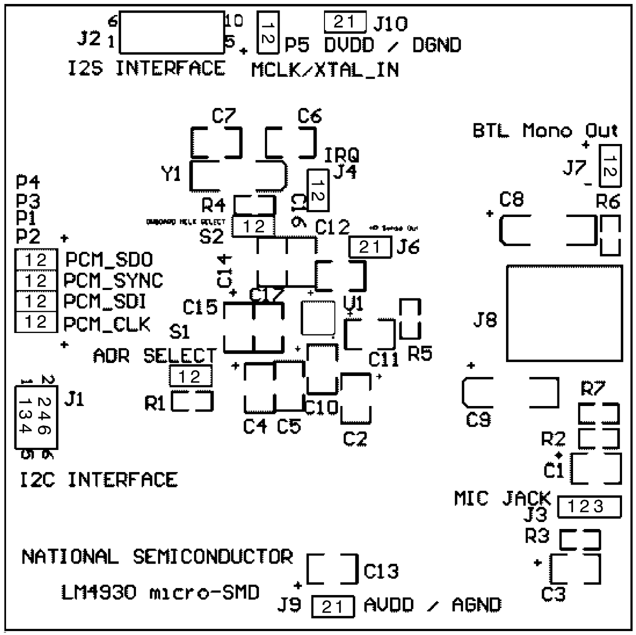

Figure 57. Pin Markings for LM4930ITL demo board

BILL OF MATERIALS FOR LM4930

Table 4. LM4930 Demo Board Bill Of Materials

Comment	Footprint	Designators
1k	0805	R6, R7
2k	0805	R2, R3
20k	0805	R1
100k	0805	R5
1M	0805	R4
22pF	1210	C6, C7
0.01µF cer	1210	C16, C17
0.1µF cer	1210	C14, C15
1µF	1210	C1, C2, C3, C4, C5, C10, C11, C12, C13
220µF	7243	C8, C9
CRYSTAL	7243	Y1
PHONE JACK STEREO SW STEREO HEADPHONE JACK (3.5MM) J8		

Table 5. Two-Wire Control Interface (J1)

Pin	Function
1	DVDD
2	SCL
3	DGND
4	NC
5	DGND
6	SDA

Table 6. PCM Interface (P4, P3, P1, P2)

Header	Function
P1	PCM_SDI
P2	PCM_CLK
P3	PCM_SYNC
P4	PCM_SDO

Table 7. I2S Interface (J2)

Pin	Function
1	MCLK
2	I2S-CLK
3	I2S-DATA
4	I2S-WS
5	DGND
6	DGND
7	DGND
8	DGND
9	DGND
10	DGND

Table 8. MIC Jack

Pin	Function
1	AGND
2	MIC-
3	MIC+

Table 9. Misc Jumpers and Headers DVDD/DGND (J10)

Pin	Function
1	DGND
2	AVDD

Table 10. Misc Jumpers and Headers AVDD/AGND (J9)

Pin	Function
1	AGND
2	AVDD

Table 11. Misc Jumpers and Headers MCLK/XTAL_IN (P5)

Pin	Function
1	DGND
2	MCLK/XTAL_IN

ADR SELECT (S1)

Jumper IN = LOW

Control interface responds to addresses 001000b (BASICCONFIG), 0010001b (VOICETESTCONFIG)), and 0010010b (GAINCONFIG)

Jumper OUT = HIGH

Control interface responds to addresses 111000b (BASICCONFIG), 1110001b (VOICETESTCONFIG)), and 1110010b (GAINCONFIG)

Table 12. HP Sense Out (J6)

Pin	Function
1	AGND
2	HPSense_Out

Table 13. IRQ (J4)

Pin	Function
1	DGND
2	IRQ

Onboard MCLK Select (S2)

Jumper IN = Onboard MCLK

Jumper OUT = External MCLK

LM4930ITL DEMO BOARD OPERATION

The LM4930ITL demo board is a complete evaluation platform, designed to give easy access to the control pins of the part and comprise all the necessary external passive components. Besides the separate analog (J9) and digital (J10) supply connectors, the board features seven other major input and control blocks: a two wire interface bus (J1) for the control lines, a PCM interface bus (P1-P4) for voiceband digital audio, an I2S interface bus (J2) for full-range digital audio, an analog mic jack input (J3) for connection to an external microphone, a BTL mono output (J7) for connection to an external speaker, a stereo headphone output (J8), and an external MCLK input (P5) for use in place of the crystal on the demoboard.

Two-wire Interface Bus (J1)

This is the main control bus for the LM4930. It is a two-wire interface with an SDA line (data) and SCL line (clock). Each transmission from the baseband controller to the LM4930 is given MSB first and must follow the timing intervals given in the Electrical Characteristics section of the datasheet to create the start and stop conditions for a proper transmission. The start condition is detected if SCL is high on the falling edge of SDA. The stop condition is detected if SCL is high on the rising edge of SDA. Repeated start signals are handled correctly. Data is then transmitted as shown in Figure 4. After the start condition has been achieved the chip address is sent, followed by a set write bit, wait for ack (SDA will be pulled low by LM4930), data bits 15-8, wait for ACK (SDA will be pulled low by LM4930), data bits 7-0, wait for ACK (SDA will be pulled low by LM4930)and finally the stop condition is given.

This same sequence follows for any control bus transmission to the LM4930. The chip address is hardwire selected by the ADR Select pin which may be jumpered high or low with its application at S1 on the demo board. The chip address is then given as a combination of the identifying bits for the LM4930 plus the 2-bit address of the desired control register (00b = BasicConfig, 01b = VoicetestConfig, 10b = GainConfig). Acceptable addresses are shown here in Table 14.

Table 14. LM4930 Control Bus Addresses

Address Bits					**Register Address**	
ADR = 0						
6	**5**	**4**	**3**	**2**	**1**	**0**
0	0	1	0	0	0	0
0	0	1	0	0	0	1
0	0	1	0	0	1	0
ADR = 1						
1	1	1	0	0	0	0
1	1	1	0	0	0	1
1	1	1	0	0	1	0

Data is sampled only if the address is in range and the R/$\overline{W}$ bit is clear. Data for each register is given in the System Control Registers section of the datasheet. Texas Instruments also features a special control board for quick evaluation of the LM4930 demo board with your PC. This is a serial control interface board, complete with header compatible with the interface header (J1) on the LM4930 board. This also features demonstration software to allow for complete control and evaluation of the various modes and functions of the LM4930 through the bus.

Pullup resistors are required to achieve reliable operation. 750Ω pullup resistors on the SDA and SCL lines achieves best results when used with TI's parallel-to-serial interface board. Lower value pullup resistors will decrease the rise and fall times on the bus which will in turn decrease susceptibility to bus noise that may cause a false trigger. The cost comes at extra current use. Control bus reliability will thus depend largely on bus noise and may vary from design to design. Low noise is critical for reliable operation.

PCM Bus Interface (P1, P2, P3, P4)

PCM_SDO (P4), PCM_SYNC (P3), PCM_SDI (P1), and PCM_CLK (P2) form the PCM interface bus for simple communication with most baseband ICs with voiceband communications and follow the PCM-1900 communications standard. The PCM interface features frame lengths of 16, 32, or 64 bits, A-law and u-law companding, linear mode, short or long frame sync, an energy-saving power down mode, and master only operation.

The PCM bus does not support a slave mode. It operates as a master only. Thus PCM_SYNC and PCM_CLK are solely generated by the LM4930. PCM_SYNC is the word sync line for the bus. It operates at a fixed frequency of 8kHz and may be set in the BASICCONFIG register (bit 5 PCM_LONG) for short or long frame sync. A short frame sync is 1 PCM_CLK cycle (PCM_LONG=0), a long frame sync is 2 PCM_CLK cycles long (PCM_LONG=1). A long sync pulse is also delayed one clock cycle relative to a short sync pulse. This is illustrated in Figure 5. PCM_CLK is the bit clock for the bus. It's frequency depends on the number of 16-bit frames per sync pulse and can be 128kHz, 256kHz, 512kHz.

The other two lines, PCM_SDO and PCM_SDI, are for serial data out and serial data in, respectively. The type of data may also be set in the BASICCONFIG register by bits 6 and 7. Bit 6 controls whether the data is linear or companded. If set to 1, the 8 MSBs are presumed to be companded data and the 8 LSBs are ignored. If cleared to 0, the data is treated as 2's complement PCM data. Bit 7 controls which PCM law is used if Bit 6 is set for companded (G711) data. If set to 1, the companded data is assumed to be A-law. If cleared to 0, the companded data is treated as µ-law.

Bits 8:9 of the BASICCONFIG register set the PCM_SYNC_MODE settings. This controls the number of 16 bit frames per sync pulse. The feature allows the LM4930 to function harmoniously with other devices or channels on the PCM bus by adjusting the number of 16 bit frames per sync pulse to 1 (00b), 2 (01b), or 4 (10b). The LM4930 will transmit PCM data in the first frame and then tri-state the PCM_SDO pin on later frames.

In addition, the LM4930 provides control to allow the PCM_CLK and PCM_SYNC clocks to continue functioning even when the LM4930 is in Standby mode. By setting bit 10 of the BASICCONFIG register to 1 PCM_ALWAYS_ON is enabled and the LM4930 will continue to drive the PCM clock and sync lines when in Standby mode. This bit should be set if another codec is using the PCM bus. Powerdown mode will disable these outputs.

I2S Interface Bus (J2)

The I2S standard provides a uni-directional serial interface designed specifically for digital audio. For the LM4930, the interface provides access to a 48kHz, 16 bit full-range stereo audio DAC. This interface uses a three port system of clock (I2S_CLK), data (I2S_DATA), and word (I2S_WS). The clock and word lines can be either master or slave as set by bit 11 in the BASICCONFIG register.

A bit clock (I2S_CLK) at 32 or 64 times the sample frequency is established by the I2S system master and a word select (I2S_WS) line is driven at a frequency equal to the sampling rate of the audio data, in this case 48kHz. The word line is registered to change on the negative edge of the bit clock. The serial data (I2S_DATA) is sent MSB first, again registered on the negative edge of the bit clock, delayed by 1 bit clock cycle relative to the changing of the word line (typical I2S format - see Figure 6).

The resolution of the I2S interface may be set by modifying the I2S_RES bit (bit 12) in the BASICCONFIG register. If set to 1, the LM4930 operates at 32 bits per frame (3.072MHz). If cleared to 0, then 16 bits per frame is selected (1.536MHz). This has a corresponding effect on the bit clock.

The I2S Interface Bus also provides for an additional MCLK connection to an external device from the LM4930 demo board. This may be used in conjunction with Texas Instruments' SPDIF->I2S Conversion Board for quick evaluation. This board features a connection header that interfaces with pins 1-5 of the I2S Interface Bus. Pins 6-10 are provided as digital ground references for the case of discrete connections.

MCLK/XTAL_IN (P5)

This is the input for an external Master Clock. The jumper at S2 must be removed (disconnecting the onboard crystal from the circuit) when using an external Master Clock.

BTL Mono Out (J7)

This is the mono speaker output, designed for use with an 8 ohm speaker. The outputs are driven in bridge-tied-load (BTL) mode, so both sides have signal. Outputs are normally biased at one half AVDD when the LM4930 is in active mode.

Additionally, if the CLASS bit is set to 1 in the VOICETESTCONFIG register (bit 0) the BTL mono output is internally configured as a buffer amplifier designed for use with an external class D amp.

Stereo Headphone Out (J8)

This is the stereo headphone output. Each channel is single-ended, with 220uF DC blocking capacitors mounted on the demo board. The jack features a typical stereo headphone pinout.

A headphone sense pin is provided at J6. This pin provides a clean logic high or low output to indicate the presence of headphones in the headphone jack. A common application circuit for this is given in the Reference Board Schematic shown in Figure 50. In this application HPSENSE_IN is pulled low by the 1k ohm resistor when no headphone is present. This gives a corresponding logic low output on the HPSENSE_OUT pin. When a headphone is placed in the jack the 1k ohm pull-down is disconnected and a 100k ohm pull-up resistor creates a high voltage condition on HPSENSE_IN. This in turn creates a logic high on HPSENSE_OUT. This output may be used to reliably drive an external microcontroller with headphone status.

MIC Jack (J3)

This jack is for connection to an external microphone like the kind typically found in mobile phones. Pin 1 is GND, pin 2 is the negative input pin, and pin 3 is the positive pin, with phantom voltage supplied by MIC_BIAS on the LM4930.

IRQ (J4)

This pin provides simple status updates from the LM4930 to an external microcontroller if desired. IRQ is logic high when the LM4930 is in a stable state and changes to low when changing modes. This can also be useful for simple software/driver development to monitor mode changes, or as a simple debugging tool.

BASIC OPERATION

The LM4930 is a highly integrated audio subsystem with many different operating modes available. These modes may be controlled in the BASICCONFIG register in bits 3:0. These mode settings are shown in the BASICCONFIG register table and are described here below:

Powerdown Mode (0000b)

Part is powered down, analog outputs are not biased. This is a minimum current mode. All part features are shut down.

Standby Mode (0001b)

The LM4930 is powered down, but outputs are still biased at one half AVDD. This comes at some current cost, but provides a much faster turn-on time with zero "click and pop" transients on the headphone out. Standby mode can be toggled into and out of rapidly and is ideal for saving power whenever continuous audio is not a requirement. All other part functions are suspended unless PCM_ALWAYS_ON (bit 10 in BASICCONFIG register) is enabled, in which case PCM_CLK and PCM_SYNC will continue to function.

Mono Speaker Mode (0010b)

Part is active. All analog outputs are biased. Audio from the voiceband codec is routed to the mono speaker out. Stereo headphone out is silent.

Headphone Call Mode (0011b)

Part is active. All analog outputs are biased. Audio from voiceband codec is routed to the stereo headphones. Both left and right channels are the same. Mono speaker out is silent.

Conference Call Mode (0100b)

Part is active. All analog outputs are biased. Audio from the voiceband codec is routed to the mono speaker out and to the stereo headphones.

L+R Mixed to Mono Speaker (0101b)

Part is active. All analog outputs are biased. Full-range audio from the 16bit/48kHz audio DAC is mixed together and routed to the mono speaker out. Stereo headphones are silent.

Headphone Stereo Audio (0110b)

Part is active. All analog outputs are biased. Full-range audio from the 16bit/48kHz audio DAC is sent to the stereo headphone jack. Each channel is heard discretely. The mono speaker is silent.

L+R Mixed to Mono Speaker + Stereo Headphone Audio (0111b)

Part is active. All analog outputs are biased. Full-range audio from the 16bit/48kHz audio DAC is sent discretely to the stereo headphone jack and also mixed together and sent to the mono speaker out.

Mixed Mode (1000b)

Part is active. All analog outputs are biased. This provides one channel (the left channel) of full range audio to the mono speaker out. Audio from the voiceband codec is then sent to the stereo headphones, the same on each channel.

Mixed Mode (1001b)

Part is active. All analog outputs are biased. Mixed voiceband and full-range audio (left channel only) is sent to the mono speaker out. Audio from the voiceband codec only is sent to the stereo headphones, the same on each channel.

Mixed Mode (1010b)

Part is active. All analog outputs are biased. Audio from the voiceband codec is sent to the mono speaker out. The left channel only of the full range audio is then sent to both the left and right channels of the stereo headphone out.

REGISTERS

The LM4930 starts on power-up with all registers cleared in Powerdown mode. Powerdown mode is the recommended time to make setup changes to the digital interfaces (PCM bus, I2S bus). Although the configuration registers can be changed in any mode, changes made during Standby or Powerdown prevent unwanted audio artifacts that may occur during rapid mode changes with the outputs active. The LM4930 also features a soft reset. This reset is enabled by setting bit 4 of the BASICCONFIG register.

The VOICETESTCONFIG register is used to set various configuration parameters on the voiceband and full-range audio codecs. SIDETONE_ATTEN (bits 4:1) refers to the level of signal from the MIC input that is fed back into the analog audio output path (commonly used in headphone applications and killed in hands-free applications). Setting the AUTOSIDE bit (bit 5) automatically mutes the sidetone in voice over mono speaker modes so feedback isn't an issue.

Quick mute functions are also located in this register, with bits 13:15 muting the mono speaker amp, the headphone amp, and the mic preamp respectively.

This register also has a CLOCK_DIV bit (bit 6) which, if set, allows for the use of a 24.576MHz clock instead of the default 12.288MHz.

The GAINCONFIG register is used to control the gain of the mono speaker amp , the headphone amp, and the mic preamp. This allows flexible mono speaker gains from -34.5dB to +12dB in 1.5dB steps, headphone amp gains of -46.5dB to 0dB in 1.5dB steps, and mic preamp gains of 17dB to 47dB in 2dB steps. Gain levels may be modified in any mode, but may wait for a zero cross detect in the DAC to eliminate volume control artifacts. This wait for zero cross may be disabled by setting the ZXD_DISABLE bit (bit 7) in the VOICETESTCONFIG register to allow immediate changes.

ANALOG INPUTS AND OUTPUTS

The LM4930 features an analog mono BTL output for connection to an 8Ω external speaker. This output can provide up to 1W of power into an 8Ω load with a 5V analog supply. A single-ended stereo headphone output is also featured, providing up to 30mW of power per channel into 32Ω with a 5V analog supply.

A Headphone Sense output is provided on J6 for connection to an external controller. This pin goes high when a heaphone is present (when used as shown in Figure 50) and will function in all modes independent of other operations the LM4930 may be currently processing.

The MIC Jack input (J3) provides for a low level analog input. Pin 3 provides the power to the MIC and the positive input of the LM4930. Gain for the MIC preamp is set in the GAINCONFIG register.

REVISION HISTORY

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4930ITLX/NOPB	ACTIVE	DSBGA	YZR	36	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	G B6	Samples
LM4930LQ/NOPB	ACTIVE	WQFN	NJN	44	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-30 to 85	L4930LQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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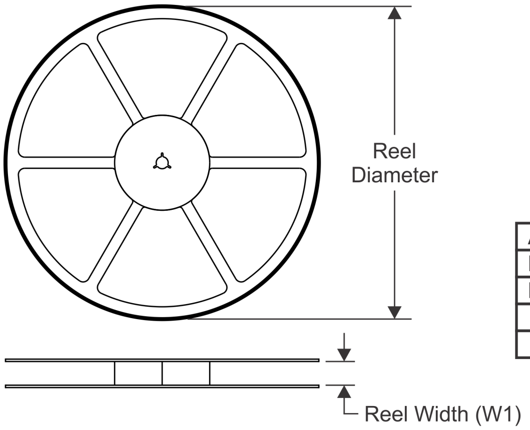
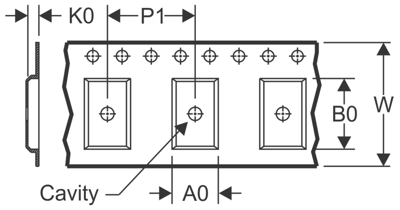
TAPE AND REEL INFORMATION

REEL DIMENSIONS

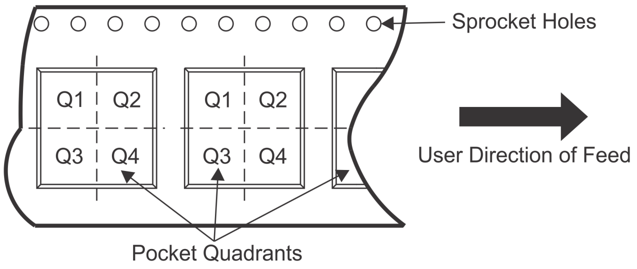


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

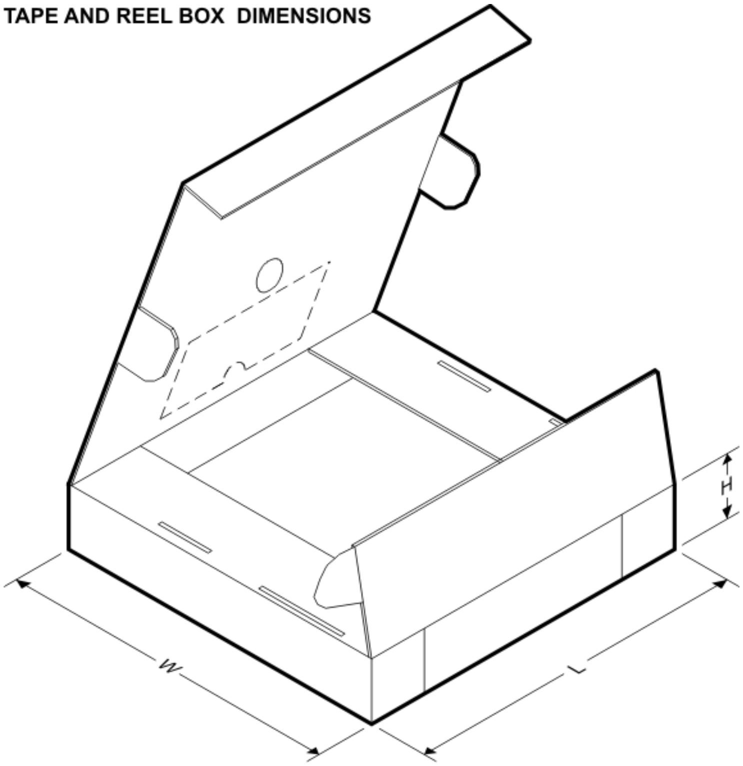
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4930ITLX/NOPB	DSBGA	YZR	36	1000	178.0	12.4	3.43	3.59	0.76	8.0	12.0	Q1
LM4930LQ/NOPB	WQFN	NJN	44	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

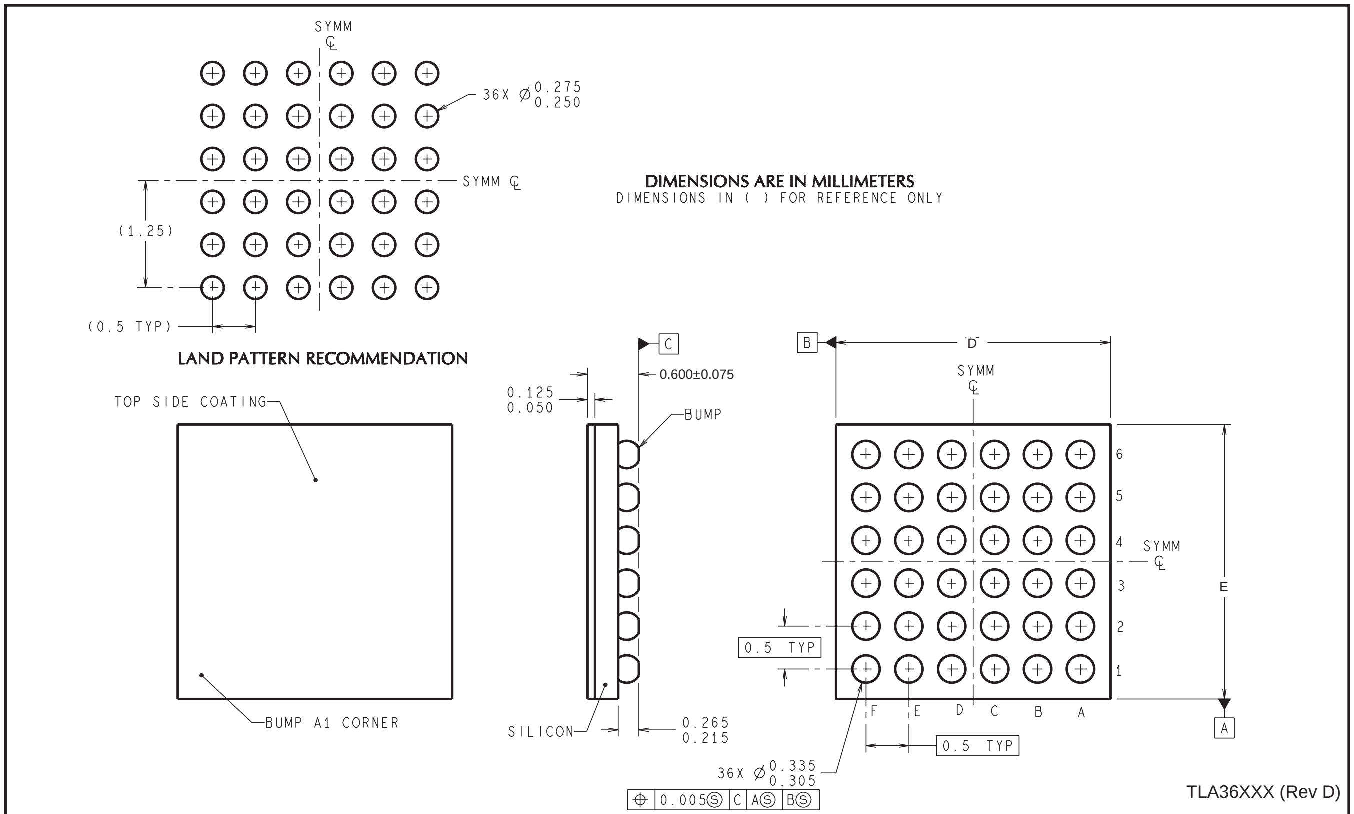
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4930ITLX/NOPB	DSBGA	YZR	36	1000	210.0	185.0	35.0
LM4930LQ/NOPB	WQFN	NJN	44	250	210.0	185.0	35.0

YZR0036



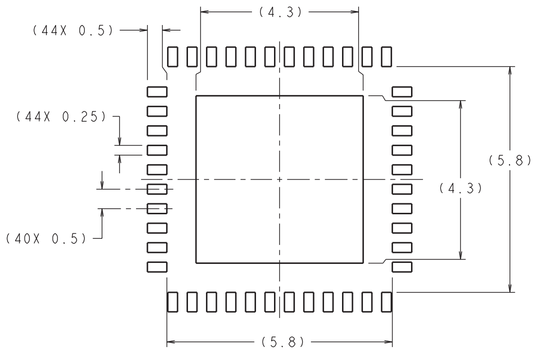
TLA36XXX (Rev D)

D: Max = 3.458 mm, Min =3.397 mm

E: Max = 3.292 mm, Min =3.232 mm

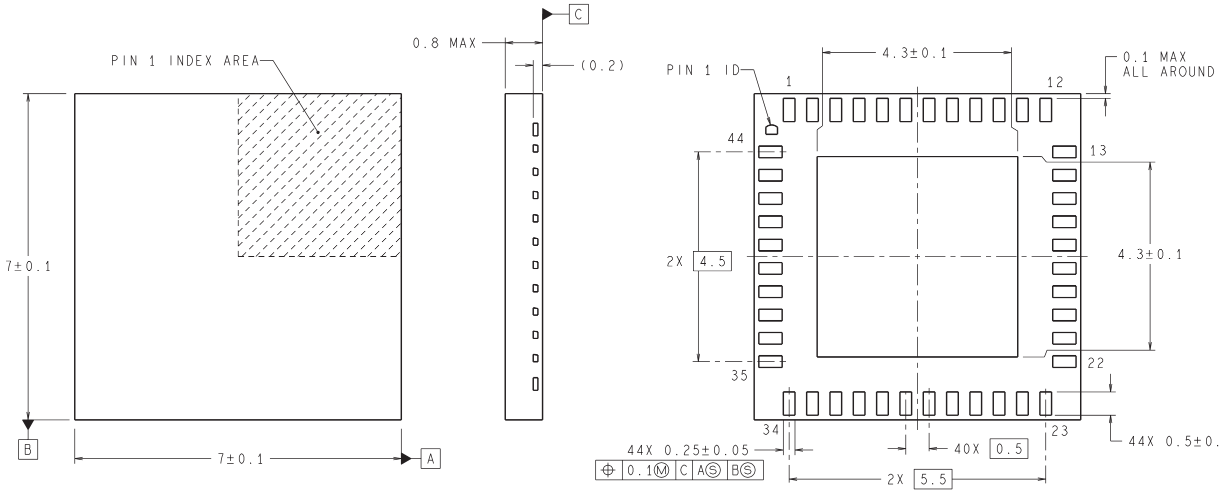
4215058/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.



RECOMMENDED LAND PATTERN
1:1 RATION WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS



LQA44A (REV B)

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