THE DATASHEET OF

LM3880MF-1AE/NOPB

LM3880 Three-Rail Simple Power Sequencer

1 Features

- Qualified for Automotive Applications
- Simple Solution for Sequencing 3 Voltage Rails from a Single Input Signal
- Easily Cascade up to 3 Devices to Sequence as Many as 9 Voltage Rails
- Power-Up and Power-Down Control
- Tiny 2.9-mm x 1.9-mm Footprint
- Low Quiescent Current of 25 µA
- Input Voltage Range of 2.7 V to 5.5 V
- Standard Timing Options Available

2 Applications

- Advanced Driver Assistance Systems (ADAS)
- Automotive Camera Modules
- Security Cameras
- Servers
- Networking Elements
- FPGA Power Supply Sequencing
- Microprocessor and Microcontroller Sequencing
- Multiple Supply Sequencing

3 Description

The LM3880 simple power supply sequencer offers the easiest method to control power up sequencing and power down sequencing of multiple Independent voltage rails. By staggering the startup sequence, it is possible to avoid latch conditions or large in-rush currents that can affect the reliability of the system.

Available in a 6-pin SOT-23-6 package, the Simple Sequencer contains a precision enable pin and three open-drain output flags. The open-drain output flags permit that they can be pulled up to distinct voltage supplies separate from the sequencer V_{DD} (so long as they do not exceed the recommended maximum voltage of 0.3V greater than V_{DD}), so as to interface with ICs requiring a range of different enable signals. When the LM3880 is enabled, the three output flags will sequentially release, after individual time delays, thus permitting the connected power supplies to start up. The output flags will follow a reverse sequence during power down to avoid latch conditions.

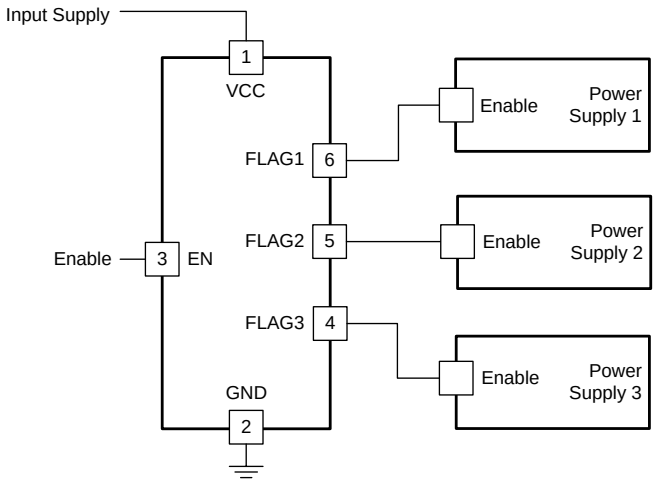
EPROM capability allows every delay and sequence to be fully adjustable. Contact Texas Instruments if a nonstandard configuration is required.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3880	DBV SOT (6)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simple Power Supply Sequencing



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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- Updated Features to specify how many rails can be sequenced by a single device ... 1
- Added feature that devices can be cascaded ... 1
- Specified device dimensions in Features ... 1
- Specified FPGA Power Supply Sequencing in Applications ... 1
- Added note in description about open drain FLAG pins ... 1
- Added I/O column to *Pin Functions* table ... 3
- Changed *Part Nomenclature* section to *Device Nomenclature* section ... 19

Changes from Revision J (December 2014) to Revision K — **Page**

- Changed *Handling Ratings* to *ESD Ratings* and moved storage temperature to *Absolute Maximum Ratings* ... 4
- Removed “Customized Timing and Sequence” section ... 12
- Added cross references to timing diagrams ... 19

Changes from Revision I (March 2013) to Revision J — **Page**

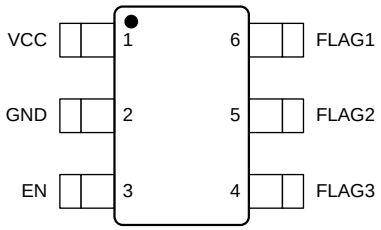
- Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 4

Changes from Revision H (March 2013) to Revision I — **Page**

- Changed layout of National Data Sheet to TI format. ... 19

5 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
EN	3	I	Precision enable pin
FLAG1	6	O	Open-drain output 1
FLAG2	5	O	Open-drain output 2
FLAG3	4	O	Open-drain output 3
GND	2	G	Ground
VCC	1	I	Input supply

(1) I = input, O = output, G = ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)(2)

	MIN	MAX	UNIT
VCC	–0.3	6	V
EN, FLAG1, FLAG2, FLAG3	–0.3	6	V
Maximum Flag ON current		50	mA
Maximum Junction temperature		150	°C
Lead temperature (Soldering, 5 s)		260	°C
Storage temperature T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VCC to GND	2.7	5.5	V
EN, FLAG1, FLAG2, FLAG3	–0.3	V_{CC} + 0.3	V
Junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM3880 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	127.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

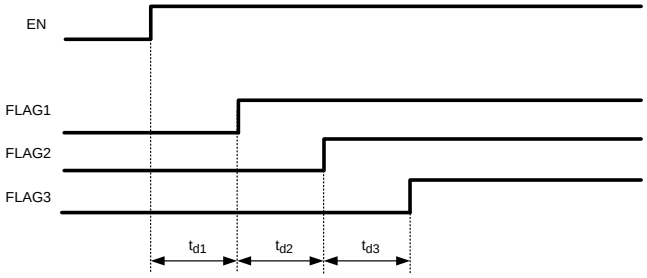
6.5 Electrical Characteristics

Limits apply to all timing options and V_{CC} = 3.3 V, unless otherwise specified. Minimum and Maximum limits apply over the full Operating Temperature Range (T_J = -40°C to +125°C) and are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
I_Q	Operating Quiescent current			25	80	µA
OPEN-DRAIN FLAGS						
I_{FLAG}	FLAGx Leakage Current	V_{FLAGx} = 3.3 V		1	20	nA
V_{OL}	FLAGx Output Voltage Low	I_{FLAGx} = 1.2 mA			0.4	V
POWER-UP SEQUENCE						
t_{d1}	Timer delay 1 accuracy	All Other Timing Options	–15%		15%	
		2 ms Timing Option	–20%		20%	
t_{d2}	Timer delay 2 accuracy	All Other Timing Options	–15%		15%	
		2 ms Timing Option	–20%		20%	
t_{d3}	Timer delay 3 accuracy	All Other Timing Options	–15%		15%	
		2 ms Timing Option	–20%		20%	
POWER-DOWN SEQUENCE						
t_{d4}	Timer delay 4 accuracy	All Other Timing Options	–15%		15%	
		2 ms Timing Option	–20%		20%	
t_{d5}	Timer delay 5 accuracy	All Other Timing Options	–15%		15%	
		2 ms Timing Option	–20%		20%	
t_{d6}	Timer delay 6 accuracy	All Other Timing Options	–15%		15%	
		2 ms Timing Option	–20%		20%	
TIMING DELAY ERROR						
($t_{d(x)}$ – 400 µs) / $t_{d(x+1)}$	Ratio of timing delays	For x = 1 or 4	95%		105%	
		For x = 1 or 4, 2 ms option	90%		110%	
$t_{d(x)}$ / $t_{d(x+1)}$	Ratio of timing delays	For x = 2 or 5	95%		105%	
		For x = 2 or 5, 2 ms option	90%		110%	
ENABLE PIN						
V_{EN}	EN pin threshold		1.0	1.25	1.4	V
I_{EN}	EN pin pullup current	V_{EN} = 0 V		7		µA

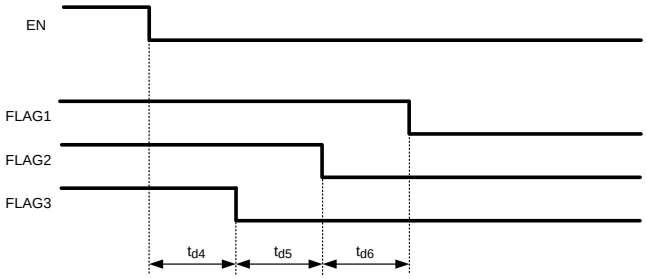
(1) Limits are 100% production tested at 25°. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.

Timing Requirements



All standard options use Sequence 1 for output flags rise and fall order. Refer to section 11.1.2 for details of different sequences possible.

Figure 1. Power-Up Sequence



All standard options use Sequence 1 for output flags rise and fall order. Refer to section 11.1.2 for details of different sequences possible.

Figure 2. Power-Down Sequence

6.6 Typical Characteristics

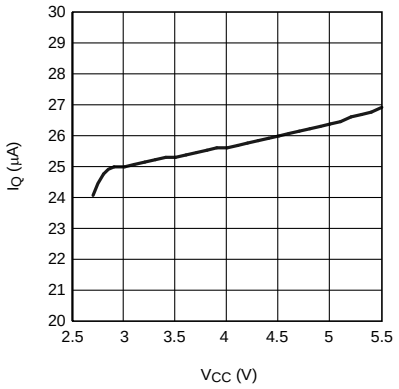


Figure 3. Quiescent Current vs VCC

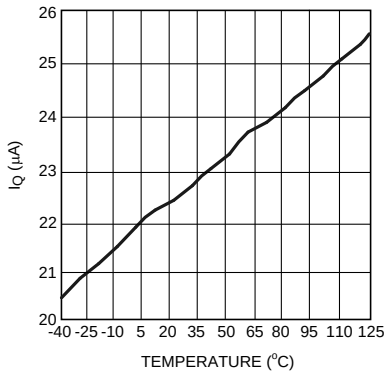


Figure 4. Quiescent Current vs Temperature (VCC = 3.3 V)

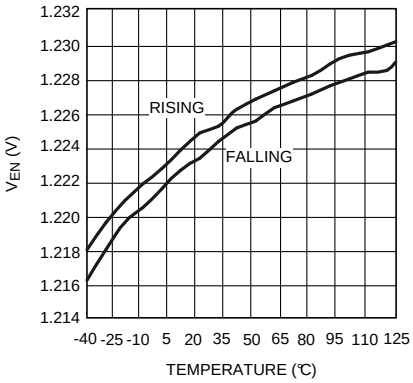


Figure 5. Enable Threshold vs Temperature

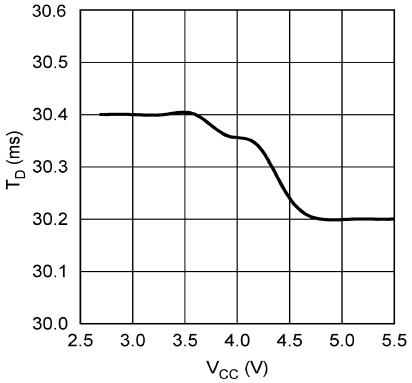


Figure 6. Time Delay (30 ms) vs Vcc

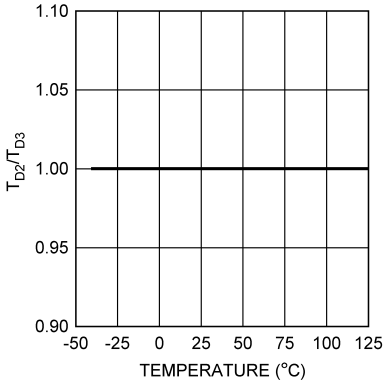


Figure 7. Time Delay Ratio vs Temperature

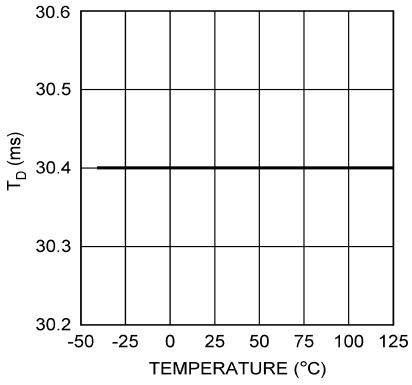


Figure 8. Time Delay (30 ms) vs Temperature

Typical Characteristics (continued)

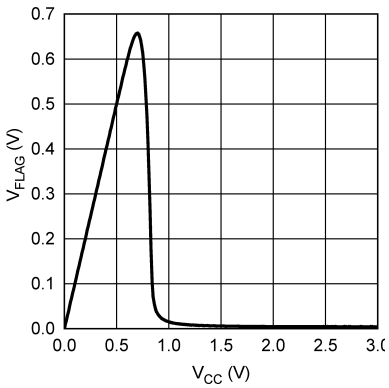


Figure 9. Flag V_{OL} vs Vcc (R_{FLAG} = 100 kΩ)

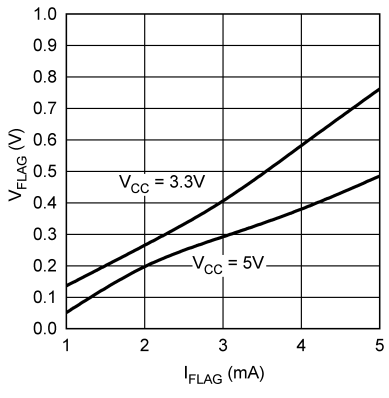


Figure 10. Flag Voltage vs Current

7 Detailed Description

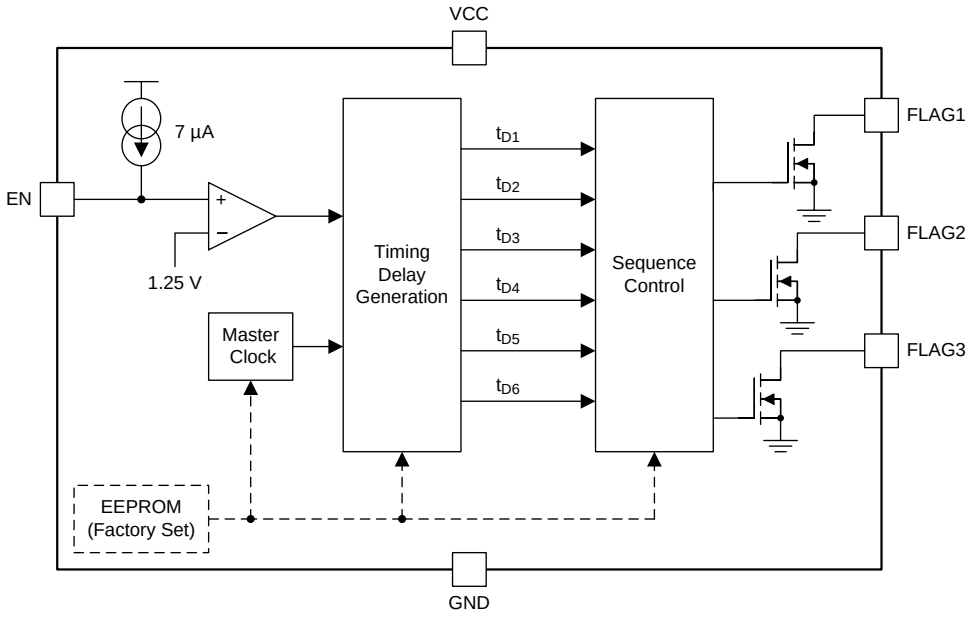
7.1 Overview

The LM3880 simple power supply sequencer provides a simple solution for sequencing multiple rails in a controlled manner. Six independent timers are integrated to control the timing sequence (power up and power down) of three open-drain output flags. These flags permit connection to either a shutdown or enable pin of linear regulators and switchers to control the operation of the power supplies. This allows design of a complete power system without concern for large inrush currents or latch-up conditions that can occur.

The timing sequence of the device is controlled entirely by the enable (EN) pin. Upon power up, all the flags are held low until this precision enable is pulled high. When the EN pin is asserted, the power-up sequence starts. An internal counter delays the first flag (FLAG1) from rising until a fixed time period has expired. When the first flag is released, another timer will begin to delay the release of the second flag (FLAG2). This process repeats until all three flags have sequentially been released.

The power-down sequence is the same as power-up sequence, but in reverse. When the EN pin is deasserted a timer will begin that delays the third flag (FLAG3) from pulling low. The second and first flag will then follow in a sequential manner after their appropriate delays. The three timers that are used to control the power-down scheme can also be individually programmed and are completely independent of the power-up timers.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable Pin Operation

The timing sequence of the LM3880 is controlled by the assertion of the enable signal. The enable pin is designed with an internal comparator, referenced to a bandgap voltage (1.25 V), to provide a precision threshold. This allows a delayed timing to be externally set using a capacitor or to start the sequencing based on a certain event, such as a line voltage reaching 90% of nominal. For an additional delayed sequence from the rail powering VCC, simply attach a capacitor to the EN pin as shown in Figure 11.

Feature Description (continued)

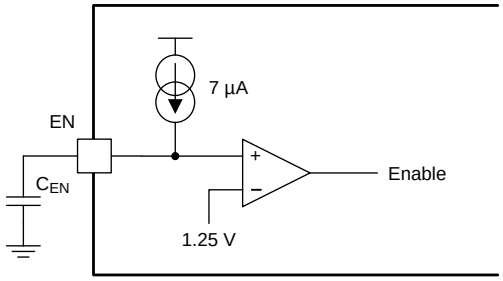


Figure 11. Capacitor Timing

Using the internal pullup current source to charge the external capacitor (C_{EN}) the enable pin delay can be calculated by Equation 1:

$$t_{enable\_delay} = \frac{1.25V \times C_{EN}}{7\ \mu A} \quad (1)$$

A resistor divider can also be used to enable the device based on a certain voltage threshold. Take care when sizing the resistor divider to include the effects of the internal current source.

One of the features of the EN pin is that it provides glitch free operation. The first timer will start counting at a rising threshold, but will always reset if the EN pin is deasserted before the first output flag is released. This can be shown in Figure 12:

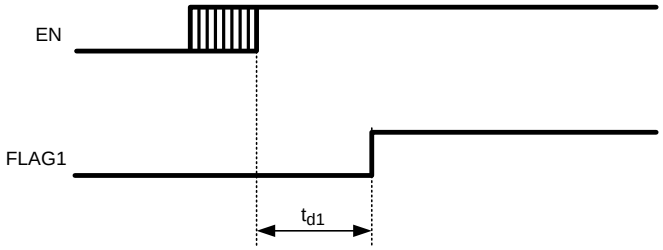


Figure 12. EN Glitch

7.3.2 Incomplete Sequence Operation

If the enable signal remains high for the entire power-up sequence, then the part will operate as shown in the standard timing diagrams. However, if the enable signal is de-asserted before the power-up sequence is completed the part will enter a controlled shutdown. This allows the system to walk through a controlled power cycling, preventing any latch conditions from occurring. This state only occurs if the enable pin is deasserted after the completion of timer 1, but before the entire power-up sequence is completed.

When this event occurs, the falling edge of EN pin resets the current timer and will allow the remaining power-up cycle to complete before beginning the power-down sequence. The power down sequence starts approximately 120 ms after the final power-up flag. This allows output voltages in the system to stabilize before everything is shut down. An example of this operation can be seen in Figure 13:

Feature Description (continued)

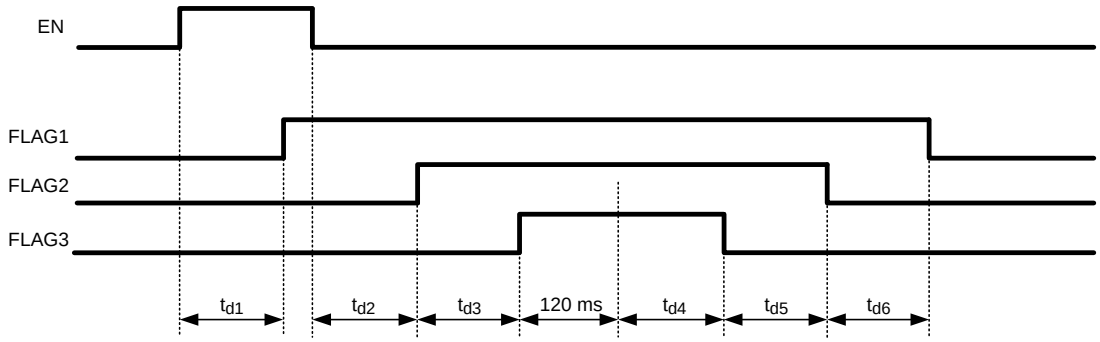


Figure 13. Incomplete Power-Up Sequence

When the enable signal is deasserted, the part will commence its power-down sequence. If the enable signal is pulled high before the power-down sequence is completed, the part will ensure completion of the power-down sequence before starting power-up. This ensures that the system does not partially power down and power up and helps prevent latch-up events, such as in FPGAs and microprocessors. This state only occurs if the enable pin is pulled high after the completion of timer 1, but before the entire power-down sequence is completed.

When this event occurs, the rising edge of enable pin resets the current timer and will allow the remaining power-down cycle to complete before beginning the power-up sequence. The power-up sequence starts approximately 120 ms after the final power-down flag. This allows the system to fully shut down before it is powered up. An example of this operation can be seen in Figure 14:

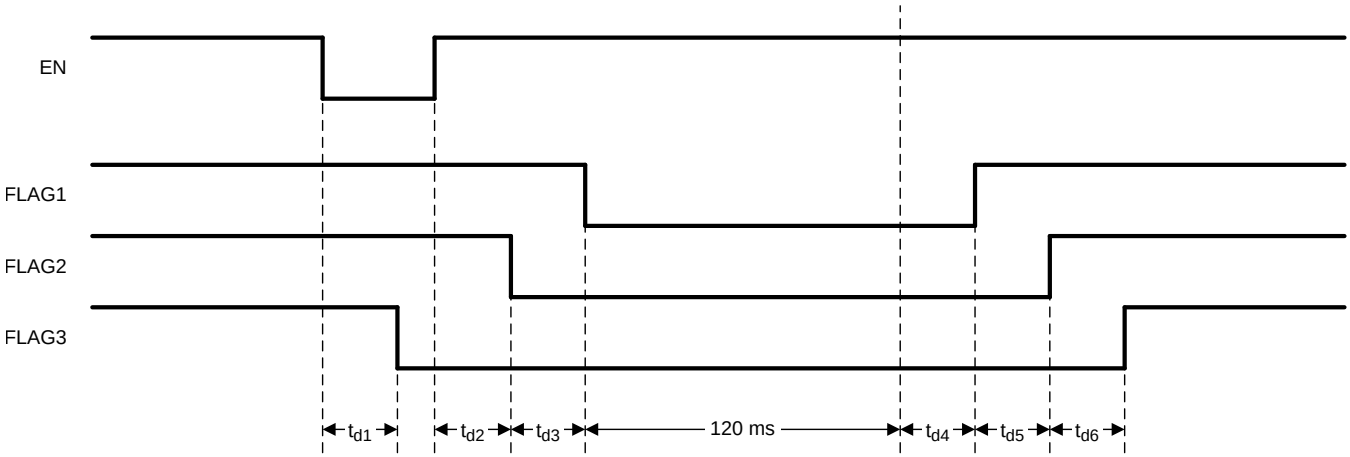


Figure 14. Incomplete Power-Down Sequence

All the internal timers are generated by a master clock that has an extremely low tempco. This allows for tight accuracy across temperature and a consistent ratio between the individual timers. There is a slight additional delay of approximately 400 µs to timers 1 and 4, which is a result of the EPROM refresh. This refresh time is in addition to the programmed delay time and will be almost insignificant to all but the shortest of timer delays.

7.4 Device Functional Modes

7.4.1 Power Up With EN Pin

The timing sequence of the Simple Power Supply Sequencer is controlled entirely by the enable (EN) pin. Upon power up, all the flags are held low until this precision enable is pulled high. After the EN pin is asserted, the power-up sequence will commence.

7.4.2 Power Down With EN Pin

When EN pin is deasserted, the power down sequence will commence. A timer will begin that delays the third flag (FLAG3) from pulling low. The second and first flag will then follow in a sequential manner after their appropriate delays.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Open Drain Flags Pullup

The Simple Power Supply Sequencer contains three open-drain output flags which need to be pulled up for proper operation. 100-kΩ resistors can be used as pullup resistors.

8.1.2 Enable the Device

See *Enable Pin Operation*.

8.2 Typical Application

8.2.1 Simple Sequencing of Three Power Supplies

The Simple Power Supply Sequencer is used to implement a power-up and power-down sequence of three power supplies.

Sequence 1 for the LM3880, e.g. orderable part number LM3880MF-1AA has a power-up sequence (1 – 2 – 3) and power-down sequence (3 – 2 –1). See Table 3 and Table 4 for other sequence options or contact TI if other sequence options are desired.

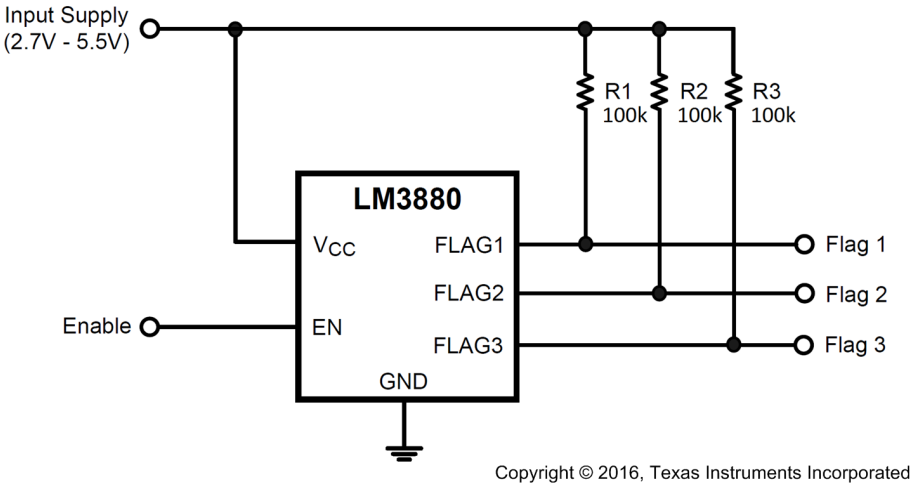


Figure 15. Typical Application Circuit

Typical Application (continued)

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters. The circuit shown in Figure 15 can have various power-down sequences depending on the sequence the part is programmed for. See Table 3 for different power-down sequence options.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Supply voltage range	2.7 V to 5.5 V
Flag Output voltage, EN high	Input Supply
Flag Output voltage, EN low	0 V
Flag Timing Delay	30 ms
Power-Up Sequence	1 - 2 - 3
Power-Down Sequence	3 - 2 - 1

8.2.1.2 Detailed Design Procedure

Table 2. Bill of Materials

DESIGNATOR	DESCRIPTION	DEVICE	QUANTITY	MANUFACTURER
U1	LM3880, Sequence 1, 30 ms timing	LM3880	1	Texas Instruments
R1	100-kΩ Resistor, 0603	CRCW0603100KFKEA	1	Vishay
R2	100-kΩ Resistor, 0603	CRCW0603100KFKEA	1	Vishay
R3	100-kΩ Resistor, 0603	CRCW0603100KFKEA	1	Vishay

This application uses the Sequence 1 and 30-ms timing options of the Simple Power Supply Sequencer. See *Application Curves* for details on the sequence and timing option.

8.2.1.3 Application Curves

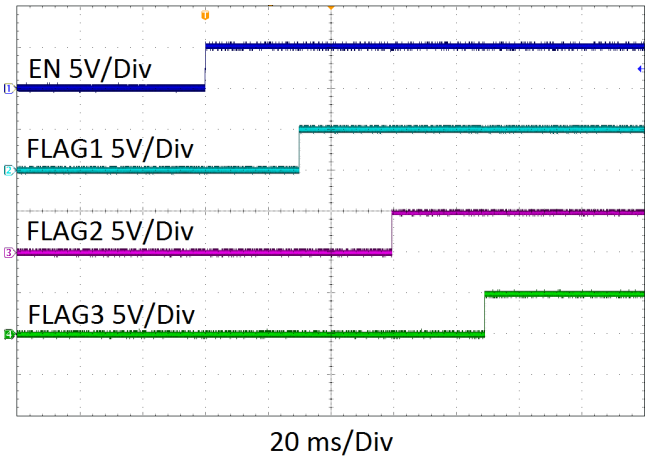


Figure 16. Power-Up Sequence for LM3880MF-1AE

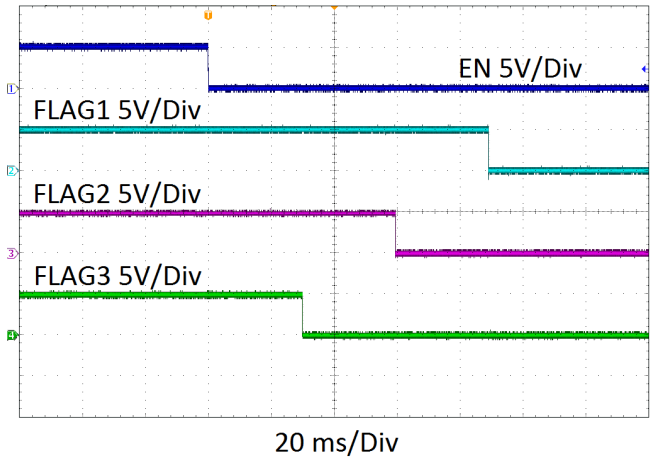


Figure 17. Power-Down Sequence for LM3880MF-1AE

8.2.2 Sequencing Using Independent Flag Supply

For applications requiring a flag output voltage that is different from the VCC, a separate Flag Supply may be used to pullup the open-drain outputs of the simple power supply sequencer. This is useful when interfacing the flag outputs with inputs that require a different voltage than VCC. The designer must ensure the flag supply voltage is not taken above VCC + 0.3 V as specified in the *Recommended Operating Conditions*.

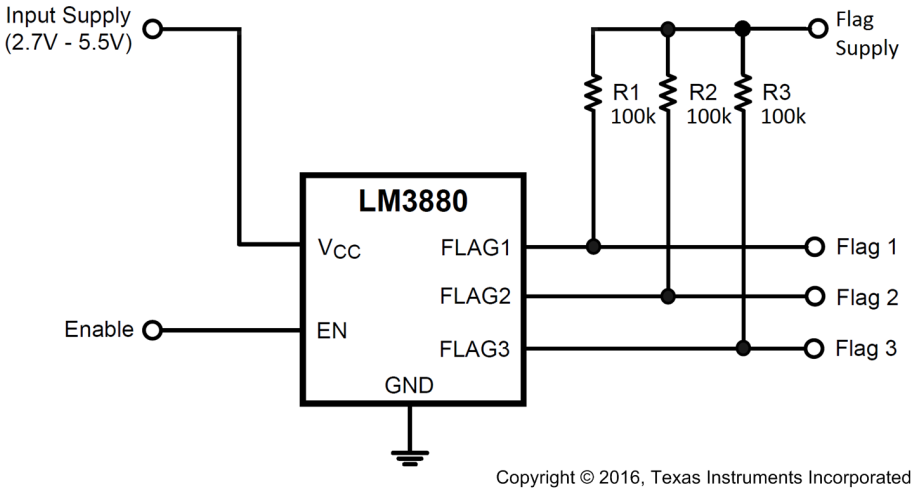


Figure 18. Sequencing Using Independent Flag Supply

8.3 Do's and Don'ts

Connecting the EN pin to VCC is not recommended. During power up, the EN voltage should be kept below the EN threshold until VCC rises above the minimum operating voltage. This will be violated if EN is connected to VCC, and undefined operation at the flag outputs can occur, especially during slow VCC rising slew rates. For systems requiring only power-up sequencing, a capacitor at the EN pin can be used to create a delay or a resistor divider can be used to enable the device based on a certain voltage threshold. While these solutions will work for power-up, it will not power-down the flag outputs in sequential fashion since the flag outputs will simply follow the input supply. For systems requiring both power-up and power-down sequencing, an external enable signal should be used, such as a GPIO signal from a microcontroller, to properly control power-up and power-down of the flag outputs.

Do's and Don'ts (continued)

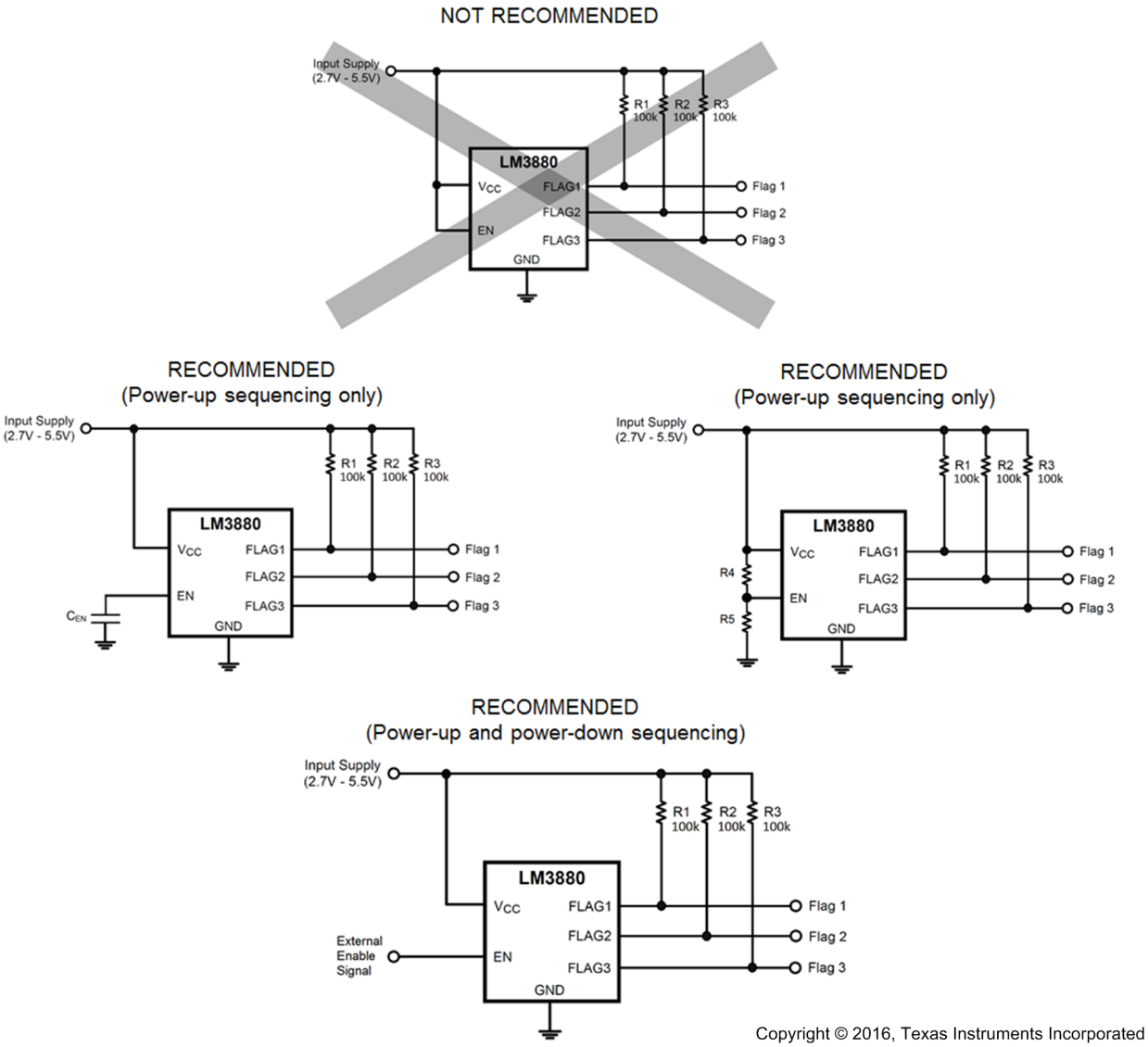


Figure 19. Recommended EN Connection

9 Power Supply Recommendations

The VCC pin should be located as close as possible to the input supply (2.7–5.5 V). An input capacitor is not required but is recommended when noise might be present on the VCC pin. A 0.1-μF ceramic capacitor may be used to bypass this noise.

10 Layout

10.1 Layout Guidelines

- Pullup resistors should be connected between the flag output pins and a positive input supply, usually VCC. An independent flag supply may also be used. These resistors should be placed as close as possible to the Simple Power Supply Sequencer and the flag supply. Minimal trace length is recommended to make the connections. A typical value for the pullup resistors is 100 kΩ.
- For very tight sequencing requirements, minimal and equal trace lengths should be used to connect the flag outputs to the desired inputs. This will reduce any propagation delay and timing errors between the flag outputs along the line.

10.2 Layout Example

Figure 20 and Figure 21 are layout examples for the LM3880. These examples are taken from the LM3880EVAL.

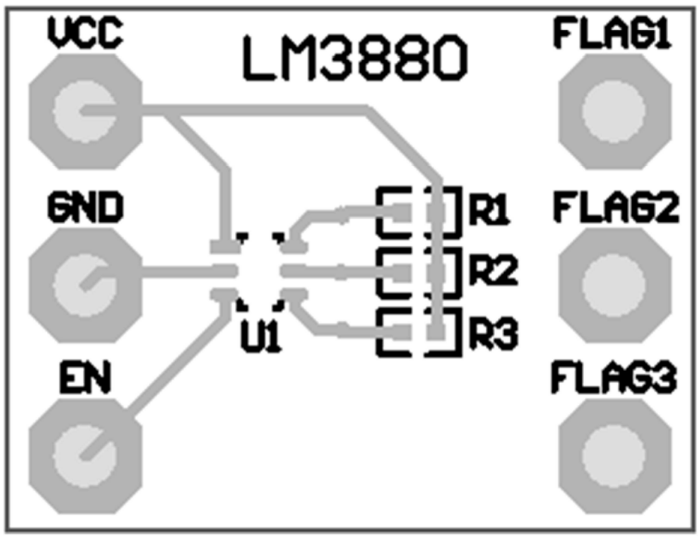


Figure 20. LM3880 Top

Layout Example (continued)

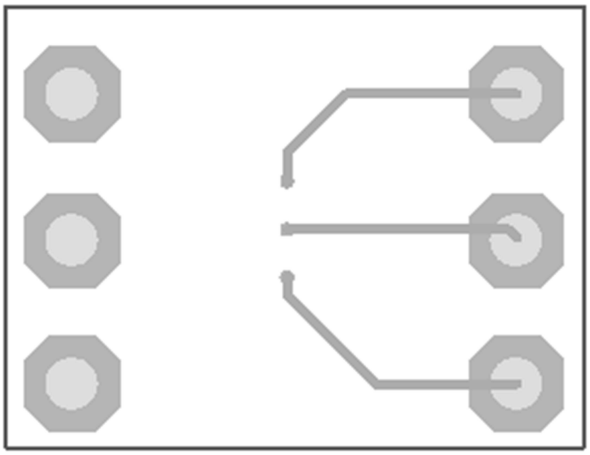


Figure 21. LM3880 Bottom

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 Device Nomenclature

The list of parts available to order appear in the Package Option Addendum.

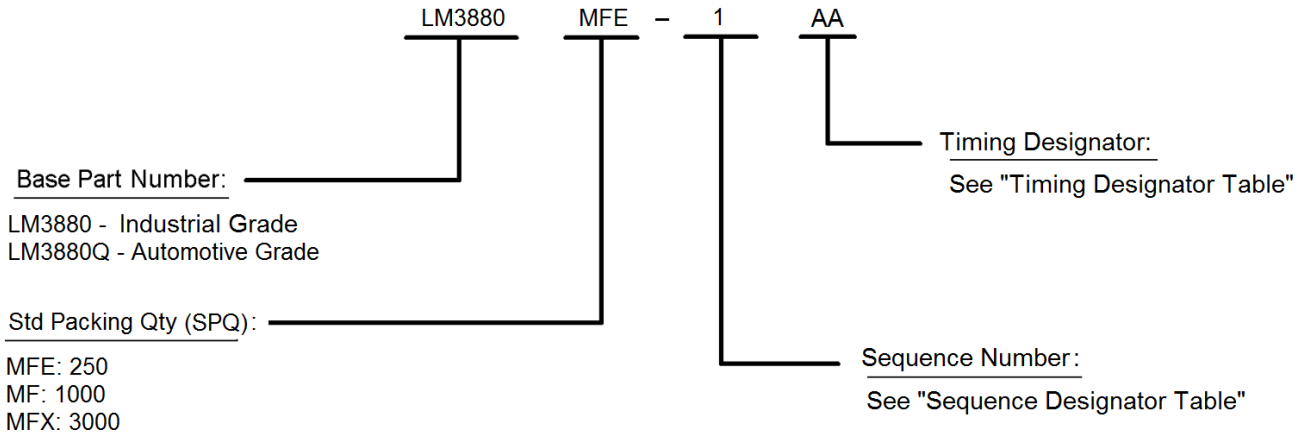


Figure 22. Device Nomenclature

Table 3. Sequence Designator Table (1)

SEQUENCE NUMBER	FLAG ORDER	
	POWER UP	POWER DOWN
1	1 - 2 - 3	3 - 2 - 1
2	1 - 2 - 3	3 - 1 - 2
3	1 - 2 - 3	2 - 3 - 1
4	1 - 2 - 3	2 - 1 - 3
5	1 - 2 - 3	1 - 3 - 2
6	1 - 2 - 3	1 - 2 - 3

(1) See Figure 1 and Figure 2.

Table 4. Timing Designator Table(1)

TIMING DESIGNATOR	DELAYS (ms)					
	t_{d1}	t_{d2}	t_{d3}	t_{d4}	t_{d5}	t_{d6}
AA	10	10	10	10	10	10
AB	30	30	30	30	30	30
AC	60	60	60	60	60	60
AD	120	120	120	120	120	120
AE	2	2	2	2	2	2
AF	16	16	16	16	16	16

(1) See Figure 1 and Figure 2.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3880MF-1AA	NRND	SOT-23	DBV	6	1000	TBD	Call TI	Call TI	-40 to 125	F20A	
LM3880MF-1AA/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F20A	Samples
LM3880MF-1AB/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F21A	Samples
LM3880MF-1AC/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F22A	Samples
LM3880MF-1AD/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F23A	Samples
LM3880MF-1AE/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F25A	Samples
LM3880MF-1AF/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F31A	Samples
LM3880MFE-1AA/NOPB	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F20A	Samples
LM3880MFE-1AB/NOPB	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F21A	Samples
LM3880MFE-1AC/NOPB	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F22A	Samples
LM3880MFE-1AD/NOPB	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F23A	Samples
LM3880MFE-1AE/NOPB	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F25A	Samples
LM3880MFE-1AF/NOPB	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F31A	Samples
LM3880MFX-1AA/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F20A	Samples
LM3880MFX-1AB/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F21A	Samples
LM3880MFX-1AC/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F22A	Samples
LM3880MFX-1AD/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F23A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3880MFX-1AE/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F25A	Samples
LM3880MFX-1AF/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F31A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LM3880 :

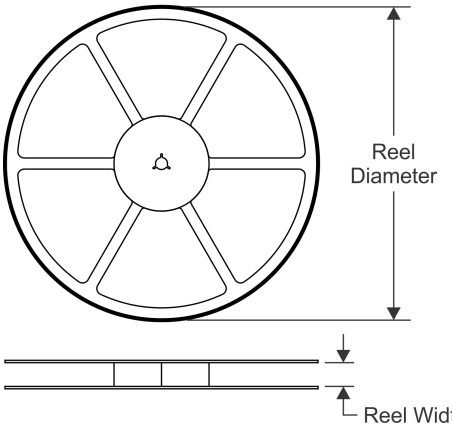
- Automotive: LM3880-Q1

NOTE: Qualified Version Definitions:

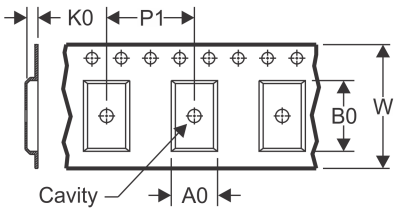
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

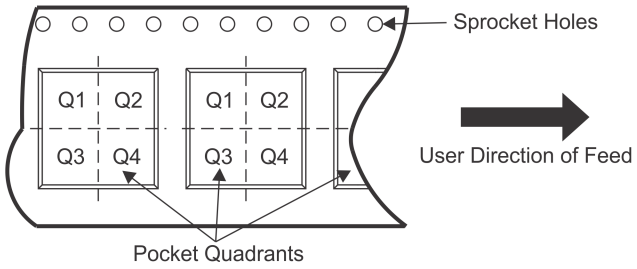


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3880MF-1AA	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3880MF-1AA/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3880MF-1AB/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3880MF-1AC/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3880MF-1AD/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3880MF-1AE/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3880MF-1AF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3880MFE-1AA/NOPB	SOT-23	DBV	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3880MFE-1AB/NOPB	SOT-23	DBV	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3880MFE-1AC/NOPB	SOT-23	DBV	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3880MFE-1AD/NOPB	SOT-23	DBV	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3880MFE-1AE/NOPB	SOT-23	DBV	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3880MFE-1AF/NOPB	SOT-23	DBV	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3880MFX-1AA/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
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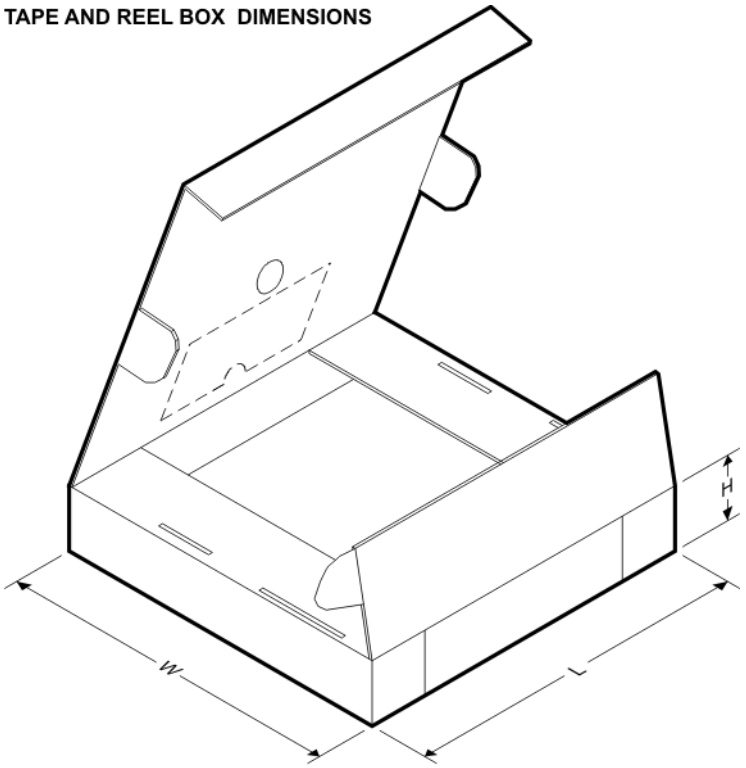
LM3880MFX-1AD/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3880MFX-1AE/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3880MFX-1AF/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3880MF-1AA	SOT-23	DBV	6	1000	210.0	185.0	35.0
LM3880MF-1AA/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
LM3880MF-1AB/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
LM3880MF-1AC/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
LM3880MF-1AD/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
LM3880MF-1AE/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
LM3880MF-1AF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
LM3880MFE-1AA/NOPB	SOT-23	DBV	6	250	210.0	185.0	35.0
LM3880MFE-1AB/NOPB	SOT-23	DBV	6	250	210.0	185.0	35.0
LM3880MFE-1AC/NOPB	SOT-23	DBV	6	250	210.0	185.0	35.0
LM3880MFE-1AD/NOPB	SOT-23	DBV	6	250	210.0	185.0	35.0
LM3880MFE-1AE/NOPB	SOT-23	DBV	6	250	210.0	185.0	35.0
LM3880MFE-1AF/NOPB	SOT-23	DBV	6	250	210.0	185.0	35.0
LM3880MFX-1AA/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0
LM3880MFX-1AB/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0
LM3880MFX-1AC/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0

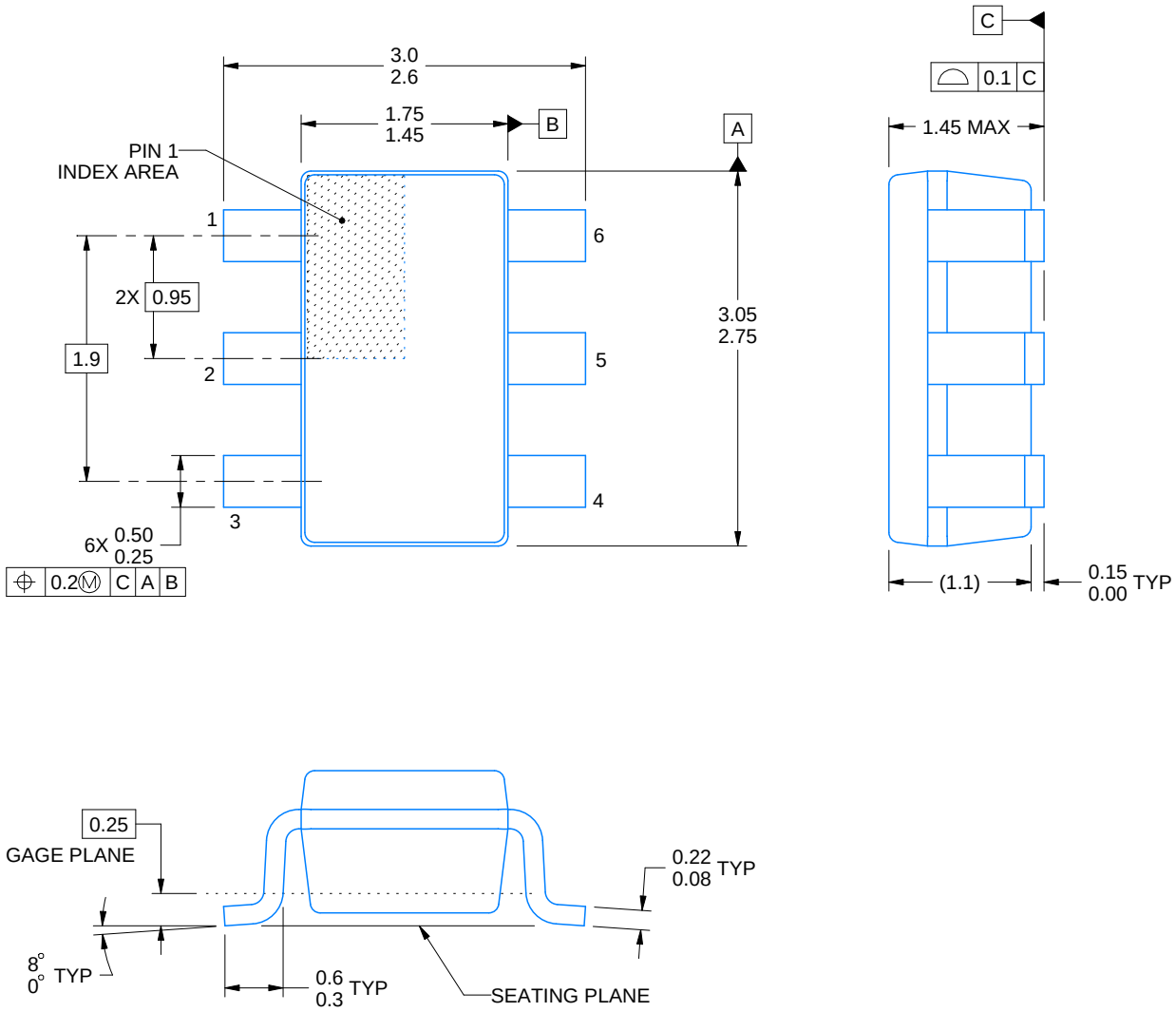
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3880MFX-1AD/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0
LM3880MFX-1AE/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0
LM3880MFX-1AF/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

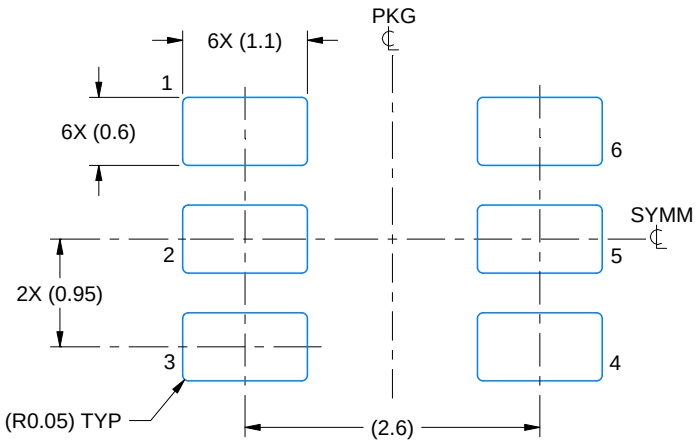
SMALL OUTLINE TRANSISTOR



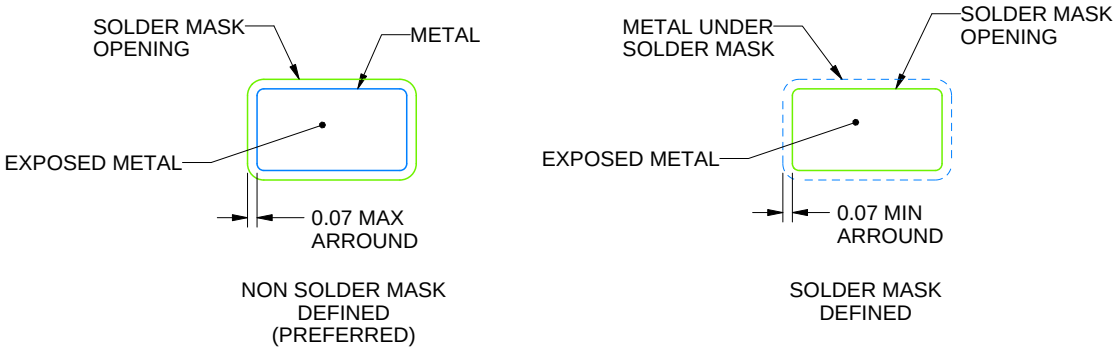
4214840/B 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

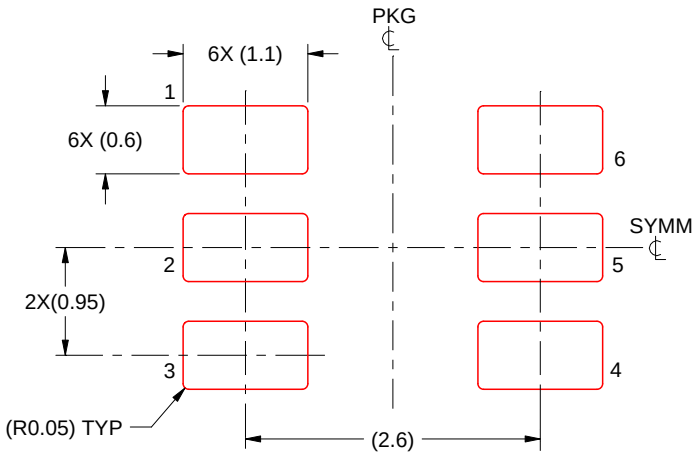


SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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