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LC87F5DC8A

CMOS IC

FROM 128K byte, RAM 4096 byte on-chip

8-bit 1-chip Microcontroller

Overview

The LC87F5DC8A is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 83.3 ns, integrate on a single chip a number of hardware features such as 128K-byte flash ROM (onboard rewritable), 4K-byte RAM, onchip debugging function, two sophisticated 16-bit timers/counters (may be divided into 8-bit timers), four 8-bit timers with a prescaler, a base timer serving as a time-of-day clock, two synchronous SIO ports (with automatic block transmission/reception capabilities), an asynchronous/synchronous SIO port, two UART ports (full duplex), four 12-bit PWM channels, an 8-bit 15-channel AD converter, a high-speed clock counter, a system clock frequency divider, and a 29-source 10-vector interrupt feature.

Features

■Flash ROM

- Single 5V power supply, on-board writeable
- Block erase in 128 byte units
- 131072 × 8 bits (LC87F5DC8A)

■RAM

- 4096 × 9 bits (LC87F5DC8A)

■ Bus Cycle Time

- 83.3ns (12MHz)

Note: Bus cycle time indicates the speed to read ROM.

■ Minimum Instruction Cycle Time (tCYC)

- 250ns (12MHz)

* This product is licensed from Silicon Storage Technology, Inc. (USA).

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■ Ports

- Normal withstand voltage I/O ports
 - Ports whose I/O direction can be designated in 1-bit units 62 (P1n, P2n, P3n, P70 to P73, P8n, PAn, PBn, PCn, S2Pn, PWM0, PWM1, XT2)
 - Ports whose I/O direction can be designated in 4-bit units 8 (P0n)
- Normal withstand voltage input port 1 (XT1)
- Dedicated oscillator ports 2 (CF1, CF2)
- Reset pins 1 ($\overline{\text{RES}}$)
- Power pins 8 (V_{SS1} to V_{SS4} , V_{DD1} to V_{DD4})

■ Timers

- Timer 0: 16-bit timer/counter with capture register
 - Mode 0: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) × 2-channels
 - Mode 1: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) + 8-bit counter (with two 8-bit capture registers)
 - Mode 2: 16-bit timer with an 8-bit programmable prescaler (with two 16-bit capture registers)
 - Mode 3: 16-bit counter (with 2 16-bit capture registers)
- Timer 1: 16-bit timer/counter that support PWM/toggle output
 - Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter (with toggle outputs)
 - Mode 1: 8-bit PWM with an 8-bit prescaler × 2-channels
 - Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also from the lower-order 8 bits)
 - Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8 bits can be used as PWM)
- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base Timer
 - 1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
 - 2) Interrupts programmable in 5 different time schemes.

■ High-speed Clock Counter

- Can count clocks with a maximum clock rate of 20MHz (at a main clock of 10MHz).
- Can generate output real-time.

■ Serial interface

- SIO0: 8 bit synchronous serial interface
 - 1) LSB first/MSB first mode selectable
 - 2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)
 - 3) Automatic continuous data transmission (1 to 256 bits)
- SIO1: 8 bit asynchronous/synchronous serial interface
 - Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
 - Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
 - Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
 - Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)
- SIO2: 8 bit synchronous serial interface
 - 1) LSB first mode
 - 2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 Tcyc)
 - 3) Automatic continuous data transmission (1 to 32 bytes)

LC87F5DC8A

■UART: 2 channels

- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2 bits in continuous transmission mode)
- Built-in baudrate generator (with baudrates of 16/3 to 8192/3 tCYC)

■AD Converter: 8 bits × 15 channels

■PWM: Multifrequency 12-bit PWM × 4 channels

■Remote Control Receiver Circuit (sharing pins with P73, INT3, and T0IN)

- Noise filtering function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)
- The noise filtering function is available for the INT3, T0IN, or T0HCP signal at P73. When P73 is read with an instruction, the signal level at that pin is read regardless of the availability of the noise filtering function.

■Watchdog Timer

- External RC watchdog timer
- Interrupt and reset signals selectable

■Interrupts

- 29 sources, 10 vector addresses

- 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
- 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector	Selectable Level	Interrupt signal
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/base timer
5	00023H	H or L	T0H/INT6
6	0002BH	H or L	T1L/T1H/INT7
7	00033H	H or L	SIO0/UART1 receive/UART2 receive
8	0003BH	H or L	SIO1/SIO2/UART1 transmit/UART2 transmit
9	00043H	H or L	ADC/T6/T7/PWM4, PWM5
10	0004BH	H or L	Port 0/T4/T5/PWM0, PWM1

- Priority levels $X > H > L$
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels: 2048 levels maximum (the stack is allocated in RAM.)

■High-speed Multiplication/Division Instructions

- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation Circuits

- RC oscillation circuit (internal): For system clock
- CF oscillation circuit: For system clock, with internal Rf
- Crystal oscillation circuit: For low-speed system clock
- Multifrequency RC oscillation circuit (internal): For system clock

LC87F5DC8A

■ System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2μs, 2.4μs, 4.8μs, 9.6μs, 19.2μs, 38.4μs, and 76.8μs (at a main clock rate of 10MHz).

■ Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
 - 1) Oscillation is not halted automatically.
 - 2) Canceled by a system reset or occurrence of interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
 - 1) The CF, RC, and crystal oscillators automatically stop operation.
 - 2) There are three ways of resetting the HOLD mode.
 - (1) Setting the reset pin to the low level.
 - (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
 - (3) Having an interrupt source established at port 0
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
 - 1) The CF and RC oscillators automatically stop operation.
 - 2) The state of crystal oscillation established when the HOLD mode is entered is retained.
 - 3) There are four ways of resetting the X'tal HOLD mode.
 - (1) Setting the reset pin to the low level.
 - (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level.
 - (3) Having an interrupt source established at port 0.
 - (4) Having an interrupt source established in the base timer circuit.

■ On-chip debugging function

- Permits software debugging with the test device installed on the target board.

■ Shipping Form

- QIP80E (14×20): Lead-free type
- TQFP80J (12×12): Lead-free type

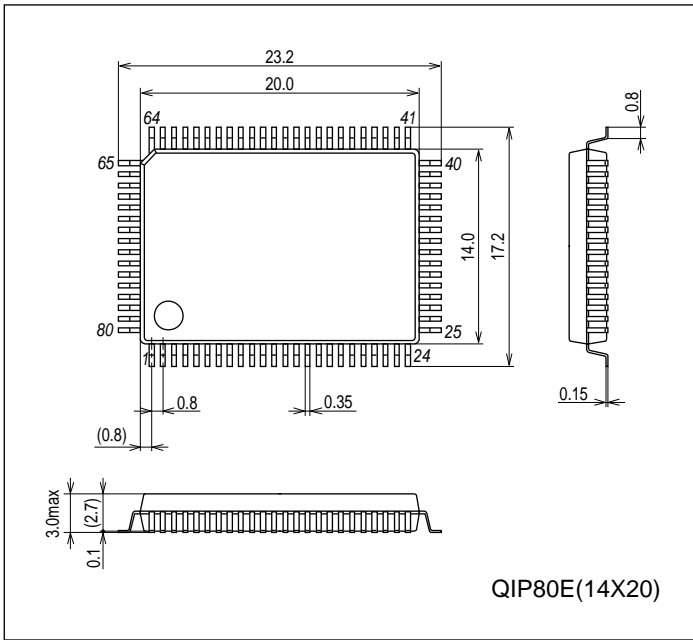
■ Development Tools

- Evaluation (EVA) chip: LC87EV690
- Emulator: EVA62S + ECB876600D + SUB875D00 + POD80QFP or POD80SQFP
ICE-B877300 + SUB875D00 + POD80QFP or POD80SQFP
- Flash ROM writer adapter: W87F54256Q(QIP80E), W87F54256SQ(TQFP80)

Package Dimensions

unit : mm (typ)

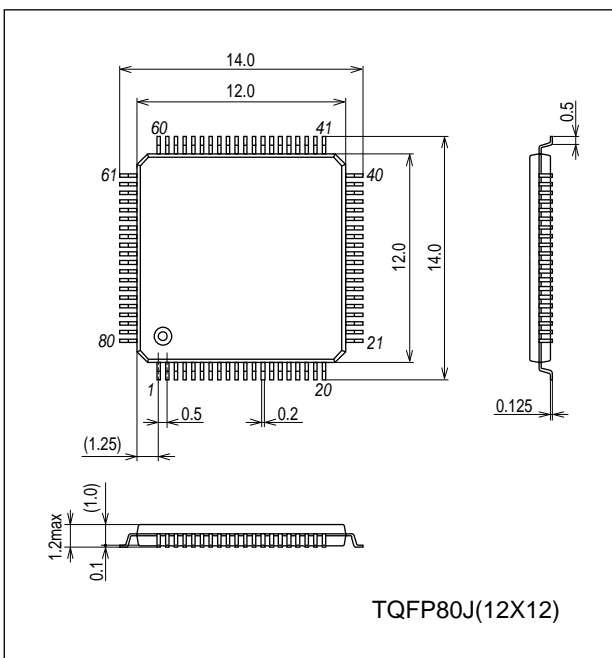
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Package Dimensions

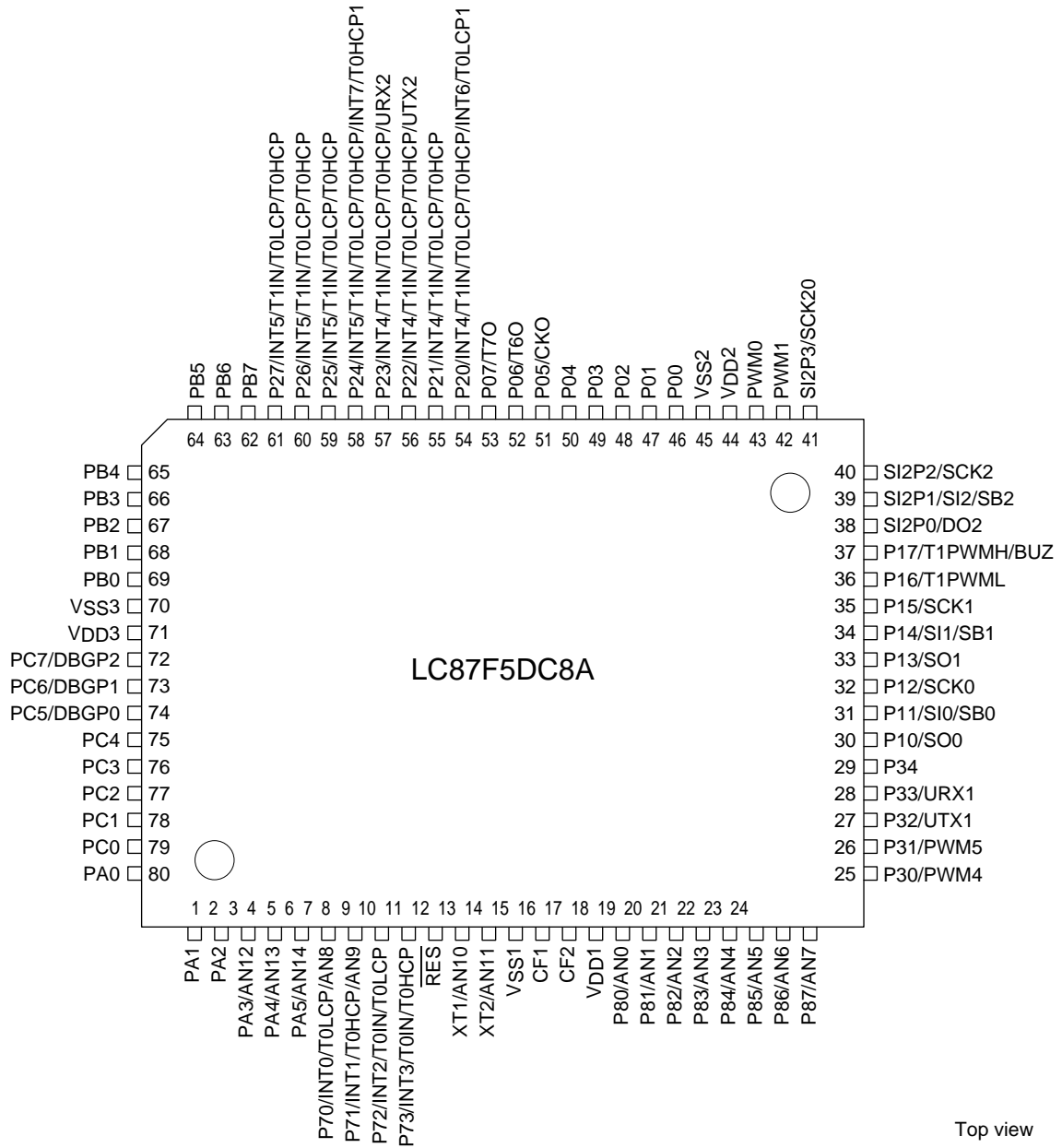
unit : mm (typ)

3290



LC87F5DC8A

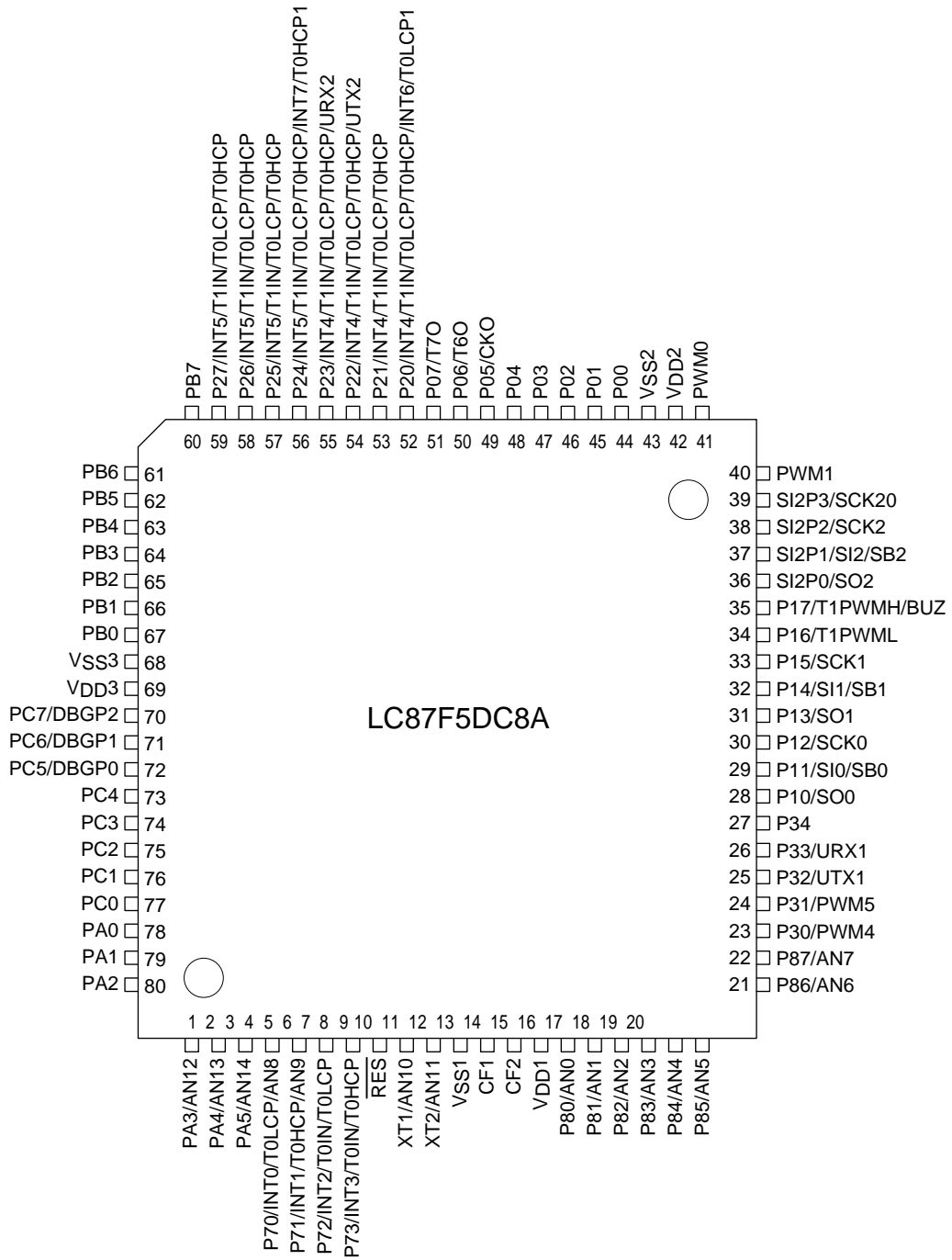
Pin Assignment



Top view

QIP80E (14x20) "Lead-free Type"

LC87F5DC8A



Top view

TQFP80J (12×12) “Lead-free Type”

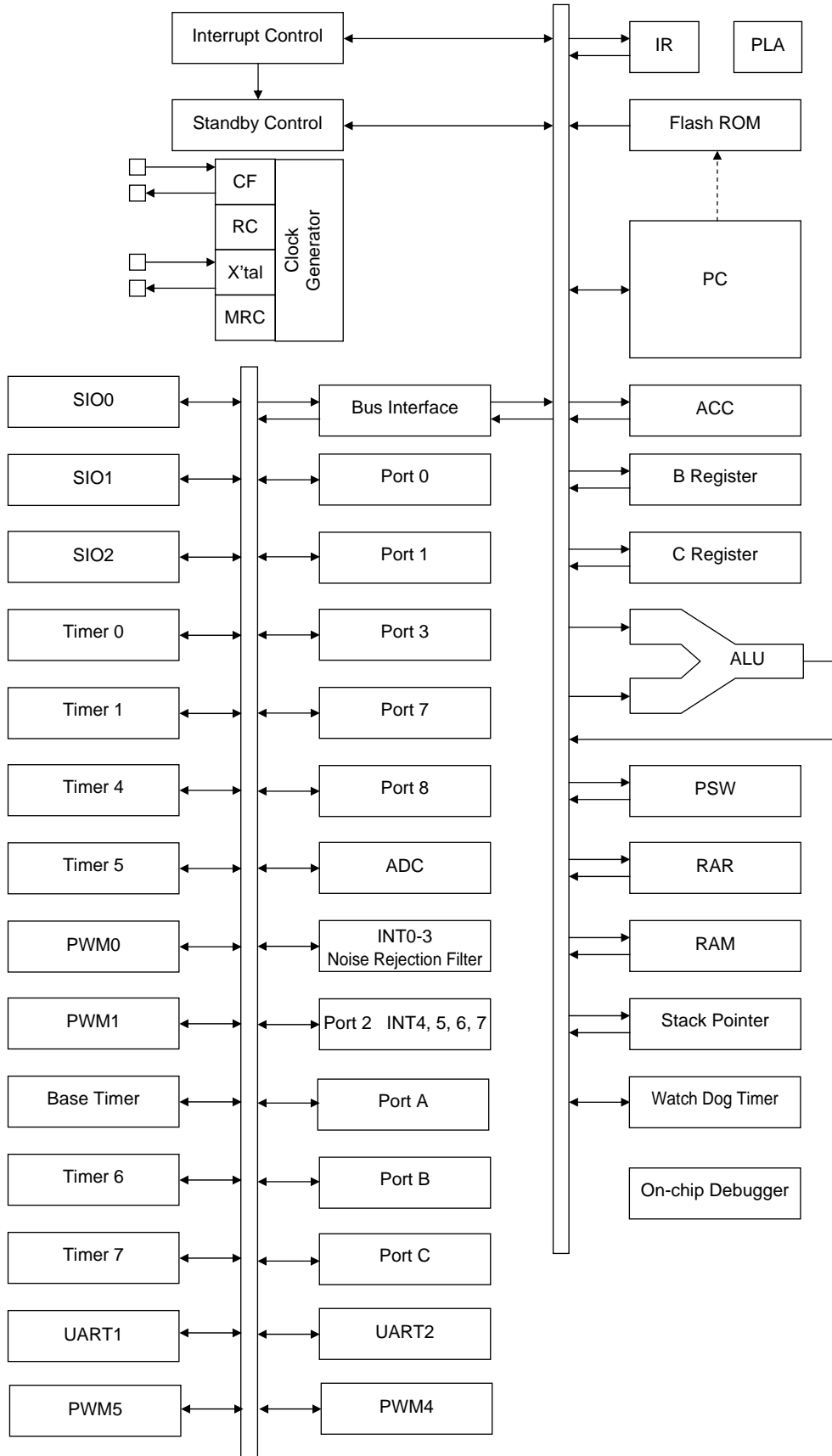
LC87F5DC8A

QIP	NAME	TQFP
1	PA1	79
2	PA2	80
3	PA3/AN12	1
4	PA4/AN13	2
5	PA5/AN14	3
6	P70/INT0/T0LCP/AN8	4
7	P71/INT1/T0HCP/AN9	5
8	P72/INT2/T0IN/T0LCP	6
9	P73/INT3/T0IN/T0HCP	7
10	RES	8
11	XT1/AN10	9
12	XT2/AN11	10
13	VSS1	11
14	CF1	12
15	CF2	13
16	VDD1	14
17	P80/AN0	15
18	P81/AN1	16
19	P82/AN2	17
20	P83/AN3	18
21	P84/AN4	19
22	P85/AN5	20
23	P86/AN6	21
24	P87/AN7	22
25	P30/PWM4	23
26	P31/PWM5	24
27	P32/UTX1	25
28	P33/URX1	26
29	P34	27
30	P10/SO0	28
31	P11/SI0/SB0	29
32	P12/SCK0	30
33	P13/SO1	31
34	P14/SI1/SB1	32
35	P15/SCK1	33
36	P16/T1PWML	34
37	P17/T1PWMH/BUZ	35
38	SI2P0/SO2	36
39	SI2P1/SI2/SB2	37
40	SI2P2/SCK2	38

QIP	NAME	TQFP
41	SI2P3/SCK20	39
42	PWM1	40
43	PWM0	41
44	VDD2	42
45	VSS2	43
46	P00	44
47	P01	45
48	P02	46
49	P03	47
50	P04	48
51	P05/CKO	49
52	P06/T6O	50
53	P07/T7O	51
54	P20/INT4/T1IN/T0LCP/T0HCP/ INT6/T0LCP1	52
55	P21/INT4/T1IN/T0LCP/T0HCP	53
56	P22/INT4/T1IN/T0LCP/T0HCP/ UTX2	54
57	P23/INT4/T1IN/T0LCP/T0HCP/ URX2	55
58	P24/INT5/T1IN/T0LCP/T0HCP/ INT7/T0HCP1	56
59	P25/INT5/T1IN/T0LCP/T0HCP	57
60	P26/INT5/T1IN/T0LCP/T0HCP	58
61	P27/INT5/T1IN/T0LCP/T0HCP	59
62	PB7	60
63	PB6	61
64	PB5	62
65	PB4	63
66	PB3	64
67	PB2	65
68	PB1	66
69	PB0	67
70	VSS3	68
71	VDD3	69
72	PC7/DBGP2	70
73	PC6/DBGP1	71
74	PC5/DBGP0	72
75	PC4	73
76	PC3	74
77	PC2	75
78	PC1	76
79	PC0	77
80	PA0	78

LC87F5DC8A

System Block Diagram



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Pin Description

Name	I/O	Function description	Option																														
V _{SS1} V _{SS2} V _{SS3}	-	Power supply pin (-)	No																														
V _{DD1} V _{DD2} V _{DD3}	-	Power supply pin (+)	No																														
Port 0 P00 to P07	I/O	<ul style="list-style-type: none"> 8-bit I/O port I/O specifiable in 4-bit units Pull-up resistors can be turned on and off in 4-bit units HOLD release input Port 0 interrupt input Pin functions <ul style="list-style-type: none"> P05 :System clock output P06 : Timer 6 toggle output P07 : Timer 7 toggle output 	Yes																														
Port 1 P10 to P17	I/O	<ul style="list-style-type: none"> 8-bit I/O port I/O specifiable in 1-bit units Pull-up resistors can be turned on and off in 1-bit units Pin functions <ul style="list-style-type: none"> P10 : SIO0 data output P11 : SIO0 data input, bus I/O P12 : SIO0 clock I/O P13 : SIO1 data output P14 : SIO1 data input, bus I/O P15 : SIO1 clock I/O P16 : Timer 1PWML output P17 : Timer 1PWMLH output, beeper output 	Yes																														
Port 2 P20 to P27	I/O	<ul style="list-style-type: none"> 8-bit I/O port I/O specifiable in 1-bit units Pull-up resistors can be turned on and off in 1-bit units Other functions <ul style="list-style-type: none"> P20 : INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input/INT6 input/timer 0L capture 1 input P21 : INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input P22 : INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input/UART2 transmit P23 : INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input/UART2 receive P24 : INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input/INT7 input/timer 0H capture 1 input P25 to P27 : INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/timer 0H capture input Interrupt acknowledge type <p>Interrupt acknowledge type</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th></th> <th>Rising</th> <th>Falling</th> <th>Rising & Falling</th> <th>H level</th> <th>L level</th> </tr> </thead> <tbody> <tr> <td>INT4</td> <td>Y</td> <td>Y</td> <td>Y</td> <td>N</td> <td>N</td> </tr> <tr> <td>INT5</td> <td>Y</td> <td>Y</td> <td>Y</td> <td>N</td> <td>N</td> </tr> <tr> <td>INT6</td> <td>Y</td> <td>Y</td> <td>Y</td> <td>N</td> <td>N</td> </tr> <tr> <td>INT7</td> <td>Y</td> <td>Y</td> <td>Y</td> <td>N</td> <td>N</td> </tr> </tbody> </table>		Rising	Falling	Rising & Falling	H level	L level	INT4	Y	Y	Y	N	N	INT5	Y	Y	Y	N	N	INT6	Y	Y	Y	N	N	INT7	Y	Y	Y	N	N	Yes
	Rising	Falling	Rising & Falling	H level	L level																												
INT4	Y	Y	Y	N	N																												
INT5	Y	Y	Y	N	N																												
INT6	Y	Y	Y	N	N																												
INT7	Y	Y	Y	N	N																												
Port 3 P30 to P34	I/O	<ul style="list-style-type: none"> 5-bit I/O port I/O specifiable in 1-bit units Pull-up resistor can be turned on and off in 1-bit units Pin functions <ul style="list-style-type: none"> P30: PWM4 output P31: PWM5 output P32: UART1 transmit P33: UART1 receive 	Yes																														

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LC87F5DC8A

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Pin Name	I/O	Function description	Option																														
Port 7 P70 to P73	I/O	<ul style="list-style-type: none"> • 4-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units • Other functions <p>P70 : INT0 input/HOLD release input/timer 0L capture input/Output for watchdog timer P71 : INT1 input/HOLD release input/timer 0H capture input P72 : INT2 input/HOLD release input/timer 0 event input/timer 0L capture input P73 : INT3 input with noise filter/timer 0 event input/timer 0H capture input</p> <p>Interrupt acknowledge type</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th></th> <th>Rising</th> <th>Falling</th> <th>Rising & Falling</th> <th>H level</th> <th>L level</th> </tr> </thead> <tbody> <tr> <td>INT0</td> <td>Y</td> <td>Y</td> <td>N</td> <td>Y</td> <td>Y</td> </tr> <tr> <td>INT1</td> <td>Y</td> <td>Y</td> <td>N</td> <td>Y</td> <td>Y</td> </tr> <tr> <td>INT2</td> <td>Y</td> <td>Y</td> <td>Y</td> <td>N</td> <td>N</td> </tr> <tr> <td>INT3</td> <td>Y</td> <td>Y</td> <td>Y</td> <td>N</td> <td>N</td> </tr> </tbody> </table> <ul style="list-style-type: none"> • AD converter input port : AN8 (P70), AN9 (P71) 		Rising	Falling	Rising & Falling	H level	L level	INT0	Y	Y	N	Y	Y	INT1	Y	Y	N	Y	Y	INT2	Y	Y	Y	N	N	INT3	Y	Y	Y	N	N	No
	Rising	Falling	Rising & Falling	H level	L level																												
INT0	Y	Y	N	Y	Y																												
INT1	Y	Y	N	Y	Y																												
INT2	Y	Y	Y	N	N																												
INT3	Y	Y	Y	N	N																												
Port 8 P80 to P87	I/O	<ul style="list-style-type: none"> • 8-bit I/O port • I/O specifiable in 1-bit units • Other functions <p>P80 to P87: AD converter input port</p>	No																														
Port A PA0 to PA5	I/O	<ul style="list-style-type: none"> • 6-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units 	Yes																														
Port B PB0 to PB7	I/O	<ul style="list-style-type: none"> • 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units 	Yes																														
Port C PC0 to PC7	I/O	<ul style="list-style-type: none"> • 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units • Pin functions <p>PC5 to PC7 : On-chip Debugger</p>	Yes																														
SIO2 Port SI2P0 to SI2P3	I/O	<ul style="list-style-type: none"> • 4-bit I/O port • I/O specifiable in 1-bit units • Shared functions: <p>SI2P0: SIO2 data output SI2P1: SIO2 data input, bus input/output SI2P2: SIO2 clock input/output SI2P3: SIO2 clock output</p>	No																														
PWM0	O	<ul style="list-style-type: none"> • PWM0 output port • General-purpose I/O available 	No																														
PWM1	O	<ul style="list-style-type: none"> • PWM1 output port • General-purpose I/O available 	No																														
$\overline{\text{RES}}$	I	Reset pin	No																														
XT1	I	<ul style="list-style-type: none"> • Input terminal for 32.768kHz X'tal oscillation • Shared functions: <p>AN10: AD converter input port General-purpose input port Must be connected to VDD1 if not to be used</p>	No																														
XT2	I/O	<ul style="list-style-type: none"> • Output terminal for 32.768kHz X'tal oscillation • Shared functions: <p>AN11: AD converter input port General-purpose I/O port Must be set for oscillation and kept open if not to be used</p>	No																														
CF1	I	Ceramic resonator input pin	No																														
CF2	O	Ceramic resonator output pin	No																														

LC87F5DC8A

Port Output Configuration

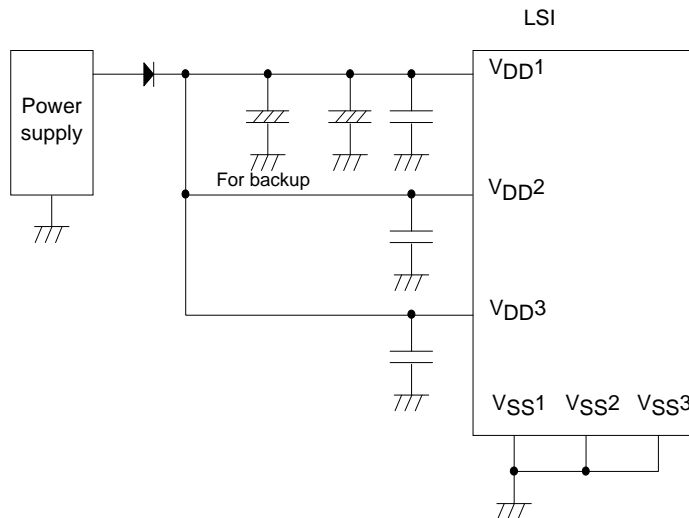
The table below lists the types of port outputs and the presence/absence of a pull-up resistor. Data can be read into any input port even if it is in the output mode.

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-Up Resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	N-channel open drain	No
P10 to P17 P20 to P27 P30 to P34	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
PA0 to PA5 PB0 to PB7 PC0 to PC7	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
P70	-	No	N-channel open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
P80 to P87	-	No	N-channel open drain	No
SI2P0, SI2PS SI2P3 PWM0, PWM1	-	No	CMOS	No
SI2P1	-	No	CMOS (When selected as ordinary port) N-channel open drain (When SIO2 data is selected)	No
XT1	-	No	Input only	No
XT2	-	No	Output for 32.768kHz quartz oscillator N-channel open drain (when in general-purpose output mode)	No

Note 1: Programmable pull-up resistors for port 0 are controlled in 4-bit units (P00 to 03, P04 to 07).

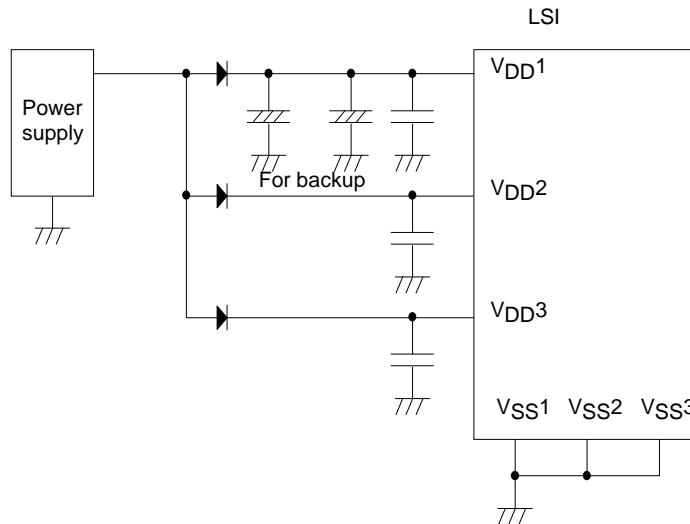
*1: Make the following connection to minimize the noise input to the VDD1 pin and prolong the backup time. Be sure to electrically short the VSS1, VSS2, and VSS3 pins.

Example 1: When backup is active in the HOLD mode, the high level of the port outputs is supplied by the backup capacitors.



LC87F5DC8A

Example 2: The high-level output at the ports is unstable when the HOLD mode backup is in effect.



Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS1} = V_{SS2} = V_{SS3} = 0\text{V}$

Parameter	Symbol	Pins/Remarks	Conditions	Specification				
				$V_{DD}[\text{V}]$	min	typ	max	unit
Maximum Supply voltage	$V_{DD\text{MAX}}$	V_{DD1} , V_{DD2} , V_{DD3}	$V_{DD1}=V_{DD2}=V_{DD3}$		-0.3		+6.5	V
Input voltage	$V_I(1)$	XT1, CF1			-0.3		$V_{DD}+0.3$	
Input/Output Voltage	$V_{IO}(1)$	Ports 0, 1, 2 Ports 3, 7, 8 Ports A, B, C SI2P0 to SI2P3 PWM0, PWM1, XT2			-0.3		$V_{DD}+0.3$	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2, 3 Ports A, B, C SI2P0 to SI2P3	CMOS output select per 1 application pin		-10		mA
		IOPH(2)	PWM0, PWM1	Per 1 application pin		-20		
		IOPH(3)	P71 to P73	Per 1 application pin		-5		
	Average output current (Note1-1)	IOM(1)	Ports 0, 1, 2, 3 Ports A, B, C SI2P0 to SI2P3	CMOS output select per 1 application pin		-7.5		
		IOM(2)	PWM0, PWM1	Per 1 application pin		-15		
		IOM(3)	P71 to P73	Per 1 application pin		-3		
	Total output current	$\Sigma\text{IOAH}(1)$	P71 to P73	Total of all applicable pins		-10		
		$\Sigma\text{IOAH}(2)$	Ports 1, 3 PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins		-25		
		$\Sigma\text{IOAH}(3)$	Ports 0	Total of all applicable pins		-25		
		$\Sigma\text{IOAH}(4)$	Port 0, 1, 3 PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins		-45		
		$\Sigma\text{IOAH}(5)$	Ports 2, B	Total of all applicable pins		-25		
		$\Sigma\text{IOAH}(6)$	Ports A, C	Total of all applicable pins		-25		
		$\Sigma\text{IOAH}(7)$	Ports 2, A, B, C	Total of all applicable pins		-45		

Note 1-1: Average output current is average of current in 100ms interval.

Continued on next page.

LC87F5DC8A

Continued from preceding page.

Parameter	Symbol	Pins/Remarks	Conditions	Specification				unit
				V _{DD} [V]	min	typ	max	
Low level output current	Peak output current	IOPL(1)	P02-P07 Ports 1, 2, 3 Ports A, B, C SI2P0 to SI2P3 PWM0, PWM1	Per 1 application pin			20	mA
		IOPL(2)	P00, P01	Per 1 application pin			30	
		IOPL(3)	Ports 7, 8, XT2	Per 1 application pin			10	
	Average output current (Note1-1)	IOML(1)	P02-P07 Ports 1, 2, 3 Ports A, B, C SI2P0 to SI2P3 PWM0, PWM1	Per 1 application pin			15	
		IOML(2)	P00, P01	Per 1 application pin			20	
		IOML(3)	Ports 7, 8, XT2	Per 1 application pin			7.5	
	Total output current	ΣIOAL(1)	Port 7, XT2	Total of all applicable pins			15	
		ΣIOAL(2)	Port 8	Total of all applicable pins			15	
		ΣIOAL(3)	Ports 7, 8, XT2	Total of all applicable pins			20	
		ΣIOAL(4)	Port 1, 3 PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins			45	
ΣIOAL(5)		Port 0	Total of all applicable pins			45		
ΣIOAL(6)		Port 0, 1, 3 PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins			80		
ΣIOAL(7)		Ports 2, B	Total of all applicable pins			45		
ΣIOAL(8)		Ports A, C	Total of all applicable pins			45		
ΣIOAL(9)		Ports 2, A, B, C	Total of all applicable pins			80		
Maximum power Consumption	Pdmax	QIP80E				368	mW	
		TQFP80J				325		
Operating temperature range	Topr				-20	70	°C	
Storage temperature range	Tstg				-55	125		

Note 1-1: Average output current is average of current in 100ms interval.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

LC87F5DC8A

Recommended Operating Range at $T_a = -20^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{SS1} = V_{SS2} = V_{SS3} = 0\text{V}$

Parameter	Symbol	Pins/Remarks	Conditions	Specification				unit
				V_{DD} [V]	min	typ	max	
Operating supply voltage (Note2-1)	$V_{DD}(1)$	$V_{DD1}=V_{DD2}=V_{DD3}$	$0.245\mu\text{s} \leq t_{CYC} \leq 200\mu\text{s}$		2.8		5.5	V
			$0.367\mu\text{s} \leq t_{CYC} \leq 200\mu\text{s}$		2.5		5.5	
			$1.47\mu\text{s} \leq t_{CYC} \leq 200\mu\text{s}$		2.2		5.5	
Memory sustaining supply voltage	VHD	$V_{DD1}=V_{DD2}=V_{DD3}$	RAM and register contents in HOLD mode.		2.0		5.5	
High level input voltage	$V_{IH}(1)$	Ports 1, 2, 3 SI2P0 to SI2P3 P71 to P73 P70 port input/ interrupt side		2.2 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	V
	$V_{IH}(2)$	Ports 0, 8 Ports A, B, C PWM0,PWM1		2.2 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(3)$	P70 Watchdog timer side		2.2 to 5.5	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(4)$	XT1, XT2, CF1, RES		2.2 to 5.5	$0.75V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Ports 1, 2, 3 SI2P0 to SI2P3		2.2 to 5.5	V_{SS}		$0.1V_{DD}$ +0.4	V
	$V_{IL}(2)$	P71 to P73 P70 port input/ interrupt		2.2 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(3)$	Ports 0, 8 Ports A, B, C		4.0 to 5.5	V_{SS}		$0.15V_{DD}$ +0.4	
	$V_{IL}(4)$	PWM0,PWM1		2.2 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(5)$	Port 70 Watchdog Timer		2.2 to 5.5	V_{SS}		$0.8V_{DD}$ -1.0	
	$V_{IL}(6)$	XT1, XT2, CF1, RES		2.2 to 5.5	V_{SS}		$0.25V_{DD}$	
Instruction cycle time	t_{CYC} (Note2-2)			2.8 to 5.5	0.245		200	μs
				2.5 to 5.5	0.367		200	
				2.2 to 5.5	1.470		200	
External system clock frequency	FEXCF(1)	CF1	<ul style="list-style-type: none"> • CF2 pin open • System clock frequency division rate = 1/1 • External system clock duty = $50\pm 5\%$ 	2.8 to 5.5	0.1		12	MHz
				2.5 to 5.5	0.1		8	
				2.2 to 5.5	0.1		2	
				2.8 to 5.5	0.2		24.4	
				2.5 to 5.5	0.2		16	
				2.2 to 5.5	0.2		4	
Oscillation frequency Range (Note2-3)	FmCF(1)	CF1, CF2	12MHz ceramic oscillation See Fig. 1.	2.8 to 5.5		12		MHz
	FmCF(2)	CF1, CF2	8MHz ceramic oscillation See Fig. 1.	2.5 to 5.5		8		
	FmCF(3)	CF1, CF2	4MHz ceramic oscillation See Fig. 1.	2.2 to 5.5		4		
	FmRC		Internal RC oscillation	2.2 to 5.5	0.3	1.0	2.0	
	FmMRC		Frequency variable RC oscillation source oscillation	2.2 to 5.5		16		
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation. See Fig. 2.	2.2 to 5.5		32.768		

Note 2-1: V_{DD} must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

Note 2-2: Relationship between t_{CYC} and oscillation frequency is $3/F_{mCF}$ at a division ratio of 1/1 and $6/F_{mCF}$ at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

LC87F5DC8A

Electrical Characteristics at Ta = -20°C to +70°C, VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
High level input current	I _{IH} (1)	Ports 0, 1, 2 Ports 3, 7, 8 Ports A, B, C SI2P0 to SI2P3 RES PWM0, PWM1	Output disable Pull-up resistor OFF V _{IN} =V _{DD} (including the off-leak current of the output Tr.)	2.2 to 5.5			1	μA
	I _{IH} (2)	XT1, XT2	Using as an input port V _{IN} =V _{DD}	2.2 to 5.5			1	
	I _{IH} (3)	CF1	V _{IN} =V _{DD}	2.2 to 5.5			15	
Low level input current	I _{IL} (1)	Ports 0, 1, 2 Ports 3, 7, 8 Ports A, B, C SI2P0 to SI2P3 RES PWM0, PWM1	Output disable Pull-up resistor OFF V _{IN} =V _{SS} (including the off-leak current of the output Tr.)	2.2 to 5.5	-1			μA
	I _{IL} (2)	XT1, XT2	Using as an input port V _{IN} =V _{SS}	2.2 to 5.5	-1			
	I _{IL} (3)	CF1	V _{IN} =V _{SS}	2.2 to 5.5	-15			
High level output voltage	V _{OH} (1)	Ports 0, 1, 2, 3	I _{OH} =-1.0mA	4.5 to 5.5	V _{DD} -1			V
	V _{OH} (2)	Ports A, B, C	I _{OH} =-0.4mA	3.0 to 5.5	V _{DD} -0.4			
	V _{OH} (3)	SI2P0 to SI2P	I _{OH} =-0.2mA	2.2 to 5.5	V _{DD} -0.4			
	V _{OH} (4)	Ports 71, 72, 73	I _{OH} =-0.4mA	3.0 to 5.5	V _{DD} -0.4			
	V _{OH} (5)		I _{OH} =-0.2mA	2.2 to 5.5	V _{DD} -0.4			
	V _{OH} (6)	PWM0, PWM1	I _{OH} =-10mA	4.5 to 5.5	V _{DD} -1.5			
	V _{OH} (7)	P30, P31(PWM4,5 output mode)	I _{OH} =-1.6mA	3.0 to 5.5	V _{DD} -0.4			
	V _{OH} (8)		I _{OH} =-1.0mA	2.2 to 5.5	V _{DD} -0.4			
Low level output voltage	V _{OL} (1)	Ports 0, 1, 2, 3	I _{OL} =10mA	4.5 to 5.5			1.5	V
	V _{OL} (2)	Ports A, B, C	I _{OL} =1.6mA	3.0 to 5.5			0.4	
	V _{OL} (3)	SI2P0 to SI2P3 PWM0, PWM1	I _{OL} =1.0mA	2.2 to 5.5			0.4	
	V _{OL} (4)	P00, P01	I _{OL} =30mA	4.5 to 5.5			1.5	
	V _{OL} (5)		I _{OL} =5.0mA	3.0 to 5.5			0.4	
	V _{OL} (6)		I _{OL} =2.5mA	2.2 to 5.5			0.4	
	V _{OL} (7)	Ports 7, 8, XT2	I _{OL} =1.6mA	3.0 to 5.5			0.4	
	V _{OL} (8)		I _{OL} =1.0mA	2.2 to 5.5			0.4	
Pull-up resistation	R _{pu}	Ports 0, 1, 2, 3 Port 7 Ports A, B, C	V _{OH} =0.9V _{DD}	2.2 to 5.5	15	40	70	kΩ
Hysteresis Voltage	V _{HIS}	RES Ports 1, 2, 7 SI2P0 to SI2P3		2.2 to 5.5		0.1V _{DD}		V
Pin capacitance	CP	All pins	<ul style="list-style-type: none"> • For pins other than that under test : V_{IN}=V_{SS} • f=1MHz • Ta=25°C 	2.2 to 5.5		10		pF

LC87F5DC8A

Serial I/O Characteristics at Ta=-20 to +70°C, V_{SS1}=V_{SS2}=V_{SS3}=0V

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter		Symbol	Pins/ Remarks	Conditions	V _{DD} [V]	Specification				
						min	typ	max	unit	
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	<ul style="list-style-type: none"> • See Fig. 6. 	2.2 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1a)	<ul style="list-style-type: none"> • Continuous data transmission/reception mode • SIO2 is not in use simultaneous. • See Fig. 6. • (Note 4-1-2) 			4			
		tSCKHA(1b)	<ul style="list-style-type: none"> • Continuous data transmission/reception mode • SIO2 is in use simultaneous. • See Fig. 6. • (Note 4-1-2) 	6						
	Output clock	Frequency	tSCK(2)	SCK0(P12)	<ul style="list-style-type: none"> • CMOS output selected. • See Fig. 6. 	2.2 to 5.5	4/3			tSCK
		Low level pulse width	tSCKL(2)				1/2			
		High level pulse width	tSCKH(2)				1/2			
tSCKHA(2a)			<ul style="list-style-type: none"> • Continuous data transmission/reception mode • SIO2 is not in use simultaneous. • CMOS output selected. • See Fig. 6. 	tSCKH(2) +2tCYC				tSCKH(2) + (10/3)tCYC	tCYC	
	tSCKHA(2b)	<ul style="list-style-type: none"> • Continuous data transmission/reception mode • SIO2 is in use simultaneous. • CMOS output selected. • See Fig. 6. 	tSCKH(2) +2tCYC		tSCKH(2) + (16/3)tCYC	tCYC				
Serial input	Data setup time	tsDI(1)	SI0(P11), SB0(P11)	<ul style="list-style-type: none"> • Must be specified with respect to rising edge of SIOCLK • See fig. 6. 	2.2 to 5.5	0.03				
	Data hold Time	thDI(1)				0.03				
Serial output	Input clock	Output delay time	tdD0(1)	<ul style="list-style-type: none"> • Continuous data transmission/reception mode • (Note 4-1-3) 	2.2 to 5.5			(1/3)tCYC +0.05	μs	
			tdD0(2)			<ul style="list-style-type: none"> • Synchronous 8-bit mode. • (Note 4-1-3) 				1tCYC +0.05
	Output clock	tdD0(3)	<ul style="list-style-type: none"> • (Note 4-1-3) 				(1/3)tCYC +0.05			

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SIORUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

LC87F5DC8A

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter		Symbol	Pins/ Remarks	Conditions	V _{DD} [V]	Specification				
						min	typ	max	unit	
Serial clock	Input clock	Frequency	Tsck(3)	SCK1(P15)	• See Fig. 6.	2.2 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected. • See Fig. 6.	2.2 to 5.5	2			tSCK
		Low level pulse width	tSCKL(4)				1/2			
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time	tsDI(2)	SI1(P14), SB1(P14)	• Must be specified with respect to rising edge of SIOCLK • See fig. 6.	2.2 to 5.5	0.03				
	Data hold time	thDI(2)				0.03				
Serial output	Output delay time	tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6.	2.2 to 5.5			(1/3)tCYC +0.05	μs	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

LC87F5DC8A

3. SIO2 Serial I/O Characteristics (Note 4-3-1)

Parameter	Symbol	Pins/ Remarks	Conditions	V _{DD} [V]	Specification										
					min	typ	max	unit							
Serial clock	Input clock	Frequency	tSCK(5)	SCK2 (SI2P2)	2.2 to 5.5				tCYC						
		Low level pulse width	tSCKL(5)							• See Fig. 6.	2				
		High level pulse width	tSCKH(5)								1				
	Output clock	Frequency	tSCK(6)	SCK2 (SI2P2), SCK2O (SI2P3)		2.2 to 5.5					tSCK				
			Low level pulse width									tSCKL(6)	• CMOS output selected. • See Fig. 6.	4/3	
			High level pulse width									tSCKH(6)		1/2	
Serial input	Input clock	tSCKHA(5a)	SCK2 (SI2P2)	2.2 to 5.5				tCYC							
		tSCKHA(5b)							• Continuous data transmission/ reception mode of SIO0 is not in use simultaneous. • See Fig. 6. • (Note 4-3-2)	4					
									• Continuous data transmission/ reception mode of SIO0 is in use simultaneous. • See Fig. 6. • (Note 4-3-2)	7					
	Output clock	Frequency	tSCK(6)		SCK2 (SI2P2), SCK2O (SI2P3)	2.2 to 5.5					tCYC				
			Low level pulse width									tSCKL(6)	• Continuous data transmission/ reception mode of SIO0 is not in use simultaneous. • CMOS output selected. • See Fig. 6.	tSCKH(6) + (5/3)tCYC	tSCKH(6) + (10/3)tCYC
			High level pulse width									tSCKH(6)	• Continuous data transmission/ reception mode of SIO0 is in use simultaneous. • CMOS output selected. • See Fig. 6.	tSCKH(6) + (5/3)tCYC	tSCKH(6) + (19/3)tCYC
Serial input	Data setup time	tsDI(3)	SI2(SI2P1), SB2(SI2P1)	2.2 to 5.5				μs							
	Data hold Time	thDI(3)							• Must be specified with respect to rising edge of SIOCLK • See fig. 6.	0.03					
Serial output	Output delay time	tdD0(5)	SO2 (SI2P0), SB2(SI2P1)	2.2 to 5.5				μs							
										• Must be specified with respect to falling edge of SIOCLK • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6.	(1/3)tCYC +0.05				

Note 4-3-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-3-2: To use serial-clock-input, a time from SI2RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

LC87F5DC8A

Pulse Input Conditions at Ta = -20°C to +70°C, VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P20 to P23), INT5(P24 to P27), INT6(P20), INT7(P24)	<ul style="list-style-type: none"> Interrupt source flag can be set. Event inputs for timer 0 or 1 are enabled. 	2.2 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	<ul style="list-style-type: none"> Interrupt source flag can be set. Event inputs for timer 0 are enabled. 	2.2 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) (The noise rejection clock is selected to 1/32.)	<ul style="list-style-type: none"> Interrupt source flag can be set. Event inputs for timer 0 are enabled. 	2.2 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) (The noise rejection clock is selected to 1/128.)	<ul style="list-style-type: none"> Interrupt source flag can be set. Event inputs for timer 0 are enabled. 	2.2 to 5.5	256			
	tPIL(5)	RES	Reset acceptable.	2.2 to 5.5	200			μs

AD Converter Characteristics at Ta = -20°C to +70°C, VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
Resolution	N	AN0(P80) to AN7(P87), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2), AN12(PA3), AN13(PA4), AN14(PA5)		3.0 to 5.5		8		bit
Absolute precision	ET		(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD		AD conversion time=32 × tCYC (when ADCR2=0) (Note 6-2)	4.5 to 5.5	11.74 (tCYC=0.367μs)		97.92 (tCYC=3.06μs)	μs
				3.0 to 5.5	31.36 (tCYC=0.980μs)		97.92 (tCYC=3.06μs)	
			4.5 to 5.5	15.68 (tCYC=0.245μs)		97.92 (tCYC=1.53μs)		
							3.0 to 5.5	
Analog input voltage range	VAIN			3.0 to 5.5	V _{SS}		V _{DD}	V
Analog port input current	I _{AINH}		VAIN=V _{DD}	3.0 to 5.5			1	μA
	I _{AINL}		VAIN=V _{SS}	3.0 to 5.5	-1			

Note 6-1: The quantization error ($\pm 1/2\text{LSB}$) is excluded from the absolute accuracy value.

Note 6-2: The conversion time refers to the interval from the time the instruction for starting the converter is issued till the complete digital value corresponding to the analog input value is loaded in the required register.

LC87F5DC8A

Consumption Current Characteristics at Ta = -20°C to +70°C, VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	VDD1 =VDD2 =VDD3	<ul style="list-style-type: none"> FmCF=12MHz ceramic oscillation mode FmX'tal=32.768kHz by crystal oscillation mode System clock set to 12MHz side Internal RC oscillation stopped frequency variable RC oscillation stopped 1/1 frequency division ratio. 	4.5 to 5.5		9.5	22	mA
	IDDOP(2)			2.8 to 4.5		5.5	15	
	IDDOP(3)		<ul style="list-style-type: none"> FmCF=8MHz ceramic oscillation mode FmX'tal=32.768kHz by crystal oscillation mode System clock set to 8MHz side Internal RC oscillation stopped frequency variable RC oscillation stopped 1/1 frequency division ratio. 	4.5 to 5.5		7	16.5	
	IDDOP(4)			2.5 to 4.5		4	12	
	IDDOP(5)		<ul style="list-style-type: none"> FmCF=4MHz ceramic oscillation mode FmX'tal=32.768kHz by crystal oscillation mode System clock set to 4MHz side Internal RC oscillation stopped frequency variable RC oscillation stopped 1/2 frequency division ratio. 	4.5 to 5.5		2.8	6.5	
	IDDOP(6)			2.2 to 4.5		1.5	4.5	
	IDDOP(7)		<ul style="list-style-type: none"> FmCF=0Hz(oscillation stopped) FmX'tal=32.768kHz by crystal oscillation mode System clock set to internal RC oscillation frequency variable RC oscillation stopped 1/2 frequency division ratio. 	4.5 to 5.5		1	4.5	
	IDDOP(8)			2.2 to 4.5		0.55	3.5	
	IDDOP(9)		<ul style="list-style-type: none"> FmCF=0Hz(oscillation stopped) FmX'al=32.768kHz by crystal oscillation mode. System clock set to 1MHz with frequency variable RC oscillation Internal RC oscillation stopped 1/2 frequency division ratio. 	4.5 to 5.5		1.3	5.5	
	IDDOP(10)			2.2 to 4.5		0.7	4.5	
	IDDOP(11)		<ul style="list-style-type: none"> FmCF=0Hz(oscillation stopped) FmX'al=32.768kHz by crystal oscillation mode. System clock set to 32.768kHz side. Internal RC oscillation stopped frequency variable RC oscillation stopped 1/2 frequency division ratio. 	4.5 to 5.5		40	120	
	IDDOP(12)			2.2 to 4.5		20	80	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

Continued on next page.

LC87F5DC8A

Continued from preceding page.

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(1)	V _{DD1} =V _{DD2} =V _{DD3}	<ul style="list-style-type: none"> • HALT mode • FmCF=12MHz ceramic oscillation mode • FmX'tal=32.768kHz by crystal oscillation mode 	4.5 to 5.5		3.8	8.2	mA
	IDDHALT(2)		<ul style="list-style-type: none"> • System clock set to 12MHz side • Internal RC oscillation stopped • frequency variable RC oscillation stopped • 1/1 frequency division ratio. 	2.8 to 5.5		2.2	4.4	
	IDDHALT(3)		<ul style="list-style-type: none"> • HALT mode • FmCF=8MHz ceramic oscillation mode • FmX'tal=32.768kHz by crystal oscillation mode 	4.5 to 5.5		2.8	5.9	
	IDDHALT(4)		<ul style="list-style-type: none"> • System clock set to 8MHz side • Internal RC oscillation stopped • frequency variable RC oscillation stopped • 1/1 frequency division ratio. 	2.5 to 5.5		1.5	3.0	
	IDDHALT(5)		<ul style="list-style-type: none"> • HALT mode • FmCF=4MHz ceramic oscillation mode • FmX'tal=32.768kHz by crystal oscillation mode 	4.5 to 5.5		1.2	2.7	
	IDDHALT(6)		<ul style="list-style-type: none"> • System clock set to 4MHz side • Internal RC oscillation stopped • frequency variable RC oscillation stopped • 1/2 frequency division ratio. 	2.2 to 4.5		0.6	1.5	
	IDDHALT(7)		<ul style="list-style-type: none"> • HALT mode • FmCF=0Hz(oscillation stopped) • FmX'tal=32.768kHz by crystal oscillation mode • System clock set to internal RC oscillation 	4.5 to 5.5		0.4	1.1	
	IDDHALT(8)		<ul style="list-style-type: none"> • frequency variable RC oscillation stopped • 1/2 frequency division ratio. 	2.2 to 4.5		0.2	0.8	
	IDDHALT(9)		<ul style="list-style-type: none"> • HALT mode • FmCF=0Hz(oscillation stopped) • FmX'al=32.768kHz by crystal oscillation mode. 	4.5 to 5.5		1.2	4	
	IDDHALT(10)		<ul style="list-style-type: none"> • System clock set to 1MHz with frequency variable RC oscillation • Internal RC oscillation stopped • 1/2 frequency division ratio. 	2.2 to 4.5		0.6	3	
	IDDHALT(11)		<ul style="list-style-type: none"> • HALT mode • FmCF=0Hz(oscillation stopped) • FmX'al=32.768kHz by crystal oscillation mode. • System clock set to 32.768kHz side. 	4.5 to 5.5		20	70	
	IDDHALT(12)		<ul style="list-style-type: none"> • Internal RC oscillation stopped • frequency variable RC oscillation stopped • 1/2 frequency division ratio. 	2.2 to 4.5		10	50	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

Continued on next page.

LC87F5DC8A

Continued from preceding page.

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
Current drain during HOLD mode	IDDHOLD(1)	V _{DD1}	<ul style="list-style-type: none"> HOLD mode CF1=VDD or open (External clock mode) 	4.5 to 5.5		0.04	10	μA
	IDDHOLD(2)			2.2 to 4.5		0.02	5	
Current drain during time-base clock HOLD mode	IDDHOLD(3)	V _{DD1}	<ul style="list-style-type: none"> Timer HOLD mode CF1=VDD or open (External clock mode) FmXtal=32.768kHz by crystal oscillation mode 	4.5 to 5.5		18	60	
	IDDHOLD(4)			2.2 to 4.5		6	40	

F-ROM Programming Characteristics at Ta = +10°C to +55°C, V_{SS1} = V_{SS2} = V_{SS3} = 0V

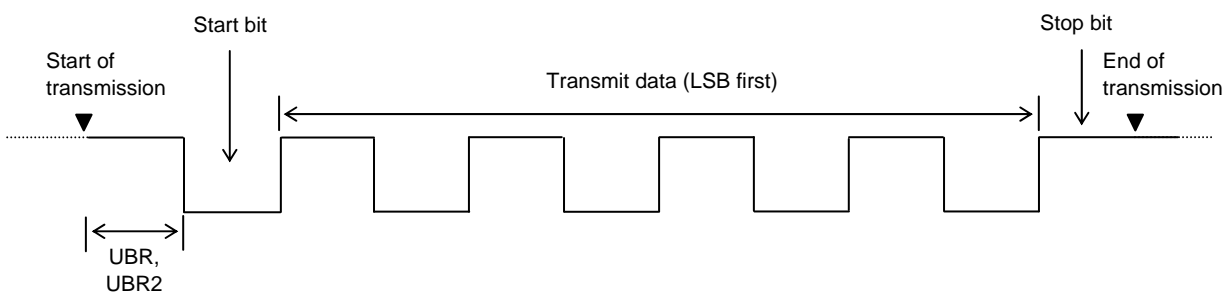
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	V _{DD1}	<ul style="list-style-type: none"> 128-byte programming Erasing current including 	3.0 to 5.5		25	40	mA
Programming time	tFW(1)		<ul style="list-style-type: none"> 128-byte programming Erasing current including Time for setting up 128 byte data is excluded. 	3.0 to 5.5		22.5	45	ms

UART (Full Duplex) Operating Conditions at Ta = -20°C to +70°C, V_{SS1} = V_{SS2} = V_{SS3} = 0V

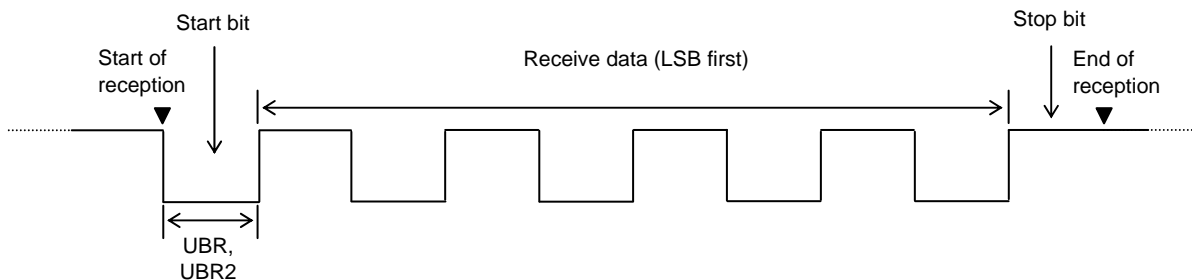
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
Clock rate	UBR,UBR2	UTX1(P32), RTX1(P33), UTX2(P22), RTX2(P23)		2.2 to 5.5	16/3		8192/3	tCYC

Data length: 7/8/9 bits (LSB first)
 Stop bits: 1-bit(2-bit in continuous data transmission)
 Parity bits: None

*Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data=55H)



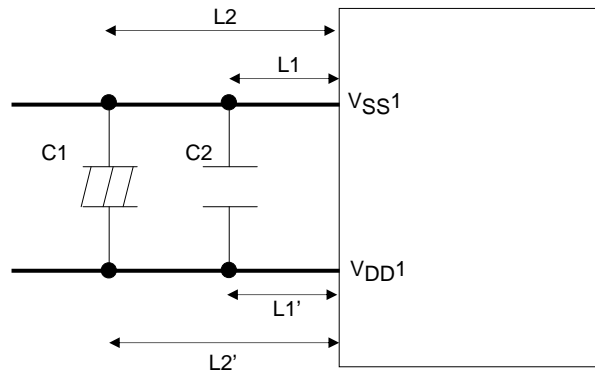
*Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data=55H)



V_{DD1}, V_{SS1} Terminal condition

It is necessary to place capacitors between V_{DD1} and V_{SS1} as describe below.

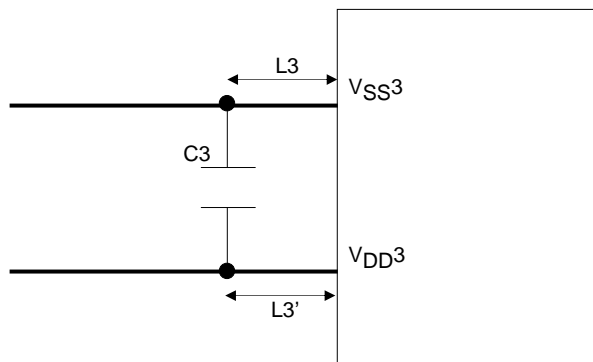
- Place capacitors as close to V_{DD1} and V_{SS1} as possible.
- Place capacitors so that the length of each terminal to the each leg of the capacitor be equal ($L1 = L1'$, $L2 = L2'$).
- Place high capacitance capacitor C1 and low capacitance capacitor C2 in parallel.
- Capacitance of C2 must be more than 0.1 μ F.
- Use thicker pattern for V_{DD1} and V_{SS1}.



V_{DD3}, V_{SS3} Terminal condition

It is necessary to place capacitors between V_{DD3} and V_{SS3} as describe below.

- Place capacitors as close to V_{DD3} and V_{SS3} as possible.
- Place capacitors so that the length of each terminal to the each leg of the capacitor be equal ($L3 = L3'$).
- Capacitance of C3 must be more than 0.1 μ F.
- Use thicker pattern for V_{DD3} and V_{SS3}.



LC87F5DC8A

Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf1 [Ω]	Rd1 [Ω]		typ [ms]	max [ms]	
12MHz	MURATA	CSTCE12M0G52-R0	(10)	(10)	OPEN	470	2.8V to 5.5V	0.05	0.15	Internal C1,C2
8MHz		CSTCE8M00G52-R0	(10)	(10)	OPEN	2.2k	2.7V to 5.5V	0.05	0.15	Internal C1,C2
		CSTLS8M00G53-B0	(15)	(15)	OPEN	680	2.5V to 5.5V	0.05	0.15	Internal C1,C2
4MHz		CSTCR4M00G53-R0	(15)	(15)	OPEN	3.3k	2.2V to 5.5V	0.05	0.15	Internal C1,C2
		CSTLS4M00G53-R0	(15)	(15)	OPEN	3.3k	2.2V to 5.5V	0.05	0.15	Internal C1,C2

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after VDD goes above the operating voltage lower limit (see Figure 4).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	SEIKO EPSON	MC-306	18	18	Open	560k	2.2 to 5.5	1.3	3.0	Applicable CL value = 12.5pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 4).

Note : The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

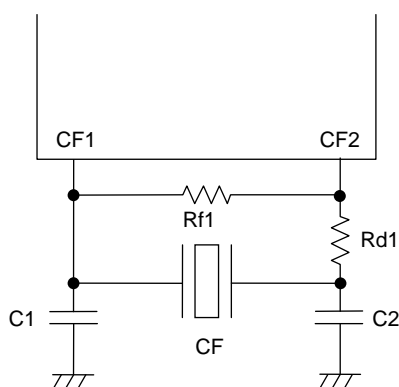


Figure 1 Ceramic Oscillation Circuit

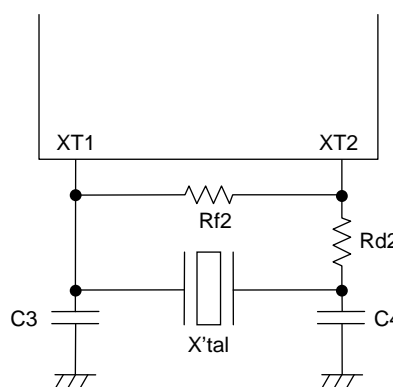


Figure 2 Crystal Oscillation Circuit

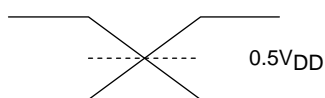
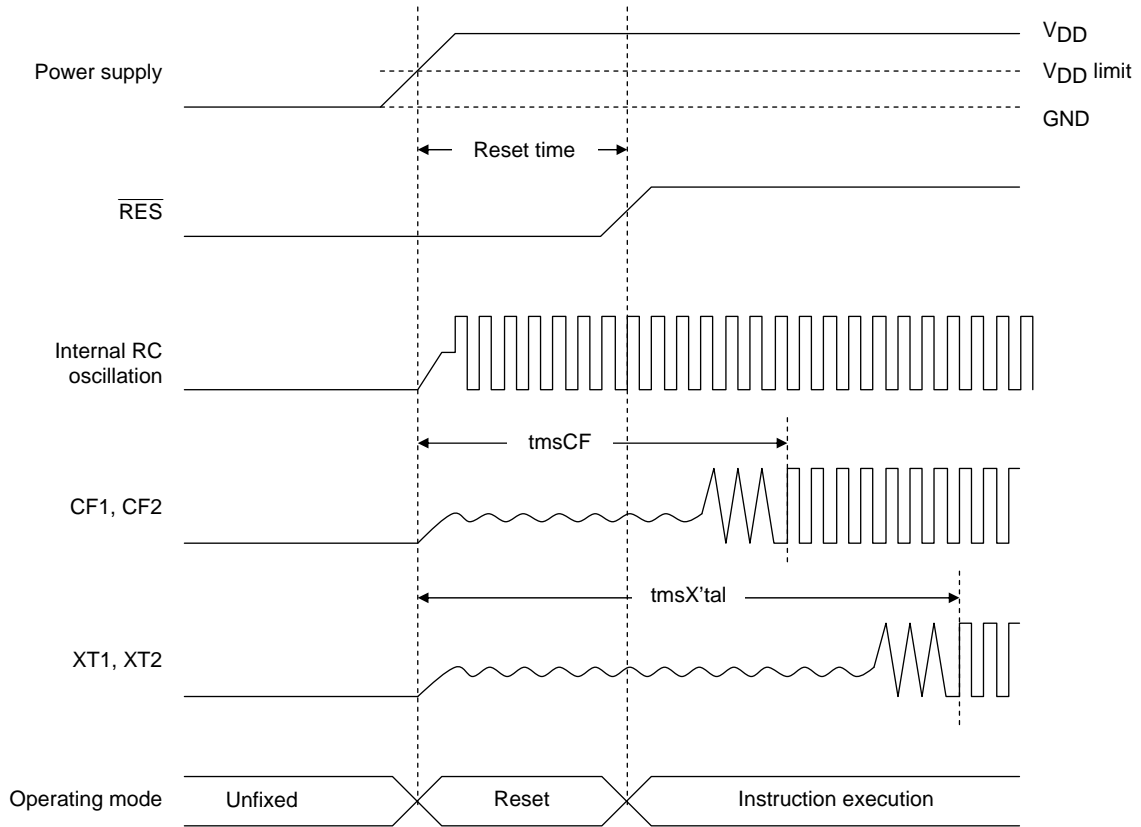
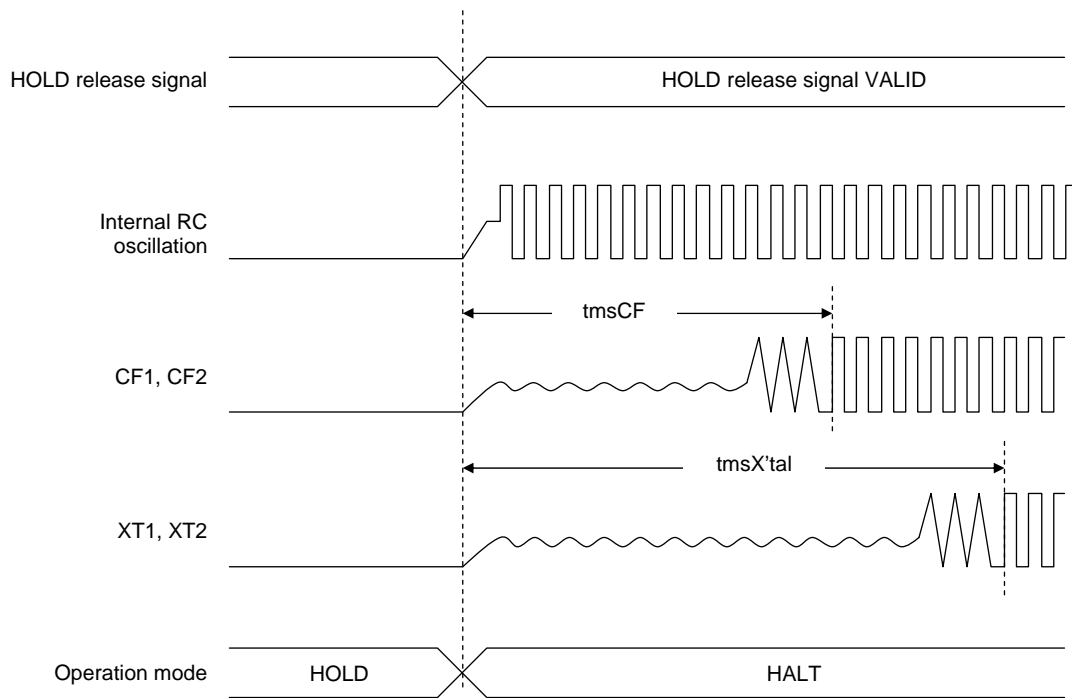


Figure 3 AC Timing Point

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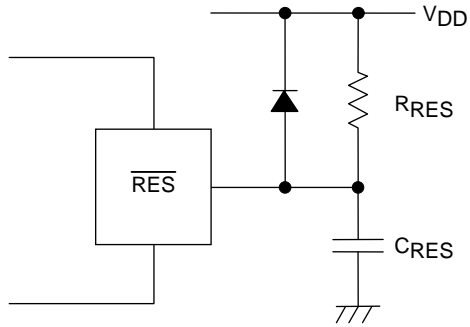
Reset Time and Oscillation Stabilizing Time



HOLD Reset Signal and Oscillation Stabilizing Time

Figure 4 Oscillation Stabilizing Times

LC87F5DC8A



Note :
 Select C_{RES} and R_{RES} value to assure that at least $200\mu s$ reset time is generated after the V_{DD} becomes higher than the minimum operating voltage.

Figure 5 Reset Circuit

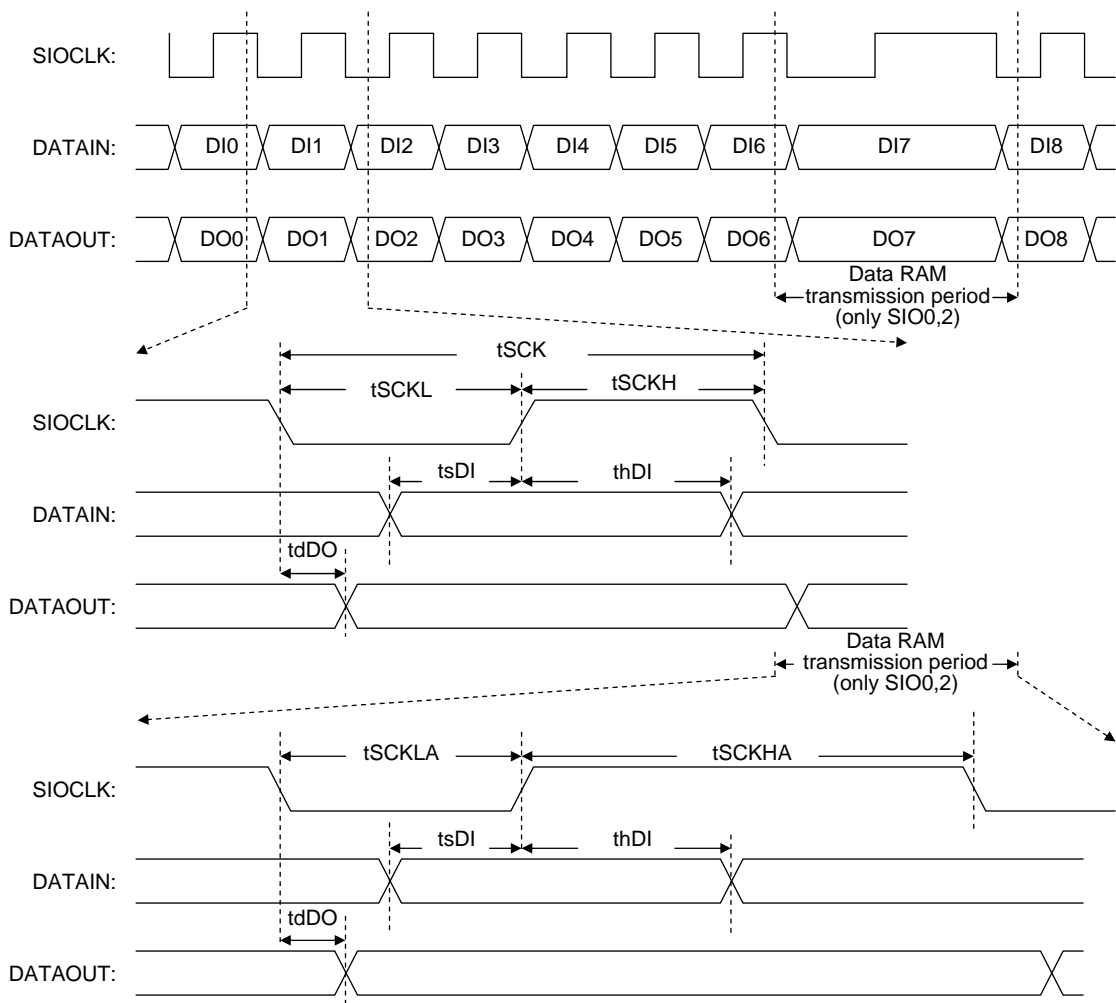


Figure 6 Serial Input/Output Test Condition

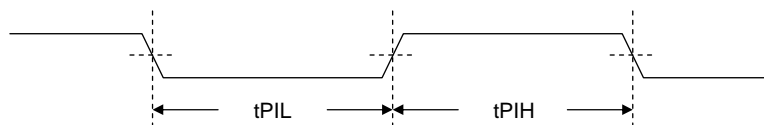


Figure 7 Pulse Input Timing Condition

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