THE DATASHEET OF

ISPPAC-POWR607-01SN24I

ispPAC®-POWR607

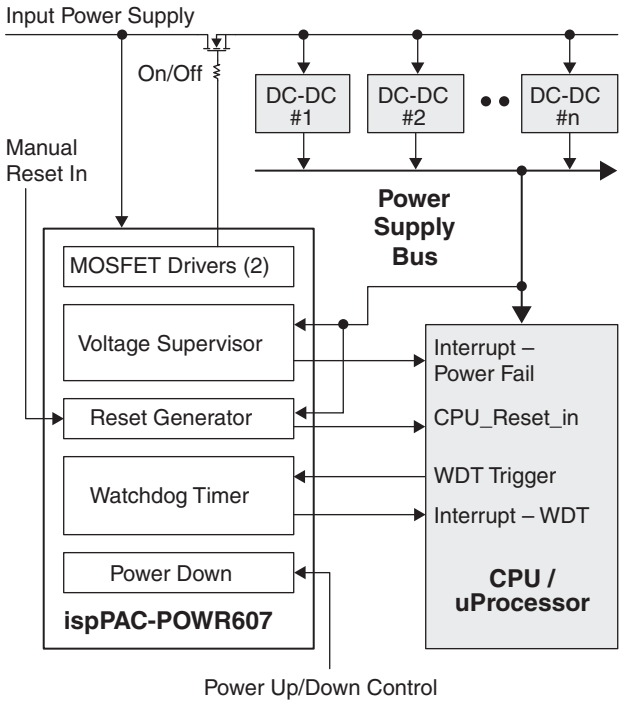
In-System Programmable Power Supply Supervisor, Reset Generator and Watchdog Timer

April 2015 Data Sheet DS1011

Features

- **Power-Down Mode I_{CC} < 10 µA**
- **Programmable Threshold Monitors**
  - Simultaneously monitors up to six power supplies
  - Programmable analog trip points (1% step size; 192 steps)
  - Programmable glitch filter
  - Power-off detection (75 mV)
- **Embedded Programmable Timers**
  - Four independent timers
  - 32 µs to 2 second intervals for timing sequences
- **Embedded PLD for Logical Control**
  - Rugged 16-macrocell CPLD architecture
  - 81 product terms / 28 inputs
  - Implements state machines and combinatorial functions
- **Digital I/O**
  - Two dedicated digital inputs
  - Five programmable digital I/O pins
- **Two High-Voltage FET Drivers**
  - Power supply ramp up/down control
  - Independently configurable for FET control or digital output
- **Wide Supply Range (2.64 V to 3.96 V)**
  - In-system programmable through JTAG
  - Industrial temperature range: –40 °C to +105 °C
  - 24-pin and 32-pin QFNS packages, lead-free option

Application Block Diagram



Description

The Power Manager II ispPAC-POWR607 is a general-purpose power-supply monitor, reset generator and watchdog timer, incorporating both in-system programmable logic and analog functions implemented in non-volatile E^2CMOS® technology. The ispPAC-POWR607 device provides six independent analog input channels to monitor power supply voltages. Two general-purpose digital inputs are also provided for miscellaneous control functions.

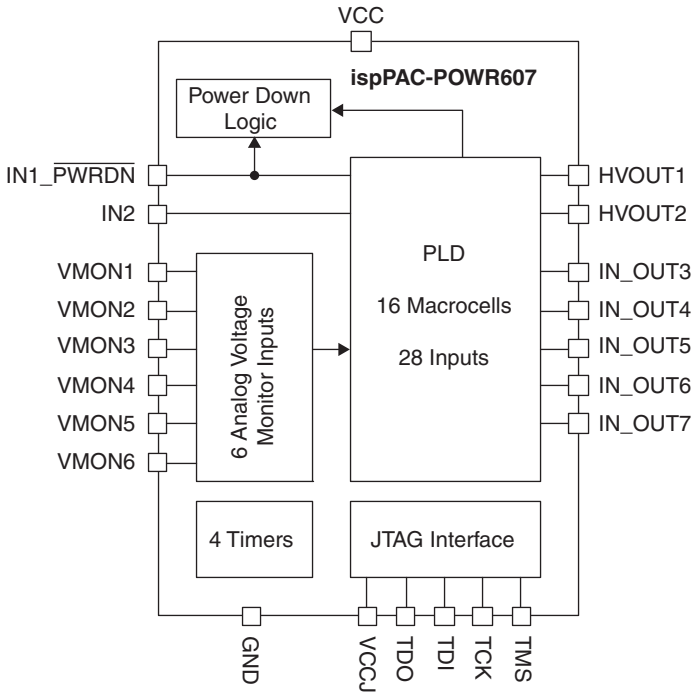
The ispPAC-POWR607 provides up to seven open-drain digital outputs that can be used for controlling DC-DC converters, low-drop-out regulators (LDOs) and opto-couplers, as well as for supervisory and general-purpose logic interface functions. Two of these outputs (HVOUT1-HVOUT2) can be configured as high-voltage MOSFET drivers. In high-voltage mode these outputs provide 9V for driving the gates of n-channel MOSFETs used as high-side power switches to control power supply ramp up and ramp down rate. The remaining five digital, open drain outputs can optionally be configured as digital inputs to sense more input signals as needed, such as manual reset, etc.

The diagram above shows how a ispPAC-POWR607 is used in a typical application. It controls power to the microprocessor system, generates the CPU reset and monitors critical power supply voltages, generating interrupts whenever faults are detected. It also provides a watchdog timer function to detect CPU operating and bus timeout errors.

The ispPAC-POWR607 incorporates a 16-macrocell CPLD. Figure 1 shows the analog input comparators and digital inputs used as inputs to the CPLD array. The digital output pins providing the external control signals are driven by the CPLD. Four independently program-

mable timers also interface with the CPLD and can create delays and time-outs ranging from 32µs to 2 seconds. The CPLD is programmed using LogiBuilder™, an easy-to-learn language integrated into the PAC-Designer® software. Control sequences are written to monitor the status of any of the analog input channel comparators or the digital inputs.

Figure 1. ispPAC-POWR607 Block Diagram



Pin Descriptions

24-Pin QFNS Pin Number	32-Pin QFNS Pin Number	Pin Name	Pin Type	Voltage Range	Description
8, 9	11, 12	GND	Ground	Ground	Ground[1]
23	30	HVOUT1	Open Drain Output[2]	0 V to 10 V	Open-Drain Output 1
			FET Gate Driver	0 V to 9 V	High-voltage FET Gate Driver 1
24	31	HVOUT2	Open Drain Output[2]	0 V to 10 V	Open-Drain Output 2
			FET Gate Driver	0 V to 9 V	High-voltage FET Gate Driver 2
20	27	IN_OUT3	Digital Input[9]	0 V to 5.5 V	PLD Input 3
			Open Drain Output[2]		Open Drain Output 3
19	26	IN_OUT4	Digital Input[9]	0 V to 5.5 V	PLD Input 4
			Open Drain Output[2]		Open Drain Output 4
18	23	IN_OUT5	Digital Input[9]	0 V to 5.5 V	PLD Input 5
			Open Drain Output[2]		Open Drain Output 5
17	22	IN_OUT6	Digital Input[9]	0 V to 5.5 V	PLD Input 6
			Open Drain Output[2]		Open Drain Output 6
15	20	IN_OUT7	Digital Input[9]	0 V to 5.5 V	PLD Input 7
			Open Drain Output[2]		Open Drain Output 7
22	29	IN1_$\overline{\text{PWRDN}}$	Digital Input[10]	0 V to 5.5 V[3]	PLD Logic Input 1.[4, 5] When not used, this pin should be pulled down with a 10 kΩ resistor.

Pin Descriptions (Cont.)

24-Pin QFNS Pin Number	32-Pin QFNS Pin Number	Pin Name	Pin Type	Voltage Range	Description
21	28	IN2	Digital Input[10]	0 V to 5.5 V[3]	PLD Logic Input 2. When not used, this pin should be tied to GND.
12	15	TCK	Digital Input	0 V to 5.5 V	JTAG Test Clock Input
13	18	TDI	Digital Input	0 V to 5.5 V	JTAG Test Data In - Internal Pull-up
11	14	TDO	Digital Output	0 V to 5.5 V	JTAG Test Data Out
14	19	TMS	Digital Input	0 V to 5.5 V	JTAG Test Mode Select - Internal Pull-up
3, 16	4, 21	VCC	Power	2.64 V to 3.96 V	Power Supply[6]
10	13	VCCJ	Power	2.25 V to 3.6 V	VCC for JTAG Logic Interface Pins[7]
1	2	VMON1	Analog Input	–0.3 V to 5.9 V[8]	Voltage Monitor Input 1
2	3	VMON2	Analog Input	–0.3 V to 5.9 V[8]	Voltage Monitor Input 2
4	5	VMON3	Analog Input	–0.3 V to 5.9 V[8]	Voltage Monitor Input 3
5	6	VMON4	Analog Input	–0.3 V to 5.9 V[8]	Voltage Monitor Input 4
6	7	VMON5	Analog Input	–0.3 V to 5.9 V[8]	Voltage Monitor Input 5
7	10	VMON6	Analog Input	–0.3 V to 5.9 V[8]	Voltage Monitor Input 6
Die Pad	Die Pad	NC	No Connection	Not applicable	No internal connection

1. GND pins must be connected together on the circuit board.
2. Open-drain outputs require an external pull-up resistor to a supply.
3. IN1_$\overline{\text{PWRDN}}$ and IN2 are inputs to the PLD. The thresholds for these pins are referenced by the voltage on VCC.
4. The power-down function is E^2CMOS programmable and when enabled is input level sensitive (enter power-down mode = low; exit power-down mode = high).
5. Source of the power-down initiation can be assigned to either the IN1_$\overline{\text{PWRDN}}$ pin or to an internally generated PLD output signal called PLD_PWRDN. When generated internally by the PLD, the IN1_$\overline{\text{PWRDN}}$ pin is only used to exit power-down mode (IN1_$\overline{\text{PWRDN}}$ pin = high).
6. VCC pins must be connected together on the circuit board.
7. In power-down mode, VCCJ is internally pulled to GND to turn off the JTAG I/O pins. It is important, therefore, that the VCCJ pin be open whenever power-down mode is initiated. If connected to a power supply during power-down mode, VCCJ will draw approximately 2.2 mA.
8. The VMON inputs can be biased independently from VCC. Unused VMON inputs should be tied to GND.
9. Thresholds of IN_OUT3...IN_OUT7 in the input mode are referenced by the voltage on VCC.
10. IN1_$\overline{\text{PWRDN}}$, IN2 and IN_OUT3...INOUT7 pins configured as inputs are clocked by the internal MCLK signal.

32-Pin QFNS No Connect Pins

32-Pin QFNS Pin Number	Pin Name	Pin Type	Voltage Range	Description
1, 8, 9, 16, 17, 24, 25, 32	NC	No Connection	Not applicable	No internal connection

Absolute Maximum Ratings

Absolute maximum ratings are shown in the table below. Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions of this specification is not implied.

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CC}	Core supply		–0.5	4.5	V
V_{CCJ}	JTAG logic supply		–0.5	6	V
V_{IN}	Digital input voltage (all digital I/O pins)		–0.5	6	V
V_{MON}	V_{MON} input voltage		–0.5	6	V
V_{TRI}	Voltage applied to tri-stated pins	HVOUT[1:2]	–0.5	11	V
		IN_OUT[3:7]	–0.5	6	V
T_S	Storage temperature		–65	150	°C
T_A	Ambient temperature		–65	125	°C
$I_{SINKMAX}$	Maximum sink current on any output			23	mA

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CC}	Core supply voltage at pin		2.64	3.96	V
V_{CCJ}	JTAG logic supply voltage at pin		2.25	3.6	V
V_{IN}	Input voltage at digital input pins		–0.3	5.5	V
V_{MON}	Input voltage at V_{MON} pins		–0.3	5.9	V
V_{OUT}	Open-drain output voltage	IN_OUT[3:7] pins	–0.3	5.5	V
		HVOUT[1:2] pins in open-drain mode	–0.3	10.4	V
T_{APROG}	Ambient temperature during programming	(Note 1)	–40	85	°C
T_A	Ambient temperature	Power applied[1]	–40	105	°C
T_{JOP}	Operating junction temperature	Power applied[1]	–40	108	°C

1. The die pad on the bottom of the QFNS package does not need to be electrically or thermally connected to ground.

Analog Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{CC}[1]	Supply current			3.5	5	mA
I_{CCJ}[2]	Supply current				1	mA
I_{CC_PWRDN}[3]	Power-down mode supply current	ICC + pin leakage currents[2]			10	µA

1. Includes currents on both V_{CC} pins.
2. In power-down mode, VCCJ is internally pulled to GND to turn off the JTAG I/O pins. It is important, therefore, that the VCCJ pin be open whenever power-down mode is initiated. If connected to a power supply during power-down mode, VCCJ will draw approximately 2.2 mA.
3. Leakage measured in power-down mode with applied pin voltages as follows: VCC = 3.96 V; IN1_$\overline{\text{PWRDN}}$, GND = 0 V; IN2, VMONx and IN_OUTx = 5.5 V; HVOUTx configured as FET drivers (HVOUTx configured as open drain outputs have minor leakage path to ground and are not counted in total); VCCJ, TDI, TDO, TMS and TCK = open.

Voltage Monitors

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
R_{IN}	Input resistance		55	65	75	kΩ
C_{IN}	Input capacitance			8		pF
V_{MON} Range	Programmable trip-point range		0.075		5.811	V
V_Z Sense	Near-ground sense threshold		70	75	80	mV
V_{MON} Accuracy	Absolute accuracy of any trip-point[1]			±0.5	1.5	%
HYST	Hysteresis of any trip-point (relative to setting)			1		%

1. Guaranteed by characterization across V_{CC} range, operating temperature, process.

High Voltage FET Drivers

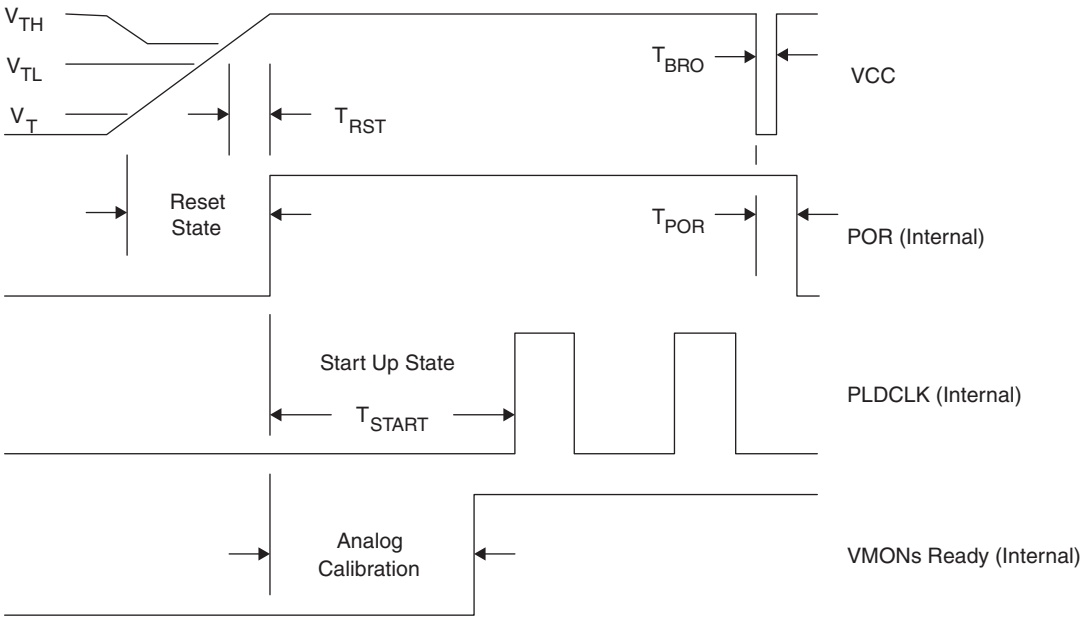
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{PP}	Gate driver output voltage		8.1	9	9.9	V
I_{OUTSRC}	Gate driver source current (HIGH state)	Controlled ramp setting		15		µA
$I_{OUTSINK}$	Gate driver sink current (LOW state)	FET turn off mode	1.0	2.5		mA

Power-On Reset (Internal)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
T_{RST}	Delay from V_{TH} to start-up state				100	µs
T_{START}	Duration of start-up state				300	µs
T_{BRO}	Minimum duration brown out required to enter reset state		1		5	µs
T_{POR}	Delay from brown out to reset state				7	µs
V_{TL}	Threshold below which POR is LOW[1]				2.2	V
V_{TH}	Threshold above which POR is HIGH[1]		2.5			V
V_T	Threshold above which POR is valid[1]		0.8			V

1. Corresponds to VCC supply voltage.

Figure 2. Internal Power-On Reset

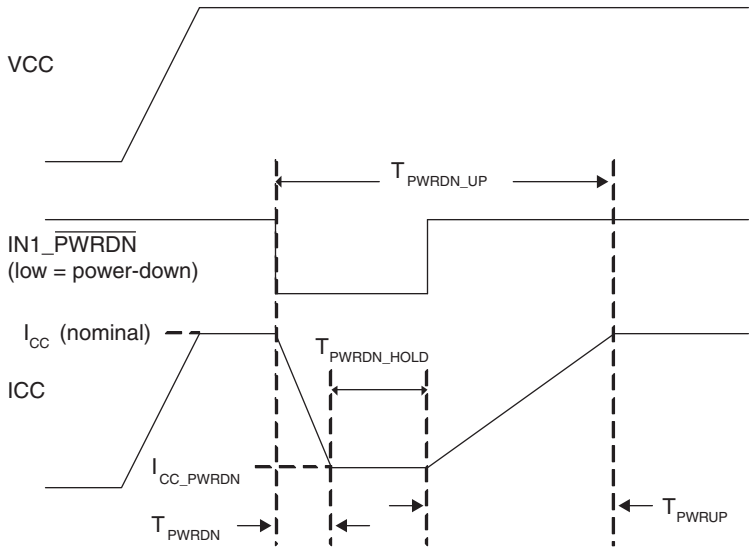


AC/Transient Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Voltage Monitors						
t_{PD12}	Propagation delay input to output glitch filter OFF			12		µs
t_{PD48}	Propagation delay input to output glitch filter ON			48		µs
Oscillators						
f_{PLDCLK}	PLDCLK frequency		240	250	260	kHz
Timers						
Timeout Range	Range of programmable timers (128 steps)		0.032		1966	ms
Resolution	Spacing between available adjacent timer intervals				13	%
Accuracy	Timer accuracy		–6.67		–12.5	%
Power-Down Mode						
T_{PWRDN}	Time to enter power-down mode	Device previously on	100			µs
T_{PWRDN_HOLD}	Minimum required time in power-down mode before power-up can occur		100			µs
T_{PWRUP}	Time to exit power-down mode		300			µs
T_{PWRDN_UP}	Total time to enter and then exit power-down mode		500			µs

Figure 3. Power-Down Mode Timing



Digital Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IL},I_{IH}	Input leakage, no pull-up/pull-down				+/–10	µA
$I_{OH-HVOUT}$	Output leakage current	HVOUT[1:2] in open drain mode and pulled up to 10 V		35	60	µA
I_{PU}	Input pull-up current (TMS, TDI)			70		µA
V_{IL}	Voltage input, logic low[1]	TDI, TMS, TCK, IN[1:2], IN_OUT[3:7][2], V_{CCJ} = 3.3 V supply			0.8	V
		TDI, TMS, TCK, V_{CCJ} = 2.5 V supply			0.7	
V_{IH}	Voltage input, logic high[1]	TDI, TMS, TCK, IN[1:2], IN_OUT[3:7][2], V_{CCJ} = 3.3 V supply	2.0			V
		TDI, TMS, TCK, V_{CCJ} = 2.5 V supply	1.7			
V_{OL}	HVOUT[1:2] (open drain mode),	I_{SINK} = 10 mA			0.8	V
	IN_OUT[3:7][3]	I_{SINK} = 20 mA			0.8	
	TDO	I_{SINK} = 4 mA			0.4	
V_{OH}	TDO	I_{SRC} = 4 mA			V_{CC} - 0.4	V
$I_{SINKTOTAL}$[4]	All digital outputs				67	mA

1. IN_OUT[3:7], IN[1:2] referenced to V_{CC}; TDO, TDI, TMS, and TCK referenced to V_{CCJ}.
2. When configured as inputs.
3. When configured as open drain outputs.
4. Sum of maximum current sink from all digital outputs combined. Reliable operation is not guaranteed if this value is exceeded.

Timing for JTAG Operations

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{ISPEN}	Program enable delay time		10	—	—	µs
t_{ISPDIS}	Program disable delay time		30	—	—	µs
t_{HVDIS}	High voltage discharge time, program		30	—	—	µs
t_{HVDIS}	High voltage discharge time, erase		200	—	—	µs
t_{CEN}	Falling edge of TCK to TDO active		—	—	10	ns
t_{CDIS}	Falling edge of TCK to TDO disable		—	—	10	ns
t_{SU1}	Setup time		5	—	—	ns
t_H	Hold time		10	—	—	ns
t_{CKH}	TCK clock pulse width, high		20	—	—	ns
t_{CKL}	TCK clock pulse width, low		20	—	—	ns
f_{MAX}	Maximum TCK clock frequency		—	—	25	MHz
t_{CO}	Falling edge of TCK to valid output		—	—	10	ns
t_{PWV}	Verify pulse width		30	—	—	µs
t_{PWP}	Programming pulse width		20	—	—	ms

Figure 4. Erase (User Erase or Erase All) Timing Diagram

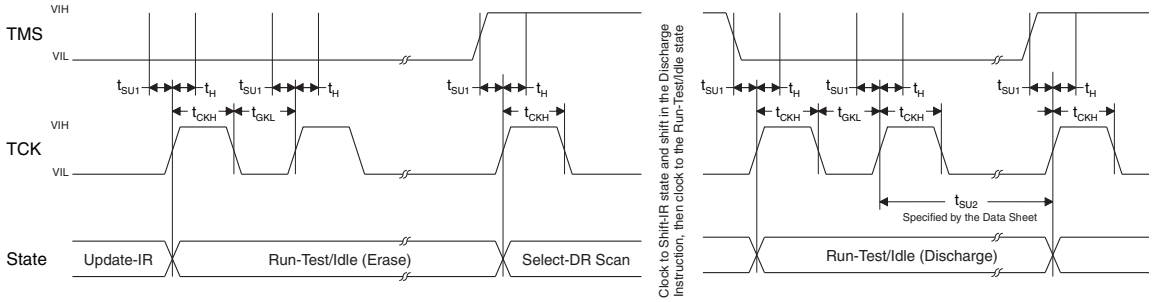


Figure 5. Programming Timing Diagram

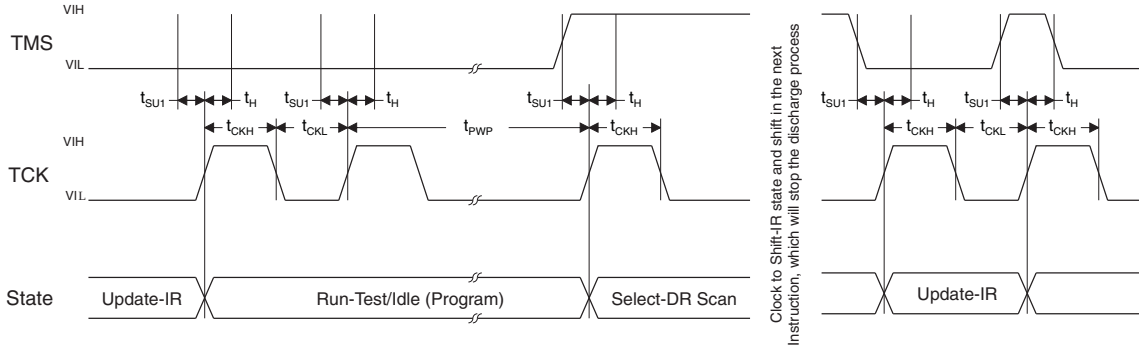


Figure 6. Verify Timing Diagram

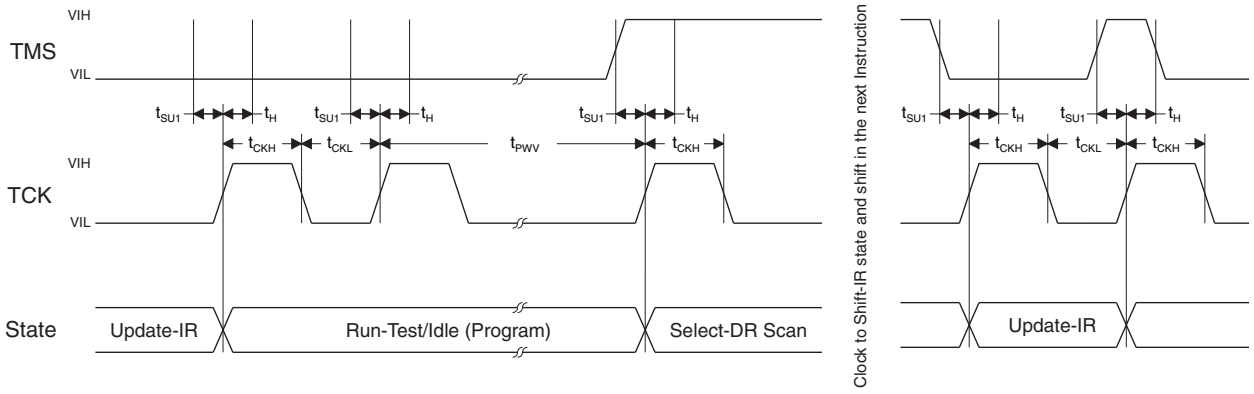
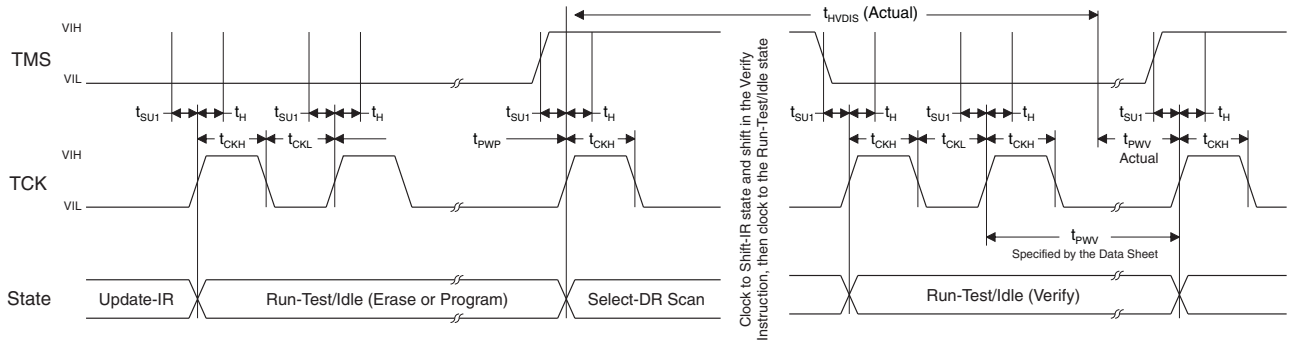


Figure 7. Discharge Timing Diagram



Theory of Operation

Analog Monitor Inputs

The ispPAC-POWR607 provides six independently programmable voltage monitor input circuits as shown in Figure 8. One programmable trip-point comparator is connected to each analog monitoring input. Each comparator reference has 192 programmable trip points over the range of 0.667 V to 5.811 V. Additionally, a 75 mV 'zero-detect' threshold is selectable which allows the voltage monitors to determine if a monitored signal has dropped to ground level. This feature is especially useful for determining if a power supply's output has decayed to a substantially inactive condition after it has been switched off.

Figure 8. ispPAC-POWR607 Voltage Monitors

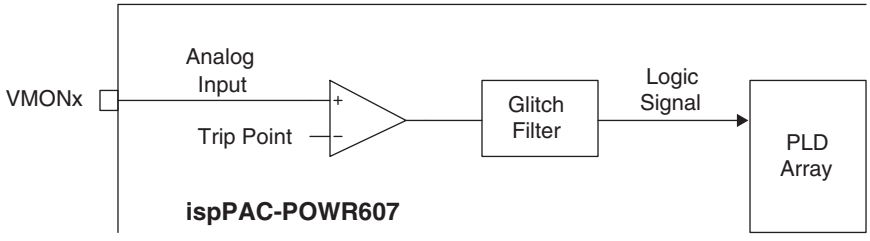


Figure 8 shows the functional block diagram of one of the six voltage monitor inputs - 'x' (where x = 1...6). Each voltage monitor can be divided into two sections: Analog Input, and Filtering.

The voltage input is monitored by a programmable trip-point comparator. Table 1 and Table 2 show all trip points and ranges to which any comparator's threshold can be set.

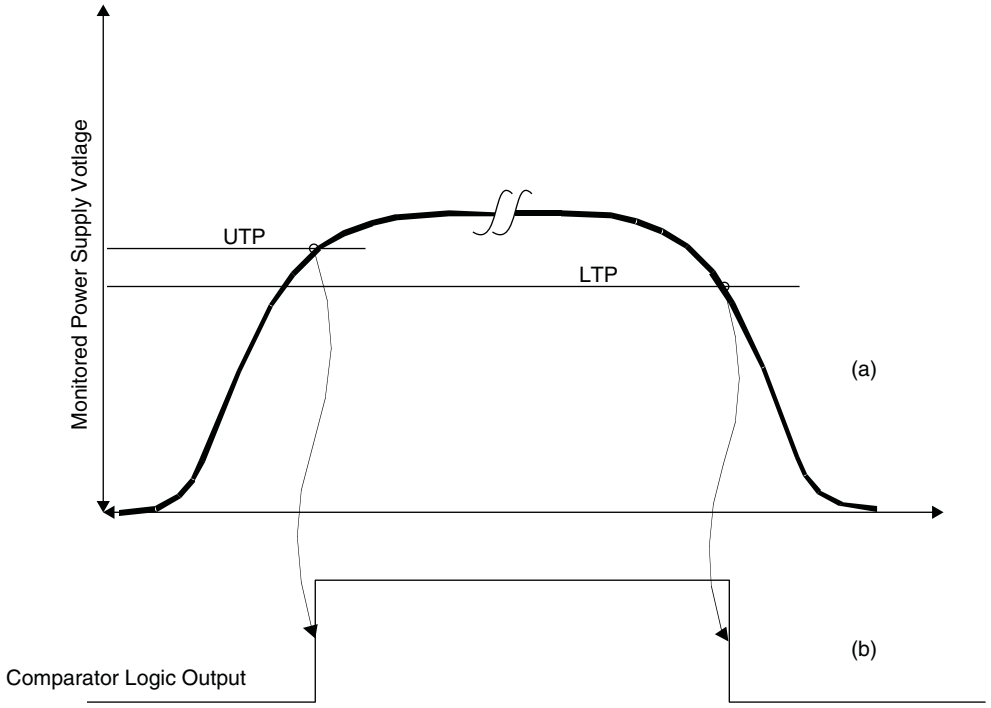
Each comparator outputs a HIGH signal to the PLD array if the voltage at its positive terminal (VMONx pin) is greater than its programmed trip point setting, otherwise it outputs a LOW signal.

A hysteresis of approximately 1% of the setpoint is provided by the comparators to reduce false triggering as a result of input noise. The hysteresis provided by the voltage monitor is a function of the input divider setting. Table 3 lists the typical hysteresis versus voltage monitor trip-point.

Programmable Over-Voltage and Under-Voltage Thresholds

Figure 9 (a) shows the power supply ramp-up and ramp-down voltage waveforms. Because of hysteresis, the comparator outputs change state at different thresholds depending on the direction of excursion of the monitored power supply.

Figure 9. (a) Power Supply Voltage Ramp-up and Ramp-down Waveform and the Resulting Comparator Output, (b) Corresponding to Upper and Lower Trip Points



During power supply ramp-up the comparator output changes from logic 0 to 1 when the power supply voltage crosses the upper trip point (UTP). During ramp down the comparator output changes from logic state 1 to 0 when the power supply voltage crosses the lower trip point (LTP). To monitor for over voltage fault conditions, the UTP should be used. To monitor under-voltage fault conditions, the LTP should be used.

Table 1 and Table 2 show both the under-voltage and over-voltage trip points, which are automatically selected in software depending on whether the user is monitoring for an over-voltage condition or an under-voltage condition.

Table 1. Trip Point Table Used For Over-Voltage Detection (in Volts)

REF/ MON	F	E	D	C	B	A	9	8	7	6	5	4
1F	0.798	0.950	1.131	1.347	1.596	1.904	2.268	2.693	3.192	3.803	4.878	5.811
1E	0.790	0.941	1.120	1.333	1.580	1.885	2.245	2.666	3.159	3.764	4.829	5.751
1D	0.782	0.931	1.109	1.319	1.564	1.866	2.222	2.638	3.126	3.725	4.779	5.692
1C	0.774	0.921	1.097	1.306	1.547	1.847	2.198	2.611	3.095	3.686	4.729	5.632
1B	0.766	0.911	1.086	1.292	1.531	1.827	2.175	2.584	3.062	3.647	4.679	5.573
1A	0.757	0.902	1.074	1.278	1.515	1.808	2.152	2.556	3.029	3.609	4.629	5.514
19	0.749	0.892	1.063	1.264	1.498	1.788	2.129	2.529	2.997	3.570	4.580	5.454
18	0.741	0.882	1.051	1.250	1.482	1.769	2.106	2.501	2.964	3.531	4.530	5.395
17	0.733	0.872	1.039	1.237	1.466	1.749	2.083	2.473	2.931	3.492	4.480	5.336
16	0.725	0.864	1.028	1.223	1.449	1.730	2.060	2.446	2.899	3.453	4.430	5.277
15	0.716	0.854	1.016	1.209	1.433	1.710	2.037	2.418	2.866	3.414	4.380	5.217
14	0.708	0.844	1.005	1.195	1.417	1.691	2.014	2.391	2.834	3.375	4.331	5.158
13	0.700	0.835	0.993	1.181	1.400	1.671	1.990	2.364	2.801	3.337	4.281	5.099
12	0.692	0.825	0.981	1.168	1.384	1.652	1.967	2.336	2.769	3.298	4.231	5.040
11	0.684	0.815	0.970	1.154	1.369	1.632	1.944	2.309	2.736	3.259	4.181	4.980
10	0.676	0.805	0.958	1.140	1.352	1.614	1.921	2.281	2.703	3.220	4.131	4.921
Low V	75 mV											

Table 2. Trip Point Table Used For Under-Voltage Detection (in Volts)

REF/ MON	F	E	D	C	B	A	9	8	7	6	5	4
1F	0.790	0.941	1.120	1.333	1.580	1.885	2.245	2.666	3.159	3.764	4.829	5.751
1E	0.782	0.931	1.109	1.319	1.564	1.866	2.222	2.638	3.126	3.725	4.779	5.692
1D	0.774	0.921	1.097	1.306	1.547	1.847	2.198	2.611	3.095	3.686	4.729	5.632
1C	0.766	0.911	1.086	1.292	1.531	1.827	2.175	2.584	3.062	3.647	4.679	5.573
1B	0.757	0.902	1.074	1.278	1.515	1.808	2.152	2.556	3.029	3.609	4.629	5.514
1A	0.749	0.892	1.063	1.264	1.498	1.788	2.129	2.529	2.997	3.570	4.580	5.454
19	0.741	0.882	1.051	1.250	1.482	1.769	2.106	2.501	2.964	3.531	4.530	5.395
18	0.733	0.872	1.039	1.237	1.466	1.749	2.083	2.473	2.931	3.492	4.480	5.336
17	0.725	0.864	1.028	1.223	1.449	1.730	2.060	2.446	2.899	3.453	4.430	5.277
16	0.716	0.854	1.016	1.209	1.433	1.710	2.037	2.418	2.866	3.414	4.380	5.217
15	0.708	0.844	1.005	1.195	1.417	1.691	2.014	2.391	2.834	3.375	4.331	5.158
14	0.700	0.835	0.993	1.181	1.400	1.671	1.990	2.364	2.801	3.337	4.281	5.099
13	0.692	0.825	0.981	1.168	1.384	1.652	1.967	2.336	2.769	3.298	4.231	5.040
12	0.684	0.815	0.970	1.154	1.369	1.632	1.944	2.309	2.736	3.259	4.181	4.980
11	0.676	0.805	0.958	1.140	1.352	1.614	1.921	2.281	2.703	3.220	4.131	4.921
10	0.667	0.796	0.947	1.126	1.336	1.594	1.897	2.254	2.671	3.181	4.082	4.861
Low V	75 mV											

Table 3. Comparator Hysteresis vs. Trip-Point

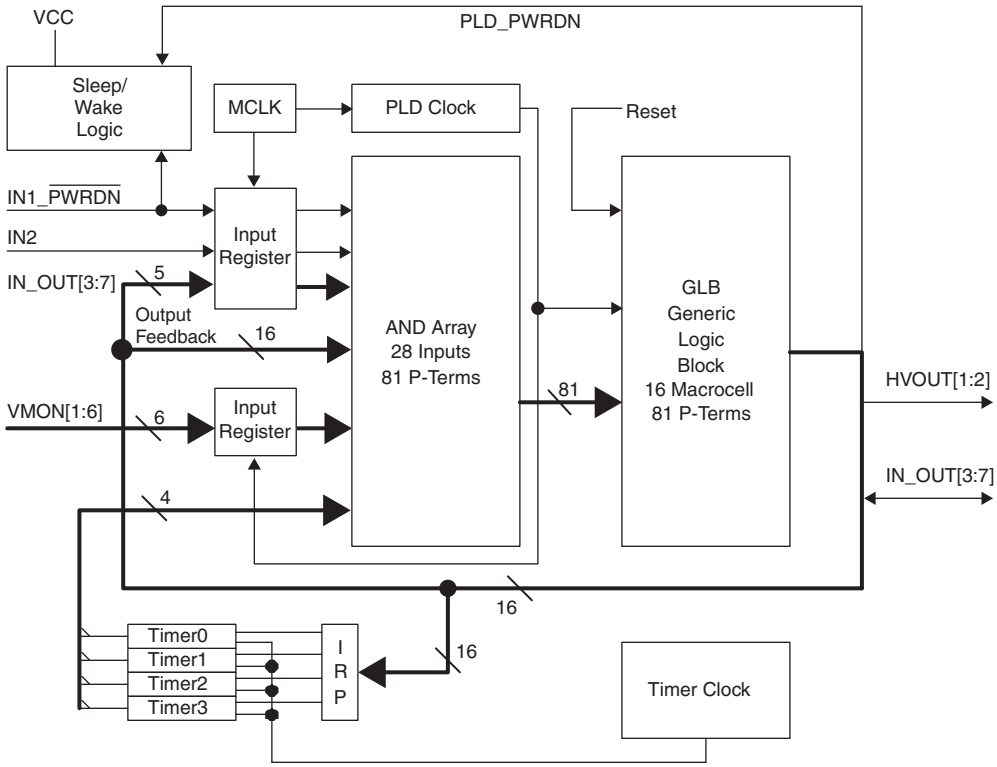
Trip-point Range (V)		Hysteresis (mV)
Low Limit	High Limit	
0.667	0.798	8
0.796	0.950	10
0.947	1.131	12
1.126	1.347	14
1.336	1.596	17
1.594	1.904	19
1.897	2.268	23
2.254	2.693	28
2.671	3.192	33
3.181	3.803	39
4.082	4.878	50
4.861	5.811	60
75 mV		0 (Disabled)

The second section in the ispPAC-POWR607's input voltage monitor is a digital filter. When enabled, the comparator output will be delayed by a filter time constant of 48 µs, and is especially useful for reducing the possibility of false triggering from noise that may be present on the voltages being monitored. When the filter is disabled, the comparator output will be delayed by 12 µs. In both cases, enabled or disabled, the filters also provide synchronization of the input signals to the PLD clock. This synchronous sampling feature effectively eliminates the possibility of race conditions from occurring in any subsequent logic that is implemented in the ispPAC-POWR607's internal PLD logic.

PLD Block

Figure 10 shows the ispPAC-POWR607 PLD architecture, which is derived from Lattice's ispMACH™ 4000 CPLD. The PLD architecture allows flexibility in designing various state machines and control functions for power supply management. The AND array has 28 inputs and generates 81 product terms. The product terms are fed into a single logic block made up of 16 macrocells. The output signals of the ispPAC-POWR607 device are derived from the PLD as shown in Figure 10.

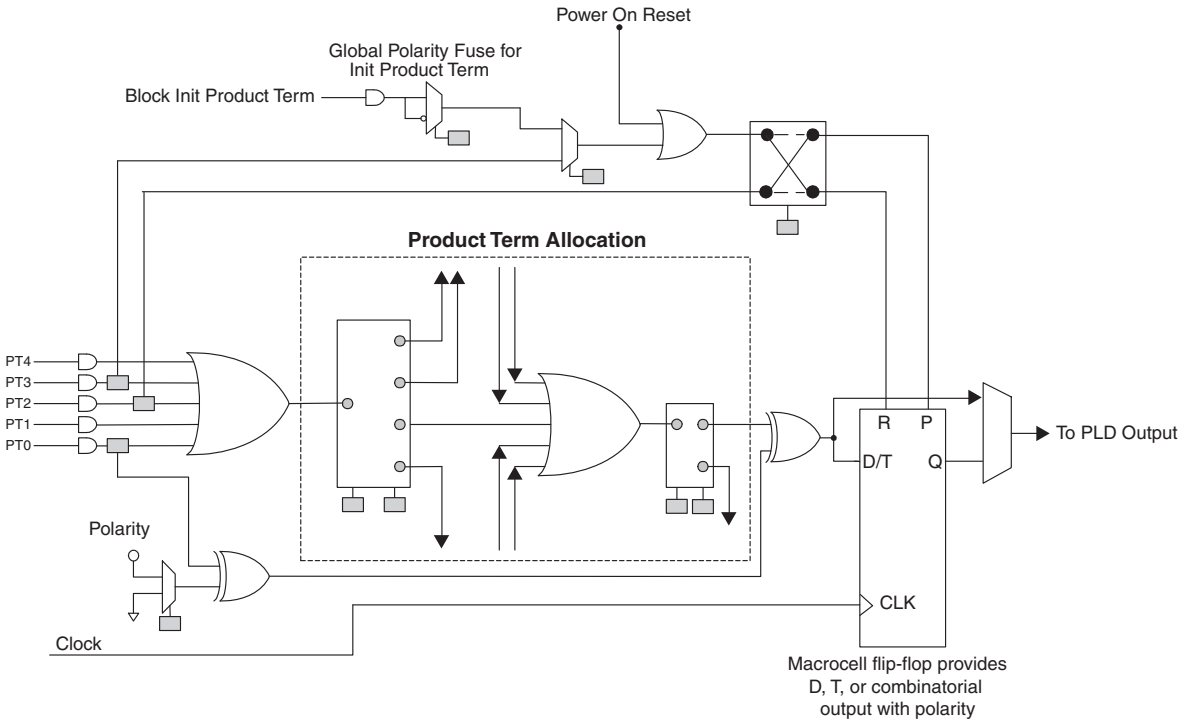
Figure 10. ispPAC-POWR607 PLD Architecture



Macrocell Architecture

The macrocell shown in Figure 11 is the heart of the PLD. The basic macrocell has five product terms that feed the OR gate and the flip-flop. The flip-flop in each macrocell is independently configured. It can be programmed to function as a D-Type or T-Type flip-flop. Combinatorial functions are realized by bypassing the flip-flop. The polarity control and XOR gates provide additional flexibility for logic synthesis. The flip-flop's clock is driven from the common PLD clock that is generated by dividing the 8 MHz master clock (MCLK) by 32. The macrocell also supports asynchronous reset and preset functions, derived from either product terms or the power-on reset signal. The resources within the macrocells share routing and contain a product term allocation array. The product term allocation array greatly expands the PLD's ability to implement complex logical functions by allowing logic to be shared between adjacent blocks and distributing the product terms to allow for wider decode functions. All the digital inputs are registered by MCLK and all VMON comparator outputs are registered using the PLD Clock to synchronize them to the PLD logic as shown in Figure 10.

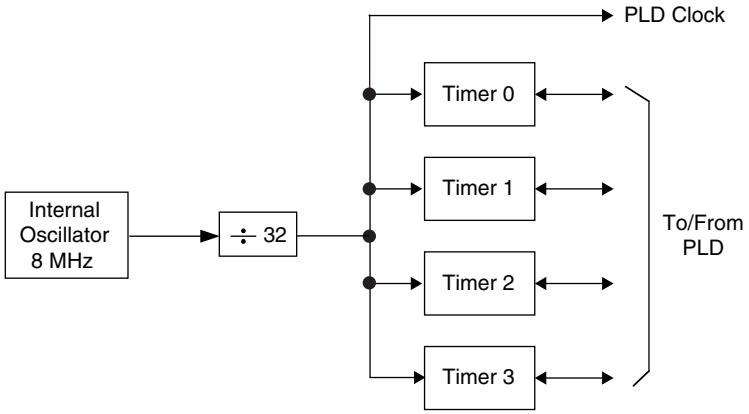
Figure 11. ispPAC-POWR607 Macrocell Block Diagram



Clock and Timer Functions

Figure 12 shows a block diagram of the ispPAC-POWR607's internal clock and timer systems. The master clock operates at a fixed frequency of 8 MHz, from which a fixed 250 kHz PLD clock is derived.

Figure 12. Clock and Timer System



The internal oscillator runs at a fixed frequency of 8 MHz. This signal is used as a source for the PLD and timer clocks. It is also used for clocking the comparator outputs and clocking the digital filters in the voltage monitor circuits.

A divide-by-32 prescaler divides the internal 8 MHz oscillator down to 250 kHz for the PLD clock and for the programmable timers. Each of the four timers provides independent timeout intervals ranging from 32 µs to 1.96 seconds in 128 steps.

Digital Inputs and Optional Device Power Down

The ispPAC-POWR607 has two dedicated digital input pins which are registered by MCLK as shown in Figure 10 and then connect to the input AND array of the PLD (IN[1:2]). The pins are standard CMOS inputs and are referenced to VCC.

The optional power-down mode is a programmable feature controlled via the IN1_$\overline{\text{PWRDN}}$ pin. It is used to power-down the ispPAC-POWR607 and power it up again as desired. When in power-down mode, the ispPAC-POWR607 draws a minimal amount of supply current (less than 10 µA max). The device is brought out of power-down mode by applying a logic high signal on the level sensitive IN1_$\overline{\text{PWRDN}}$ pin.

When it exits power-down mode, the ispPAC-POWR607 is internally reset to its initial power-on state before resuming normal operation. The logic and limited memory needed to “wakeup” on cue are all that remain on during power-down mode. Other functions and capabilities, such as voltage monitoring, FET drive capability and PLD logic states are all lost when the ispPAC-POWR607 is in power-down mode. Open drain outputs and MOSFET driver pins go into Hi-Z mode and all digital inputs, except IN1_$\overline{\text{PWRDN}}$, stop responding to logic input signals.

There are two E^2CMOS bits associated with the ispPAC-POWR607 power-down function. Configuring these bits for specific power-down functionality is achieved using PAC-Designer, a software design tool for Lattice programmable mixed signal devices. Table 4 is a truth table detailing the operation of the ispPAC-POWR607 power-down logical control function.

Table 4. PWRDN Truth Table

IN1_PWRDN Input Pin	PLD_PWRDN Internal Signal	PWRDN Enable Bit	PWRDN Source Bit	Power Mode
X	X	Clear	X	Normal
1	X	Set	X	Normal
0	X	Set	IN1_PWRDN Pin	Power-down
0	0	Set	Internal Signal PLD_PWRDN	Power-down

Note: When in power-down mode, the ispPAC-POWR607 will not respond to logic inputs (except to the IN1_PWRDN pin) and all outputs will be high impedance.

To use the ispPAC-POWR607's power-down function, the E^2CMOS PWRDN enable bit must be set during initial device design configuration. Power-down is disabled otherwise (the initial default).

When power is first applied to ispPAC-POWR607, the device checks to see if a power-down condition exists, and then if it is already present will proceed immediately to the power-down state. During the brief period that the device is on, it will consume full power but it will proceed directly to power-down mode without executing any state machine instructions, etc. This time to initially detect the power-down command and then shut down is given in the power-down specifications section of the datasheet.

In addition to the IN1_$\overline{\text{PWRDN}}$ pin, Table 4 shows how an alternate signal from the PLD called PLD_PWRDN can be used to initiate power-down (not the default). This can be useful when power-down is the last step in a series of ispPAC-POWR607 PLD controlled states, such as turning off supplies in sequence or acknowledging processor signals, etc.

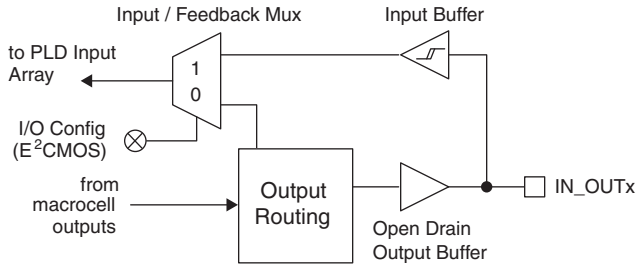
Note: The only way to exit power-down mode, regardless of how it's initiated, is with the IN1_$\overline{\text{PWRDN}}$ pin. Applying a logic high to IN1_$\overline{\text{PWRDN}}$ will always return the ispPAC-POWR607 to normal operation. Finally, whenever the ispPAC-POWR607 is in power-down mode, VCCJ is internally pulled to GND to turn off the JTAG I/O pins. It is important, therefore, that the VCCJ pin be open when power-down mode is initiated. If connected to a power supply during power-down mode, VCCJ will draw approximately 2.2 mA.

Dual Purpose Digital I/O Pins

The ispPAC-POWR607 provides seven possible digital outputs, HVOUT[1:2] and IN_OUT[3:7]. Any number of these pins can be configured to act as open drain outputs, providing a high degree of flexibility when interfacing to logic signals, LEDs, opto-couplers, and power supply control inputs. The HVOUT[1:2] pins can also be configured as high voltage FET drivers and are discussed more in the next section. The digital I/O pins can also be programmed to be true digital inputs.

It should be noted the IN_OUT[3:7] pins are not true bidirectional pins and individually they can only act as an input or as an output, but not both at the same time. A simplified diagram of how this is accomplished is shown in Figure 13. There is a user configurable E^2CMOS bit for each of the IN_OUT[3:7] pins that determines whether the pin is a dedicated input or open drain output.

Figure 13. Programmable Digital Input/Output Pins (IN_OUT)



The architecture takes advantage of routing that normally feeds all PLD macrocell outputs back into the input AND array. Output pins are realized when some number of macrocell outputs are selected from the PLD to become digital open drain outputs. When programmed to be outputs, IN_OUTx pins are configured exactly this way. When programmed to be digital input pins, the open drain buffer is permanently turned off (set to Hi-Z) and the input from IN_OUTx pin goes to the input array instead of the macrocell's output. The macrocell output is still available and can be connected to a different output pin if desired. When the IN-OUTx pins are configured as digital input pins, the signal is registered by MCLK prior to going to the input AND array the same as the IN1 and IN2 digital inputs.

High-Voltage Outputs

The ispPAC-POWR607's HVOUT1-HVOUT2 output pins can be programmed to operate either as high-voltage FET drivers or optionally as open drain digital outputs. Figure 14 shows the details of the HVOUT gate drivers. Each of these outputs is controlled from the PLD.

Figure 14. Basic Function Diagram for an Output in High Voltage MOSFET Gate Driver Mode

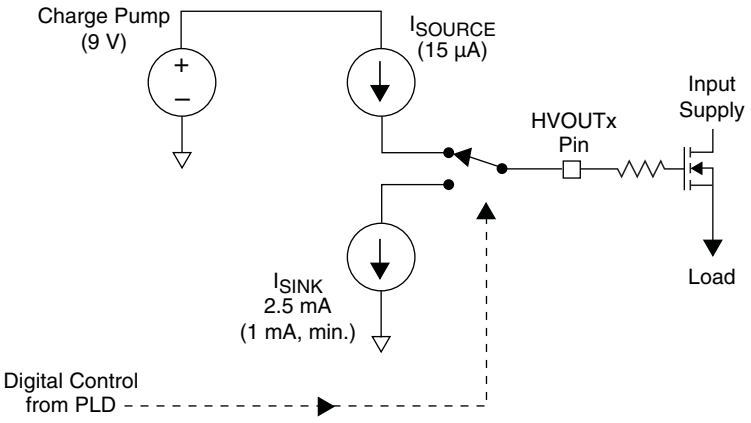


Figure 14 shows the HVOUT functionality when programmed as a FET driver. In this mode the output either sources current from a charge pump or sinks current. The voltage that the output level at the pin will rise to is typi-

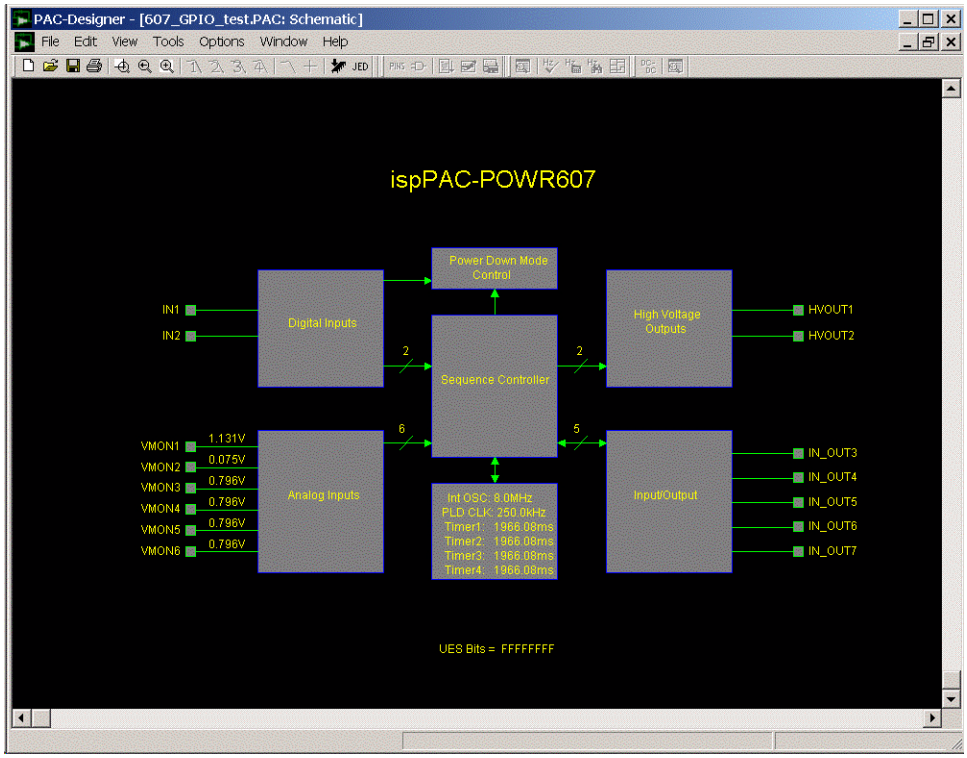
cally 9 V. (This level is not programmable, unlike other Power Manager II devices). The maximum voltage levels required depend on the gate-to-source threshold of the FET being driven and the power supply voltage being switched. The maximum voltage level needs to be sufficient to bias on the gate-to-source threshold and also accommodate the load voltage at the FET's source, when the source pin of the FET is tied to the supply of the target board. When the HVOUT pin is sourcing current (charging a FET gate) the source current is 15 µA. When the driver is turned to the off state, the driver will sink current to ground, and this sink current is typically 2.5 mA (1 mA min.) to quickly turn off the FET.

During initial power up and for short periods of time during programming, the HVOUTx pins will assume a high impedance output configuration (Hi-Z). This occurs whether the pin is configured as a high voltage MOSFET driver or as an open drain output. It happens due to the period of uncertainty before the E^2CMOS memory is resolved at initial turn on and whenever being re-programmed. To insure any FETs controlled by ispPAC-POWR607 HVOUTx pins are always off during these times, place a 10 MΩ (min) resistor between each HVOUTx pin and ground. Since this will subtract less than 1 uA from the total drive capability of the HVOUT pin in FET driver mode, it will have a negligible affect on its specified drive performance.

Software-Based Design Environment

Designers can configure the ispPAC-POWR607 using PAC-Designer, an easy to use, Microsoft Windows compatible program. Circuit designs are entered graphically and then verified, all within the PAC-Designer environment. Full device programming is supported using PC parallel port I/O operations and a download cable connected to the serial programming interface pins of the ispPAC-POWR607. A library of configurations is included with basic solutions and examples of advanced circuit techniques are available on the Lattice web site for downloading. In addition, comprehensive on-line and printed documentation is provided that covers all aspects of PAC-Designer operation. The PAC-Designer schematic window, shown in Figure 15, provides access to all configurable ispPAC-POWR607 elements via its graphical user interface. All analog input and output pins are represented. Static or non-configurable pins such as power, ground, and the serial digital interface are omitted for clarity. Any element in the schematic window can be accessed via mouse operations as well as menu commands. When completed, configurations can be saved, simulated, and downloaded to devices.

Figure 15. PAC-Designer ispPAC-POWR607 Design Entry Screen



In-System Programming

The ispPAC-POWR607 is an in-system programmable device. This is accomplished by integrating all E^2 configuration memory on-chip. Programming is performed through a 4-wire, IEEE 1149.1 compliant serial JTAG interface at normal logic levels. Once a device is programmed, all configuration information is stored on-chip, in non-volatile E^2CMOS memory cells. The specifics of the IEEE 1149.1 serial interface and all ispPAC-POWR607 instructions are described in the JTAG interface section of this data sheet.

User Electronic Signature

A user electronic signature (UES) feature is included in the E^2CMOS memory of the ispPAC-POWR607. This consists of 32 bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control data. The specifics of this feature are discussed in the IEEE 1149.1 serial interface section of this data sheet.

Electronic Security

An electronic security “fuse” (ESF) bit is provided in every ispPAC-POWR607 device to prevent unauthorized readout of the E^2CMOS configuration bit patterns. Once programmed, this cell prevents further access to the functional user bits in the device. This cell can only be erased by reprogramming the device, so the original configuration cannot be examined once programmed. Usage of this feature is optional. The specifics of this feature are discussed in the IEEE 1149.1 serial interface section of this data sheet.

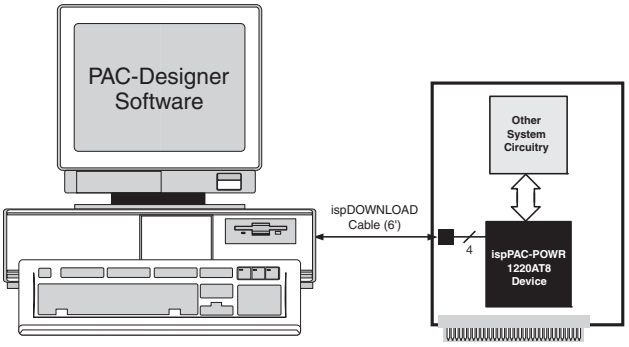
Production Programming Support

Once a final configuration is determined, an ASCII format JEDEC file can be created using the PAC-Designer software. Devices can then be ordered through the usual supply channels with the user’s specific configuration already preloaded into the devices. By virtue of its standard interface, compatibility is maintained with existing production programming equipment, giving customers a wide degree of freedom and flexibility in production planning.

Evaluation Fixture

Because the features of an ispPAC-POWR607 are all included in the larger ispPAC-POWR1220AT8 device, designs implemented in an ispPAC-POWR607 can be verified using an ispPAC-POWR1220AT8 engineering prototype board connected to the parallel port of a PC with a Lattice ispDOWNLOAD® cable. The board demonstrates proper layout techniques and can be used in real time to check circuit operation as part of the design process. Input and output connections are provided to aid in the evaluation of the functionality implemented in ispPAC-POWR607 for a given application. (Figure 16).

Figure 16. Download from a PC



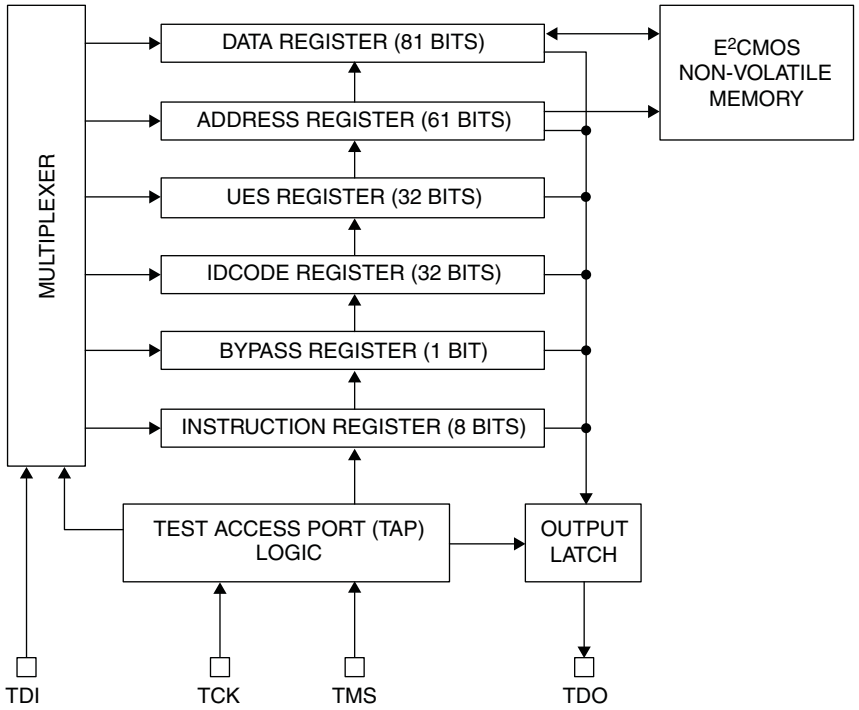
IEEE Standard 1149.1 Interface (JTAG)

Serial Port Programming Interface Communication with the ispPAC-POWR607 is facilitated via an IEEE 1149.1 test access port (TAP). It is used by the ispPAC-POWR607 as a serial programming interface. A brief description of the ispPAC-POWR607 JTAG interface follows. For complete details of the reference specification, refer to the publication, Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990 (which now includes IEEE Std 1149.1a-1993).

Overview

An IEEE 1149.1 test access port (TAP) provides the control interface for serially accessing the digital I/O of the ispPAC-POWR607. The TAP controller is a state machine driven with mode and clock inputs. Given in the correct sequence, instructions are shifted into an instruction register, which then determines subsequent data input, data output, and related operations. Device programming is performed by addressing the configuration register, shifting data in, and then executing a program configuration instruction, after which the data is transferred to internal E^2CMOS cells. It is these non-volatile cells that store the configuration or the ispPAC-POWR607. A set of instructions are defined that access all data registers and perform other internal control operations. For compatibility between compliant devices, two data registers are mandated by the IEEE 1149.1 specification. Others are functionally specified, but inclusion is strictly optional. Finally, there are provisions for optional data registers defined by the manufacturer. The two required registers are the bypass and boundary-scan registers. Figure 17 shows how the instruction and various data registers are organized in an ispPAC-POWR607.

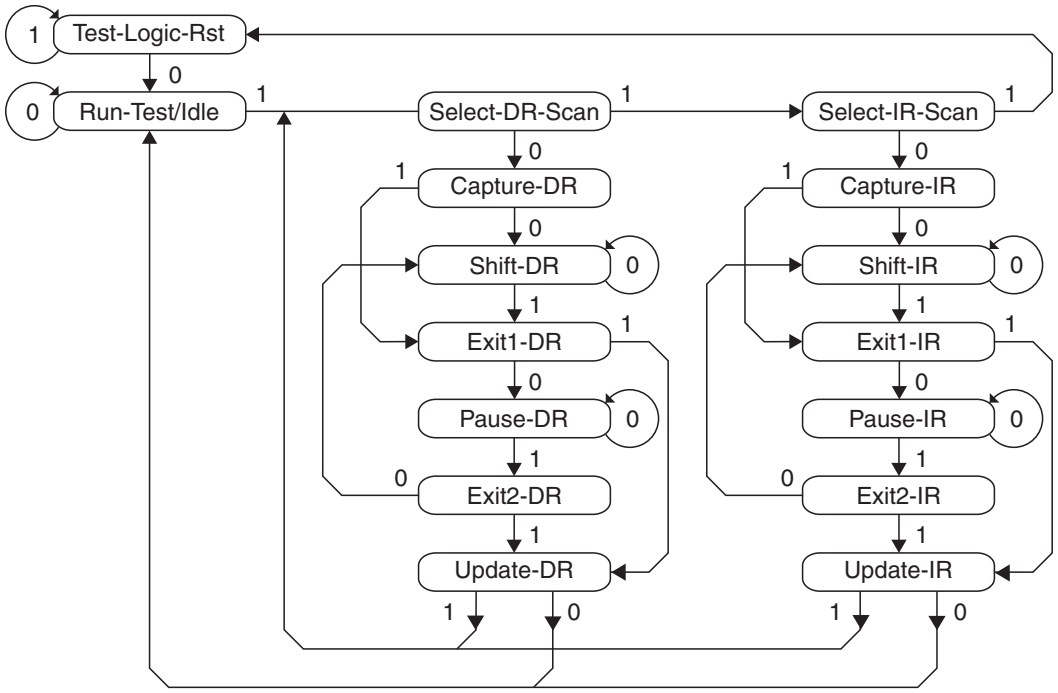
Figure 17. ispPAC-POWR607 TAP Registers



TAP Controller Specifics

The TAP is controlled by the Test Clock (TCK) and Test Mode Select (TMS) inputs. These inputs determine whether an Instruction Register or Data Register operation is performed. Driven by the TCK input, the TAP consists of a small 16-state controller design. In a given state, the controller responds according to the level on the TMS input as shown in Figure 18. Test Data In (TDI) and TMS are latched on the rising edge of TCK, with Test Data Out (TDO) becoming valid on the falling edge of TCK. There are six steady states within the controller: Test-Logic-Reset, Run- Test/Idle, Shift-Data-Register, Pause-Data-Register, Shift-Instruction-Register and Pause-Instruction-Register. But there is only one steady state for the condition when TMS is set high: the Test-Logic-Reset state. This allows a reset of the test logic within five TCKs or less by keeping the TMS input high. Test-Logic-Reset is the power-on default state.

Figure 18. TAP States



Note: The value shown adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.

When the correct logic sequence is applied to the TMS and TCK inputs, the TAP will exit the Test-Logic-Reset state and move to the desired state. The next state after Test-Logic-Reset is Run-Test/Idle. Until a data or instruction shift is performed, no action will occur in Run-Test/Idle (steady state = idle). After Run-Test/Idle, either a data or instruction shift is performed. The states of the Data and Instruction Register blocks are identical to each other differing only in their entry points. When either block is entered, the first action is a capture operation. For the Data Registers, the Capture-DR state is very simple: it captures (parallel loads) data onto the selected serial data path (previously chosen with the appropriate instruction). For the Instruction Register, the Capture-IR state will always load the IDCODE instruction. It will always enable the ID Register for readout if no other instruction is loaded prior to a Shift-DR operation. This, in conjunction with mandated bit codes, allows a “blind” interrogation of any device in a compliant IEEE 1149.1 serial chain. From the Capture state, the TAP transitions to either the Shift or Exit1 state. Normally the Shift state follows the Capture state so that test data or status information can be shifted out or new data shifted in. Following the Shift state, the TAP either returns to the Run-Test/Idle state via the Exit1 and Update states or enters the Pause state via Exit1. The Pause state is used to temporarily suspend the shifting of data through either the Data or Instruction Register while an external operation is performed. From the Pause state, shifting can resume by reentering the Shift state via the Exit2 state or be terminated by entering the Run-Test/Idle state via the Exit2 and Update states. If the proper instruction is shifted in during a Shift-IR operation, the next entry into Run-Test/Idle initiates the test mode (steady state = test). This is when the device is actually programmed, erased or verified. All other instructions are executed in the Update state.

Test Instructions

Like data registers, the IEEE 1149.1 standard also mandates the inclusion of certain instructions. It outlines the function of three required and six optional instructions. Any additional instructions are left exclusively for the manufacturer to determine. The instruction word length is not mandated other than to be a minimum of two bits, with only the BYPASS and EXTEST instruction code patterns being specifically called out (all ones and all zeroes respectively). The ispPAC-POWR607 contains the required minimum instruction set as well as one from the optional instruction set. In addition, there are several proprietary instructions that allow the device to be configured and verified. Table 5 lists the instructions supported by the ispPAC-POWR607 JTAG Test Access Port (TAP) controller:

Table 5. ispPAC-POWR607 TAP Instruction Table

Instruction	Command Code	Comments
BULK_ERASE	0000 0011	Bulk erase device
BYPASS	1111 1111	Bypass - connect TDO to TDI
DISCHARGE	0001 0100	Fast VPP discharge
ERASE_DONE_BIT	0010 0100	Erases 'Done' bit only
EXTEST	0000 0000	Bypass - connect TDO to TDI
IDCODE	0001 0110	Read contents of manufacturer ID code (32 bits)
OUTPUTS_HIGHZ	0001 1000	Force all outputs to High-Z state, including FET driver outputs
SAMPLE/PRELOAD	00011100	Sample/Preload. Default to bypass.
PROGRAM_DISABLE	0001 1110	Disable program mode
PROGRAM_DONE_BIT	0010 1111	Programs the Done bit
PROGRAM_ENABLE	0001 0101	Enable program mode
PROGRAM_SECURITY	0000 1001	Program security fuse
RESET	0010 0010	Resets device
PLD_ADDRESS_SHIFT	0000 0001	PLD_Address register (61 bits)
PLD_DATA_SHIFT	0000 0010	PLD_Data register (81 bits)
PLD_INIT_ADDR_FOR_PROG_INCR	0010 0001	Initialize the address register for auto increment
PLD_PROG_INCR	0010 0111	Program column register to E^2 and auto increment address register
PLD_PROGRAM	0000 0111	Program PLD data register to E^2
PLD_VERIFY	0000 1010	Verifies PLD column data
PLD_VERIFY_INCR	0010 1010	Load column register from E^2 and auto increment address register
UES_PROGRAM	0001 1010	Program UES bits into E^2
UES_READ	0001 0111	Read contents of UES register from E^2 (32 bits)

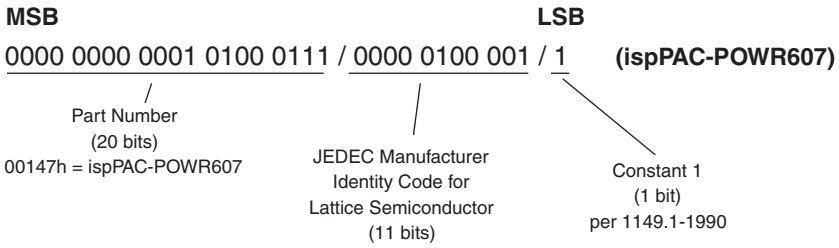
BYPASS is one of the three required instructions. It selects the Bypass Register to be connected between TDI and TDO and allows serial data to be transferred through the device without affecting the operation of the ispPAC-POWR607. The IEEE 1149.1 standard defines the bit code of this instruction to be all ones (11111111).

The required **SAMPLE/PRELOAD** instruction dictates the Boundary-Scan Register be connected between TDI and TDO. The ispPAC-POWR607 has no boundary scan register, so for compatibility it defaults to the BYPASS mode whenever this instruction is received. The bit code for this instruction is defined by Lattice as shown in Table 5.

The **EXTEST** (external test) instruction is required and would normally place the device into an external boundary test mode while also enabling the boundary scan register to be connected between TDI and TDO. Again, since the ispPAC-POWR607 has no boundary scan logic, the device is put in the BYPASS mode to ensure specification compatibility. The bit code of this instruction is defined by the 1149.1 standard to be all zeros (00000000).

The optional **IDCODE** (identification code) instruction is incorporated in the ispPAC-POWR607 and leaves it in its functional mode when executed. It selects the Device Identification Register to be connected between TDI and TDO. The Identification Register is a 32-bit shift register containing information regarding the IC manufacturer, device type and version code (Figure 19). Access to the Identification Register is immediately available, via a TAP data scan operation, after power-up of the device, or by issuing a Test-Logic-Reset instruction. The bit code for this instruction is defined by Lattice as shown in Table 5.

Figure 19. ispPAC-POWR607 ID Code



ispPAC-POWR607 Specific Instructions

There are 25 unique instructions specified by Lattice for the ispPAC-POWR607. These instructions are primarily used to interface to the various user registers and the E^2CMOS non-volatile memory. Additional instructions are used to control or monitor other features of the device. A brief description of each unique instruction is provided in detail below, and the bit codes are found in Table 5.

PLD_ADDRESS_SHIFT – This instruction is used to set the address of the PLD AND/ARCH arrays for subsequent program or read operations. This instruction also forces the outputs into the OUTPUTS_HIGHZ.

PLD_DATA_SHIFT – This instruction is used to shift PLD data into the register prior to programming or reading. This instruction also forces the outputs into the OUTPUTS_HIGHZ.

PLD_INIT_ADDR_FOR_PROG_INCR – This instruction prepares the PLD address register for subsequent PLD_PROG_INCR or PLD_VERIFY_INCR instructions.

PLD_PROG_INCR – This instruction programs the PLD data register for the current address and increments the address register for the next set of data.

PLD_PROGRAM – This instruction programs the selected PLD AND/ARCH array column. The specific column is preselected by using PLD_ADDRESS_SHIFT instruction. The programming occurs at the second rising edge of the TCK in Run-Test-Idle JTAG state. The device must already be in programming mode (PROGRAM_ENABLE instruction). This instruction also forces the outputs into the OUTPUTS_HIGHZ.

PROGRAM_SECURITY – This instruction is used to program the electronic security fuse (ESF) bit. Programming the ESF bit protects proprietary designs from being read out. The programming occurs at the second rising edge of the TCK in Run-Test-Idle JTAG state. The device must already be in programming mode (PROGRAM_ENABLE instruction). This instruction also forces the outputs into the OUTPUTS_HIGHZ.

PLD_VERIFY – This instruction is used to read the content of the selected PLD AND/ARCH array column. This specific column is preselected by using PLD_ADDRESS_SHIFT instruction. This instruction also forces the outputs into the OUTPUTS_HIGHZ.

DISCHARGE – This instruction is used to discharge the internal programming supply voltage after an erase or programming cycle and prepares ispPAC-POWR607 for a read cycle. This instruction also forces the outputs into the OUTPUTS_HIGHZ.

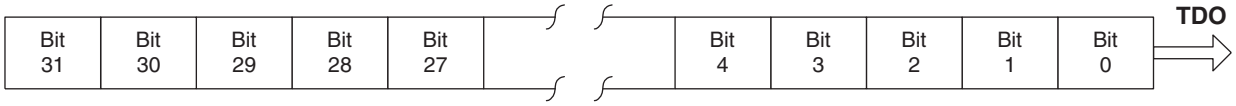
BULK_ERASE – This instruction will bulk erase all E^2CMOS bits (CFG, PLD, UES, and ESF) in the ispPAC-POWR607. The device must already be in programming mode (PROGRAM_ENABLE instruction). This instruction also forces the outputs into the OUTPUTS_HIGHZ.

OUTPUTS_HIGHZ – This instruction turns off all of the open-drain output transistors. Pins that are programmed as FET drivers will be placed in the active low state. This instruction is effective after Update-Instruction-Register JTAG state.

PROGRAM_ENABLE – This instruction enables the programming mode of the ispPAC-POWR607. This instruction also forces the outputs into the OUTPUTS_HIGHZ.

IDCODE – This instruction connects the output of the Identification Code Data Shift (IDCODE) Register to TDO (Figure 20), to support reading out the identification code.

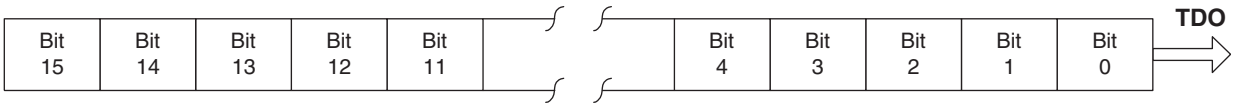
Figure 20. IDCODE Register



PROGRAM_DISABLE – This instruction disables the programming mode of the ispPAC-POWR607. The Test-Logic-Reset JTAG state can also be used to cancel the programming mode of the ispPAC-POWR607.

UES_READ – This instruction both reads the E^2CMOS bits into the UES register and places the UES register between the TDI and TDO pins (as shown in Figure 17), to support programming or reading of the user electronic signature bits.

Figure 21. UES Register



UES_PROGRAM – This instruction will program the content of the UES Register into the UES E^2CMOS memory. The device must already be in programming mode (PROGRAM_ENABLE instruction). This instruction also forces the outputs into the OUTPUTS_HIGHZ.

ERASE_DONE_BIT – This instruction clears the 'Done' bit, which prevents the ispPAC-POWR607 sequence from starting.

PROGRAM_DONE_BIT – This instruction sets the 'Done' bit, which enables the ispPAC-POWR607 sequence to start.

RESET – This instruction resets the PLD sequence and output macrocells. The condition of the ispPAC-POWR607 is the same as initial turn-on after POR is completed.

PLD_VERIFY_INCR – This instruction reads out the PLD data register for the current address and increments the address register for the next read.

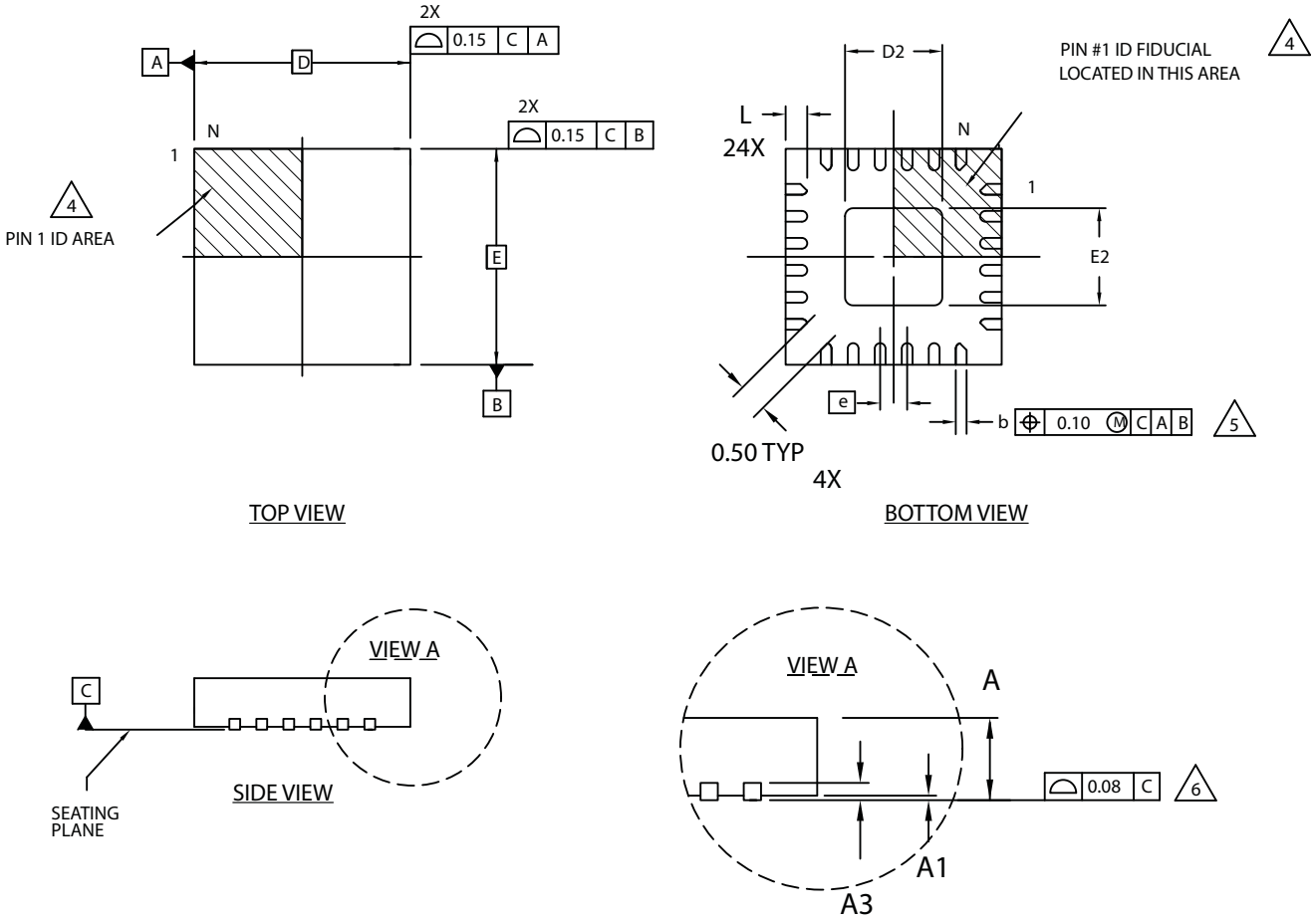
Notes:
In all of the descriptions above, OUTPUTS_HIGHZ refers both to the instruction and the state of the digital and FET driver output pins, in which all are tri-stated.

Before any of the above programming instructions are executed, the respective E^2CMOS bits need to be erased using the corresponding erase instruction.

Package Diagrams

24-Pin QFNS

Dimensions in Millimeters



NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. DRAWING CONFORMS TO JEDEC MO-220, VARIATION VGGD-9.

4. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

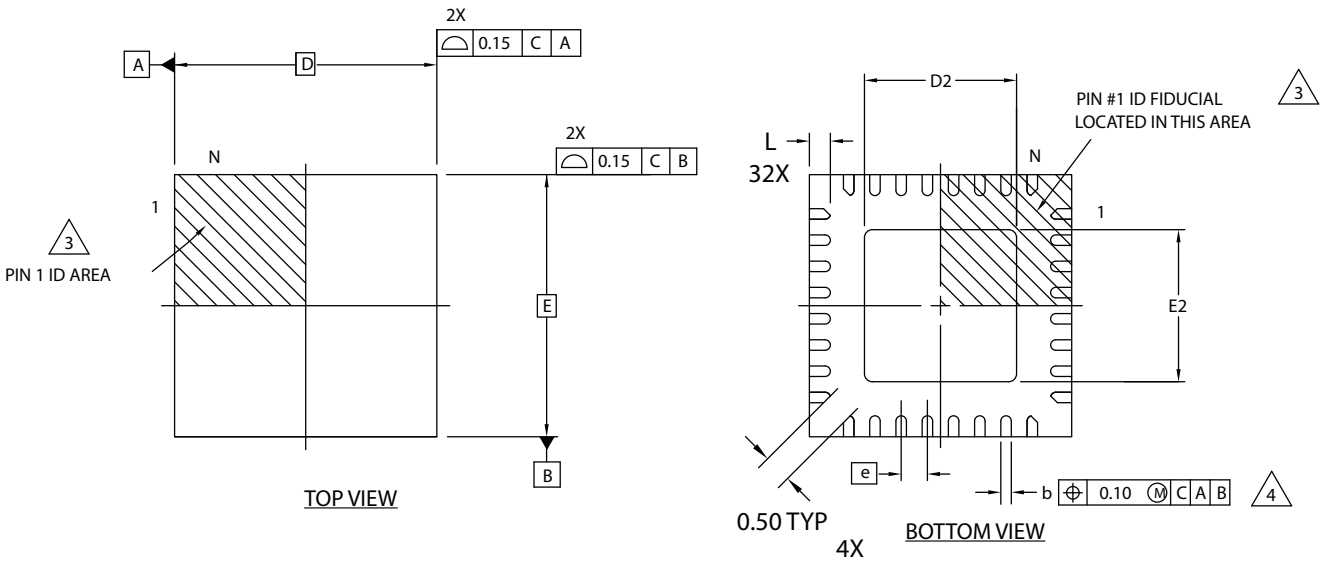
5. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.

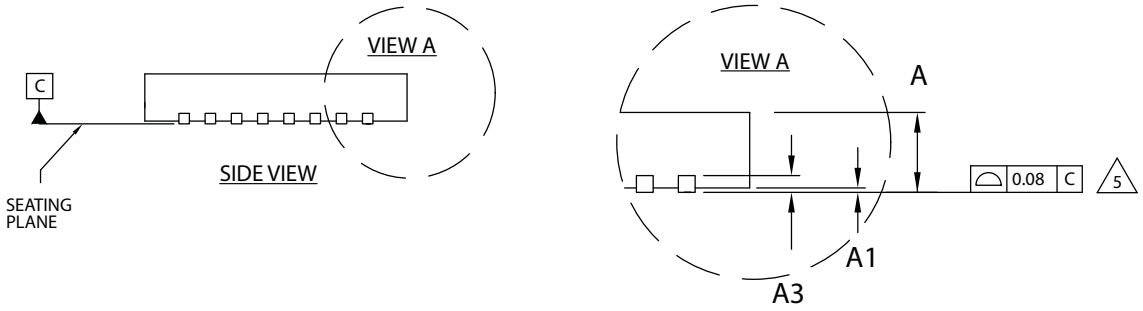
6. APPLIES TO EXPOSED PORTION OF TERMINALS.

SYMBOL	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.2 REF	
D		4.0 BSC	
D2	1.05	-	2.45
E		4.0 BSC	
E2	1.05	-	2.45
b	0.18	0.25	0.30
e		0.50 BSC	
L	0.45	0.50	0.55

32-Pin QFNS

Dimensions in millimeters





NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

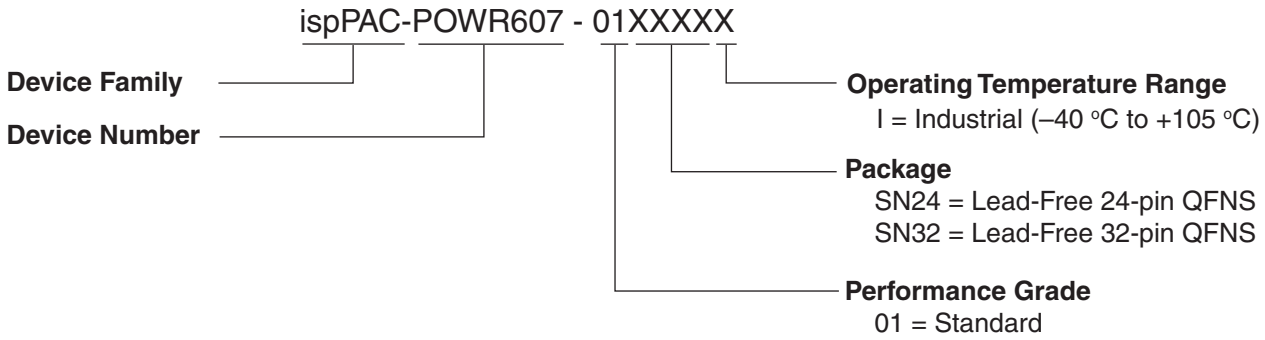
3 EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

4 DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.

5 APPLIES TO EXPOSED PORTION OF TERMINALS.

SYMBOL	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.2 REF	
D		5.0 BSC	
D2	1.25	2.70	3.75
E		5.0 BSC	
E2	1.25	2.70	3.75
b	0.18	0.24	0.30
e		0.50 BSC	
L	0.30	0.40	0.50

Part Number Description



ispPAC-POWR607 Ordering Information

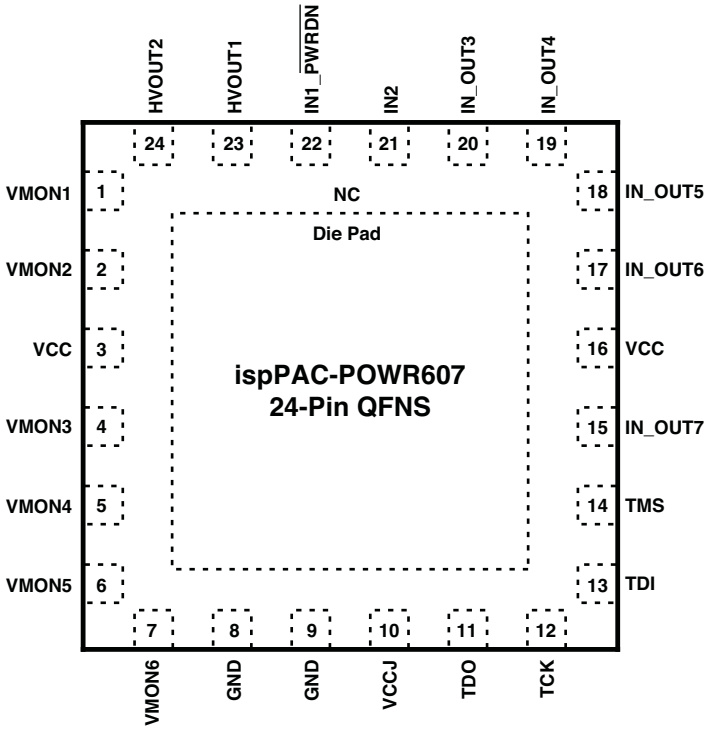
Lead-Free Packaging

Industrial

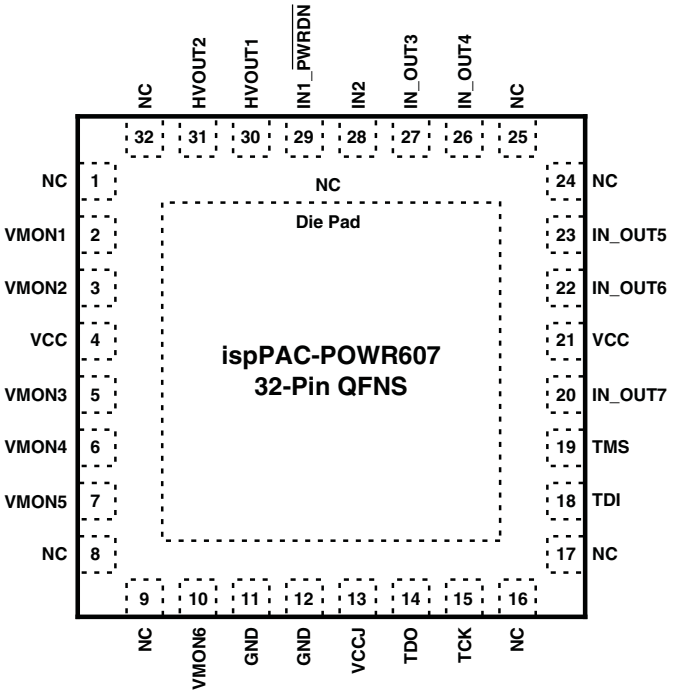
Part Number	Package	Pins
ispPAC-POWR607-01SN32I	Lead-Free QFNS	32
ispPAC-POWR607-01SN24I	Lead-Free QFNS	24

Package Options

24-Pin QFNS Package



32-Pin QFNS Package



Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
April 2015	2.0	Increased Max Temp from 85 °C to 105 °C.
		Updated Recommended Operating Conditions section. Added T_{JOP} information.
		Updated Technical Support Assistance section.
June 2012	01.7	Updated document with new corporate logo.
		Updated for 24-pin QFNS package support.
February 2009	01.6	Updated ispPAC-POWR607 PLD Architecture diagram to clarify that the digital inputs are registered inputs to the AND array.
		Updated Digital Inputs and Optional Device Power Down text section.
		Updated Dual Purpose Digital I/O Pins text section.
December 2008	01.5	Added 32-pin QFNS package Ordering Part Number information per PCN #13A-08.
June 2008	01.4	Added timing diagram and timing parameters to “Power-On Reset” specifications.
		Modified PLD Architecture figure to show input registers.
December 2007	01.3	Final data sheet.
August 2007	01.2	Changes to HVOUT pin specifications.
April 2007	01.1	References to Die Pad added to Pin Descriptions table, Recommended Operating Conditions table and Package Options diagram.
September 2006	01.0	Initial release.

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