



**THE DATASHEET OF  
IP4350CX24/LF,135**



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# IP4350CX24

9-channel SD memory card interface ESD protection filter to IEC 61000-4-2 level 4

Rev. 01 — 5 February 2010

Product data sheet

## 1. Product profile

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### 1.1 General description

The IP4350CX24 is a diode array designed to provide protection to downstream components against ElectroStatic Discharge (ESD) voltages as high as 15 kV.

The IP4350CX24 integrates 9 pairs of rail-to-rail diodes, 12 Zener diodes and 15 resistors in a single wafer-level chip-scale package. It is fabricated using monolithic silicon semiconductor technology and measures only 1.95 mm × 2.11 mm.

These features make the IP4350CX24 ideal for use in applications requiring a high degree of miniaturization, such as mobile phone handsets, cordless telephones and personal digital devices.

### 1.2 Features

- Pb-free, RoHS compliant and free of halogen and antimony (Dark Green compliant)
- All SD memory card channels with integrated ESD protection, EMI and RF filters
- ESD protection up to 15 kV on 9 channels at output terminals
- Integrated EMI and RF filters with pull-up resistors on 5 channels
- Integrated EMI and RF filters on 4 channels
- Additional SD card power supply protection
- Wafer level chip-scale package with 0.4 mm pitch
- Write protection, card detect biasing resistor integrated
- Supports electrical card detection
- Also available as IP4352CX24 with different filter behavior, same footprint

### 1.3 Applications

- SD memory card interfaces in cellular and PCS mobile handsets
- Cordless telephones
- Digital still and video cameras
- Media players
- Card readers

## 2. Pinning information

### 2.1 Pinning

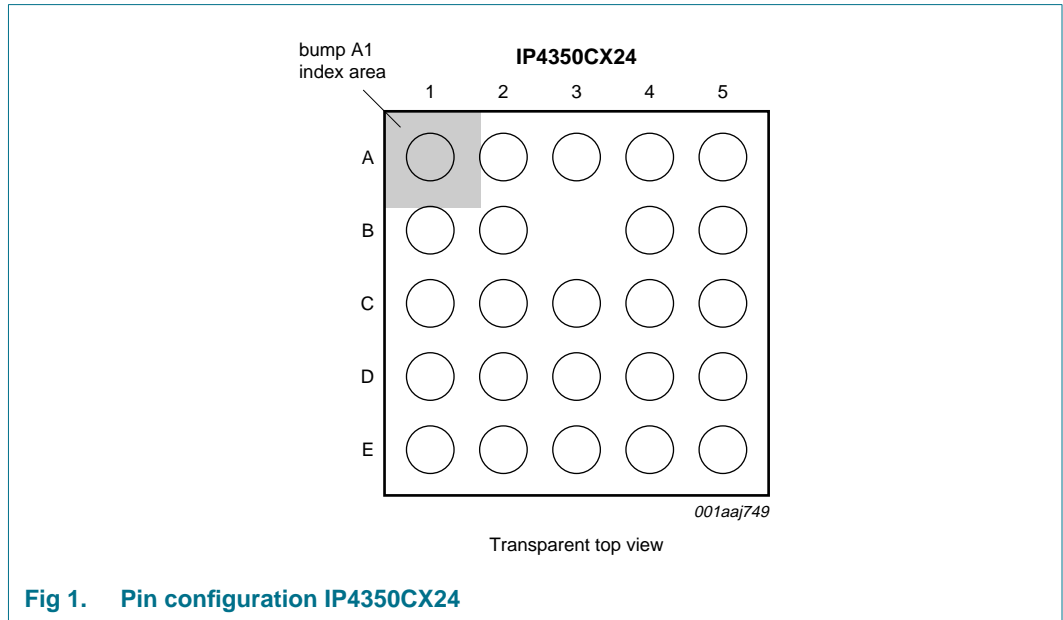


Fig 1. Pin configuration IP4350CX24

### 2.2 Pin description

Table 1. Pin description

Symbol	Pin	Type <sup>[1]</sup>	Description
DATA2	A1	I/O	data 2 input or output
DATA3	A2	I/O	data 3 input or output
GND_H	A3	S	supply ground on host side
SDDATA2	A4	I/O	data 2 input or output on SD card side
SDDATA3	A5	I/O	data 3 input or output on SD card side
CD	B1	O	card detect output
CMD	B2	I/O	command input or output on host side
SDCD	B4	I	card detect input
SDCMD	B5	I/O	command input or output on SD card side
DAT3_PD	C1	I	data 3 pull-down
WP	C2	O	write protect
DAT3_PU	C3	I	data 3 pull-up
SDWP	C4	O	write protect on SD card side
VSD	C5	S	memory card supply voltage
WP+CD	D1	I/O	write protect and card detect
CLK	D2	I/O	clock signal input or output
GND_C	D3	S	card supply ground
SDWP+CD	D4	I/O	write protect and card detect on SD card side
SDCLK	D5	I/O	clock signal on SD card side

Table 1. Pin description ...continued

Symbol	Pin	Type <sup>[1]</sup>	Description
DATA1	E1	I/O	data 1 input or output
DATA0	E2	I/O	data 0 input or output
GND_C	E3	S	card supply ground
SDDATA1	E4	I/O	data 1 input or output on SD card side
SDDATA0	E5	I/O	data 0 input or output on SD card side

[1] I = input, O = output, I/O = input and output, S = power supply.

### 3. Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
IP4350CX24	WLCSP24	wafer level chip-size package; 24 bumps; 1.95 × 2.11 × 0.61 mm	IP4350CX24/LF

### 4. Functional diagram

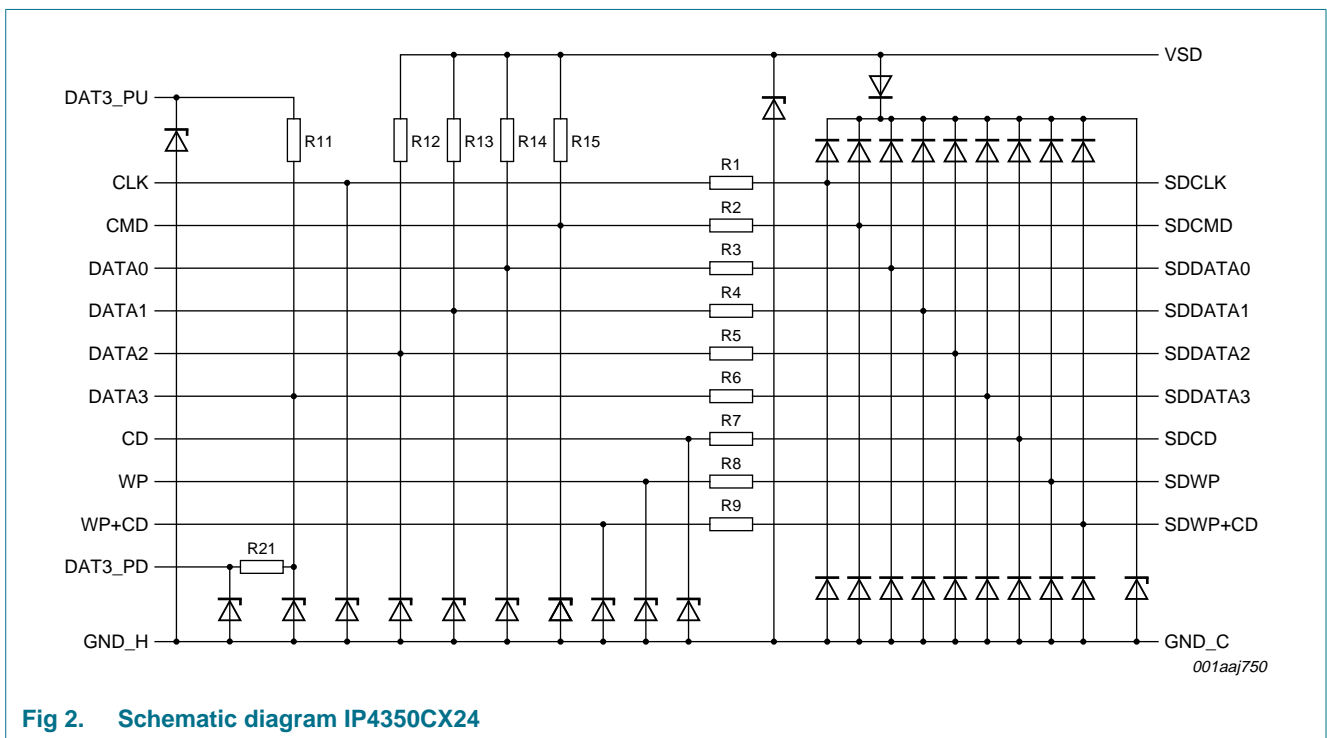


Fig 2. Schematic diagram IP4350CX24

## 5. Limiting values

**Table 3. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_I$	input voltage		-0.5	+5.0	V
$V_{ESD}$	electrostatic discharge voltage	IEC 61000-4-2, level 4; output pins A4, A5, B4, B5, C4, C5, D4, D5, E4, E5 with pins A3, D3, E3 as ground			
		contact discharge	[1] -8	+8	kV
		air discharge	-15	+15	kV
		IEC 61000-4-2, level 1, all other pins with A3, D3, E3 as ground			
		contact discharge	-2	+2	kV
		air discharge	-2	+2	kV
$P_{ch}$	channel power dissipation	continuous power; $T_{amb} = 70\text{ °C}$	-	25	mW
$P_{tot}$	total power dissipation	$T_{amb} = 70\text{ °C}$	-	100	mW
$T_{stg}$	storage temperature		-55	+150	°C
$T_{reflow(peak)}$	peak reflow temperature	10 s maximum	-	260	°C
$T_{amb}$	ambient temperature		-30	+85	°C

[1] Device is qualified with 1000 pulses of  $\pm 15$  kV contact discharges each, according to the IEC 61000-4-2 model and far exceeds the specified level 4 (8 kV contact discharge).

## 6. Characteristics

**Table 4. Characteristics**

$T_{amb} = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{S(ch)}$	channel series resistance	R1 to R9	12	15	18	$\Omega$
		R11 to R14	35	50	65	k $\Omega$
		R15	3.29	4.7	6.11	k $\Omega$
		R21	329	47	611	k $\Omega$
$C_{ch}$	channel capacitance	including diode capacitance; $V_I = 0\text{ V}$ ; $f = 1\text{ MHz}$	[1]			
		each data channel from SD card to I/O interface	-	8.8	-	pF
		CLK channel	-	7.8	-	pF
		DAT3_PD	-	6	-	pF
		DAT3_PU	-	5	-	pF
		VSD	-	37	-	pF
$V_{BR}$	breakdown voltage	$I_I = 1\text{ mA}$	6	-	-	V
$I_{LR}$	reverse leakage current	$V_I = 3\text{ V}$	-	-	100	nA

[1] Guaranteed by design.

## 7. Frequency response

**Table 5. Frequency response**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\alpha_{ij}$	insertion loss	all channels; $R_{source} = 50 \Omega$ ; $R_L = 50 \Omega$				
		$f < 400 \text{ MHz}$	-	-	3	dB
		$400 \text{ MHz} < f < 800 \text{ MHz}$	3	-	6	dB
		$800 \text{ MHz} < f < 2.5 \text{ GHz}$	6	-	15	dB
		$2.5 \text{ GHz} < f < 6.0 \text{ GHz}$	15	-	25	dB

**Table 6. Time domain response<sup>[1]</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>high speed <math>R_{source} = 50 \Omega</math>; <math>t_r = t_f = 2 \text{ ns}</math><sup>[2]</sup></b>						
$t_r$	rise time	load $20 \text{ pF} \parallel 100 \text{ k}\Omega$	-	2.3	-	ns
		load $40 \text{ pF} \parallel 100 \text{ k}\Omega$	-	3.4	-	ns
$t_f$	fall time	load $20 \text{ pF} \parallel 100 \text{ k}\Omega$	-	2.4	-	ns
		load $40 \text{ pF} \parallel 100 \text{ k}\Omega$	-	3.5	-	ns

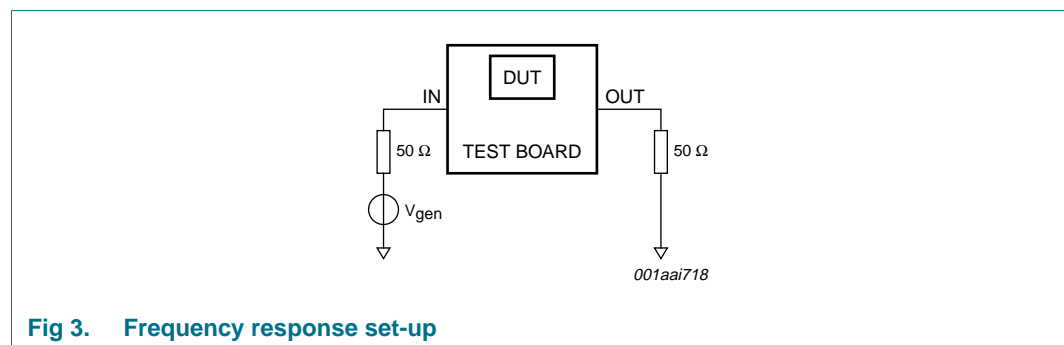
[1] All rise or fall times measured using source with 0 V to 3 V steps, 10 % to 90 %.

[2] Performed on all high speed lines (channels including R1 to R9, see [Figure 2](#)).

## 8. Application information

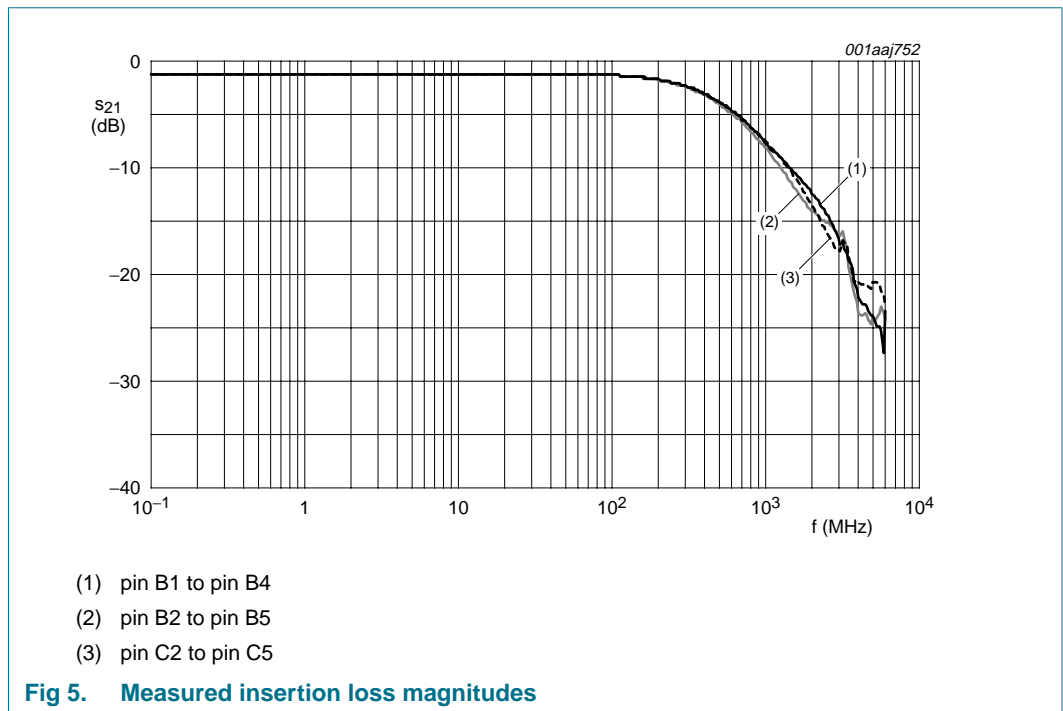
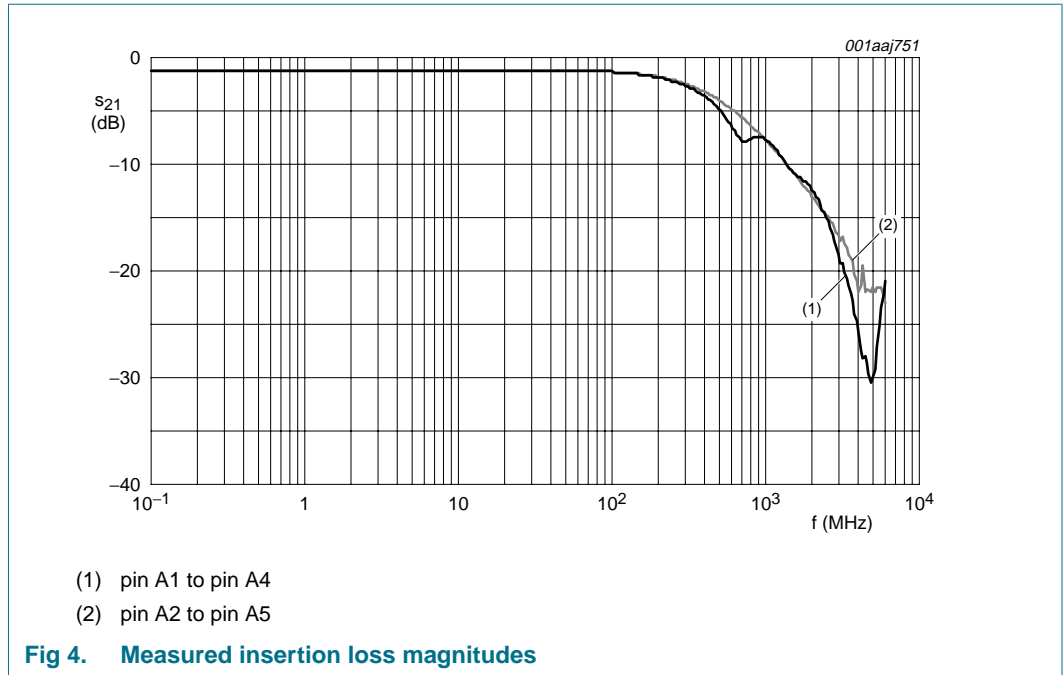
### 8.1 Insertion loss

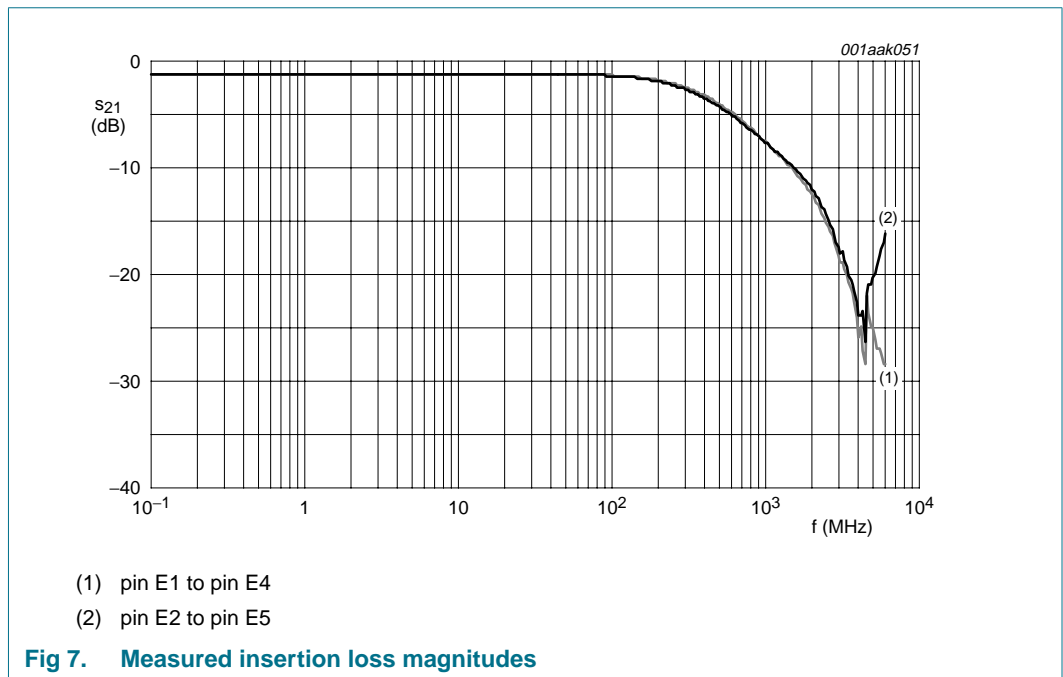
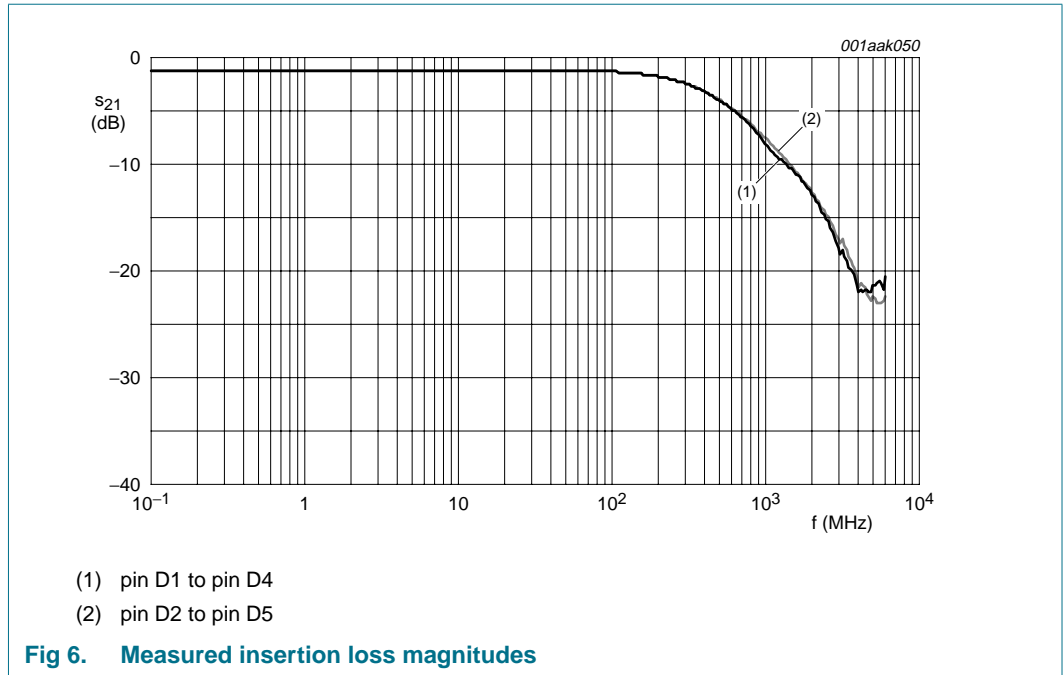
The insertion loss measurement configuration of a typical NetWork Analyzer (NWA) system is shown in [Figure 3](#). The insertion loss is measured with a test PCB utilizing laser drilled micro-via holes that connect the PCB ground plane to the IP4350CX24 ground pins.



**Fig 3. Frequency response set-up**

The frequency response curves for all channels at frequencies up to 6 GHz are shown in [Figure 4](#) to [Figure 7](#).





## 8.2 Crosstalk

The set-up for crosstalk measurements in a 50 Ω NWA system from one channel to another is shown in [Figure 8](#). Typical examples of crosstalk measurement results are depicted in [Figure 9](#), [Figure 10](#) and [Figure 11](#). Unused channels are terminated with 50 Ω to ground.

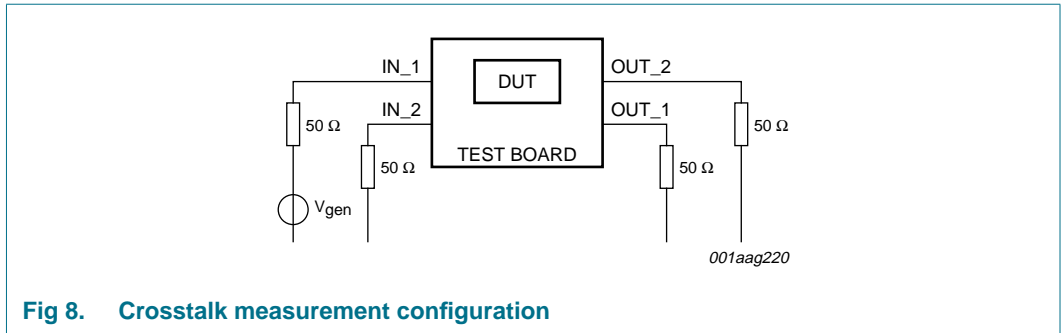


Fig 8. Crosstalk measurement configuration

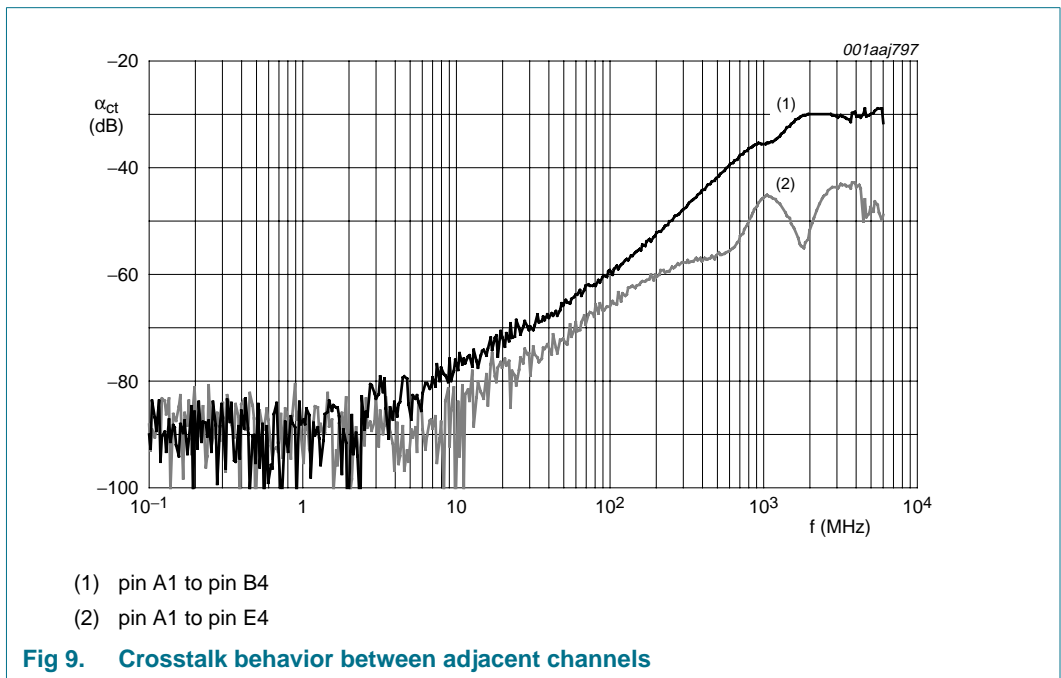
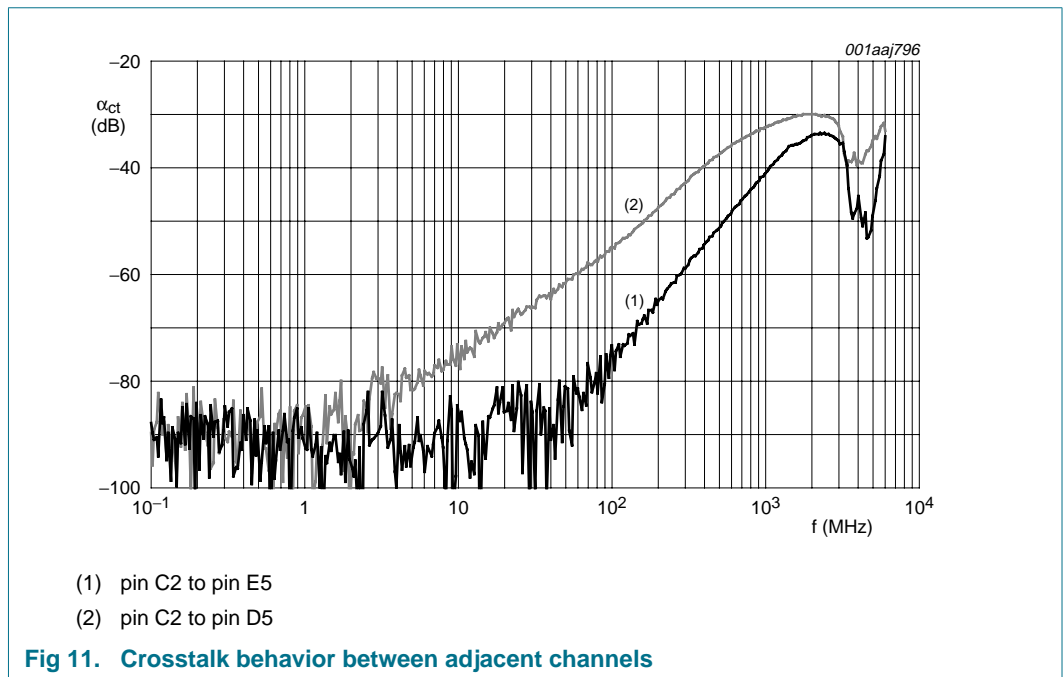
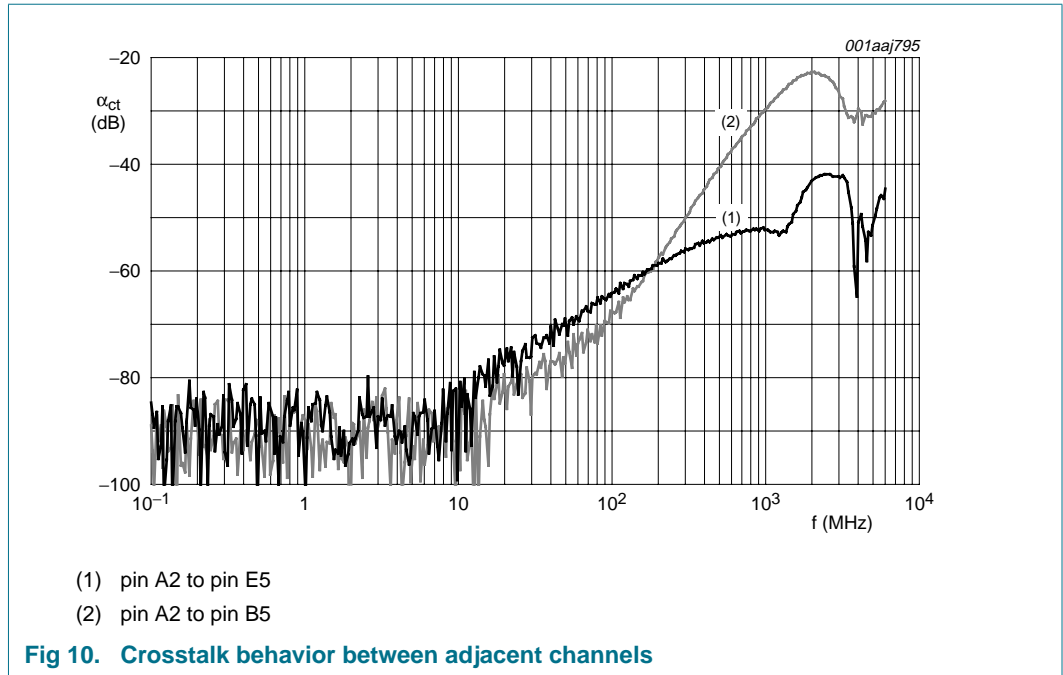


Fig 9. Crosstalk behavior between adjacent channels



9. Package outline

WLCSP24: wafer level chip-size package; 24 bumps; 1.95 x 2.11 x 0.61 mm

IP4350CX24

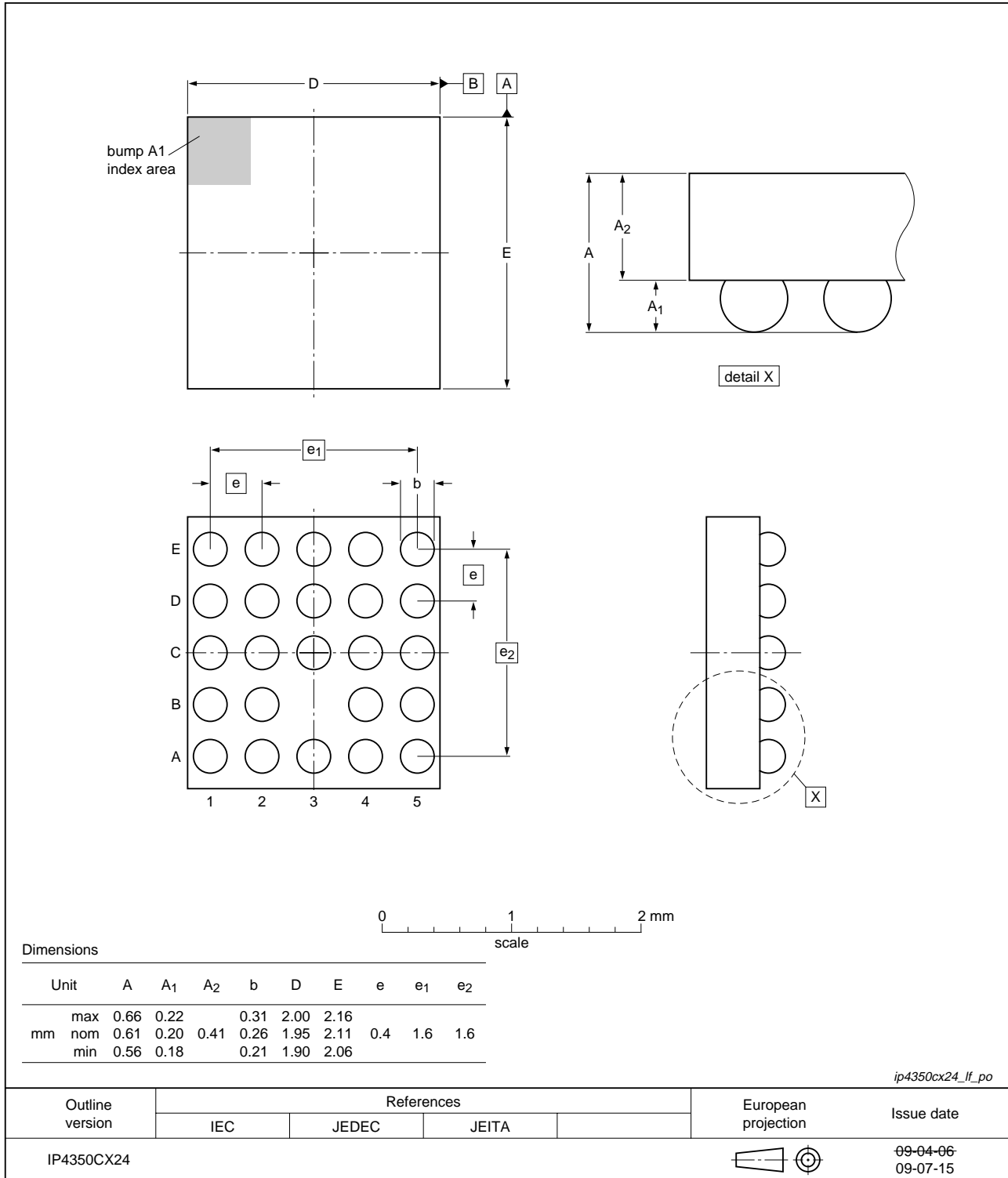


Fig 12. Package outline IP4350CX24/LF (WLCSP24)

## 10. Soldering of WLCSP packages

### 10.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note AN10439 "Wafer Level Chip Scale Package" and in application note AN10365 "Surface mount reflow soldering description".

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

### 10.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

### 10.3 Reflow soldering

Key characteristics in reflow soldering are:

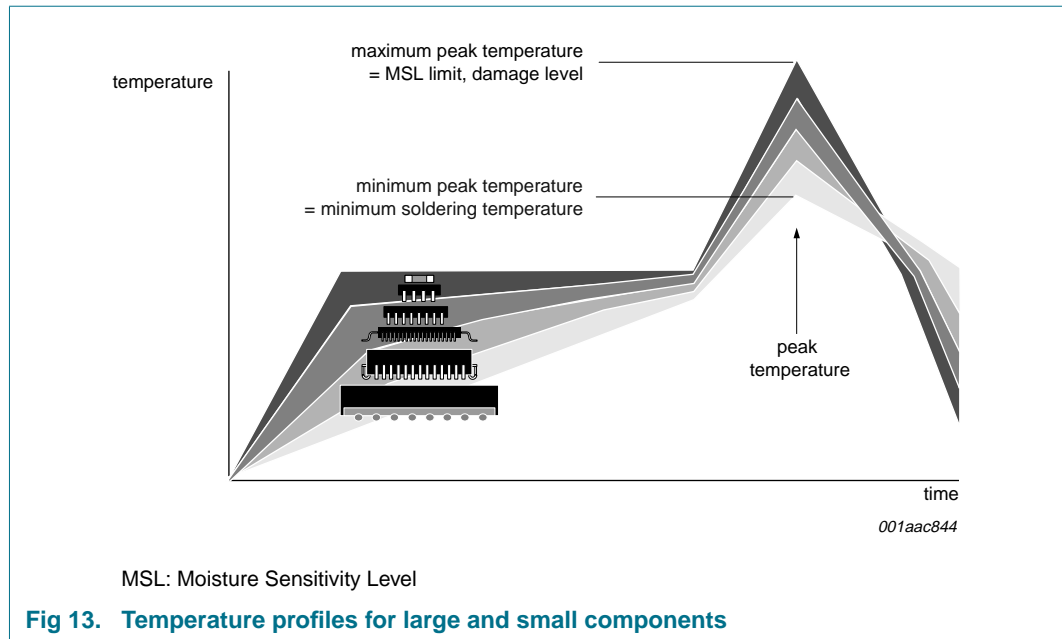
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 13](#)) than a PbSn process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 7](#).

**Table 7. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 13](#).



For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

### 10.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

### 10.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

### 10.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note AN10365 "Surface mount reflow soldering description".

### 10.3.4 Cleaning

Cleaning can be done after reflow soldering.

## 11. Abbreviations

**Table 8. Abbreviations**

Acronym	Description
DUT	Device Under Test
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
NWA	NetWork Analyzer
PCB	Printed-Circuit Board
PCS	Personal Communication System
RFI	Radio Frequency Interference
RoHS	Restriction of Hazardous Substances
SD	Secure Digital

## 12. Revision history

**Table 9. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4350CX24_1	20100205	Product data sheet	-	-

## 13. Legal information

### 13.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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## 15. Contents

<b>1</b>	<b>Product profile</b> . . . . .	<b>1</b>
1.1	General description . . . . .	1
1.2	Features . . . . .	1
1.3	Applications . . . . .	1
<b>2</b>	<b>Pinning information</b> . . . . .	<b>2</b>
2.1	Pinning . . . . .	2
2.2	Pin description . . . . .	2
<b>3</b>	<b>Ordering information</b> . . . . .	<b>3</b>
<b>4</b>	<b>Functional diagram</b> . . . . .	<b>3</b>
<b>5</b>	<b>Limiting values</b> . . . . .	<b>4</b>
<b>6</b>	<b>Characteristics</b> . . . . .	<b>4</b>
<b>7</b>	<b>Frequency response</b> . . . . .	<b>5</b>
<b>8</b>	<b>Application information</b> . . . . .	<b>5</b>
8.1	Insertion loss . . . . .	5
8.2	Crosstalk . . . . .	7
<b>9</b>	<b>Package outline</b> . . . . .	<b>10</b>
<b>10</b>	<b>Soldering of WLCSP packages</b> . . . . .	<b>11</b>
10.1	Introduction to soldering WLCSP packages . . . . .	11
10.2	Board mounting . . . . .	11
10.3	Reflow soldering . . . . .	11
10.3.1	Stand off . . . . .	12
10.3.2	Quality of solder joint . . . . .	12
10.3.3	Rework . . . . .	12
10.3.4	Cleaning . . . . .	13
<b>11</b>	<b>Abbreviations</b> . . . . .	<b>13</b>
<b>12</b>	<b>Revision history</b> . . . . .	<b>13</b>
<b>13</b>	<b>Legal information</b> . . . . .	<b>14</b>
13.1	Data sheet status . . . . .	14
13.2	Definitions . . . . .	14
13.3	Disclaimers . . . . .	14
13.4	Trademarks . . . . .	15
<b>14</b>	<b>Contact information</b> . . . . .	<b>15</b>
<b>15</b>	<b>Contents</b> . . . . .	<b>16</b>

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