



**THE DATASHEET OF
IDT71016S12YGI**





CMOS Static RAM 1 Meg (64K x 16-Bit)

IDT71016S/NS

Features

- ◆ 64K x 16 advanced high-speed CMOS Static RAM
- ◆ Equal access and cycle times
 - Commercial and Industrial: 12/15/20ns
- ◆ One Chip Select plus one Output Enable pin
- ◆ Bidirectional data inputs and outputs directly TTL-compatible
- ◆ Low power consumption via chip deselect
- ◆ Upper and Lower Byte Enable Pins
- ◆ Commercial and industrial product available in 44-pin Plastic SOJ package and 44-pin TSOP package

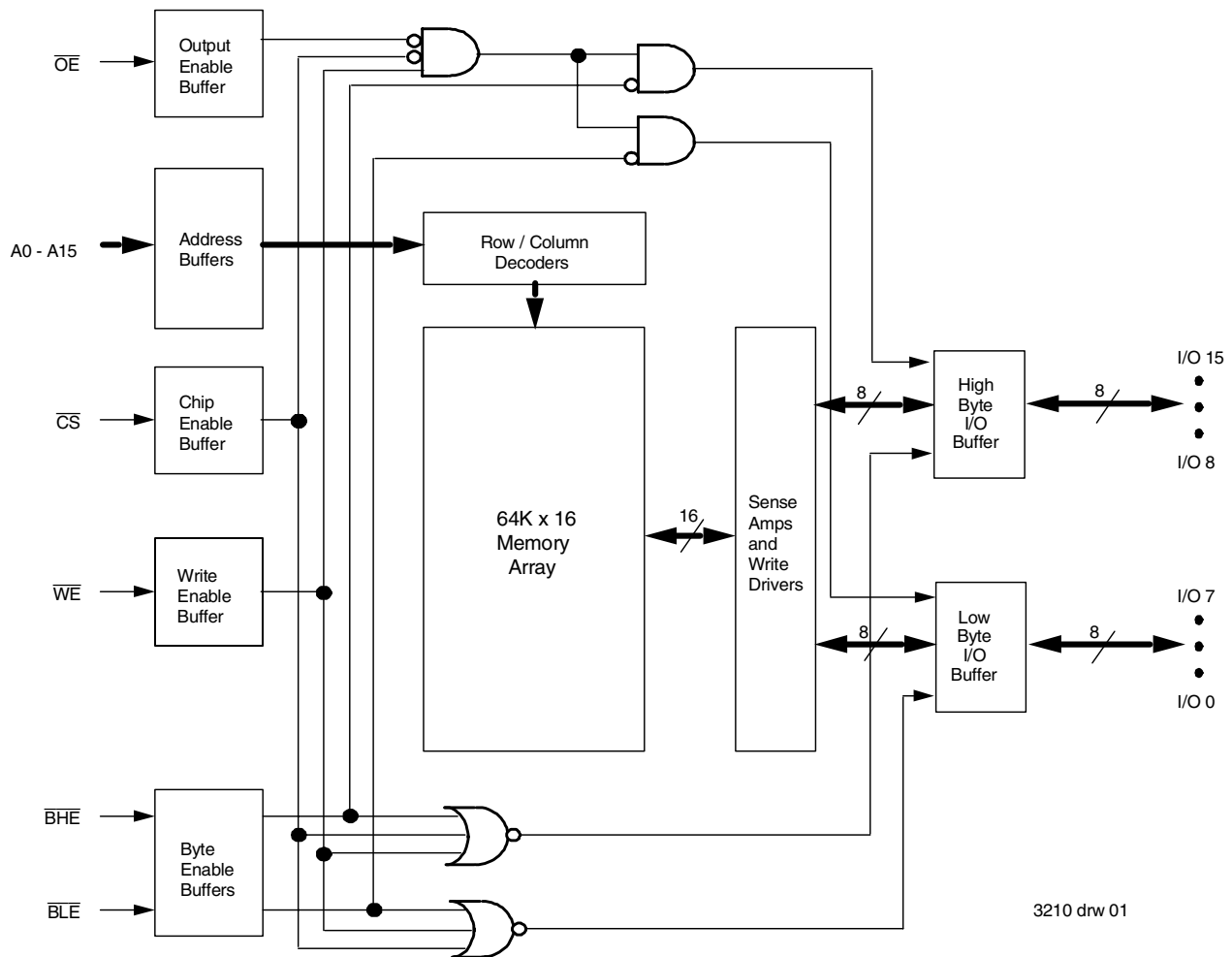
Description

The IDT71016 is a 1,048,576-bit high-speed Static RAM organized as 64K x 16. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71016 has an output enable pin which operates as fast as 7ns, with address access times as fast as 12ns. All bidirectional inputs and outputs of the IDT71016 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

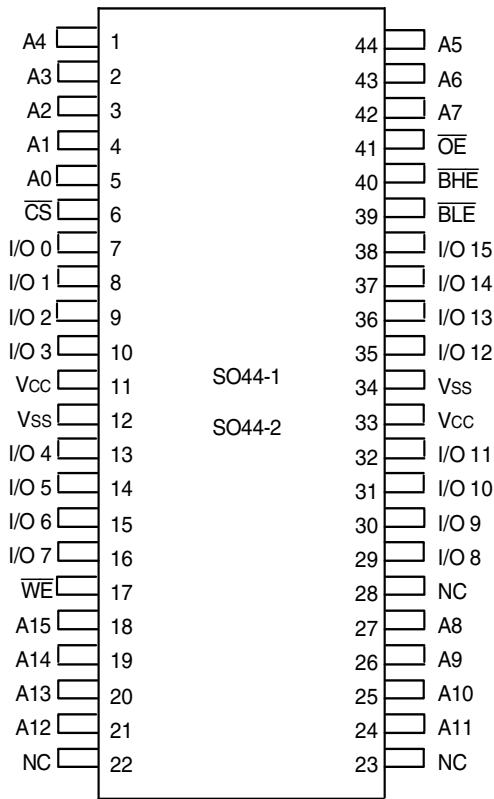
The IDT71016 is packaged in a JEDEC standard 44-pin Plastic SOJ and 44-pin TSOP Type II.

Functional Block Diagram



OCTOBER 2008

Pin Configurations



SOJ/TSOP
Top View

3210 drw 02

Pin Descriptions

| A0 - A15 | Address Inputs | Input |
|--------------------------------------|-------------------|-------|
| \overline{CS} | Chip Select | Input |
| \overline{WE} | Write Enable | Input |
| \overline{OE} | Output Enable | Input |
| \overline{BHE} | High Byte Enable | Input |
| \overline{BLE} | Low Byte Enable | Input |
| I/O ₀ - I/O ₁₅ | Data Input/Output | I/O |
| Vcc | 5.0V Power | Pwr |
| Vss | Ground | Gnd |

3210 tbl 01

Truth Table ⁽¹⁾

| \overline{CS} | \overline{OE} | \overline{WE} | \overline{BLE} | \overline{BHE} | I/O ₀ - I/O ₇ | I/O ₈ - I/O ₁₅ | Function |
|-----------------|-----------------|-----------------|------------------|------------------|-------------------------------------|--------------------------------------|----------------------|
| H | X | X | X | X | High-Z | High-Z | Deselected - Standby |
| L | L | H | L | H | DATAOUT | High-Z | Low Byte Read |
| L | L | H | H | L | High-Z | DATAOUT | High Byte Read |
| L | L | H | L | L | DATAOUT | DATAOUT | Word Read |
| L | X | L | L | L | DATAIN | DATAIN | Word Write |
| L | X | L | L | H | DATAIN | High-Z | Low Byte Write |
| L | X | L | H | L | High-Z | DATAIN | High Byte Write |
| L | H | H | X | X | High-Z | High-Z | Outputs Disabled |
| L | X | X | H | H | High-Z | High-Z | Outputs Disabled |

NOTE:

1. H = V_H, L = V_L, X = Don't care.

3210 tbl 02

Absolute Maximum Ratings⁽¹⁾

| Symbol | Rating | Value | Unit |
|----------------------------------|--------------------------------------|--------------|------|
| V _{TERM} ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +7.0 | V |
| T _A | Operating Temperature | 0 to +70 | °C |
| T _{BIAS} | Temperature Under Bias | -55 to +125 | °C |
| T _{STG} | Storage Temperature | -55 to +125 | °C |
| P _T | Power Dissipation | 1.25 | W |
| I _{OUT} | DC Output Current | 50 | mA |

3210 tbl 03

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed V_{CC} + 0.5V.

Recommended Operating Temperature and Supply Voltage

| Grade | Temperature | GND | V _{CC} |
|------------|----------------|-----|-----------------|
| Commercial | 0°C to +70°C | 0V | 5.0V ± 10% |
| Industrial | -40°C to +85°C | 0V | 5.0V ± 10% |

3210 tbl 04

Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------------|--------------------|---------------------|------|-----------------------|------|
| V _{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Ground | 0 | 0 | 0 | V |
| V _{IH} | Input High Voltage | 2.2 | — | V _{DD} + 0.5 | V |
| V _{IL} | Input Low Voltage | -0.5 ⁽¹⁾ | — | 0.8 | V |

NOTE:

- V_{IL} (min.) = -1.5V for pulse width less than t_{RC}/2, once per cycle.

3210 tbl 05

Capacitance

(T_A = +25°C, f = 1.0MHz, SOJ/TSOP Package)

| Symbol | Parameter ⁽¹⁾ | Conditions | Max. | Unit |
|------------------|--------------------------|------------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 3dV | 6 | pF |
| C _{I/O} | I/O Capacitance | V _{OUT} = 3dV | 7 | pF |

NOTE:

- This parameter is guaranteed by device characterization, but not production tested.

3210 tbl 06

DC Electrical Characteristics

(V_{CC} = 5.0V ± 10%, Commercial and Industrial Temperature Range)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|-----------------|------------------------|---|------|------|------|
| I _L | Input Leakage Current | V _{CC} = Max., V _{IN} = GND to V _{CC} | — | 5 | μA |
| I _{LO} | Output Leakage Current | V _{CC} = Max., \overline{CS} = V _{IH} , V _{OUT} = GND to V _{CC} | — | 5 | μA |
| V _{OL} | Output Low Voltage | I _{OL} = 8mA, V _{CC} = Min. | — | 0.4 | V |
| V _{OH} | Output High Voltage | I _{OH} = -4mA, V _{CC} = Min. | 2.4 | — | V |

3210 tbl 07

DC Electrical Characteristics⁽¹⁾

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

| Symbol | Parameter | 71016S12 | | 71016S15 | | 71016S20 | | Unit |
|------------------|---|----------|------|----------|------|----------|------|------|
| | | Com'l. | Ind. | Com'l. | Ind. | Com'l. | Ind. | |
| I _{CC} | Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, V _{CC} = Max., f = f _{MAX} ⁽²⁾ | 210 | 210 | 180 | 180 | 170 | 170 | mA |
| I _{SB} | Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open, V _{CC} = Max., f = f _{MAX} ⁽²⁾ | 60 | 60 | 50 | 50 | 45 | 45 | mA |
| I _{SB1} | Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, Outputs Open, V _{CC} = Max., f = 0 ⁽²⁾ V _{IN} ≤ V _{LC} or V _{IN} ≥ V _{HC} | 10 | 10 | 10 | 10 | 10 | 10 | mA |

NOTES:

- All values are maximum guaranteed values.
- f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

3210 tbl 08

AC Test Conditions

| | |
|-------------------------------|-----------------------|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 1.5ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| AC Test Load | See Figure 1, 2 and 3 |

3210 tbl 09

AC Test Loads

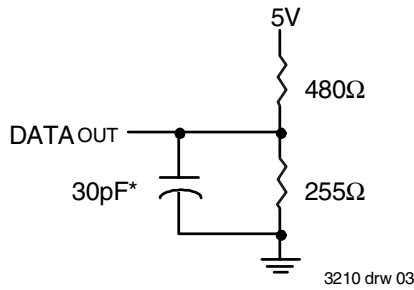


Figure 1. AC Test Load

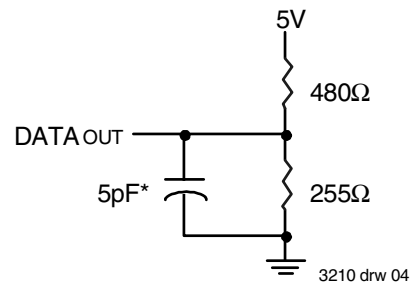


Figure 2. AC Test Load
(for t_{CLZ} , t_{OLZ} , t_{CHZ} , t_{OHZ} , t_{OW} , and t_{WHZ})

*Including jig and scope capacitance.

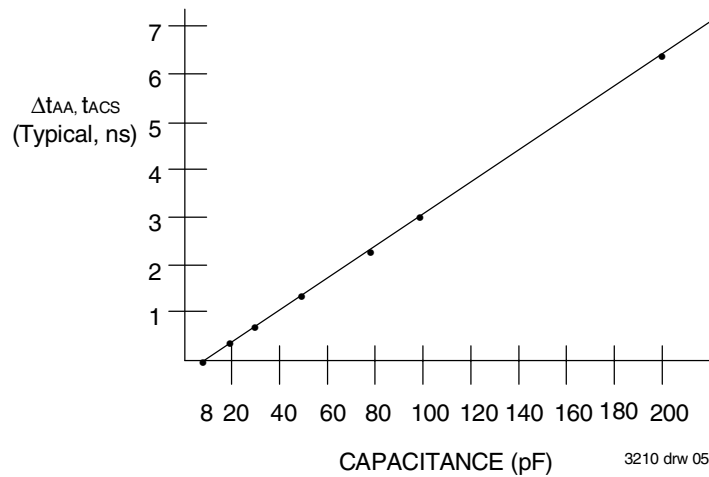


Figure 3. Output Capacitive Derating

AC Electrical Characteristics (VCC = 5.0V ± 10%, Commercial and Industrial Range)

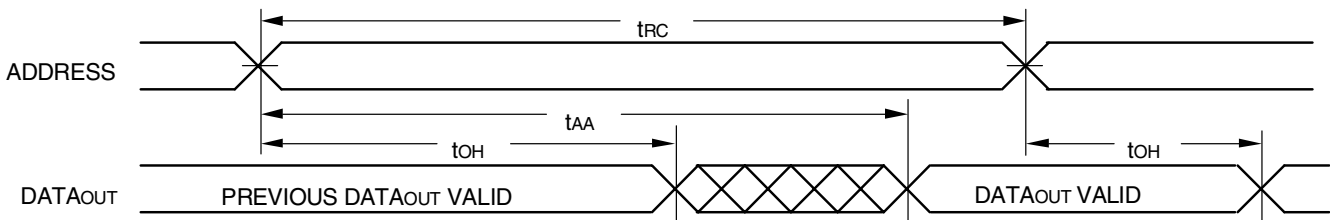
| Symbol | Parameter | 71016S12 | | 71016S15 | | 71016S20 | | Unit |
|---------------------------------|--|----------|------|----------|------|----------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | |
| t _{RC} | Read Cycle Time | 12 | — | 15 | — | 20 | — | ns |
| t _{AA} | Address Access Time | — | 12 | — | 15 | — | 20 | ns |
| t _{ACS} | Chip Select Access Time | — | 12 | — | 15 | — | 20 | ns |
| t _{CLZ} ⁽¹⁾ | Chip Select Low to Output in Low-Z | 4 | — | 5 | — | 5 | — | ns |
| t _{CHZ} ⁽¹⁾ | Chip Select High to Output in High-Z | — | 6 | — | 6 | — | 8 | ns |
| t _{OE} | Output Enable Low to Output Valid | — | 7 | — | 8 | — | 10 | ns |
| t _{OLZ} ⁽¹⁾ | Output Enable Low to Output in Low-Z | 0 | — | 0 | — | 0 | — | ns |
| t _{OHZ} ⁽¹⁾ | Output Enable High to Output in High-Z | — | 6 | — | 6 | — | 8 | ns |
| t _{OH} | Output Hold from Address Change | 4 | — | 4 | — | 5 | — | ns |
| t _{BE} | Byte Enable Low to Output Valid | — | 7 | — | 8 | — | 10 | ns |
| t _{BLZ} ⁽¹⁾ | Byte Enable Low to Output in Low-Z | 0 | — | 0 | — | 0 | — | ns |
| t _{BHZ} ⁽¹⁾ | Byte Enable High to Output in High-Z | — | 6 | — | 6 | — | 8 | ns |
| WRITE CYCLE | | | | | | | | |
| t _{WC} | Write Cycle Time | 12 | — | 15 | — | 20 | — | ns |
| t _{AW} | Address Valid to End of Write | 9 | — | 10 | — | 12 | — | ns |
| t _{CW} | Chip Select Low to End of Write | 9 | — | 10 | — | 12 | — | ns |
| t _{BW} | Byte Enable Low to End of Write | 9 | — | 10 | — | 12 | — | ns |
| t _{AS} | Address Set-up Time | 0 | — | 0 | — | 0 | — | ns |
| t _{WR} | Address Hold from End of Write | 0 | — | 0 | — | 0 | — | ns |
| t _{WP} | Write Pulse Width | 9 | — | 10 | — | 12 | — | ns |
| t _{DW} | Data Valid to End of Write | 7 | — | 8 | — | 10 | — | ns |
| t _{DH} | Data Hold Time | 0 | — | 0 | — | 0 | — | ns |
| t _{OW} ⁽¹⁾ | Write Enable High to Output in Low-Z | 1 | — | 1 | — | 1 | — | ns |
| t _{WHZ} ⁽¹⁾ | Write Enable Low to Output in High-Z | — | 6 | — | 6 | — | 8 | ns |

3210 tbl 10

NOTE:

1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

Timing Waveform of Read Cycle No. 1^(1,2,3)

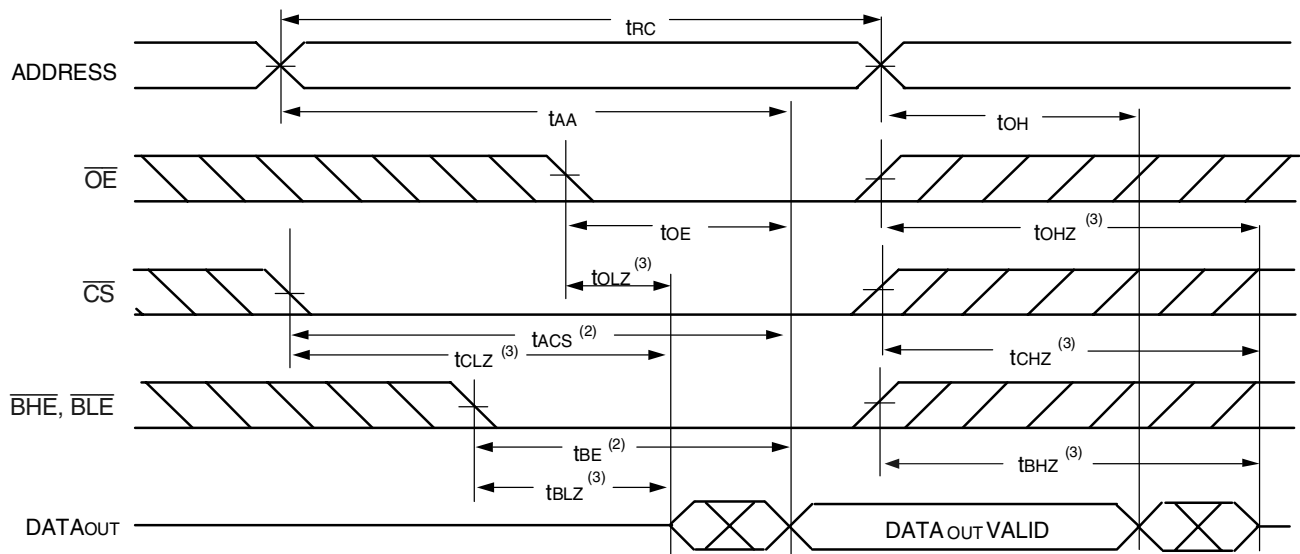


3210 drw 06

NOTES:

1. \overline{WE} is HIGH for Read Cycle.
2. Device is continuously selected, \overline{CS} is LOW.
3. \overline{OE} , \overline{BHE} , and \overline{BLE} are LOW.

Timing Waveform of Read Cycle No. 2⁽¹⁾

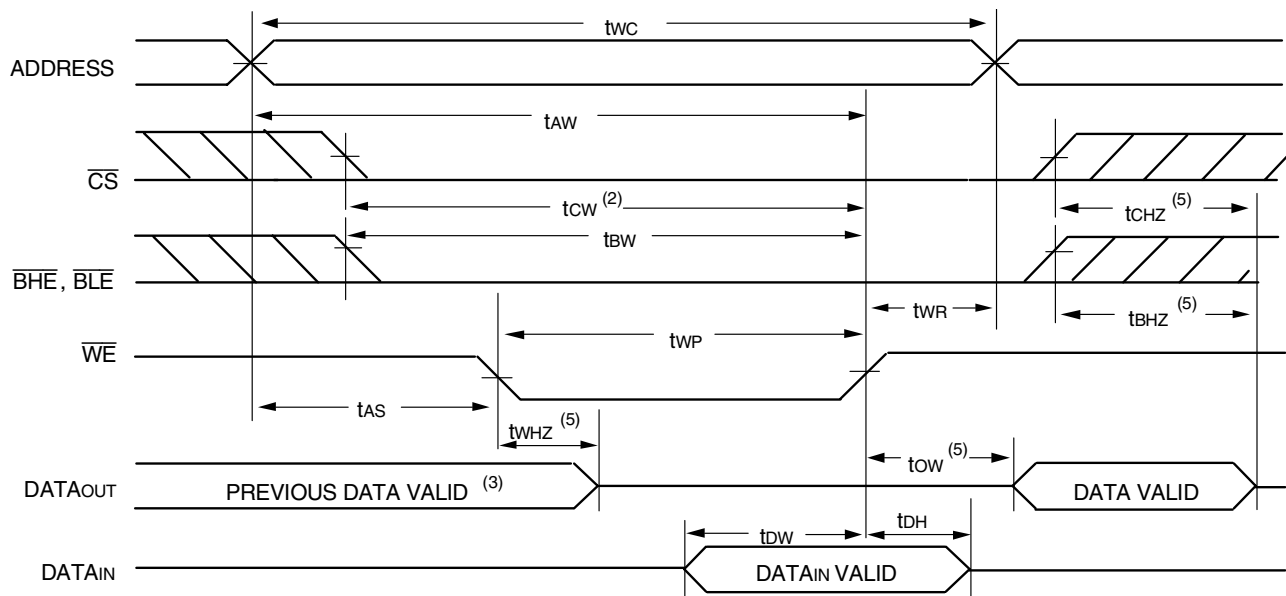


3210 drw 07

NOTES:

1. \overline{WE} is HIGH for Read Cycle.
2. Address must be valid prior to or coincident with the later of \overline{CS} , \overline{BHE} , or \overline{BLE} transition LOW; otherwise t_{AA} is the limiting parameter.
3. Transition is measured $\pm 200\text{mV}$ from steady state.

Timing Waveform of Write Cycle No. 1 (\overline{WE} Controlled Timing)^(1,2,4)

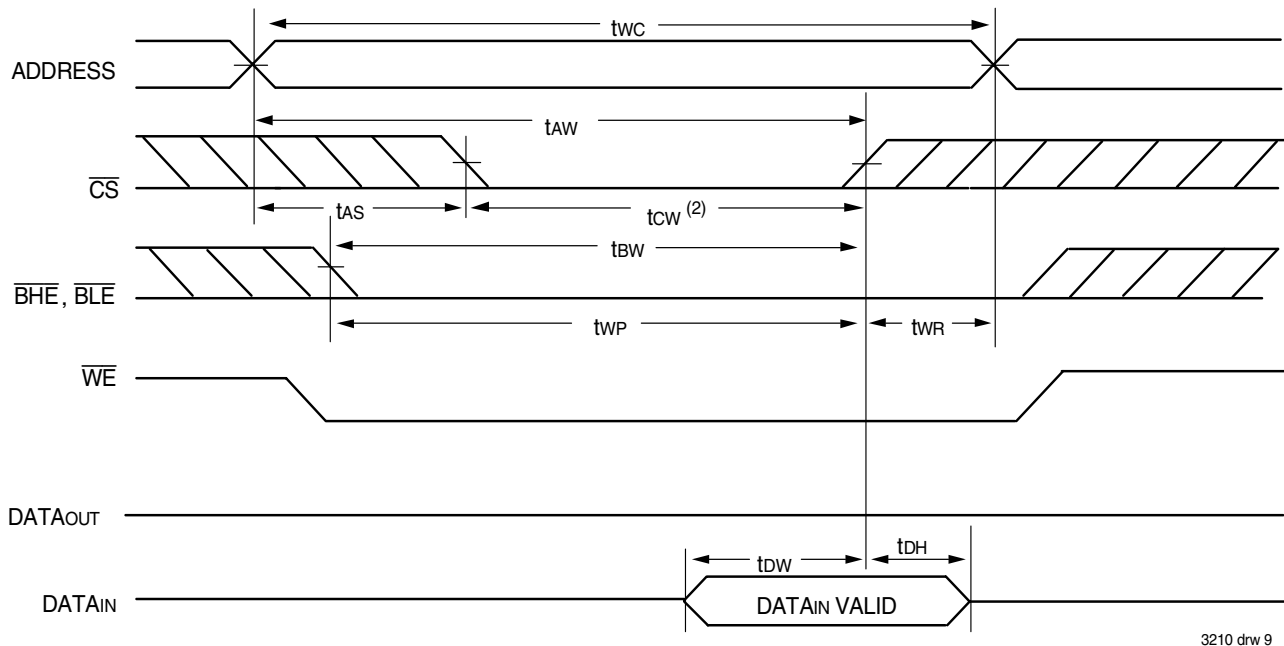


3210 drw 08

NOTES:

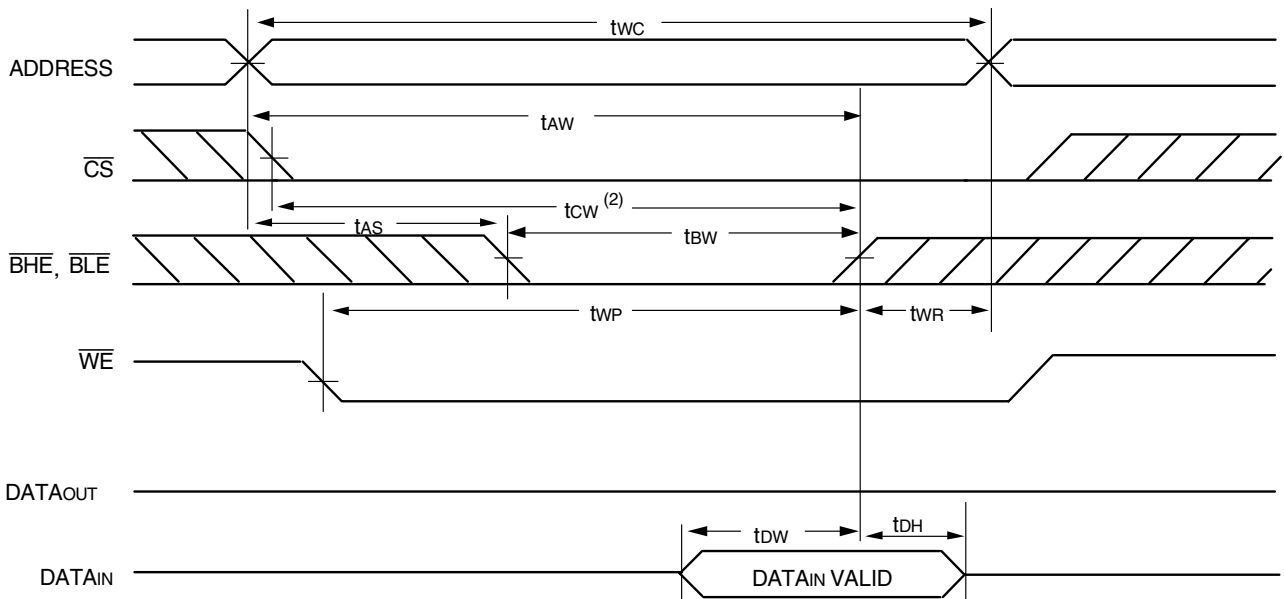
1. A write occurs during the overlap of a LOW \overline{CS} , LOW \overline{BHE} or \overline{BLE} , and a LOW \overline{WE} .
2. \overline{OE} is continuously HIGH. If during a \overline{WE} controlled write cycle \overline{OE} is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{BW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{OW} . If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP} .
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the \overline{CS} LOW or \overline{BHE} and \overline{BLE} LOW transition occurs simultaneously with or after the \overline{WE} LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

Timing Waveform of Write Cycle No. 2 ($\overline{\text{CS}}$ Controlled Timing)^(1,4)



3210 drw 9

Timing Waveform of Write Cycle No. 3 ($\overline{\text{BHE}}$, $\overline{\text{BLE}}$ Controlled Timing)^(1,4)

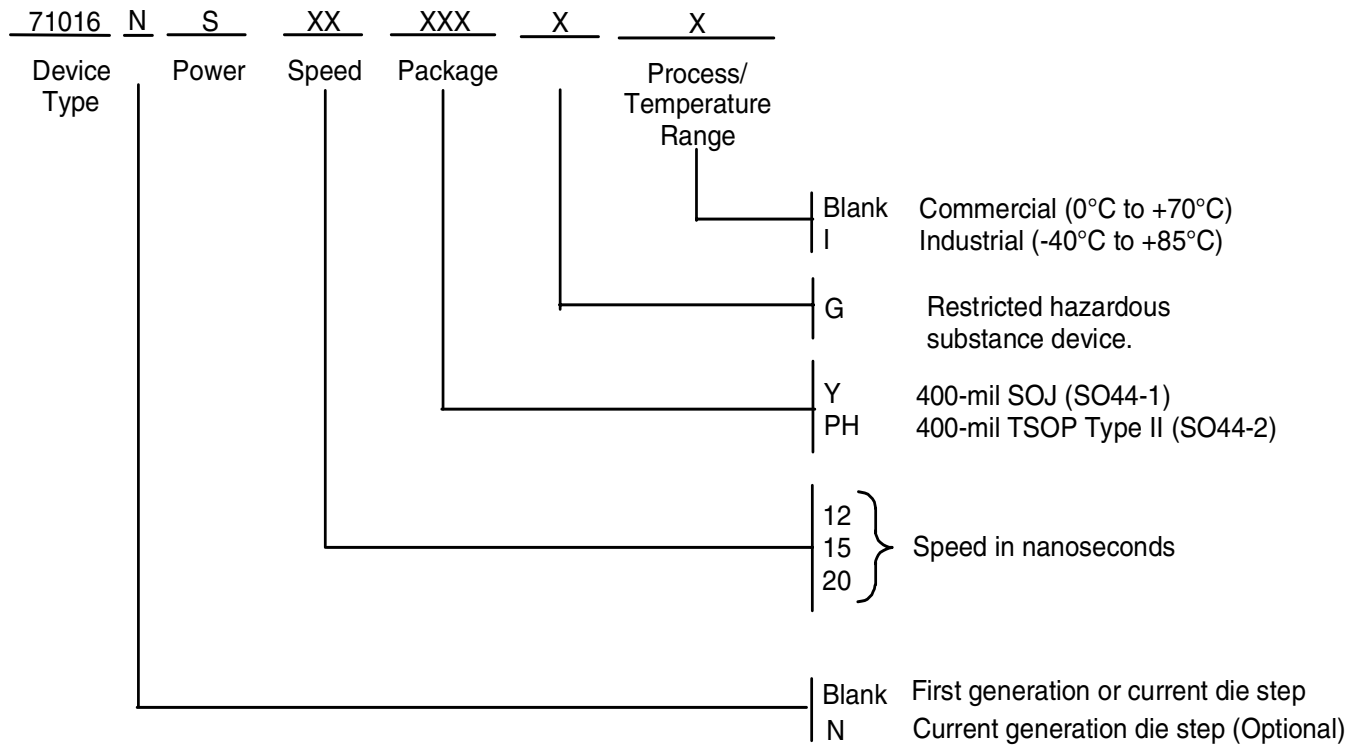


3210 drw 10

NOTES:

1. A write occurs during the overlap of a LOW $\overline{\text{CS}}$, LOW $\overline{\text{BHE}}$ or $\overline{\text{BLE}}$, and a LOW $\overline{\text{WE}}$.
2. $\overline{\text{OE}}$ is continuously HIGH. If during a $\overline{\text{WE}}$ controlled write cycle $\overline{\text{OE}}$ is LOW, tWP must be greater than or equal to tWHZ + tOW to allow the I/O drivers to turn off and data to be placed on the bus for the required tOW. If $\overline{\text{OE}}$ is HIGH during a $\overline{\text{WE}}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified tWP.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{\text{CS}}$ LOW or $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ LOW transition occurs simultaneously with or after the $\overline{\text{WE}}$ LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

Ordering Information



3210 drw 11

Datasheet Document History

| | | |
|----------|-------------|---|
| 7/30/99 | | Updated to new format |
| 8/5/99 | Pg. 3 | Expressed commercial and industrial ranges on DC Electrical table |
| | Pg. 5 | Removed Icc, ISB, and ISB1 values for S12 industrial speed |
| | Pg. 6 | Expressed commercial and industrial ranges on AC Electrical table |
| | Pg. 7 | Changed footnote #2 to commercial temperature only |
| | Pg. 8 | Revised footnotes on Write Cycle No. 1 diagram |
| | Pg. 8 | Revised footnotes on Write Cycle No. 2 and No. 3 diagrams |
| | Pg. 8 | Removed SCD 2752 footnote |
| | | Added commercial only for 12ns speed |
| 8/13/99 | Pg. 9 | Added Datasheet Document History |
| 9/30/99 | Pg. 3, 5, 8 | Added 12ns industrial temperature speed grade offering |
| 08/09/00 | | Not recommended for new designs |
| 02/01/01 | | Removed "Not recommended for new designs" |
| 01/30/04 | Pg. 8 | Added "Restricted hazardous substance device" to order information. |
| 01/30/06 | Pg. 3 | Updated Capacitance table to include TSOP. |
| 02/13/07 | Pg. 8 | Added N generation die step to data sheet ordering information. |
| 10/13/08 | Pg. 8 | Removed "IDT" from orderable part number. |



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