



**THE DATASHEET OF
IDT5V5218PGGI8**





Dual Channel Type-1/Type-2 M-LVDS to LVTTL/LVPECL/LVDS Transceiver IDT5V5218

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FEATURES

◆ Main Features

- Two independent channels
- Type-2 M-LVDS receiver supports 100 mV offset threshold
- Up to 166 MHz selectable input/output signals: LVTTTL/LVPECL/LVDS
- M-LVDS interface allows common-mode voltage: -1 V to 3.4 V
- Power up and power down glitch free
- M-LVDS interface pins in high impedance state when the device is powered down or $V_{DD} < 1.5$ V
- Capable of driving bus load from 30 Ω to 55 Ω

◆ Other Features

- Low power consumption < 220 mW
- Hot swappable
- 24-pin TSSOP package

APPLICATIONS

- Backplane transmission
- Telecommunication system
- Data communications
- ATCA clock distribution

DESCRIPTION

The IDT5V5218 is a dual-channel transceiver which can interchange data across multipoint data bus structures.

In the device, the two channels operate independently. Each channel has selectable LVTTTL/LVPECL/LVDS drivers and receivers, a selectable Type-1/Type-2 M-LVDS receiver and M-LVDS driver. It translates

between LVTTTL/LVPECL/LVDS signals and M-LVDS signals. The drivers and the receivers can be enabled or disabled by external pins. The M-LVDS driver is capable of driving bus load from 30 Ω to 55 Ω . The M-LVDS interface allows common-mode voltage range of -1 V to 3.4 V.

FUNCTIONAL BLOCK DIAGRAM

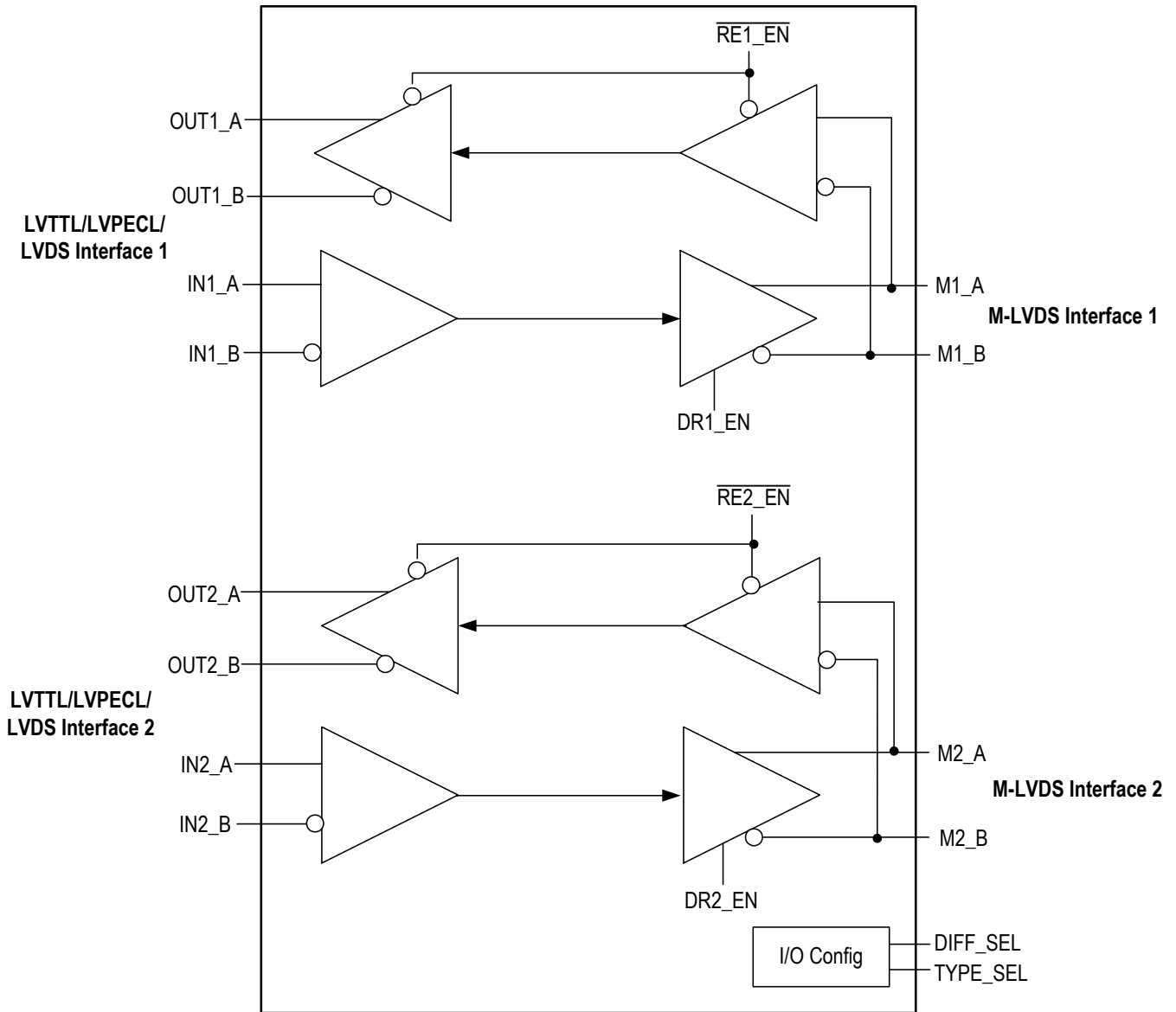


Figure-1 Functional Block Diagram

1 PIN ASSIGNMENT

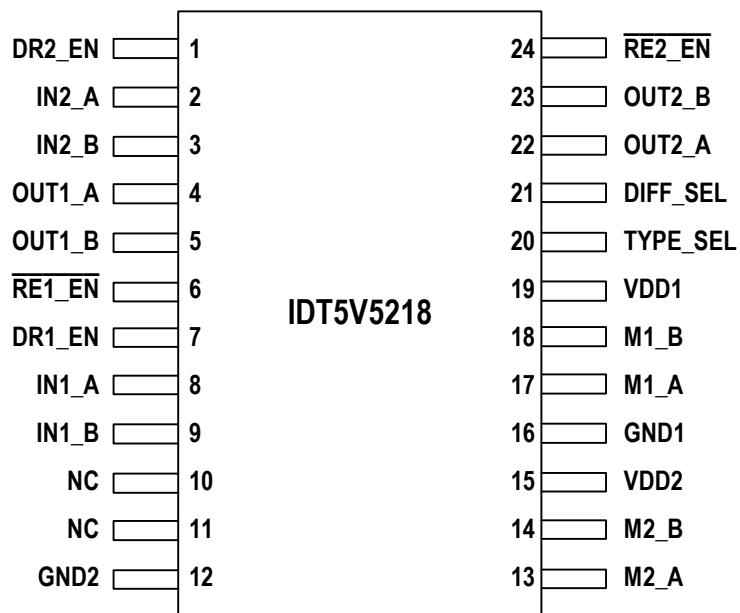


Figure-2 IDT5V5218 TSSOP24 Package Pin Assignment

2 PIN DESCRIPTION

Table-1 Pin Description

Name	Pin No.	I/O	Type	Description
Global Signal				
DR1_EN	7	I Pull-down	LVTTTL	DR1_EN: M-LVDS Driver 1 Enable This pin controls the M-LVDS driver for channel 1: high for enable and low for disable.
$\overline{\text{RE1_EN}}$	6	I Pull-up	LVTTTL	RE1_EN: Type-1/Type-2 M-LVDS Receiver 1 and LVTTTL/LVPECL/LVDS Drivers 1 Enable This pin controls the Type-1/Type-2 M-LVDS receiver and LVTTTL/LVPECL/LVDS drivers for channel 1: high for disable and low for enable. Note that the LVTTTL driver is in high impedance state when disabled.
DR2_EN	1	I Pull-down	LVTTTL	DR2_EN: M-LVDS Driver 2 Enable This pin controls the M-LVDS driver for channel 2: high for enable and low for disable.
$\overline{\text{RE2_EN}}$	24	I Pull-up	LVTTTL	RE2_EN: Type-1/Type-2 M-LVDS Receiver 2 and LVTTTL/LVPECL/LVDS Drivers 2 Enable This pin controls the Type-1/Type-2 M-LVDS receiver and LVTTTL/LVPECL/LVDS drivers for channel 2: high for disable and low for enable. Note that the LVTTTL driver is in high impedance state when disabled.
TYPE_SEL	20	I Pull-down	LVTTTL	TYPE_SEL: Type-1/Type-2 M-LVDS Receiver Selection This pin globally controls the Type-1/Type-2 M-LVDS receiver selection: high for Type-2 and low for Type-1.
DIFF_SEL	21	I Pull to VDD/2	LVTTTL	DIFF_SEL: Type Selection for LVTTTL/LVPECL/LVDS Interface Input/Output 1 and 2 This pin globally determines the type of input/output 1 and 2 of the LVTTTL/LVPECL/LVDS interface: high for LVDS, floating for LVTTTL and low for LVPECL.
LVTTTL/LVPECL/LVDS Interface				
IN1_A IN1_B	8 9	I	LVTTTL/LVPECL/LVDS LVPECL/LVDS	IN1_A/IN1_B: Positive/Negative LVPECL/LVDS Input 1 An up to 166 MHz differential signal is input on this pair of pins. The input signal can be LVPECL or LVDS, as selected by the DIFF_SEL pin. IN1_A: LVTTTL Input 1 An up to 166 MHz LVTTTL signal is input on this pin, as selected by the DIFF_SEL pin. In this case, the IN1_B pin will be in high impedance state.
IN2_A IN2_B	2 3	I	LVTTTL/LVPECL/LVDS LVPECL/LVDS	IN2_A/IN2_B: Positive/Negative LVPECL/LVDS Input 2 An up to 166 MHz differential signal is input on this pair of pins. The input signal can be LVPECL or LVDS, as selected by the DIFF_SEL pin. IN2_A: LVTTTL Input 2 An up to 166 MHz LVTTTL signal is input on this pin, as selected by the DIFF_SEL pin. In this case, the IN2_B pin will be in high impedance state.
OUT1_A OUT1_B	4 5	O	LVTTTL/LVPECL/LVDS LVPECL/LVDS	OUT1_A/OUT1_B: Positive/Negative LVPECL/LVDS Output 1 This pair of pins output an up to 166 MHz differential signal. The output signal can be LVPECL or LVDS, as selected by the DIFF_SEL pin. OUT1_A: LVTTTL Output 1 This pin outputs an up to 166 MHz LVTTTL signal, as selected by the DIFF_SEL pin. In this case, the OUT1_B pin will be in high impedance state.

Table-1 Pin Description (Continued)

Name	Pin No.	I/O	Type	Description
OUT2_A OUT2_B	22 23	O	LVTTTL/LVPECL/LVDS LVPECL/LVDS	<p>OUT2_A/OUT2_B: Positive/Negative LVPECL/LVDS Output 2 This pair of pins output an up to 166 MHz differential signal. The output signal can be LVPECL or LVDS, as selected by the DIFF_SEL pin.</p> <p>OUT2_A: LVTTTL Output 2 This pin outputs an up to 166 MHz LVTTTL signal, as selected by the DIFF_SEL pin. In this case, the OUT2_B pin will be in high impedance state.</p>
M-LVDS Interface				
M1_A M1_B	17 18	I/O	M-LVDS	M1_A/M1_B: Positive/Negative M-LVDS Data Bus Interface 1 This pair of pins are connected to the M-LVDS data bus.
M2_A M2_B	13 14	I/O	M-LVDS	M2_A/M2_B: Positive/Negative M-LVDS Data Bus Interface 2 This pair of pins are connected to the M-LVDS data bus.
Power Supply and Ground				
VDD1	19	Power	-	3.3 V Power Supply for Channel 1
VDD2	15	Power	-	3.3 V Power Supply for Channel 2
GND1	16	Ground	-	Ground for Channel 1
GND2	12	Ground	-	Ground for Channel 2
Others				
NC	10, 11	-	-	NC: No Connection

3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATING AND RECOMMENDED OPERATION CONDITIONS

Table-2 Absolute Maximum Rating

Symbol	Parameter		Range
V_{DD}	Supply Voltage		-0.5 V to 4.1 V
V_{IN}	Input Voltage	$\overline{REN_EN}^{(1)}$, DRn_EN, INn_A, INn_B	-0.5 V to 4.1 V
		Mn_A, Mn_B	-1.8 V to 4 V
V_{OUT}	Output Voltage	OUTn_A, OUTn_B	-0.3 V to 4 V
		Mn_A, Mn_B	-1.8 V to 4 V
	Electrostatic Discharge	Human Body Model Mn_A, Mn_B	± 8 kV
		All pins	± 2 kV
T_J	Junction Temperature	150°C	
T_S	Storage Temperature	-65°C to 165°C	

¹n = 1, 2

Table-3 Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Power Supply	3.0	3.3	3.6	V
V_{IH}	High Level Input Voltage	2		3.0	V
V_{IL}	Low Level Input Voltage	0		0.8	V
	Voltage at any Bus Terminal	-1.4		3.8	V
	Magnitude of Differential Input Voltage	0.05		3.0	V
T_A	Ambient Operating Temperature	-40		85	°C

3.2 LVTTTL/LVDS/LVPECL DRIVER/RECEIVER CHARACTERISTICS

3.2.1 M-LVDS TO LVTTTL

Table-4 LVTTTL DC Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IHL}	Input High Level		2.0		$V_{DD} + 0.3$	V
V_{ILL}	Input Low Level		-0.3		0.8	V
I_{ILL}	Input Leakage Current		-1.0		1.0	μ A
V_{OHL}	Output High Voltage	Output Current = 17 mA, $V_{DD} = 3$ V	2.4			V
V_{OLL}	Output Low Voltage	Output Current = 12 mA, $V_{DD} = 3$ V			0.4	V

Table-5 LVTTTL AC Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_r	Rise Time	$C_{load} = 15$ pF, 10% - 90%			1.2	ns
t_f	Fall Time	$C_{load} = 15$ pF, 10% - 90%			1.2	ns
f_{ML}	Frequency				166	MHz

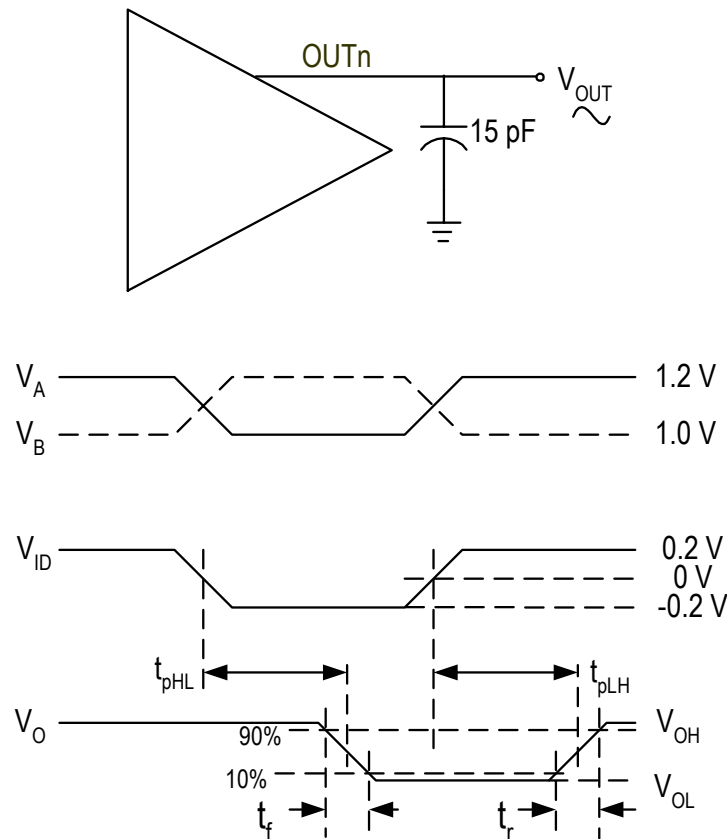


Figure-3 LVTTTL Output Test Circuit and Waveforms

3.2.2 M-LVDS TO LVDS

Table-6 LVDS DC Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CM}	Input Common-mode Voltage Range		0	1200	2400	mV
V_{DIFF}	Input Peak Differential Voltage		100		900	mV
V_{IDTH}	Input Differential Threshold		-100		100	mV
I_{IN}	Input Leakage Current				20	μ A
V_{OH}	Output Voltage High	$R_{load} = 100 \Omega \pm 1\%$	1350		1475	mV
V_{OL}	Output Voltage Low	$R_{load} = 100 \Omega \pm 1\%$	925		1100	mV
V_{OD}	Differential Output Voltage	$R_{load} = 100 \Omega \pm 1\%$	250		450	mV
V_{OS}	Output Offset Voltage	$R_{load} = 100 \Omega \pm 1\%$	1100		1300	mV
R_0	Differential Output Impedance	$V_{CM} = 1.0 \text{ V or } 1.4 \text{ V}$	80	100	120	Ohm
ΔV_{OD}	Change in V_{OD} between Logic 0 and Logic 1	$R_{load} = 100 \Omega \pm 1\%$			25	mV
ΔV_{OS}	Change in V_{OS} between Logic 0 and Logic 1	$R_{load} = 100 \Omega \pm 1\%$			25	mV
$I_{SA}I_{SB}$	Output Current	Driver shorted to GND			24	mA
I_{SAB}	Output Current	Driver shorted together			12	mA

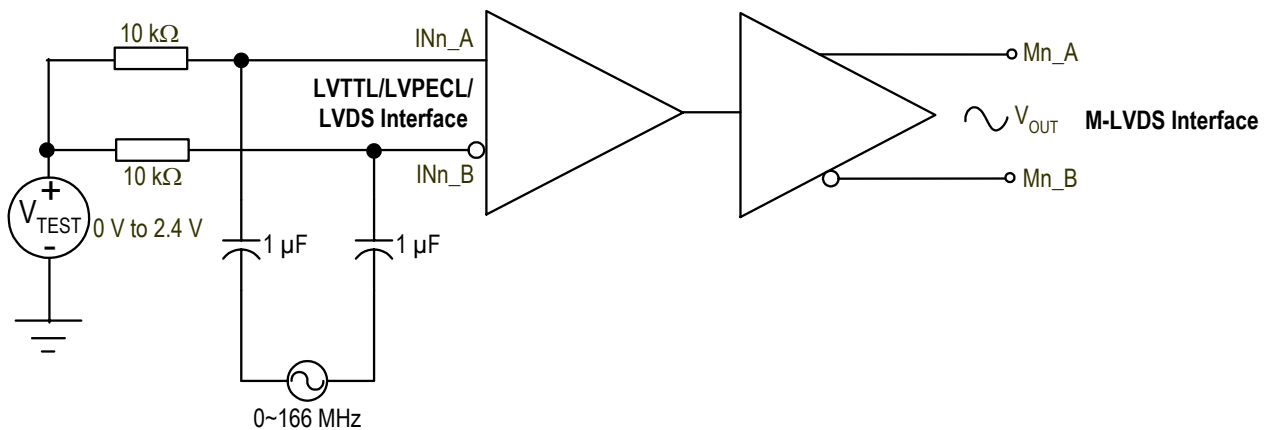


Figure-4 LVDS Receiver Input Common-mode Range Test Circuit

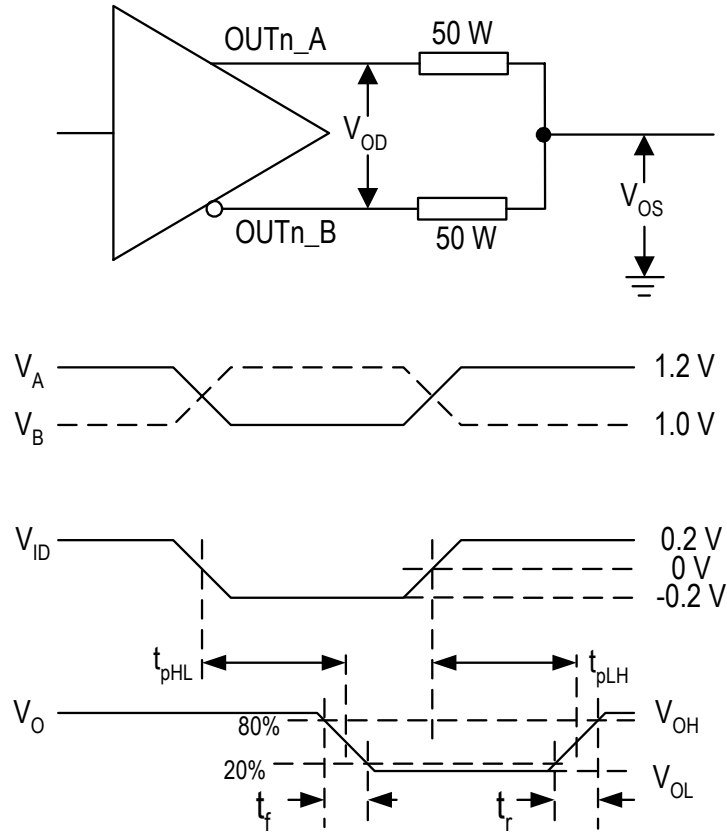


Figure-5 LVDS Driver Output Voltage Test Circuit

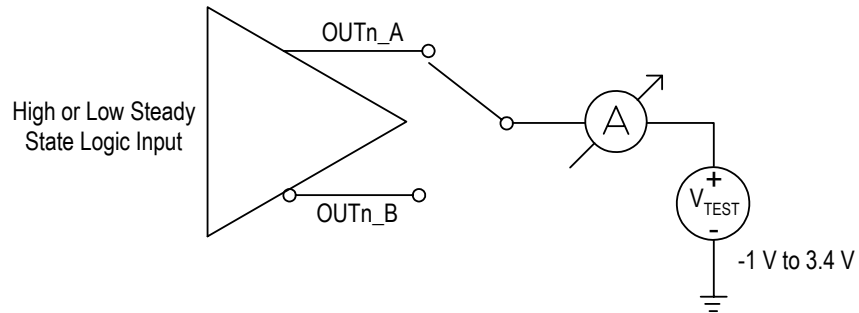


Figure-6 LVDS Driver Shorted to Ground

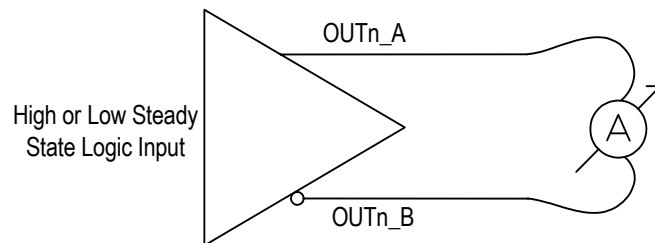


Figure-7 LVDS Driver Shorted Together

Table-7 LVDS AC Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_r	Rise Time	20% - 80%	150		350	ps
t_f	Fall Time	20% - 80%	150		350	ps
t_{TSP}	Differential Skew		-50		50	ps
f_{MM}	Frequency				166	MHz

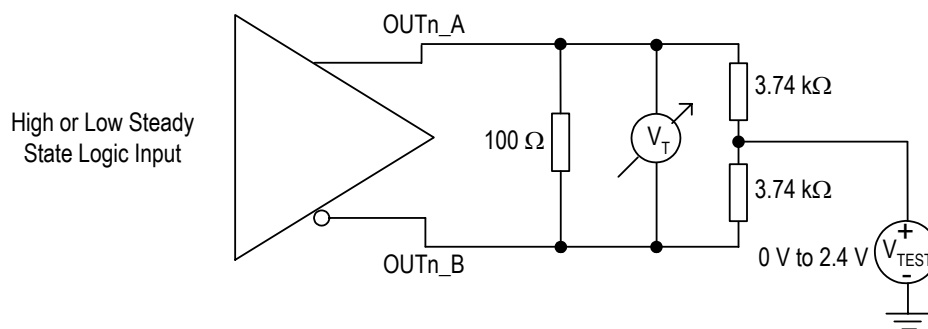


Figure-8 LVDS Output Test Circuit

3.2.3 M-LVDS TO LVPECL

Table-8 Differential LVPECL DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage, Differential Inputs	$V_{DD}-2.5$		$V_{DD}-0.5$	V
V_{IH}	Input High Voltage, Differential Inputs	$V_{DD}-2.4$		$V_{DD}-0.4$	V
V_{ID}	Input Differential Voltage	0.1		1.4	V
I_{IH}	Input High Current, $V_{ID} = 1.4$ V	-10		10	μ A
I_{IL}	Input Low Current, $V_{ID} = 1.4$ V	-10		10	μ A
V_{OL}	Output Voltage Low	$V_{DD}-2.1$		$V_{DD}-1.6$	V
V_{OH}	Output Voltage High	$V_{DD}-1.25$		$V_{DD}-0.88$	V
V_{OS}	Output Differential Voltage	580		950	mV

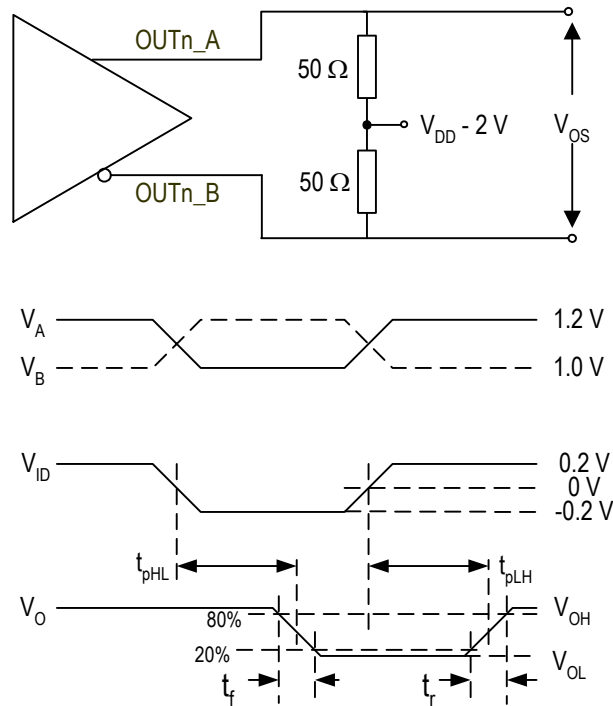


Figure-9 LVPECL Driver Output Test Circuit and Waveforms

Table-9 Differential LVPECL AC Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_r	Rise Time	20% - 80%	150		350	ps
t_f	Fall Time	20% - 80%	150		350	ps
t_{TSP}	Differential Skew		-50		50	ps
f_{MM}	Frequency				166	MHz

3.3 M-LVDS DRIVER TYPE-1/TYPE-2 RECEIVER CHARACTERISTICS

Table-10 M-LVDS Type-1 Receiver Input Threshold Test Voltages

Applied Voltages		Resulting Differential Input Voltage	Resulting Common-mode Input Voltage	Receiver Output ⁽¹⁾
V _A	V _B			
2.400	0.000	2.400	1.200	High
0.000	2.400	-2.400	1.200	Low
3.425	3.375	0.050	3.4	High
3.375	3.425	-0.050	3.4	Low
-0.975	-1.025	0.050	-1	High
-1.025	-0.975	-0.050	-1	Low

¹ The receiver is enabled (The RE1_EN or RE2_EN pin is pulled low).

Table-11 M-LVDS Type-2 Receiver Input Threshold Test Voltages

Applied Voltages		Resulting Differential Input Voltage	Resulting Common-mode Input Voltage	Receiver Output ⁽¹⁾
V _A	V _B			
2.400	0.000	2.400	1.200	High
0.000	2.400	-2.400	1.200	Low
3.475	3.325	0.150	3.4	High
3.425	3.375	0.050	3.4	Low
-0.925	-1.075	0.150	-1	High
-0.975	-1.025	0.050	-1	Low

¹ The receiver is enabled (The RE1_EN or RE2_EN pin is pulled low).

Table-12 M-LVDS DC Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{ODM}	Differential Output Voltage		480		650	mV
ΔV_{ODM}	Change in V_{ODM} for Complimentary Output States, $\Delta V_{ODM} = V_{ODM1} - V_{ODM0} $		-50		50	mV
V_{OSM}	Offset Voltage		0.8		1.2	V
ΔV_{OSM}	Change in V_{OSM} for Complimentary Output States		-50		50	mV
$V_{OSM(p-p)}$	Peak-to-peak Common-mode Output Voltage				150	mV
I_{OM}	Output Short Circuit Current				20	mA
I_{IZM}	High Impedance Input Current		-10		10	μ A
V_{THM}	Differential Input High Threshold	Type-1 Type-2	50 150			mV
V_{TLM}	Differential Input Low Threshold	Type-1 Type-2			-50 +50	mV
V_{CMM}	Input Common-mode Range	$V_{INA} - V_{INB} = 200$ mV	-1		3.4	V
I_{INM}	Input Current	Input Voltage = 0 V to 2.4 V	-20		20	μ A

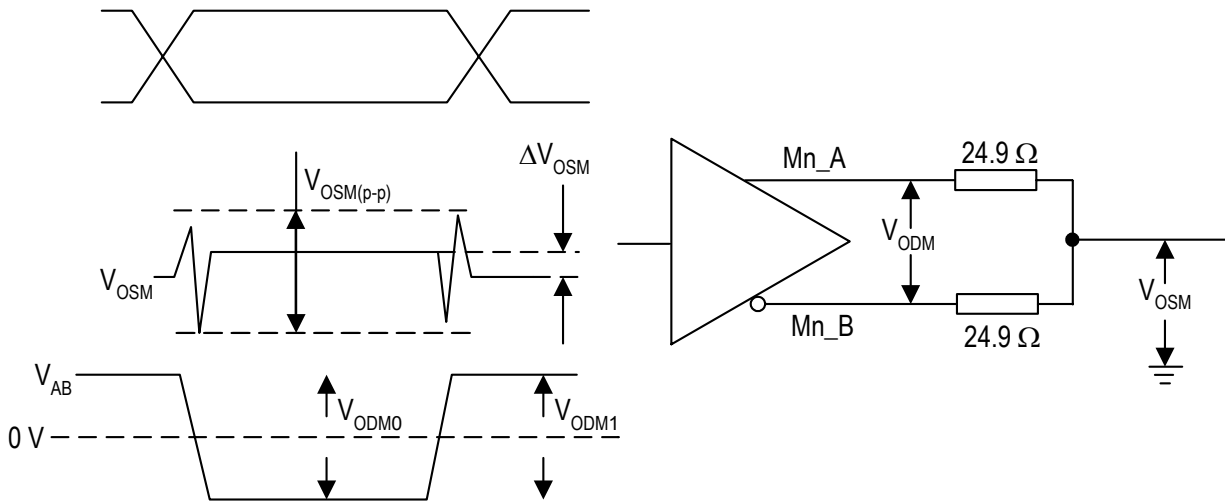


Figure-10 M-LVDS Driver Output Voltage Test Circuit

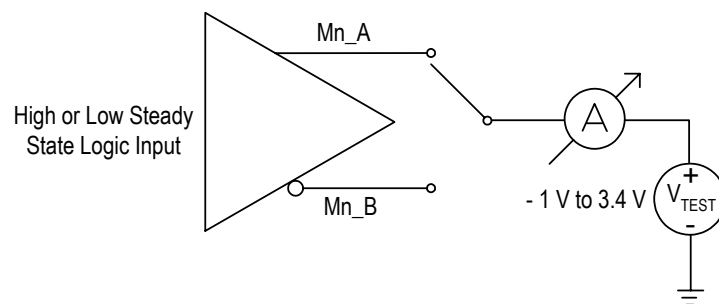


Figure-11 M-LVDS Driver Short-Circuit Test Circuit

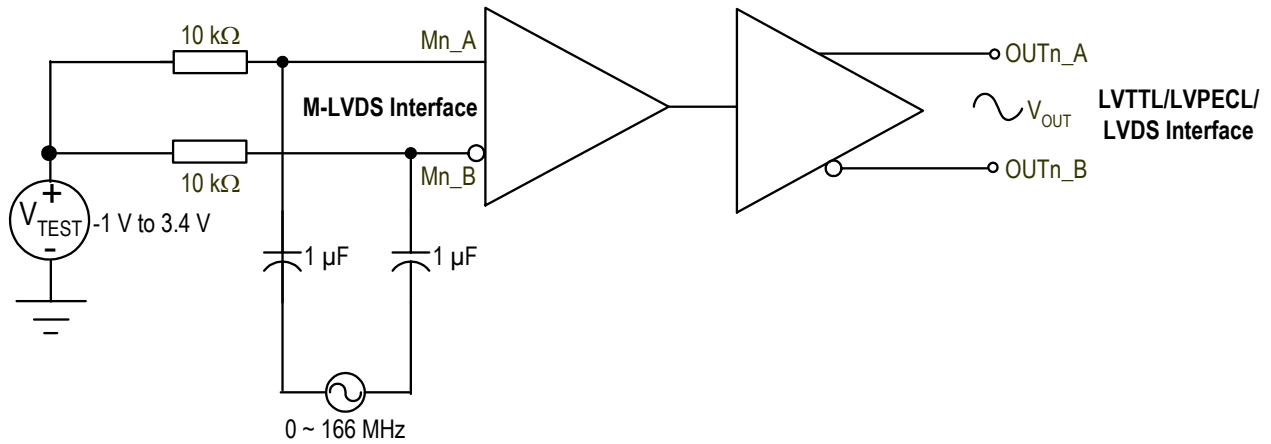


Figure-12 M-LVDS Type-1/Type-2 Receiver Input Common-mode Range Test Circuit

Table-13 M-LVDS Input Current Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_A	Receiver or Transceiver with Driver Disabled Input Current	$V_A = 3.8 \text{ V}, V_B = 1.2 \text{ V}$	0		32	μA
		$V_A = 0 \text{ V or } 2.4 \text{ V}, V_B = 1.2 \text{ V}$	-20		20	
		$V_A = -1.4 \text{ V}, V_B = 1.2 \text{ V}$	-32		0	
I_B	Receiver or Transceiver with Driver Disabled Input Current	$V_B = 3.8 \text{ V}, V_A = 1.2 \text{ V}$	0		32	μA
		$V_B = 0 \text{ V or } 2.4 \text{ V}, V_A = 1.2 \text{ V}$	-20		20	
		$V_B = -1.4 \text{ V}, V_A = 1.2 \text{ V}$	-32		0	
I_{AB}	Receiver or Transceiver with Driver Differential Current ($I_A - I_B$)	$V_A = V_B, -1.4 \text{ V} < V_A < 3.8 \text{ V}$	-4		4	μA
$I_{A(\text{OFF})}$	Receiver or Transceiver Power-off Input Current	$V_A = 3.8 \text{ V}, V_B = 1.2 \text{ V}, 0 \text{ V} < V_{DD} < 1.5 \text{ V}$	0		32	μA
		$V_A = 0 \text{ or } 2.4 \text{ V}, V_B = 1.2 \text{ V}, 0 \text{ V} < V_{DD} < 1.5 \text{ V}$	-20		20	
		$V_A = -1.4 \text{ V}, V_B = 1.2 \text{ V}, 0 \text{ V} < V_{DD} < 1.5 \text{ V}$	-32		0	
$I_{B(\text{OFF})}$	Receiver or Transceiver Power-off Input Current	$V_B = 3.8 \text{ V}, V_A = 1.2 \text{ V}, 0 \text{ V} < V_{DD} < 1.5 \text{ V}$	0		32	μA
		$V_B = 0 \text{ or } 2.4 \text{ V}, V_A = 1.2 \text{ V}, 0 \text{ V} < V_{DD} < 1.5 \text{ V}$	-20		20	
		$V_B = -1.4 \text{ V}, V_A = 1.2 \text{ V}, 0 \text{ V} < V_{DD} < 1.5 \text{ V}$	-32		0	
$I_{AB(\text{OFF})}$	Receiver or Transceiver Power-off Differential Input Current ($I_A - I_B$)	$V_A = V_B, 0 \text{ V} < V_{DD} < 1.5 \text{ V}, -1.4 \text{ V} < V_A < 3.8 \text{ V}$	-4		4	μA
C_{AB}	Transceiver with driver disabled differential input capacitance	$V_{AB} = 0.4 \sin(30E6\pi t) \text{ V}$			4	pF

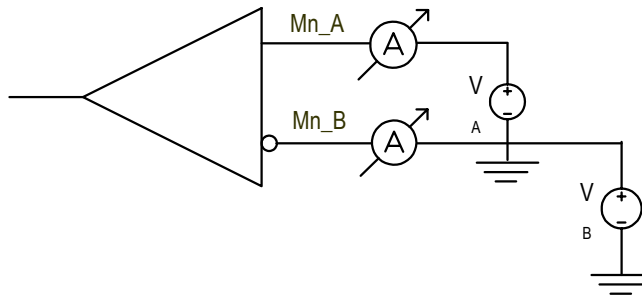


Figure-13 Various Input Currents Test Circuit

Table-14 M-LVDS AC Parameters

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Unit
t_r	Rise Time	10% - 90%	0.8		1.5	ns
t_f	Fall Time	10% - 90%	0.8		1.5	ns
t_{TSL}	Differential Skew, $t_{TSL} = \{t_{TSL1}, t_{TSL2}\}$		-100		100	ps
f_{ML}	Frequency				166	MHz

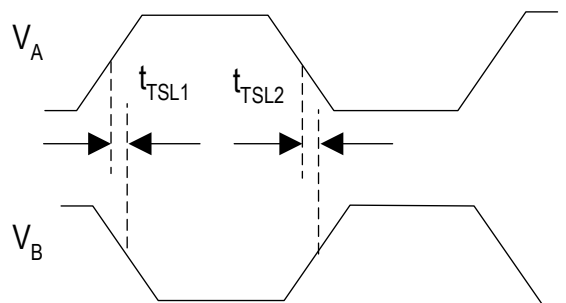


Figure-14 Differential Skew

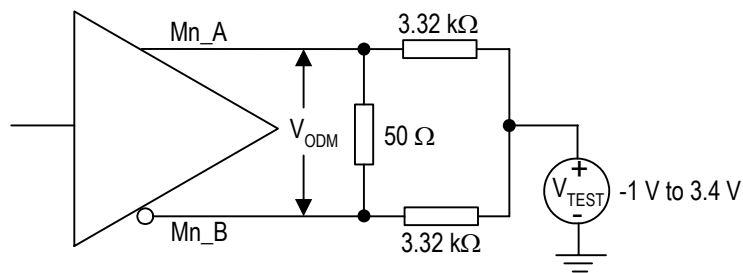


Figure-15 M-LVDS Output Voltage Test Circuit

Table-15 M-LVDS Type-1/Type-2 Receiver AC Parameters

Output mode	Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	
LVTTTL	t_{pLH}	Delay, Low to High Level	Input clock: freq = 50 MHz, Impedance = 150 Ω , Voltage = -200 mV - 200 mV. See Figure-3	2.5	5.5	6.5	ns	
	t_{pHL}	Delay, High to Low Level		2.5	5.5	6.5	ns	
	t_{sk}	Type-1		Pulse Skew, $t_{sk} = t_{pLH} - t_{pHL} $		100	300	ps
		Type-2				300	500	ps
	T_r (10% - 90%)	Rise Time			1		2.4	ns
	T_f (10% - 90%)	Fall Time			1		2.4	ns
	$T_{jit(per)}$	Period jitter, rms(1 standard deviation)				4	7	ps
		Output to Output Skew					200	ps
LVDS	t_{pLH}	Delay, Low to High Level	Input clock: freq = 50 MHz, Impedance = 150 Ω , Voltage = -200 mV - 200 mV. See Figure-5	2.5	4.0	5.5	ns	
	t_{pHL}	Delay, High to Low Level		2.5	4.0	5.5	ns	
	t_{sk}	Type-1		Pulse Skew, $t_{sk} = t_{pLH} - t_{pHL} $		150	300	ps
		Type-2				250	500	ps
	T_r (20% - 80%)	Rise Time			150	200	350	ps
	T_f (20% - 80%)	Fall Time			150	200	350	ps
	$T_{jit(per)}$	Period jitter, rms(1 standard deviation)				4	7	ps
		Output to Output Skew					200	ps
LVPECL	t_{pLH}	Delay, Low to High Level	Input clock: freq = 50 MHz, Impedance = 150 Ω , Voltage = -200 mV - 200 mV. See Figure-9	2.5	4	5.5	ns	
	t_{pHL}	Delay, High to Low Level		2.5	4	5.5	ns	
	t_{sk}	Type-1		Pulse Skew, $t_{sk} = t_{pLH} - t_{pHL} $		150	300	ps
		Type-2				200	500	ps
	T_r (20% - 80%)	Rise Time			150	250	350	ps
	T_f (20% - 80%)	Fall Time			150	250	350	ps
	$T_{jit(per)}$	Period jitter, rms(1 standard deviation)				4	7	ps
		Output to Output Skew					200	ps

Table-16 M-LVDS Receiver output DC Parameters

Output mode	Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
LVPECL	V_{OD}	Differential Output Voltage		580		950	mV
LVDS	V_{OS}	Output Offset Voltage		1100	1200	1300	mV
	V_{OD}	Differential Output Voltage		250	350	450	mV
	I_{SA}, I_{SB}	Output Current				28	mA
	V_{ODM}	Differential Output Voltage		480		650	mV

Table-17 M-LVDS Driver AC Parameter

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	
t_{pLH}	Delay, Low to High Level	Input clock: freq = 15 MHz, $T_r = T_f = 1.2$ ns, Impedance = 300Ω , Voltage = 0 V - 3.3 V. See Figure-10	2.5	3.7	5.5	ns	
t_{pHL}	Delay, High to Low Level		2.5	3.7	5.5	ns	
Tsk	LVTTTL input		Pulse Skew, $t_{sk} = t_{pLH} - t_{pHL} $		40	100	ps
	LVDS/LVPECL input				250	400	ps
T_r (10% - 90%)	Rise Time		0.7	1.1	1.5	ns	
T_f (10% - 90%)	Fall Time		0.7	1.1	1.5	ns	
$T_{jit(per)}$	Period jitter, rms (1 standard deviation)			2	3	ps	
	Output to Output Skew				100	ps	

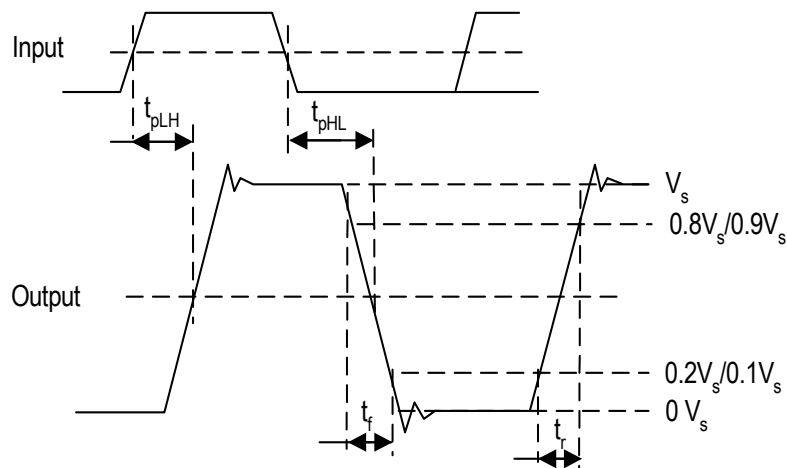
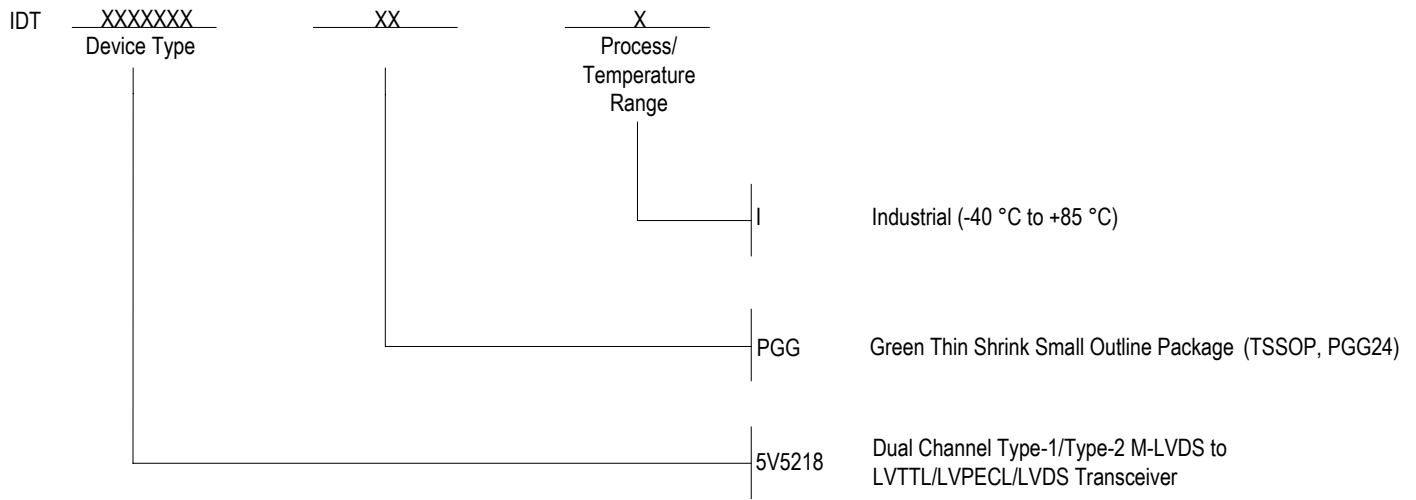


Figure-16 Timing and Voltage Definitions for the Output Signal

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