THE DATASHEET OF

9P936AGLFT

DATASHEET

Low Skew Dual Bank DDR I/II Fan-out Buffer

ICS9P936

Description

Dual DDR I/II fanout buffer for VIA Chipset

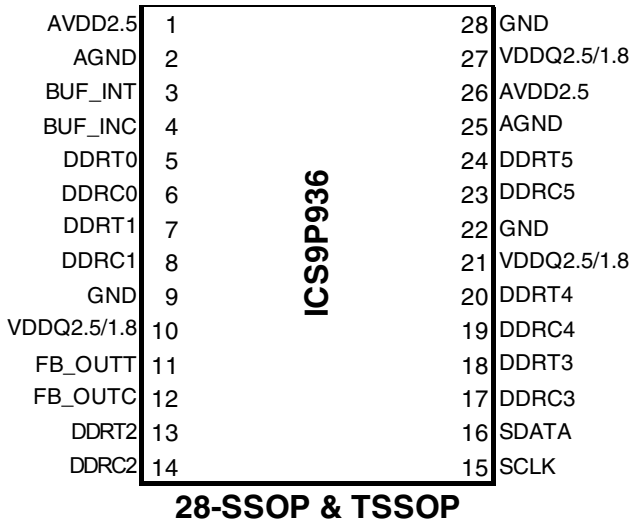
Output Features

- Low skew, fanout buffer
- SMBus for functional and output control
- Single bank 1-6 differential clock distribution
- 1 pair of differential feedback pins for input to output synchronization
- Supports up to 2 DDR DIMMs
- 266MHz (DDRI 533) output frequency support
- 400MHz (DDRII 800) output frequency support
- Programmable skew through SMBus
- Individual output control programmable through SMBus

Key Specifications

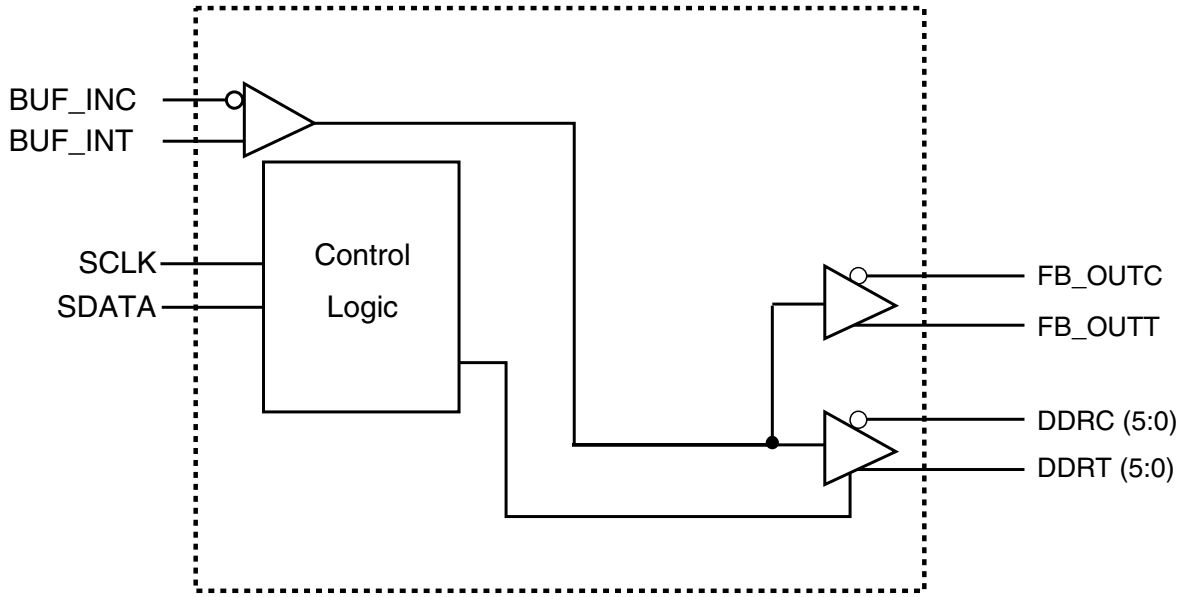
- OUTPUT - OUTPUT skew: <100ps
- Output Rise and Fall Time for DDR outputs: 650ps - 950ps
- DUTY CYCLE: 47% - 53%
- 28-pin SSOP/TSSOP package
- RoHS compliant packaging

Pin Configuration



28-SSOP & TSSOP

Funtional Block Diagram



Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	AVDD2.5	PWR	2.5V Analog Power pin for Core PLL
2	AGND	PWR	Analog Ground pin for Core PLL
3	BUF_INT	IN	True Buffer In signal for memory outputs.
4	BUF_INC	IN	Complementary Buffer In signal for memory outputs.
5	DDRT0	OUT	-40
6	DDRC0	OUT	"Complementary" Clock of differential pair output.
7	DDRT1	OUT	"True" Clock of differential pair output.
8	DDRC1	OUT	"Complementary" Clock of differential pair output.
9	GND	PWR	Ground pin.
10	VDDQ2.5/1.8	PWR	Power supply, nominal 2.5V or 1.8V for DDR or DDR 2 outputs respectively
11	FB_OUTT	OUT	True single-ended feedback output, dedicated external feedback. It switches at the same frequency as other DDR outputs.
12	FB_OUTC	OUT	Complementary single-ended feedback output, dedicated external feedback. It switches at the same frequency as other DDR outputs.
13	DDRT2	OUT	"True" Clock of differential pair output.
14	DDRC2	OUT	"Complementary" Clock of differential pair output.
15	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
16	SDATA	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
17	DDRC3	OUT	"Complementary" Clock of differential pair output.
18	DDRT3	OUT	"True" Clock of differential pair output.
19	DDRC4	OUT	"Complementary" Clock of differential pair output.
20	DDRT4	OUT	"True" Clock of differential pair output.
21	VDDQ2.5/1.8	PWR	Power supply, nominal 2.5V or 1.8V for DDR or DDR 2 outputs respectively
22	GND	PWR	Ground pin.
23	DDRC5	OUT	"Complementary" Clock of differential pair output.
24	DDRT5	OUT	"True" Clock of differential pair output.
25	AGND	PWR	Analog Ground pin for Core PLL
26	AVDD2.5	PWR	2.5V Analog Power pin for Core PLL
27	VDDQ2.5/1.8	PWR	Power supply, nominal 2.5V or 1.8V for DDR or DDR 2 outputs respectively
28	GND	PWR	Ground pin.

Absolute Max

Supply Voltage	-0.5V to 3.6V
Logic Inputs	GND –0.5 V to V_{DD} +0.5 V or 3.6V, whichever is less
Ambient Operating Temperature	0°C to +70°C
Case Temperature	115°C
Storage Temperature	–65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters (VDDQ2.5/1.8 = 1.8V +/- 0.1V)

T_A = 0 - 70°C; Supply Voltage AVDD = 2.5V +/- 0.2V(unless otherwise stated)

			SPEC			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	$V_I = V_{DDQ}$ or GND	-40			µA
Input Low Current	I_{IL}	$V_I = V_{DDQ}$ or GND			10	µA
Operating Supply Current	$I_{DDAVDD2.5}$	R_L = 120Ω, C_L = 12pf @ 266MHz		23	26	mA
	$I_{DDVDDQ2.5/1.8}$	R_L = 120Ω, C_L = 12pf @ 266MHz		164	180	mA
Input Clamp Voltage	V_{IK}	V_{DDQ} = 1.8V Iin = -18mA			-1.2	V
High-level output voltage	V_{OH}	I_{OH} = -9 mA	1.1			V
Low-level output voltage	V_{OL}	I_{OL}=9 mA			0.6	V
Input Capacitance	C_{IN}	V_I = GND or V_{DDQ}	2	3	4	pF
Output Capacitance	C_{OUT}	V_{OUT} = GND or V_{DDQ}	2	3	4	pF
Input clock slew rate	$t_{sI(i)}$	Input clock	1	2.5	4	V/ns

Recommended Operating Condition (VDDQ2.5/1.8 = 1.8V +/- 0.1V) (see note1)

T_A = 0 - 70°C; Supply Voltage AVDD = 2.5V+/-0.2V (unless otherwise stated)

			SPECIFICATION			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low level input voltage	V_{IL}	BUF_INT, BUF_INC			0.35 x V_{DDQ}	V
High level input voltage	V_{IH}	BUF_INT, BUF_INC	0.65 x V_{DDQ}			V
DC input signal voltage (note 2)	V_{IN}		-0.3		V_{DDQ} + 0.3	V
Differential input signal voltage (note 3)	V_{ID}	DC - BUF_INT, BUF_INC	0.3		V_{DDQ} + 0.4	V
		AC - BUF_INT, BUF_INC	0.6		V_{DDQ} + 0.4	V
Output differential cross-voltage (note 4)	V_{OX}		V_{DDQ}/2 - 0.1		V_{DDQ}/2 + 0.1	V
Input differential cross-voltage (note 4)	V_{IX}		V_{DDQ}/2 - 0.15	V_{DDQ}/2	V_{DDQ}/2 + 0.15	V

1. Unused inputs must be held high or low to prevent them from floating.
2. DC input signal voltage specifies the allowable DC excursion of differential input.
3. Differential inputs signal voltages specifies the differential voltage [VTR-VCP] required for switching, where VTR is the true input level and VCP is the complimentary input level.
4. Differential cross-point voltage is expected to track variations of VDD and is the voltage at which the differential signal must be changed.

Timing Requirements VDDQ2.5/1.8 = 1.8 V +/- 0.1V

T_A = 0 - 70°C Supply Voltage AVDD2.5 = 2.5V+/-0.2V (unless otherwise stated)

			SPECIFICATION		
PARAMETER	SYMBOL	CONDITIONS	-40	MAX	UNITS
Max clock frequency	$freq_{op}$		125	400	MHz
Application Frequency Range	$freq_{App}$		160	400	MHz
Input clock duty cycle	d_{tin}		40	60	%
CLK stabilization	T_{STAB}			15	µs

Switching Characteristics (VDDQ2.5/1.8 = 1.8V +/- 0.1V) (see note 1)

T_A = 0 - 70°C; Supply Voltage AVDD = 2.5V+/-0.2V, VDDQ2.5/1.8 = 1.8 V +/- 0.1V (unless otherwise stated)

			SPECIFICATION			
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Period jitter	$T_{jit\ (per)}$	Period jitter	-40		40	ps
Half-period jitter	$T_{(jit_hper)}$	Half period jitter	-60		60	ps
Cycle to Cycle	T_{cyc}-T_{cyc}	Cycle to Cycle jitter	-40		40	ps
Dynamic Phase Offset	$T_{(DPO)}$		-50		50	ps
Static Phase Offset	$T_{(SPO)}$		-50	0	50	ps
Output to Output Skew	t_{skew}	DDR(0:5)			40	ps
Output Duty Cycle	t_{duty}		47		53	ps
Output clock slew rate	$t_{sl(i)}$	Measured from 20% to 80% of VDDQ	1.5		3	V/ns

1. Switching characteristics guaranteed for operating frequency range

Electrical Characteristics - Input/Supply/Common Output Parameters (VDDQ2.5/1.8 = 2.5V +/- 0.2V)

T_A = 0 - 70°C; Supply Voltage AVDD = 2.5V+/-0.2V (unless otherwise stated)

			SPEC			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	$V_I = V_{DD}$ or GND	-10			µA
Input Low Current	I_{IL}	$V_I = V_{DD}$ or GND			10	µA
Operating Supply Current	$I_{DDAVDD2.5}$	R_L = 120Ω, C_L = 12pf @ 200MHz		20	23	mA
	$I_{DDVDDQ2.5/1.8}$	R_L = 120Ω, C_L = 12pf @ 200MHz		220	250	mA
Input Clamp Voltage	V_{IK}	V_{DDQ} = 2.5V, Iin = -18mA			-1	V
High-level output voltage	V_{OH}	I_{OH} = -12 mA	1.7			V
Low-level output voltage	V_{OL}	I_{OL} = 12 mA			0.6	V
Input Capacitance	C_{IN}	V_I = GND or V_{DDQ}	2	3	4	pF
Output Capacitance	C_{OUT}	V_{OUT} = GND or V_{DDQ}	2	3	4	pF
Input clock slew rate	$t_{sl(i)}$	Input clock	1	2.5	4	V/ns

Recommended Operating Condition (VDDQ2.5/1.8 = 2.5V +/- 0.2V) (see note1)

T_A = 0 - 70°C; Supply Voltage AVDD = 2.5V+/-0.2V (unless otherwise stated)

			SPECIFICATION			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low level input voltage	V_{IL}	BUF_INT, BUF_INC			V_{DDQ}/2 - 0.18	V
High level input voltage	V_{IH}	BUF_INT, BUF_INC	V_{DDQ}/2 + 0.18			V
DC input signal voltage (note 2)	V_{IN}		-0.3		V_{DDQ} + 0.3	V
Differential input signal voltage (note 3)	V_{ID}	DC - BUF_INT, BUF_INC	0.36		V_{DDQ} + 0.6	V
		AC - BUF_INT, BUF_INC	0.7		V_{DDQ} + 0.6	V
Output differential cross-voltage (note 4)	V_{OX}		V_{DDQ}/2 - 0.15		V_{DDQ}/2 + 0.15	V
Input differential cross-voltage (note 4)	V_{IX}		V_{DDQ}/2 - 0.2	V_{DDQ}/2	V_{DDQ}/2 + 0.2	V

1. Unused inputs must be held high or low to prevent them from floating.
2. DC input signal voltage specifies the allowable DC excursion of differential input.
3. Differential inputs signal voltages specifies the differential voltage [VTR-VCP] required for switching, where VTR is the true input level and VCP is the complimentary input level.
4. Differential cross-point voltage is expected to track variations of VDD and is the voltage at which the differential signal must be changed.

Timing Requirements VDDQ2.5/1.8 = 2.5V +/- 0.2V

T_A = 0 - 70°C Supply Voltage AVDD2.5 = 2.5V+/-0.2V (unless otherwise stated)

			SPECIFICATION		
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Max clock frequency	$freq_{op}$		45	500	MHz
Application Frequency Range	$freq_{App}$		95	233	MHz
Input clock duty cycle	d_{tin}		40	60	%
CLK stabilization	T_{STAB}			15	µs

Switching Characteristics (VDDQ2.5/1.8 = 2.5V +/- 0.2V) (see note 1)

T_A = 0 - 70°C; Supply Voltage AVDD = 2.5V+/-0.2V, VDDQ2.5/1.8 = 2.5 V +/- 0.2V (unless otherwise stated)

			SPECIFICATION			
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Period jitter	$T_{jit\ (per)}$	Period jitter	-60		60	ps
Half-period jitter	$T_{(jit_hper)}$	Half period jitter	-75		75	ps
Cycle to Cycle Jitter	T_{cyc}-T_{cyc}	Cycle to Cycle jitter	-60		60	ps
Static Phase Offset	$T_{(SPO)}$		-50	0	50	ps
Output to Output Skew	T_{skew}	DDR(0:5)			40	ps
Output Duty Cycle	t_{duty}		47		53	ps
Output clock slew rate	$t_{sl(o)}$	Measured from 20% to 80% of VDDQ	1.5		4	V/ns

1. Switching characteristics guaranteed for operating frequency range

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D4_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 6
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address $D5_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 7***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D4_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Byte 7	
	ACK
Stop Bit	

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D5_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
	Byte 7
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

I²C Table: Output Control Register

Byte 7	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	BUFF_IN_T/C	Frequency Detect	RW	OFF	ON	1
Bit 6	-	FB_OUT_T/C	FB_OUT Control	RW	Disable	Enable	1
Bit 5	-	DDR_T5/C5	Output Control	RW	Disable	Enable	1
Bit 4	-	DDR_T4/C4	Output Control	RW	Disable	Enable	1
Bit 3	-	DDR_T3/C3	Output Control	RW	Disable	Enable	1
Bit 2	-	DDR_T2/C2	Output Control	RW	Disable	Enable	1
Bit 1	-	DDR_T1/C1	Output Control	RW	Disable	Enable	1
Bit 0	-	DDR_T0/C0	Output Control	RW	Disable	Enable	1

I²C Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back, default is 0h = 15 bytes		0
Bit 6	-	BC6		RW			0
Bit 5	-	BC5		RW			0
Bit 4	-	BC4		RW			0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			1
Bit 1	-	BC1		RW			1
Bit 0	-	BC0		RW			1

I²C Table: Group Skew Control Register

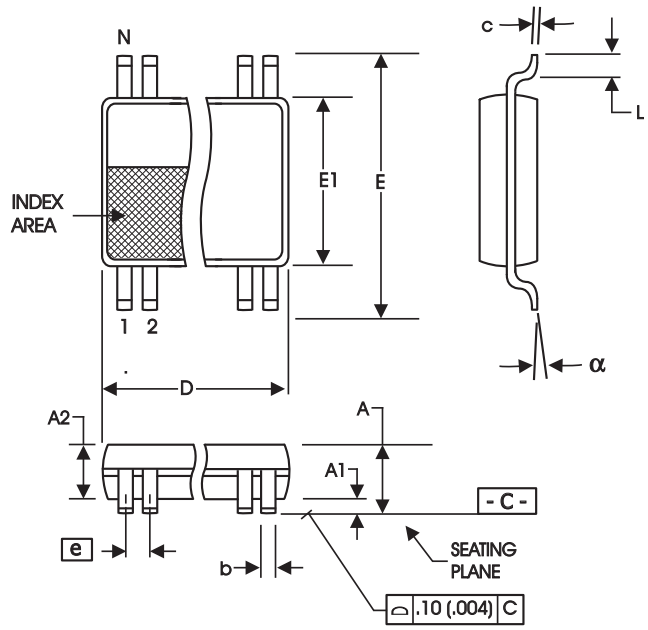
Byte 19	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	DDR_CSkw3	DDR_C Skew Control (also see table1)	RW	0000 = 0	1101 = 600	0
Bit 6	-	DDR_CSkw2		RW	0100 = 150	1110 = 750	0
Bit 5	-	DDR_CSkw1		RW	1000 = 300	1111 = 900	0
Bit 4	-	DDR_CSkw0		RW	1100 = 450	N/A	0
Bit 3	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 2	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 1	-	FBOUTSkw1	FB_OUT Skew Control (also see table 2)	RW	00 = 0	10 = 500	0
Bit 0	-	FBOUTSkw0		RW	01 = 250	11 = 750	0

I²C Table: Group Skew Control Register

Byte 20	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	DDR_TSkw3	DDR_T Skew Control (also see table1)	RW	0000 = 0	1101 = 600	0
Bit 6	-	DDR_TSkw2		RW	0100 = 150	1110 = 750	0
Bit 5	-	DDR_TSkw1		RW	1000 = 300	1111 = 900	0
Bit 4	-	DDR_TSkw0		RW	1100 = 450	N/A	0
Bit 3	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 2	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 1	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 0	-	Reserved	Reserved	RW	Reserved	Reserved	0

Note: Bytes not shown are reserved and should not be altered.

28-pin SSOP Package Drawing and Dimensions



209 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	2.00	--	.079
A1	0.05	--	.002	--
A2	1.65	1.85	.065	.073
b	0.22	0.38	.009	.015
c	0.09	0.25	.0035	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	7.40	8.20	.291	.323
E1	5.00	5.60	.197	.220
e	0.65 BASIC		0.0256 BASIC	
L	0.55	0.95	.022	.037
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

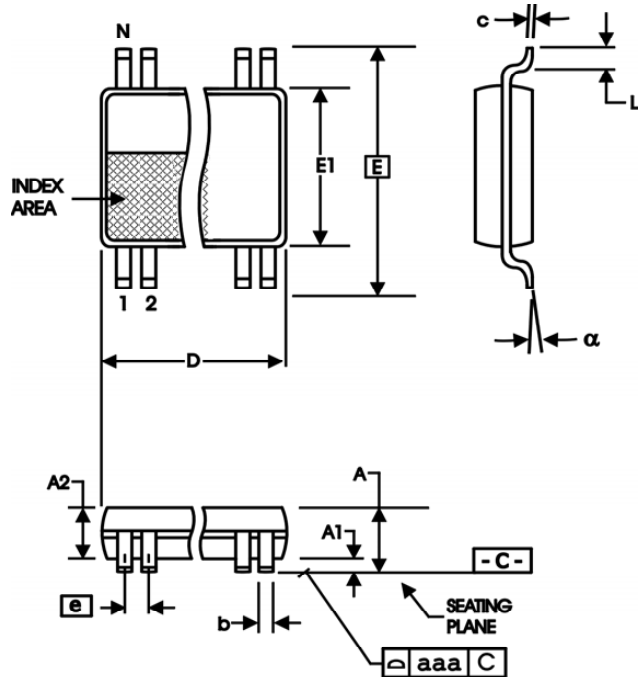
VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.90	10.50	.390	.413

Reference Doc.: JEDEC Publication 95, MO-150

10-0033

28-pin TSSOP Package Drawing and Dimensions



4.40 mm. Body, 0.65 mm. Pitch TSSOP

(173 mil) (25.6 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.60	9.80	.378	.386

Reference Doc.: JEDEC Publication 95, MO-153

10-0035

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9P936AFLF	Tubes	28-pin SSOP	0 to +70°C
9P936AFLFT	Tape and Reel	28-pin SSOP	0 to +70°C
9P936AGLF	Tubes	28-pin TSSOP	0 to +70°C
9P936AGLFT	Tape and Reel	28-pin TSSOP	0 to +70°C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.
"A" denotes the revision designator (will not correlate to datasheet revision).

Revision History

Rev.	Issue Date	Description	Page #
0.1	3/23/2005	Updated Electrical Characteristics	5-9
0.2	4/1/2005	Updated Skew programming bytes and I2c programming address	3, 10
0.3	9/12/2005	Updated LF Ordering Information	11
0.4	9/14/2005	Added TSSOP Ordering Information.	12
0.5	11/13/2006	Updated I2C.	3
0.6	4/5/2007	Updated Switching Characteristics.	6
0.7	6/26/2007	Updated Max Clock Frequency.	1, 7, 10
A	4/8/2009	Released to final.	
B	11/12/2009	1. Updated all electrical tables to specify VDDQ = 1.8V and 2.5V. 2. Updated ordering information table 3. Updated pinout and pin descriptions	Various
C	12/2/2009	1.Corrected Byte 19/20 default to 00 hex. 2.Corrected typos in electrical tables, made formatting improvements for readability.	

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