



THE DATASHEET OF ICPL2630





ICPL2630 / ICPL2631

DESCRIPTION

The ICPL2630 and ICPL2631 dual channel devices each consists of an infrared emitting diode, optically coupled to a high speed integrated photo detector logic gate with a strobable output.

FEATURES

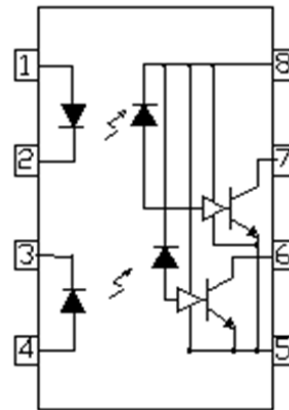
- High speed 10Mbit/s
- 10kV/ μ s min. Common Mode Transient Immunity (ICPL2631)
- High AC Isolation voltage 5000V_{rms}
- Guaranteed performance from -40°C to 85°C
- Wide Operating temperature range 55°C to 125°C
- Logic Gate Output
- RoHS Compliant
- Safety Approvals Pending

APPLICATIONS

- Line Receivers, Data Transmission
- Ground Loop Elimination
- LSTTL to TTL, LSTTL or 5V CMOS
- Data Multiplexing
- Switch Mode Power Supplies
- Pulse Transformer Replacement
- Computer Peripheral Interface

ORDER INFORMATION

- Add G after PN for 10mm lead spacing
- Add SM after PN for Surface Mount,
- Add SMT&R after PN for Surface Mount Tape & Reel



1. Anode
2. Cathode
3. Cathode
4. Anode
5. Gnd
6. Vout2
7. Vout1
8. Vcc

ABSOLUTE MAXIMUM RATINGS

Input Diode

Forward Current (each Channel)	20mA
Reverse Voltage	5V
Power dissipation (each Channel)	40mW

Output

Output Current (each Channel)	50mA
Output Voltage	7V
Supply Voltage	7V
Power Dissipation	85mW

Total Package

Isolation Voltage	5000V _{rms}
Operating Temperature	-40 to 100 °C
Storage Temperature	-55 to 125 °C
Power Dissipation	85mW
Lead Soldering Temperature (10s)	260°C

ISOCOM COMPONENTS 2004 LTD

Unit 25B, Park View Road West, Park View Industrial Estate
Hartlepool, Cleveland, TS25 1UD, United Kingdom
Tel: +44 (0)1429 863 609 Fax : +44 (0)1429 863 581
e-mail: sales@isocom.co.uk
<http://www.isocom.com>

ISOCOM COMPONENTS ASIA LTD

Hong Kong Office,
Block A, 8/F, Wah Hing Industrial mansion,
36 Tai Yau Street, San Po Kong, Kowloon, Hong Kong.
Tel: +852 2995 9217 Fax : +852 8161 6292
e-mail: sales@isocom.com.hk



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Truth Table (Positive Logic)

Input	Output
H	L
L	H

ELECTRICAL CHARACTERISTICS

INPUT ($T_A = -40^{\circ}\text{C}$ to 85°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ.	Max	Unit
Forward Voltage	V_F	$I_F = 10\text{mA}$, $T_A = 25^{\circ}\text{C}$		1.4	1.8	V
Reverse Voltage	V_R	$I_R = 10\mu\text{A}$	5.0			V
Temperature Coefficient	$\Delta V_F / \Delta T_A$	$I_F = 10\text{mA}$		-1.8		mV/ $^{\circ}\text{C}$
Input Capacitance	C_{IN}	$V_F = 0\text{V}$, $f = 1\text{MHz}$		60		pF

OUTPUT ($T_A = -40^{\circ}\text{C}$ to 85°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ.	Max	Unit
High Level Supply Current	I_{CCH}	$I_F = 0\text{mA}$, $V_{CC} = 5.5\text{V}$		12.5	18	mA
Low Level Supply Current	I_{CCL}	$I_F = 10\text{mA}$, $V_{CC} = 5.5\text{V}$		14.5	21	mA

COUPLED ($T_A = -40^{\circ}\text{C}$ to 85°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ.	Max	Unit
High Level Output Current	I_{OH}	$V_{CC} = 5.5\text{V}$, $V_O = 5.5\text{V}$, $I_F = 250\mu\text{A}$		2.1	100	μA
Low Level Output Voltage	V_{OL}	$V_{CC} = 5.5\text{V}$, $I_F = 5\text{mA}$, $I_{CL} = 13\text{mA}$		0.35	0.6	V
Input Threshold Current	I_{FT}	$V_{CC} = 5.5\text{V}$, $V_O = 0.6\text{V}$, $I_{OL} = 13\text{mA}$		2.5	5	mA



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ELECTRICAL CHARACTERISTICS

Switching Characteristics ($T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 5\text{V}$, $I_F = 7.5\text{mA}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ.	Max	Unit
Propagation Delay Time to Output High Level	t_{PLH}	$C_L = 15\text{pF}$, $R_L = 350\Omega$, $T_A = 25^\circ\text{C}$		35	100	ns
Propagation Delay Time to Output Low Level	t_{PHL}	$C_L = 15\text{pF}$, $R_L = 350\Omega$, $T_A = 25^\circ\text{C}$		40	100	ns
Pulse Width Distortion	$ t_{PHL} - t_{PLH} $	$C_L = 15\text{pF}$, $R_L = 350\Omega$		5	35	ns
Output Rise Time	t_r	$C_L = 15\text{pF}$, $R_L = 350\Omega$		40		ns
Output Fall time	t_f	$C_L = 15\text{pF}$, $R_L = 350\Omega$		10		ns
Common Mode Transient Immunity at Logic High	CM_H	ICPL2630 ICPL2631 $I_F = 0\text{mA}$, $V_{CM} = 1\text{kVp-p}$, $V_{OH} = 2.0\text{V}$, $R_L = 350\Omega$, $T_A = 25^\circ\text{C}$	5000 10000	20000		V/ μs
Common Mode Transient Immunity at Logic Low	CM_L	ICPL2630 ICPL2631 $I_F = 7.5\text{mA}$, $V_{CM} = 1\text{kVp-p}$, $V_{OL} = 0.8\text{V}$, $R_L = 350\Omega$, $T_A = 25^\circ\text{C}$	5000 10000	20000		V/ μs

Notes :

1. The V_{CC} supply must be bypassed by a $0.1\mu\text{F}$ capacitor or larger with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and Gnd pins.
2. t_{PLH} – Propagation delay is measured from the 3.75mA level on the HIGH to LOW transition of the input current pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
3. t_{PHL} – Propagation delay is measured from the 3.75mA level on the LOW to HIGH transition of the input current pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
4. t_r – Rise time is measured from the 10% to the 90% levels on the LOW to HIGH transition of the output pulse.
5. t_f – Fall time is measured from the 90% to the 10% levels on the HIGH to LOW transition of the output pulse.
6. CM_H – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the HIGH state (i.e., $V_{OUT} > 2.0\text{V}$).
7. CM_L – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the LOW output state (i.e., $V_{OUT} < 0.8\text{V}$).



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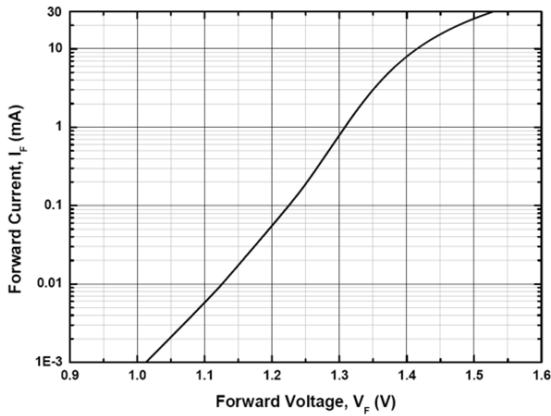


Fig 1 Forward Current vs Forward Voltage

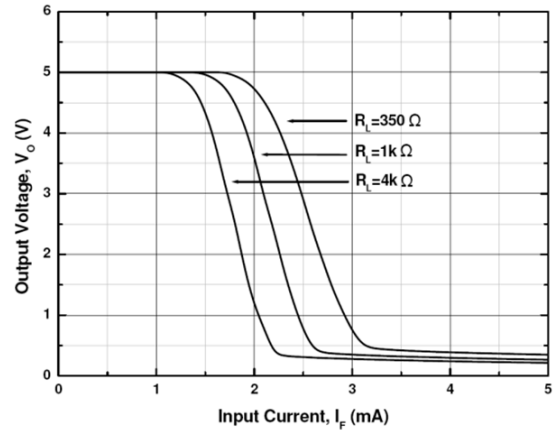


Fig 2 Output Voltage vs Input Current

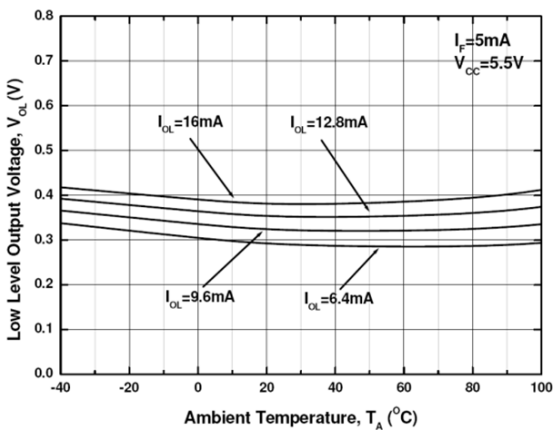


Fig 3 Low Level Output Voltage vs T_A

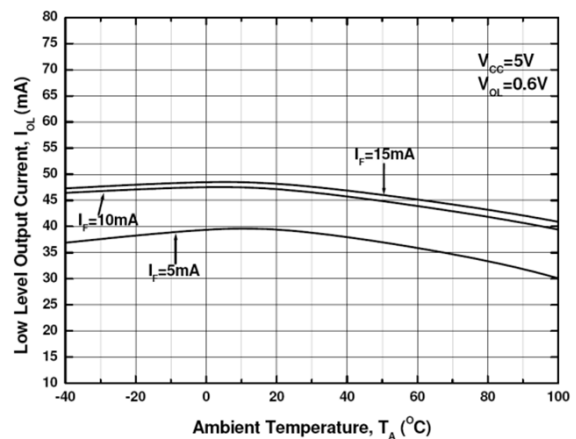


Fig 4 Low Level Output Current vs T_A

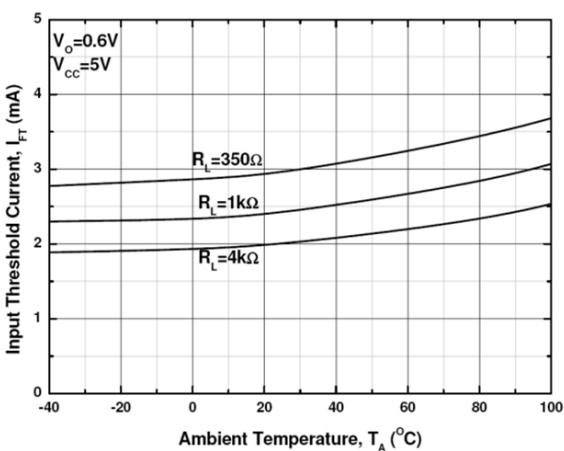


Fig 5 Input Threshold Current vs T_A

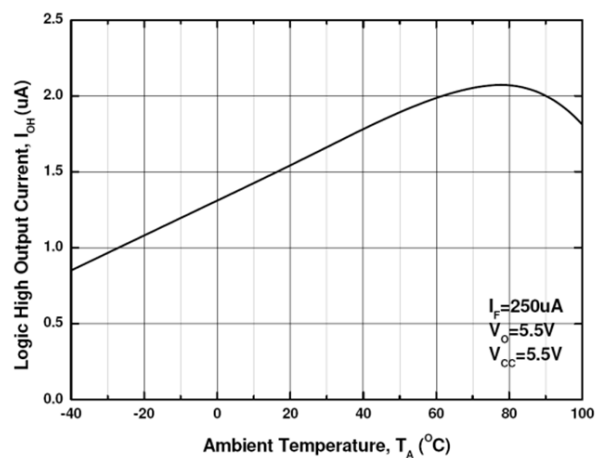


Fig 6 High Level Output Current vs T_A



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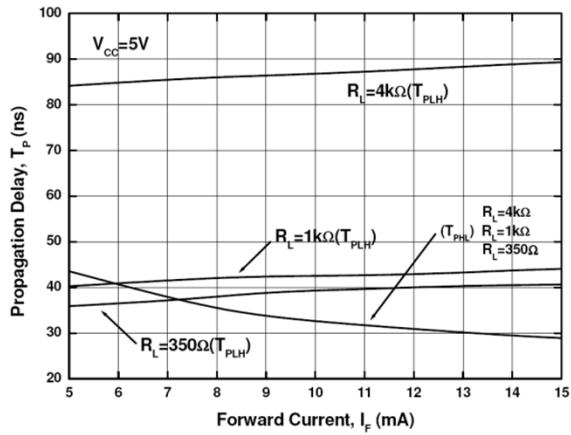


Fig 7 Propagation Delay vs Forward Current

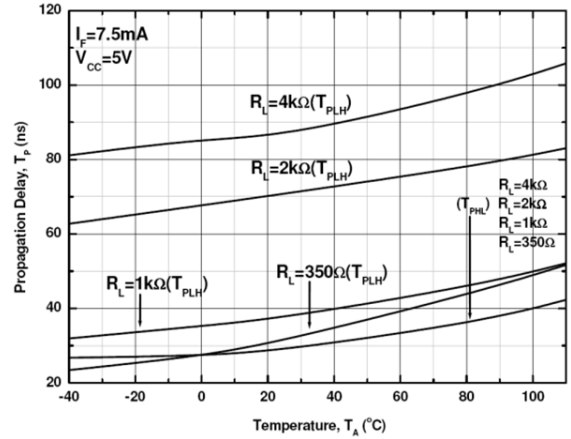


Fig 8 Propagation Delay vs T_A

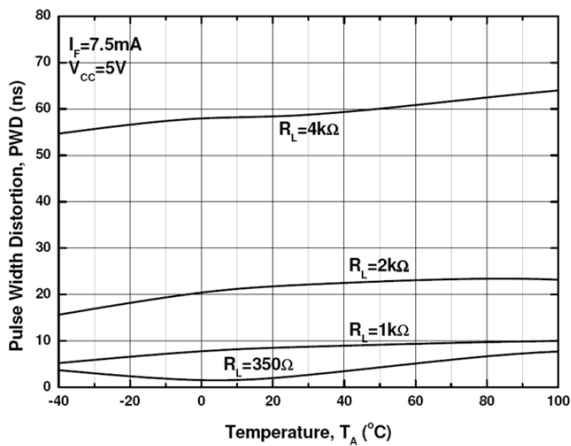


Fig 9 Pulse Width Distortion vs T_A

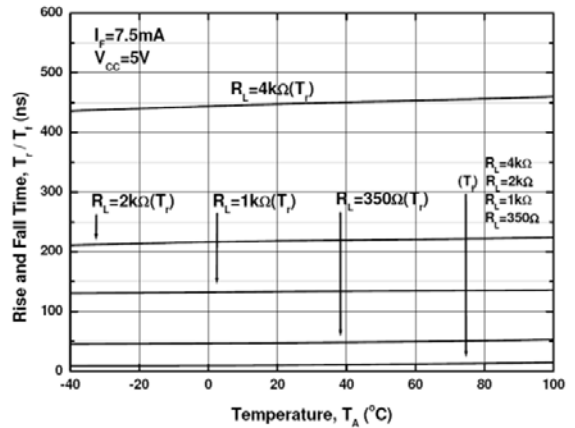


Fig 10 Rise Time and Fall Time vs T_A



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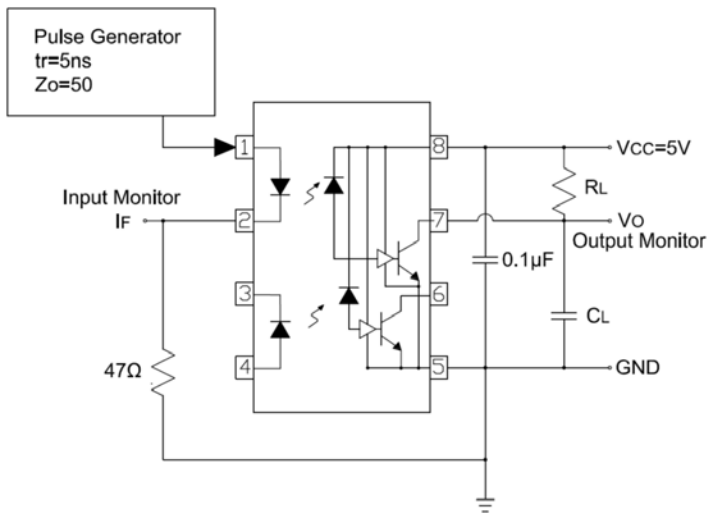


Fig 11 Switching Time Test Circuit

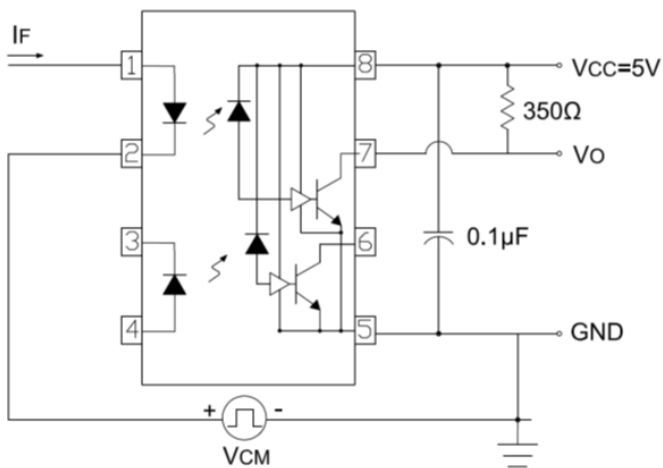
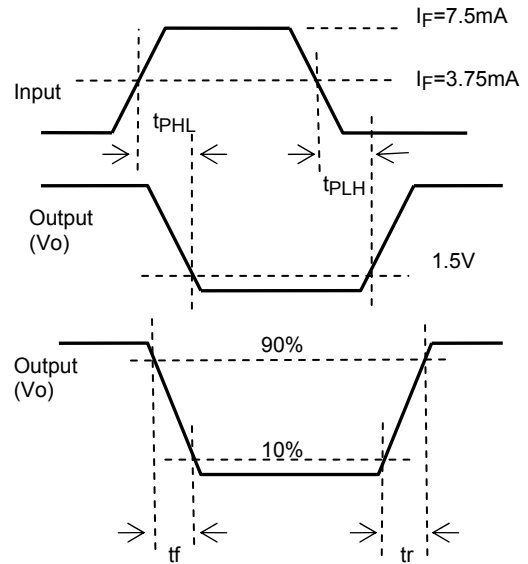
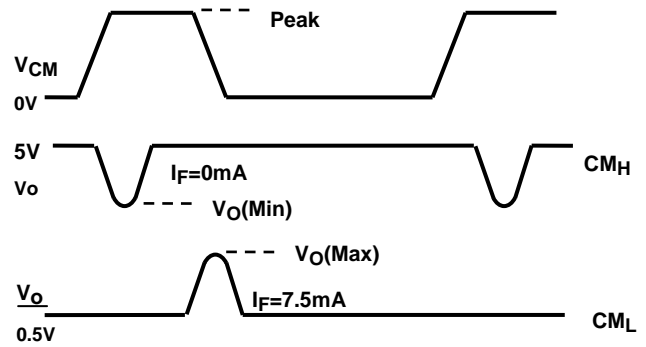


Fig 12 Common Mode Transient Immunity Test Circuit

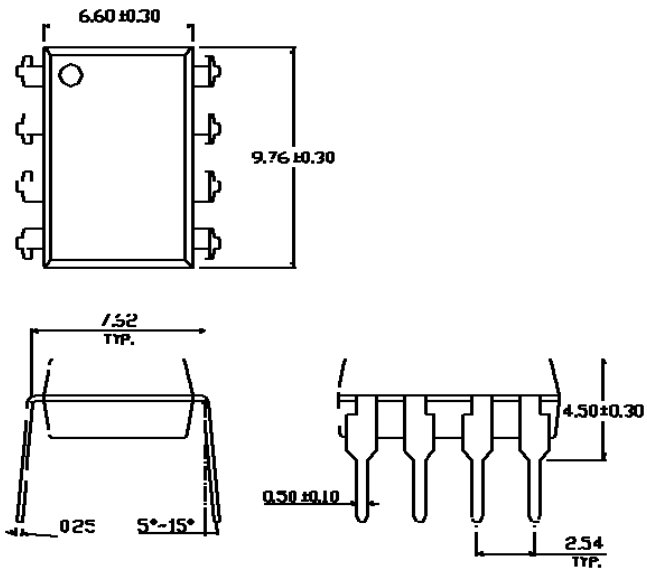




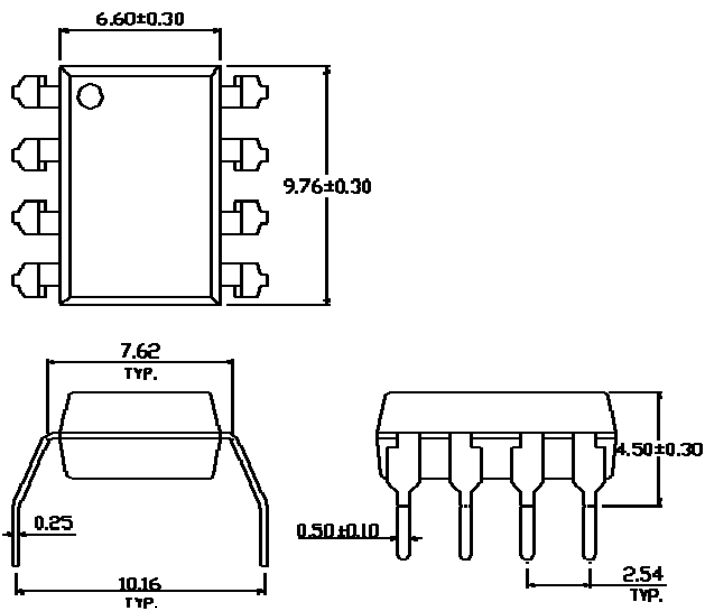
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PACKAGE DIMENSIONS (mm)

DIP



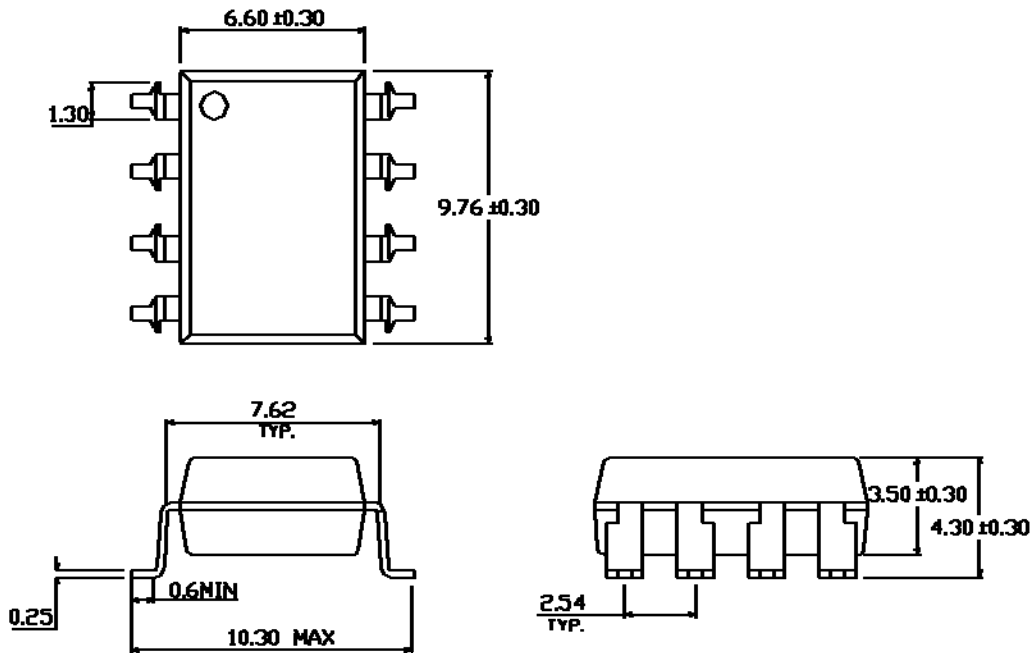
G FORM



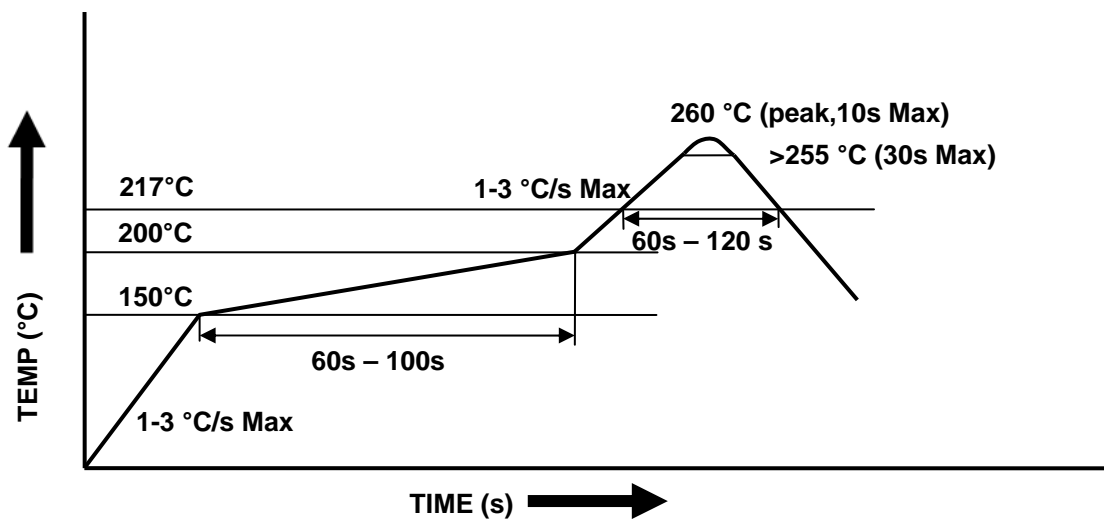


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SMD



REFLOW SOLDERING TEMPERATURE PROFILE



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