

## Features

- High-performance, Low-power AVR<sup>®</sup> 8-bit Microcontroller
- RISC Architecture
  - 130 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- Nonvolatile Program and Data Memories
  - 8K Bytes of In-System Self-programmable Flash  
Endurance: 10,000 Write/Erase Cycles
  - Optional Boot Code Section with Independent Lock bits  
In-System Programming by On-chip Boot Program  
True Read-While-Write Operation
  - 512 Bytes EEPROM  
Endurance: 100,000 Write/Erase Cycles
  - 512 Bytes Internal SRAM
  - Up to 64K Bytes Optional External Memory Space
  - Programming Lock for Software Security
- Peripheral Features
  - One 8-bit Timer/Counter with Separate Prescaler and Compare Mode
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Three PWM Channels
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Three Sleep Modes: Idle, Power-down and Standby
- I/O and Packages
  - 35 Programmable I/O Lines
  - 40-pin PDIP, 44-lead TQFP, 44-lead PLCC, and 44-pad QFN/MLF
- Operating Voltages
  - 2.7 - 5.5V for ATmega8515L
  - 4.5 - 5.5V for ATmega8515
- Speed Grades
  - 0 - 8 MHz for ATmega8515L
  - 0 - 16 MHz for ATmega8515



**8-bit AVR<sup>®</sup>  
Microcontroller  
with 8K Bytes  
In-System  
Programmable  
Flash**

**ATmega8515  
ATmega8515L**

**Summary**

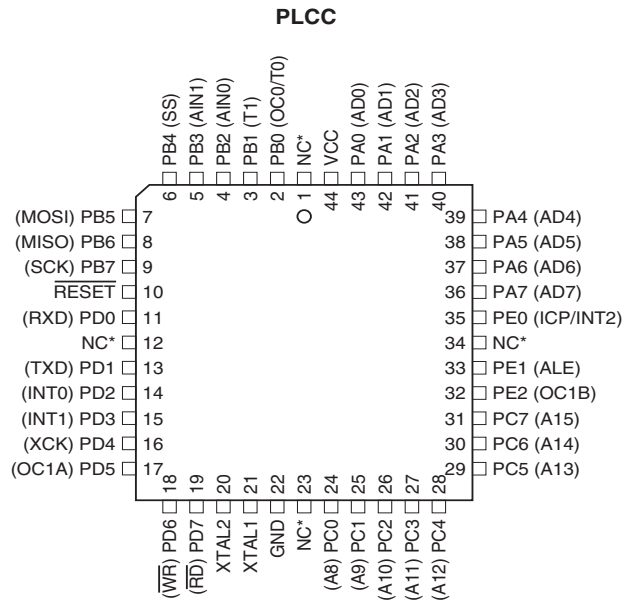
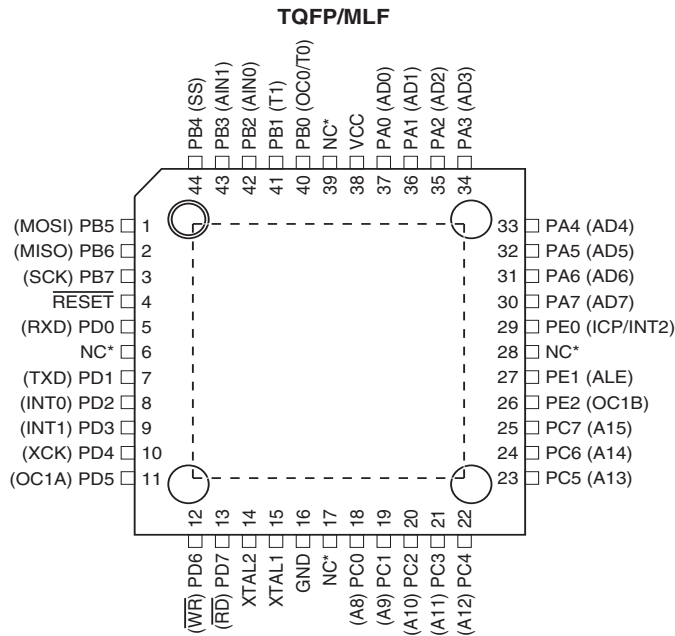
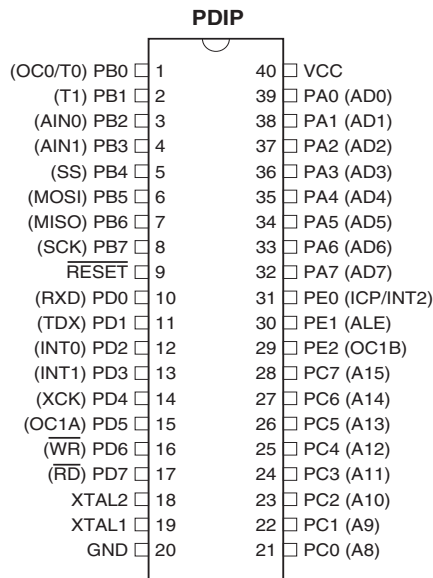
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Note: This is a summary document. A complete document is available on our Web site at [www.atmel.com](http://www.atmel.com).

# Pin Configurations

Figure 1. Pinout ATmega8515



**NOTES:**

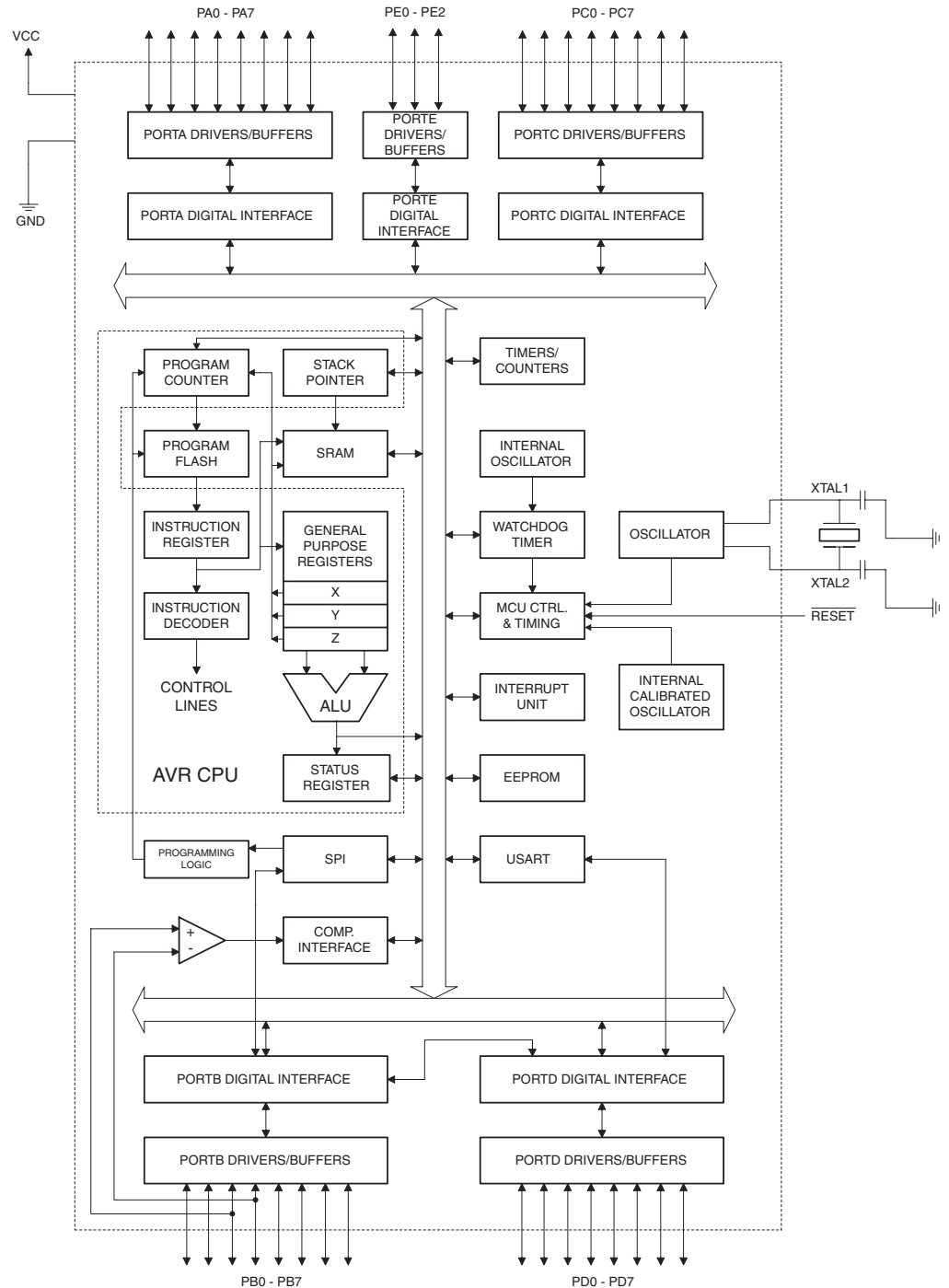
1. MLF bottom pad should be soldered to ground.
2. \* NC = Do not connect (May be used in future devices)

## Overview

The ATmega8515 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega8515 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

## Block Diagram

Figure 2. Block Diagram





The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega8515 provides the following features: 8K bytes of In-System Programmable Flash with Read-While-Write capabilities, 512 bytes EEPROM, 512 bytes SRAM, an External memory interface, 35 general purpose I/O lines, 32 general purpose working registers, two flexible Timer/Counters with compare modes, Internal and External interrupts, a Serial Programmable USART, a programmable Watchdog Timer with internal Oscillator, a SPI serial port, and three software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and Interrupt system to continue functioning. The Power-down mode saves the Register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption.

The device is manufactured using Atmel's high density nonvolatile memory technology. The On-chip ISP Flash allows the Program memory to be reprogrammed In-System through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-programmable Flash on a monolithic chip, the Atmel ATmega8515 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega8515 is supported with a full suite of program and system development tools including: C Compilers, Macro assemblers, Program debugger/simulators, In-circuit Emulators, and Evaluation kits.

## Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

## AT90S4414/8515 and ATmega8515 Compatibility

The ATmega8515 provides all the features of the AT90S4414/8515. In addition, several new features are added. The ATmega8515 is backward compatible with AT90S4414/8515 in most cases. However, some incompatibilities between the two microcontrollers exist. To solve this problem, an AT90S4414/8515 compatibility mode can be selected by programming the S8515C Fuse. ATmega8515 is 100% pin compatible with AT90S4414/8515, and can replace the AT90S4414/8515 on current printed circuit boards. However, the location of Fuse bits and the electrical characteristics differs between the two devices.

### AT90S4414/8515 Compatibility Mode

Programming the S8515C Fuse will change the following functionality:

- The timed sequence for changing the Watchdog Time-out period is disabled. See "Timed Sequences for Changing the Configuration of the Watchdog Timer" on page 53 for details.
- The double buffering of the USART Receive Registers is disabled. See "AVR USART vs. AVR UART – Compatibility" on page 137 for details.
- PORTE(2:1) will be set as output, and PORTE0 will be set as input.

## Pin Descriptions

|                          |   |
|--------------------------|---|
| <b>VCC</b>               | Digital supply voltage.   |
| <b>GND</b>               | Ground.   |
| <b>Port A (PA7..PA0)</b> | <p>Port A is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.</p> <p>Port A also serves the functions of various special features of the ATmega8515 as listed on page 67.</p> |
| <b>Port B (PB7..PB0)</b> | <p>Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.</p> <p>Port B also serves the functions of various special features of the ATmega8515 as listed on page 67.</p>                                |
| <b>Port C (PC7..PC0)</b> | <p>Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.</p>  |
| <b>Port D (PD7..PD0)</b> | <p>Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.</p> <p>Port D also serves the functions of various special features of the ATmega8515 as listed on page 72.</p>                                |
| <b>Port E (PE2..PE0)</b> | <p>Port E is an 3-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running.</p> <p>Port E also serves the functions of various special features of the ATmega8515 as listed on page 74.</p>                                |
| <b><u>RESET</u></b>      | Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 18 on page 46. Shorter pulses are not guaranteed to generate a reset.   |
| <b>XTAL1</b>             | Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.  |
| <b>XTAL2</b>             | Output from the inverting Oscillator amplifier.   |



## Resources

A comprehensive set of development tools, application notes and datasheets are available for download on <http://www.atmel.com/avr>.

## **About Code Examples**

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C Compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C Compiler documentation for more details.



# Register Summary

| Address                                   | Name     | Bit 7  | Bit 6  | Bit 5  | Bit 4   | Bit 3      | Bit 2  | Bit 1  | Bit 0  | Page     |
|---|----------|--|--------|--------|---------|------------|--------|--------|--------|----------|
| \$3F (\$5F)                               | SREG     | I  | T      | H      | S       | V          | N      | Z      | C      | 10       |
| \$3E (\$5E)                               | SPH      | SP15   | SP14   | SP13   | SP12    | SP11       | SP10   | SP9    | SP8    | 12       |
| \$3D (\$5D)                               | SPL      | SP7  | SP6    | SP5    | SP4     | SP3        | SP2    | SP1    | SP0    | 12       |
| \$3C (\$5C)                               | Reserved |  |        |        |         |            |        |        |        |          |
| \$3B (\$5B)                               | GICR     | INT1   | INT0   | INT2   | -       | -          | -      | IVSEL  | IVCE   | 57, 78   |
| \$3A (\$5A)                               | GIFR     | INTF1  | INTF0  | INTF2  | -       | -          | -      | -      | -      | 79       |
| \$39 (\$59)                               | TIMSK    | TOIE1  | OCIE1A | OCIE1B | -       | TICIE1     | -      | TOIE0  | OCIE0  | 93, 124  |
| \$38 (\$58)                               | TIFR     | TOV1   | OCF1A  | OCF1B  | -       | ICF1       | -      | TOV0   | OCF0   | 93, 125  |
| \$37 (\$57)                               | SPMCR    | SPMIE  | RWWWSB | -      | RWWWSRE | BLBSET     | PGWRT  | PGERS  | SPMEN  | 170      |
| \$36 (\$56)                               | EMCUCR   | SM0  | SRL2   | SRL1   | SRL0    | SRW01      | SRW00  | SRW11  | ISC2   | 29,42,78 |
| \$35 (\$55)                               | MCUCR    | SRE  | SRW10  | SE     | SM1     | ISC11      | ISC10  | ISC01  | ISC00  | 29,41,77 |
| \$34 (\$54)                               | MCUCSR   | -  | -      | SM2    | -       | WDRF       | BORF   | EXTRF  | PORF   | 41,49    |
| \$33 (\$53)                               | TCCR0    | FOC0   | WGM00  | COM01  | COM00   | WGM01      | CS02   | CS01   | CS00   | 91       |
| \$32 (\$52)                               | TCNT0    | Timer/Counter0 (8 Bits)                              |        |        |         |            |        |        |        | 93       |
| \$31 (\$51)                               | OCR0     | Timer/Counter0 Output Compare Register               |        |        |         |            |        |        |        | 93       |
| \$30 (\$50)                               | SFIOR    | -  | XMBK   | XMM2   | XMM1    | XMM0       | PUD    | -      | PSR10  | 31,66,96 |
| \$2F (\$4F)                               | TCCR1A   | COM1A1   | COM1A0 | COM1B1 | COM1B0  | FOC1A      | FOC1B  | WGM11  | WGM10  | 119      |
| \$2E (\$4E)                               | TCCR1B   | ICNC1  | ICES1  | -      | WGM13   | WGM12      | CS12   | CS11   | CS10   | 122      |
| \$2D (\$4D)                               | TCNT1H   | Timer/Counter1 - Counter Register High Byte          |        |        |         |            |        |        |        | 123      |
| \$2C (\$4C)                               | TCNT1L   | Timer/Counter1 - Counter Register Low Byte           |        |        |         |            |        |        |        | 123      |
| \$2B (\$4B)                               | OCR1AH   | Timer/Counter1 - Output Compare Register A High Byte |        |        |         |            |        |        |        | 123      |
| \$2A (\$4A)                               | OCR1AL   | Timer/Counter1 - Output Compare Register A Low Byte  |        |        |         |            |        |        |        | 123      |
| \$29 (\$49)                               | OCR1BH   | Timer/Counter1 - Output Compare Register B High Byte |        |        |         |            |        |        |        | 123      |
| \$28 (\$48)                               | OCR1BL   | Timer/Counter1 - Output Compare Register B Low Byte  |        |        |         |            |        |        |        | 123      |
| \$27 (\$47)                               | Reserved |  |        |        |         |            |        |        |        | -        |
| \$26 (\$46)                               | Reserved |  |        |        |         |            |        |        |        | -        |
| \$25 (\$45)                               | ICR1H    | Timer/Counter1 - Input Capture Register High Byte    |        |        |         |            |        |        |        | 124      |
| \$24 (\$44)                               | ICR1L    | Timer/Counter1 - Input Capture Register Low Byte     |        |        |         |            |        |        |        | 124      |
| \$23 (\$43)                               | Reserved |  |        |        |         |            |        |        |        | -        |
| \$22 (\$42)                               | Reserved |  |        |        |         |            |        |        |        | -        |
| \$21 (\$41)                               | WDTCSR   | -  | -      | -      | WDCE    | WDE        | WDP2   | WDP1   | WDP0   | 51       |
| \$20 <sup>(1)</sup> (\$40) <sup>(1)</sup> | UBRRH    | URSEL  | -      | -      | -       | UBRR[11:8] |        |        |        | 159      |
|   | UCSRC    | URSEL  | UMSEL  | UPM1   | UPM0    | USBS       | UCSZ1  | UCSZ0  | UCPOL  | 157      |
| \$1F (\$3F)                               | EEARH    | -  | -      | -      | -       | -          | -      | -      | EEAR8  | 19       |
| \$1E (\$3E)                               | EEARL    | EEPROM Address Register Low Byte                     |        |        |         |            |        |        |        | 19       |
| \$1D (\$3D)                               | EEDR     | EEPROM Data Register                                 |        |        |         |            |        |        |        | 20       |
| \$1C (\$3C)                               | EECR     | -  | -      | -      | -       | EERIE      | EEMWE  | EERE   | EERE   | 20       |
| \$1B (\$3B)                               | PORTA    | PORTA7   | PORTA6 | PORTA5 | PORTA4  | PORTA3     | PORTA2 | PORTA1 | PORTA0 | 75       |
| \$1A (\$3A)                               | DDRA     | DDA7   | DDA6   | DDA5   | DDA4    | DDA3       | DDA2   | DDA1   | DDA0   | 75       |
| \$19 (\$39)                               | PINA     | PINA7  | PINA6  | PINA5  | PINA4   | PINA3      | PINA2  | PINA1  | PINA0  | 75       |
| \$18 (\$38)                               | PORTB    | PORTB7   | PORTB6 | PORTB5 | PORTB4  | PORTB3     | PORTB2 | PORTB1 | PORTB0 | 75       |
| \$17 (\$37)                               | DDRB     | DDB7   | DDB6   | DDB5   | DDB4    | DDB3       | DDB2   | DDB1   | DDB0   | 75       |
| \$16 (\$36)                               | PINB     | PINB7  | PINB6  | PINB5  | PINB4   | PINB3      | PINB2  | PINB1  | PINB0  | 75       |
| \$15 (\$35)                               | PORTC    | PORTC7   | PORTC6 | PORTC5 | PORTC4  | PORTC3     | PORTC2 | PORTC1 | PORTC0 | 75       |
| \$14 (\$34)                               | DDRC     | DDC7   | DDC6   | DDC5   | DDC4    | DDC3       | DDC2   | DDC1   | DDC0   | 75       |
| \$13 (\$33)                               | PINC     | PINC7  | PINC6  | PINC5  | PINC4   | PINC3      | PINC2  | PINC1  | PINC0  | 76       |
| \$12 (\$32)                               | PORTD    | PORTD7   | PORTD6 | PORTD5 | PORTD4  | PORTD3     | PORTD2 | PORTD1 | PORTD0 | 76       |
| \$11 (\$31)                               | DDRD     | DDD7   | DDD6   | DDD5   | DDD4    | DDD3       | DDD2   | DDD1   | DDD0   | 76       |
| \$10 (\$30)                               | PIND     | PIND7  | PIND6  | PIND5  | PIND4   | PIND3      | PIND2  | PIND1  | PIND0  | 76       |
| \$0F (\$2F)                               | SPDR     | SPI Data Register                                    |        |        |         |            |        |        |        | 133      |
| \$0E (\$2E)                               | SPSR     | SPIF   | WCOL   | -      | -       | -          | -      | -      | SPI2X  | 133      |
| \$0D (\$2D)                               | SPCR     | SPIE   | SPE    | DORD   | MSTR    | CPOL       | CPHA   | SPR1   | SPR0   | 131      |
| \$0C (\$2C)                               | UDR      | USART I/O Data Register                              |        |        |         |            |        |        |        | 155      |
| \$0B (\$2B)                               | UCSRA    | RXC  | TXC    | UDRE   | FE      | DOR        | PE     | U2X    | MPCM   | 155      |
| \$0A (\$2A)                               | UCSRB    | RXCIE  | TXCIE  | UDRIE  | RXEN    | TXEN       | UCSZ2  | RXB8   | TXB8   | 156      |
| \$09 (\$29)                               | UBRRL    | USART Baud Rate Register Low Byte                    |        |        |         |            |        |        |        | 159      |
| \$08 (\$28)                               | ACSR     | ACD  | ACBG   | ACO    | ACI     | ACIE       | ACIC   | ACIS1  | ACIS0  | 164      |
| \$07 (\$27)                               | PORTE    | -  | -      | -      | -       | -          | PORTE2 | PORTE1 | PORTE0 | 76       |
| \$06 (\$26)                               | DDRE     | -  | -      | -      | -       | -          | DDE2   | DDE1   | DDE0   | 76       |
| \$05 (\$25)                               | PINE     | -  | -      | -      | -       | -          | PINE2  | PINE1  | PINE0  | 76       |
| \$04 (\$24)                               | OSCCAL   | Oscillator Calibration Register                      |        |        |         |            |        |        |        | 39       |

- Notes:
1. Refer to the USART description for details on how to access UBRRH and UCSRC.
  2. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

3. Some of the Status Flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O Register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers \$00 to \$1F only.

# Instruction Set Summary

| Mnemonics                                | Operands | Description                              | Operation   | Flags         | #Clocks |
|--|----------|--|---|---------------|---------|
| <b>ARITHMETIC AND LOGIC INSTRUCTIONS</b> |          |  |   |               |         |
| ADD                                      | Rd, Rr   | Add two Registers                        | $Rd \leftarrow Rd + Rr$                               | Z,C,N,V,H     | 1       |
| ADC                                      | Rd, Rr   | Add with Carry two Registers             | $Rd \leftarrow Rd + Rr + C$                           | Z,C,N,V,H     | 1       |
| ADIW                                     | RdI,K    | Add Immediate to Word                    | $Rdh:Rdl \leftarrow Rdh:Rdl + K$                      | Z,C,N,V,S     | 2       |
| SUB                                      | Rd, Rr   | Subtract two Registers                   | $Rd \leftarrow Rd - Rr$                               | Z,C,N,V,H     | 1       |
| SUBI                                     | Rd, K    | Subtract Constant from Register          | $Rd \leftarrow Rd - K$                                | Z,C,N,V,H     | 1       |
| SBC                                      | Rd, Rr   | Subtract with Carry two Registers        | $Rd \leftarrow Rd - Rr - C$                           | Z,C,N,V,H     | 1       |
| SBCI                                     | Rd, K    | Subtract with Carry Constant from Reg.   | $Rd \leftarrow Rd - K - C$                            | Z,C,N,V,H     | 1       |
| SBIW                                     | RdI,K    | Subtract Immediate from Word             | $Rdh:Rdl \leftarrow Rdh:Rdl - K$                      | Z,C,N,V,S     | 2       |
| AND                                      | Rd, Rr   | Logical AND Registers                    | $Rd \leftarrow Rd \bullet Rr$                         | Z,N,V         | 1       |
| ANDI                                     | Rd, K    | Logical AND Register and Constant        | $Rd \leftarrow Rd \bullet K$                          | Z,N,V         | 1       |
| OR                                       | Rd, Rr   | Logical OR Registers                     | $Rd \leftarrow Rd \vee Rr$                            | Z,N,V         | 1       |
| ORI                                      | Rd, K    | Logical OR Register and Constant         | $Rd \leftarrow Rd \vee K$                             | Z,N,V         | 1       |
| EOR                                      | Rd, Rr   | Exclusive OR Registers                   | $Rd \leftarrow Rd \oplus Rr$                          | Z,N,V         | 1       |
| COM                                      | Rd       | One's Complement                         | $Rd \leftarrow \$FF - Rd$                             | Z,C,N,V       | 1       |
| NEG                                      | Rd       | Two's Complement                         | $Rd \leftarrow \$00 - Rd$                             | Z,C,N,V,H     | 1       |
| SBR                                      | Rd,K     | Set Bit(s) in Register                   | $Rd \leftarrow Rd \vee K$                             | Z,N,V         | 1       |
| CBR                                      | Rd,K     | Clear Bit(s) in Register                 | $Rd \leftarrow Rd \bullet (\$FF - K)$                 | Z,N,V         | 1       |
| INC                                      | Rd       | Increment                                | $Rd \leftarrow Rd + 1$                                | Z,N,V         | 1       |
| DEC                                      | Rd       | Decrement                                | $Rd \leftarrow Rd - 1$                                | Z,N,V         | 1       |
| TST                                      | Rd       | Test for Zero or Minus                   | $Rd \leftarrow Rd \bullet Rd$                         | Z,N,V         | 1       |
| CLR                                      | Rd       | Clear Register                           | $Rd \leftarrow Rd \oplus Rd$                          | Z,N,V         | 1       |
| SER                                      | Rd       | Set Register                             | $Rd \leftarrow \$FF$                                  | None          | 1       |
| MUL                                      | Rd, Rr   | Multiply Unsigned                        | $R1:R0 \leftarrow Rd \times Rr$                       | Z,C           | 2       |
| MULS                                     | Rd, Rr   | Multiply Signed                          | $R1:R0 \leftarrow Rd \times Rr$                       | Z,C           | 2       |
| MULSU                                    | Rd, Rr   | Multiply Signed with Unsigned            | $R1:R0 \leftarrow Rd \times Rr$                       | Z,C           | 2       |
| FMUL                                     | Rd, Rr   | Fractional Multiply Unsigned             | $R1:R0 \leftarrow (Rd \times Rr) \lll 1$              | Z,C           | 2       |
| FMULS                                    | Rd, Rr   | Fractional Multiply Signed               | $R1:R0 \leftarrow (Rd \times Rr) \lll 1$              | Z,C           | 2       |
| FMULSU                                   | Rd, Rr   | Fractional Multiply Signed with Unsigned | $R1:R0 \leftarrow (Rd \times Rr) \lll 1$              | Z,C           | 2       |
| <b>BRANCH INSTRUCTIONS</b>               |          |  |   |               |         |
| RJMP                                     | k        | Relative Jump                            | $PC \leftarrow PC + k + 1$                            | None          | 2       |
| IJMP                                     |          | Indirect Jump to (Z)                     | $PC \leftarrow Z$                                     | None          | 2       |
| RCALL                                    | k        | Relative Subroutine Call                 | $PC \leftarrow PC + k + 1$                            | None          | 3       |
| ICALL                                    |          | Indirect Call to (Z)                     | $PC \leftarrow Z$                                     | None          | 3       |
| RET                                      |          | Subroutine Return                        | $PC \leftarrow STACK$                                 | None          | 4       |
| RETI                                     |          | Interrupt Return                         | $PC \leftarrow STACK$                                 | I             | 4       |
| CPSE                                     | Rd,Rr    | Compare, Skip if Equal                   | if (Rd = Rr) $PC \leftarrow PC + 2$ or 3              | None          | 1/2/3   |
| CP                                       | Rd,Rr    | Compare                                  | $Rd - Rr$   | Z, N, V, C, H | 1       |
| CPC                                      | Rd,Rr    | Compare with Carry                       | $Rd - Rr - C$   | Z, N, V, C, H | 1       |
| CPI                                      | Rd,K     | Compare Register with Immediate          | $Rd - K$  | Z, N, V, C, H | 1       |
| SBRC                                     | Rr, b    | Skip if Bit in Register Cleared          | if (Rr(b)=0) $PC \leftarrow PC + 2$ or 3              | None          | 1/2/3   |
| SBRS                                     | Rr, b    | Skip if Bit in Register is Set           | if (Rr(b)=1) $PC \leftarrow PC + 2$ or 3              | None          | 1/2/3   |
| SBIC                                     | P, b     | Skip if Bit in I/O Register Cleared      | if (P(b)=0) $PC \leftarrow PC + 2$ or 3               | None          | 1/2/3   |
| SBIS                                     | P, b     | Skip if Bit in I/O Register is Set       | if (P(b)=1) $PC \leftarrow PC + 2$ or 3               | None          | 1/2/3   |
| BRBS                                     | s, k     | Branch if Status Flag Set                | if (SREG(s) = 1) then $PC \leftarrow PC + k + 1$      | None          | 1/2     |
| BRBC                                     | s, k     | Branch if Status Flag Cleared            | if (SREG(s) = 0) then $PC \leftarrow PC + k + 1$      | None          | 1/2     |
| BREQ                                     | k        | Branch if Equal                          | if (Z = 1) then $PC \leftarrow PC + k + 1$            | None          | 1/2     |
| BRNE                                     | k        | Branch if Not Equal                      | if (Z = 0) then $PC \leftarrow PC + k + 1$            | None          | 1/2     |
| BRCS                                     | k        | Branch if Carry Set                      | if (C = 1) then $PC \leftarrow PC + k + 1$            | None          | 1/2     |
| BRCC                                     | k        | Branch if Carry Cleared                  | if (C = 0) then $PC \leftarrow PC + k + 1$            | None          | 1/2     |
| BRSH                                     | k        | Branch if Same or Higher                 | if (C = 0) then $PC \leftarrow PC + k + 1$            | None          | 1/2     |
| BRLO                                     | k        | Branch if Lower                          | if (C = 1) then $PC \leftarrow PC + k + 1$            | None          | 1/2     |
| BRMI                                     | k        | Branch if Minus                          | if (N = 1) then $PC \leftarrow PC + k + 1$            | None          | 1/2     |
| BRPL                                     | k        | Branch if Plus                           | if (N = 0) then $PC \leftarrow PC + k + 1$            | None          | 1/2     |
| BRGE                                     | k        | Branch if Greater or Equal, Signed       | if (N $\oplus$ V = 0) then $PC \leftarrow PC + k + 1$ | None          | 1/2     |
| BRLT                                     | k        | Branch if Less Than Zero, Signed         | if (N $\oplus$ V = 1) then $PC \leftarrow PC + k + 1$ | None          | 1/2     |
| BRHS                                     | k        | Branch if Half Carry Flag Set            | if (H = 1) then $PC \leftarrow PC + k + 1$            | None          | 1/2     |
| BRHC                                     | k        | Branch if Half Carry Flag Cleared        | if (H = 0) then $PC \leftarrow PC + k + 1$            | None          | 1/2     |
| BRTS                                     | k        | Branch if T Flag Set                     | if (T = 1) then $PC \leftarrow PC + k + 1$            | None          | 1/2     |
| BRTC                                     | k        | Branch if T Flag Cleared                 | if (T = 0) then $PC \leftarrow PC + k + 1$            | None          | 1/2     |
| BRVS                                     | k        | Branch if Overflow Flag is Set           | if (V = 1) then $PC \leftarrow PC + k + 1$            | None          | 1/2     |
| BRVC                                     | k        | Branch if Overflow Flag is Cleared       | if (V = 0) then $PC \leftarrow PC + k + 1$            | None          | 1/2     |
| BRIE                                     | k        | Branch if Interrupt Enabled              | if (I = 1) then $PC \leftarrow PC + k + 1$            | None          | 1/2     |
| BRID                                     | k        | Branch if Interrupt Disabled             | if (I = 0) then $PC \leftarrow PC + k + 1$            | None          | 1/2     |

| Mnemonics                            | Operands | Description                      | Operation  | Flags   | #Clocks |
|--------------------------------------|----------|----------------------------------|--|---------|---------|
| <b>DATA TRANSFER INSTRUCTIONS</b>    |          |                                  |  |         |         |
| MOV                                  | Rd, Rr   | Move Between Registers           | $Rd \leftarrow Rr$   | None    | 1       |
| MOVW                                 | Rd, Rr   | Copy Register Word               | $Rd+1:Rd \leftarrow Rr+1:Rr$                                       | None    | 1       |
| LDI                                  | Rd, K    | Load Immediate                   | $Rd \leftarrow K$  | None    | 1       |
| LD                                   | Rd, X    | Load Indirect                    | $Rd \leftarrow (X)$  | None    | 2       |
| LD                                   | Rd, X+   | Load Indirect and Post-Inc.      | $Rd \leftarrow (X), X \leftarrow X + 1$                            | None    | 2       |
| LD                                   | Rd, -X   | Load Indirect and Pre-Dec.       | $X \leftarrow X - 1, Rd \leftarrow (X)$                            | None    | 2       |
| LD                                   | Rd, Y    | Load Indirect                    | $Rd \leftarrow (Y)$  | None    | 2       |
| LD                                   | Rd, Y+   | Load Indirect and Post-Inc.      | $Rd \leftarrow (Y), Y \leftarrow Y + 1$                            | None    | 2       |
| LD                                   | Rd, -Y   | Load Indirect and Pre-Dec.       | $Y \leftarrow Y - 1, Rd \leftarrow (Y)$                            | None    | 2       |
| LDD                                  | Rd, Y+q  | Load Indirect with Displacement  | $Rd \leftarrow (Y + q)$  | None    | 2       |
| LD                                   | Rd, Z    | Load Indirect                    | $Rd \leftarrow (Z)$  | None    | 2       |
| LD                                   | Rd, Z+   | Load Indirect and Post-Inc.      | $Rd \leftarrow (Z), Z \leftarrow Z + 1$                            | None    | 2       |
| LD                                   | Rd, -Z   | Load Indirect and Pre-Dec.       | $Z \leftarrow Z - 1, Rd \leftarrow (Z)$                            | None    | 2       |
| LDD                                  | Rd, Z+q  | Load Indirect with Displacement  | $Rd \leftarrow (Z + q)$  | None    | 2       |
| LDS                                  | Rd, k    | Load Direct from SRAM            | $Rd \leftarrow (k)$  | None    | 2       |
| ST                                   | X, Rr    | Store Indirect                   | $(X) \leftarrow Rr$  | None    | 2       |
| ST                                   | X+, Rr   | Store Indirect and Post-Inc.     | $(X) \leftarrow Rr, X \leftarrow X + 1$                            | None    | 2       |
| ST                                   | -X, Rr   | Store Indirect and Pre-Dec.      | $X \leftarrow X - 1, (X) \leftarrow Rr$                            | None    | 2       |
| ST                                   | Y, Rr    | Store Indirect                   | $(Y) \leftarrow Rr$  | None    | 2       |
| ST                                   | Y+, Rr   | Store Indirect and Post-Inc.     | $(Y) \leftarrow Rr, Y \leftarrow Y + 1$                            | None    | 2       |
| ST                                   | -Y, Rr   | Store Indirect and Pre-Dec.      | $Y \leftarrow Y - 1, (Y) \leftarrow Rr$                            | None    | 2       |
| STD                                  | Y+q, Rr  | Store Indirect with Displacement | $(Y + q) \leftarrow Rr$  | None    | 2       |
| ST                                   | Z, Rr    | Store Indirect                   | $(Z) \leftarrow Rr$  | None    | 2       |
| ST                                   | Z+, Rr   | Store Indirect and Post-Inc.     | $(Z) \leftarrow Rr, Z \leftarrow Z + 1$                            | None    | 2       |
| ST                                   | -Z, Rr   | Store Indirect and Pre-Dec.      | $Z \leftarrow Z - 1, (Z) \leftarrow Rr$                            | None    | 2       |
| STD                                  | Z+q, Rr  | Store Indirect with Displacement | $(Z + q) \leftarrow Rr$  | None    | 2       |
| STS                                  | k, Rr    | Store Direct to SRAM             | $(k) \leftarrow Rr$  | None    | 2       |
| LPM                                  |          | Load Program memory              | $R0 \leftarrow (Z)$  | None    | 3       |
| LPM                                  | Rd, Z    | Load Program memory              | $Rd \leftarrow (Z)$  | None    | 3       |
| LPM                                  | Rd, Z+   | Load Program memory and Post-Inc | $Rd \leftarrow (Z), Z \leftarrow Z + 1$                            | None    | 3       |
| SPM                                  |          | Store Program memory             | $(Z) \leftarrow R1:R0$   | None    | -       |
| IN                                   | Rd, P    | In Port                          | $Rd \leftarrow P$  | None    | 1       |
| OUT                                  | P, Rr    | Out Port                         | $P \leftarrow Rr$  | None    | 1       |
| PUSH                                 | Rr       | Push Register on Stack           | $STACK \leftarrow Rr$  | None    | 2       |
| POP                                  | Rd       | Pop Register from Stack          | $Rd \leftarrow STACK$  | None    | 2       |
| <b>BIT AND BIT-TEST INSTRUCTIONS</b> |          |                                  |  |         |         |
| SBI                                  | P.b      | Set Bit in I/O Register          | $I/O(P,b) \leftarrow 1$  | None    | 2       |
| CBI                                  | P.b      | Clear Bit in I/O Register        | $I/O(P,b) \leftarrow 0$  | None    | 2       |
| LSL                                  | Rd       | Logical Shift Left               | $Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$                     | Z,C,N,V | 1       |
| LSR                                  | Rd       | Logical Shift Right              | $Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$                     | Z,C,N,V | 1       |
| ROL                                  | Rd       | Rotate Left Through Carry        | $Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$ | Z,C,N,V | 1       |
| ROR                                  | Rd       | Rotate Right Through Carry       | $Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$ | Z,C,N,V | 1       |
| ASR                                  | Rd       | Arithmetic Shift Right           | $Rd(n) \leftarrow Rd(n+1), n=0..6$                                 | Z,C,N,V | 1       |
| SWAP                                 | Rd       | Swap Nibbles                     | $Rd(3..0) \leftarrow Rd(7..4), Rd(7..4) \leftarrow Rd(3..0)$       | None    | 1       |
| BSET                                 | s        | Flag Set                         | $SREG(s) \leftarrow 1$   | SREG(s) | 1       |
| BCLR                                 | s        | Flag Clear                       | $SREG(s) \leftarrow 0$   | SREG(s) | 1       |
| BST                                  | Rr, b    | Bit Store from Register to T     | $T \leftarrow Rr(b)$   | T       | 1       |
| BLD                                  | Rd, b    | Bit load from T to Register      | $Rd(b) \leftarrow T$   | None    | 1       |
| SEC                                  |          | Set Carry                        | $C \leftarrow 1$   | C       | 1       |
| CLC                                  |          | Clear Carry                      | $C \leftarrow 0$   | C       | 1       |
| SEN                                  |          | Set Negative Flag                | $N \leftarrow 1$   | N       | 1       |
| CLN                                  |          | Clear Negative Flag              | $N \leftarrow 0$   | N       | 1       |
| SEZ                                  |          | Set Zero Flag                    | $Z \leftarrow 1$   | Z       | 1       |
| CLZ                                  |          | Clear Zero Flag                  | $Z \leftarrow 0$   | Z       | 1       |
| SEI                                  |          | Global Interrupt Enable          | $I \leftarrow 1$   | I       | 1       |
| CLI                                  |          | Global Interrupt Disable         | $I \leftarrow 0$   | I       | 1       |
| SES                                  |          | Set Signed Test Flag             | $S \leftarrow 1$   | S       | 1       |
| CLS                                  |          | Clear Signed Test Flag           | $S \leftarrow 0$   | S       | 1       |
| SEV                                  |          | Set Twos Complement Overflow.    | $V \leftarrow 1$   | V       | 1       |
| CLV                                  |          | Clear Twos Complement Overflow   | $V \leftarrow 0$   | V       | 1       |
| SET                                  |          | Set T in SREG                    | $T \leftarrow 1$   | T       | 1       |
| CLT                                  |          | Clear T in SREG                  | $T \leftarrow 0$   | T       | 1       |
| SEH                                  |          | Set Half Carry Flag in SREG      | $H \leftarrow 1$   | H       | 1       |
| CLH                                  |          | Clear Half Carry Flag in SREG    | $H \leftarrow 0$   | H       | 1       |
| <b>MCU CONTROL INSTRUCTIONS</b>      |          |                                  |  |         |         |



| Mnemonics | Operands | Description    | Operation                                | Flags | #Clocks |
|-----------|----------|----------------|--|-------|---------|
| NOP       |          | No Operation   |  | None  | 1       |
| SLEEP     |          | Sleep          | (see specific descr. for Sleep function) | None  | 1       |
| WDR       |          | Watchdog Reset | (see specific descr. for WDR/timer)      | None  | 1       |



## Ordering Information

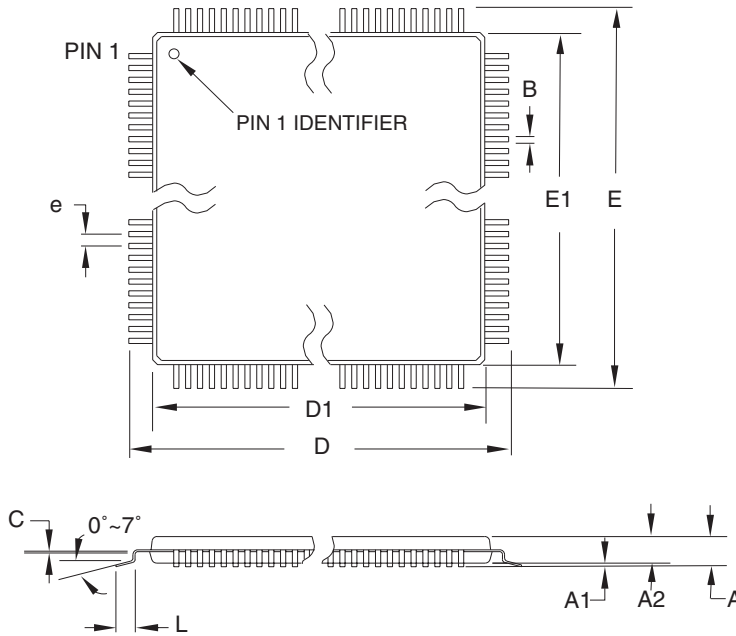
| Speed (MHz)                    | Power Supply                   | Ordering Code                  | Package <sup>(1)</sup> | Operation Range             |                               |
|--------------------------------|--------------------------------|--------------------------------|------------------------|-----------------------------|-------------------------------|
| 8                              | 2.7 - 5.5V                     | ATmega8515L-8AC                | 44A                    | Commercial<br>(0°C to 70°C) |                               |
|                                |                                | ATmega8515L-8PC                | 40P6                   |                             |                               |
|                                |                                | ATmega8515L-8JC                | 44J                    |                             |                               |
|                                |                                | ATmega8515L-8MC <sup>(2)</sup> | 44M1                   |                             |                               |
|                                |                                | ATmega8515L-8AI                | 44A                    |                             | Industrial<br>(-40°C to 85°C) |
|                                |                                | ATmega8515L-8PI                | 40P6                   |                             |                               |
|                                |                                | ATmega8515L-8JI                | 44J                    |                             |                               |
|                                |                                | ATmega8515L-8MI                | 44M1                   |                             |                               |
|                                | ATmega8515L-8AU <sup>(2)</sup> | 44A                            |                        |                             |                               |
|                                | ATmega8515L-8JU <sup>(2)</sup> | 44J                            |                        |                             |                               |
|                                | ATmega8515L-8MU <sup>(2)</sup> | 44M1                           |                        |                             |                               |
|                                | 16                             | 4.5 - 5.5V                     | ATmega8515-16AC        | 44A                         | Commercial<br>(0°C to 70°C)   |
|                                |                                |                                | ATmega8515-16PC        | 40P6                        |                               |
|                                |                                |                                | ATmega8515-16JC        | 44J                         |                               |
| ATmega8515-16MC                |                                |                                | 44M1                   |                             |                               |
| Industrial<br>(-40°C to 85°C)  |                                | ATmega8515-16AI                | 44A                    |                             |                               |
|                                |                                | ATmega8515-16PI                | 40P6                   |                             |                               |
|                                |                                | ATmega8515-16JI                | 44J                    |                             |                               |
|                                |                                | ATmega8515-16MI                | 44M1                   |                             |                               |
|                                |                                | ATmega8515-16AU <sup>(2)</sup> | 44A                    |                             |                               |
|                                |                                | ATmega8515-16JU <sup>(2)</sup> | 44J                    |                             |                               |
| ATmega8515-16MU <sup>(2)</sup> | 44MI                           |                                |                        |                             |                               |

- Note:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities..
  2. Pb-free packaging alternative, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

| Package Type |   |
|--------------|---|
| <b>44A</b>   | 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)                                     |
| <b>40P6</b>  | 40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)  |
| <b>44J</b>   | 44-lead, Plastic J-Leaded Chip Carrier (PLCC)   |
| <b>44M1</b>  | 44-pad, 7 x 7 x 1.0 mm body, lead pitch 0.50 mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF) |

# Packaging Information

44A



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

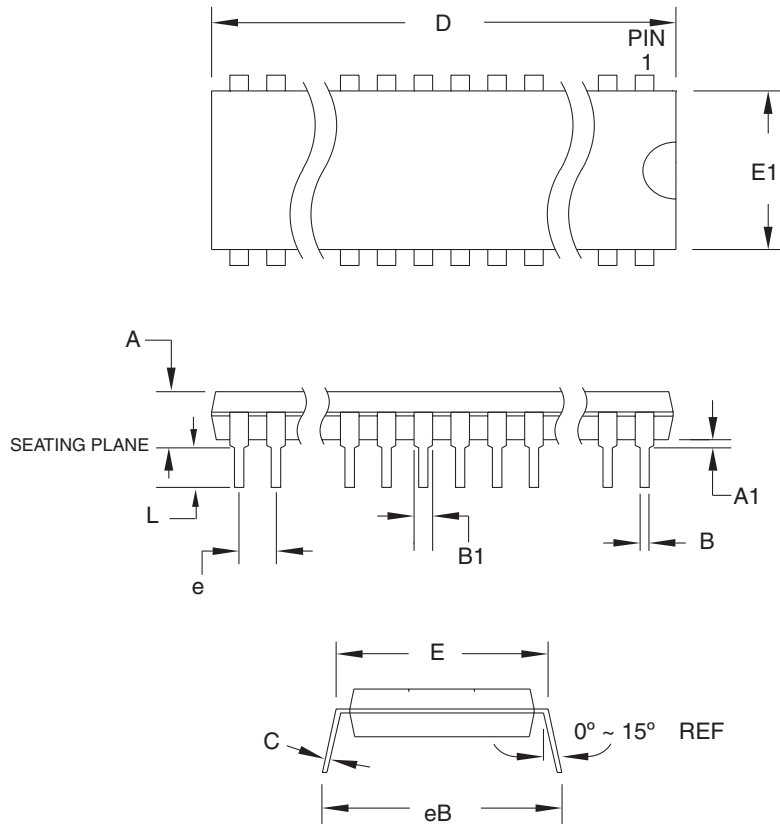
| SYMBOL | MIN      | NOM   | MAX   | NOTE   |
|--------|----------|-------|-------|--------|
| A      | -        | -     | 1.20  |        |
| A1     | 0.05     | -     | 0.15  |        |
| A2     | 0.95     | 1.00  | 1.05  |        |
| D      | 11.75    | 12.00 | 12.25 |        |
| D1     | 9.90     | 10.00 | 10.10 | Note 2 |
| E      | 11.75    | 12.00 | 12.25 |        |
| E1     | 9.90     | 10.00 | 10.10 | Note 2 |
| B      | 0.30     | -     | 0.45  |        |
| C      | 0.09     | -     | 0.20  |        |
| L      | 0.45     | -     | 0.75  |        |
| e      | 0.80 TYP |       |       |        |

- Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
  3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

|  |  |                    |             |
|--|--|--------------------|-------------|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | <b>TITLE</b>   | <b>DRAWING NO.</b> | <b>REV.</b> |
|  | <b>44A</b> , 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness,<br>0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP) | 44A                | B           |

40P6



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

| SYMBOL | MIN       | NOM | MAX    | NOTE   |
|--------|-----------|-----|--------|--------|
| A      | –         | –   | 4.826  |        |
| A1     | 0.381     | –   | –      |        |
| D      | 52.070    | –   | 52.578 | Note 2 |
| E      | 15.240    | –   | 15.875 |        |
| E1     | 13.462    | –   | 13.970 | Note 2 |
| B      | 0.356     | –   | 0.559  |        |
| B1     | 1.041     | –   | 1.651  |        |
| L      | 3.048     | –   | 3.556  |        |
| C      | 0.203     | –   | 0.381  |        |
| eB     | 15.494    | –   | 17.526 |        |
| e      | 2.540 TYP |     |        |        |

- Notes: 1. This package conforms to JEDEC reference MS-011, Variation AC.  
2. Dimensions D and E1 do not include mold Flash or Protrusion.  
Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01



2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**

**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual  
Inline Package (PDIP)

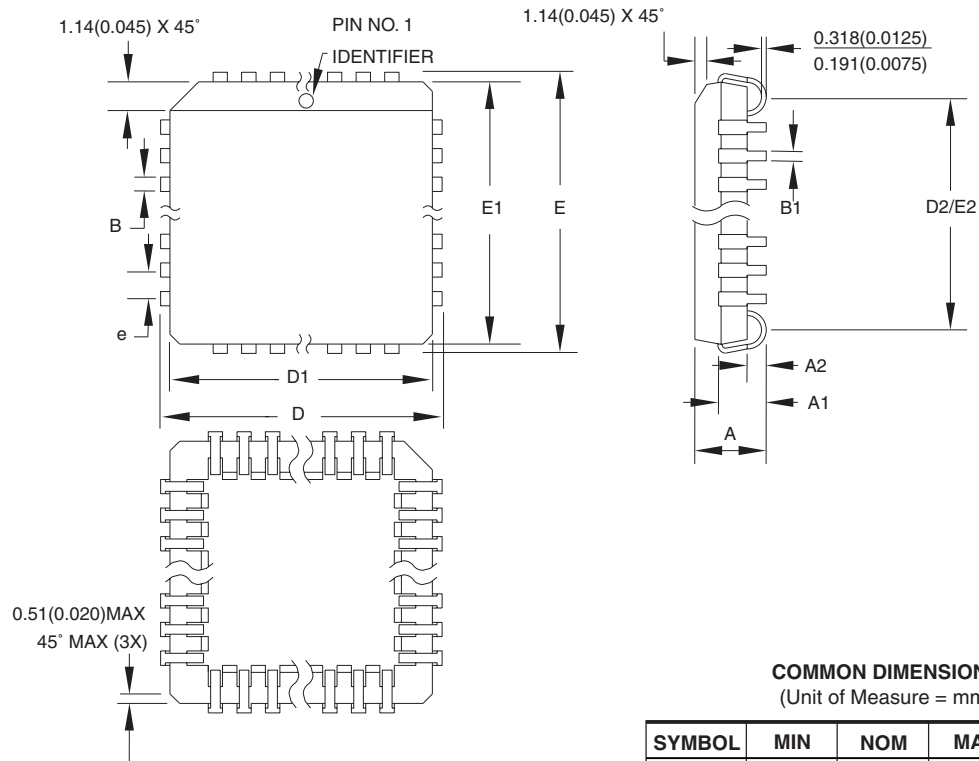
**DRAWING NO.**

40P6

**REV.**

B





**COMMON DIMENSIONS**  
(Unit of Measure = mm)

| SYMBOL | MIN       | NOM | MAX    | NOTE   |
|--------|-----------|-----|--------|--------|
| A      | 4.191     | -   | 4.572  |        |
| A1     | 2.286     | -   | 3.048  |        |
| A2     | 0.508     | -   | -      |        |
| D      | 17.399    | -   | 17.653 |        |
| D1     | 16.510    | -   | 16.662 | Note 2 |
| E      | 17.399    | -   | 17.653 |        |
| E1     | 16.510    | -   | 16.662 | Note 2 |
| D2/E2  | 14.986    | -   | 16.002 |        |
| B      | 0.660     | -   | 0.813  |        |
| B1     | 0.330     | -   | 0.533  |        |
| e      | 1.270 TYP |     |        |        |

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
  3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



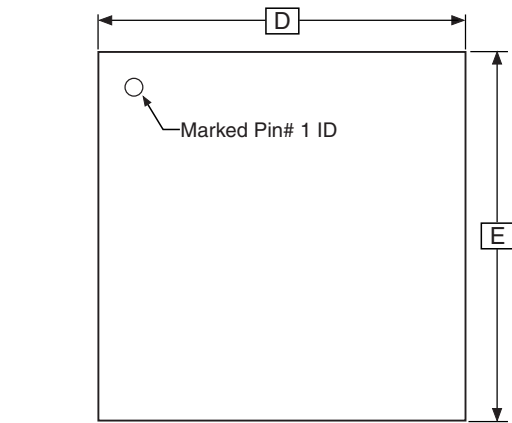
2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**  
**44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)**

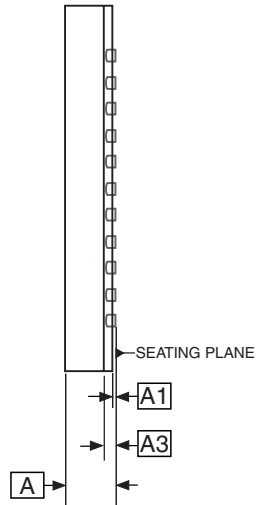
**DRAWING NO.**  
44J

**REV.**  
B

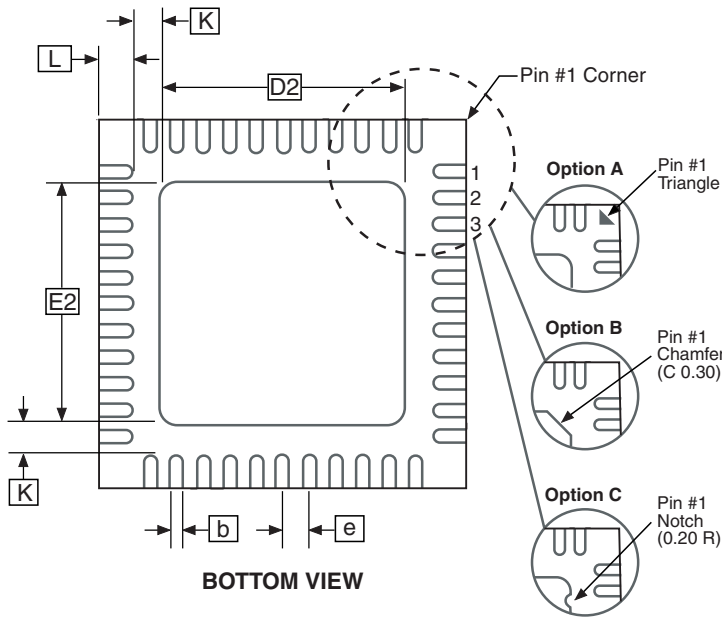
44M1



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS  
(Unit of Measure = mm)

| SYMBOL | MIN      | NOM  | MAX  | NOTE |
|--------|----------|------|------|------|
| A      | 0.80     | 0.90 | 1.00 |      |
| A1     | —        | 0.02 | 0.05 |      |
| A3     | 0.25 REF |      |      |      |
| b      | 0.18     | 0.23 | 0.30 |      |
| D      | 6.90     | 7.00 | 7.10 |      |
| D2     | 5.00     | 5.20 | 5.40 |      |
| E      | 6.90     | 7.00 | 7.10 |      |
| E2     | 5.00     | 5.20 | 5.40 |      |
| e      | 0.50 BSC |      |      |      |
| L      | 0.59     | 0.64 | 0.69 |      |
| K      | 0.20     | 0.26 | 0.41 |      |

Note: JEDEC Standard MO-220, Fig. 1 (SAW Singulation) VKKD-3.

5/27/06

**ATMEL** 2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**  
44M1, 44-pad, 7 x 7 x 1.0 mm Body, Lead Pitch 0.50 mm,  
5.20 mm Exposed Pad, Micro Lead Frame Package (MLF)

**DRAWING NO.**  
44M1

**REV.**  
G

## Errata

The revision letter in this section refers to the revision of the ATmega8515 device.

### ATmega8515(L) Rev. C and D

#### 1. **First Analog Comparator conversion may be delayed**

If the device is powered by a slow rising VCC, the first Analog Comparator conversion will take longer than expected on some devices.

##### **Problem Fix/Workaround**

When the device has been powered or reset, disable then enable the Analog Comparator before the first conversion.

**Datasheet Revision History**

Please note that the referring page numbers in this section are referring to this document. The referring revision in this section are referring to the document revision.

**Rev. 2512J-10/06**

1. Updated TOP/BOTTOM description for all Timer/Counters Fast PWM mode.
2. Updated “Errata” on page 18.

**Rev. 2512I-08/06**

1. Updated “Ordering Information” on page 13.

**Rev. 2512H-04/06**

1. Added “Resources” on page 6.
2. Updated cross reference in “Phase Correct PWM Mode” on page 113.
3. Updated “Timer/Counter Interrupt Mask Register – TIMSK(1)” on page 124.
4. Updated “Serial Peripheral Interface – SPI” on page 126.
5. Removed obsolete section of “Calibration Byte” on page 181.
6. Updated Table 10 on page 38, Table 52 on page 120, Table 94 on page 196 and Table 96 on page 199.

**Rev. 2512G-03/05**

1. MLF-package alternative changed to “Quad Flat No-Lead/Micro Lead Frame Package QFN/MLF”.
2. Updated “Electrical Characteristics” on page 197
3. Updated “Ordering Information” on page 13.

**Rev. 2512E-09/03**

1. Updated “Calibrated Internal RC Oscillator” on page 39.

**Rev. 2512E-09/03**

1. Removed “Preliminary” from the datasheet.
2. Updated Table 18 on page 46 and “Absolute Maximum Ratings” and “DC Characteristics” in “Electrical Characteristics” on page 197.
3. Updated chapter “ATmega8515 Typical Characteristics” on page 207.

**Rev. 2512D-02/03**

1. Added “EEPROM Write During Power-down Sleep Mode” on page 23.
2. Improved the description in “Phase Correct PWM Mode” on page 88.
3. Corrected OCn waveforms in Figure 53 on page 111.
4. Added note under “Filling the Temporary Buffer (page loading)” on page 173 about writing to the EEPROM during an SPM page load.
5. Updated Table 93 on page 195.
6. Updated “Packaging Information” on page 14.

**Rev. 2512C-10/02**

1. Added “Using all Locations of External Memory Smaller than 64 KB” on page 31.
2. Removed all TBD.
3. Added description about calibration values for 2, 4, and 8 MHz.
4. Added variation in frequency of “External Clock” on page 40.
5. Added note about  $V_{BOT}$ , Table 18 on page 46.
6. Updated about “Unconnected pins” on page 64.
7. Updated “16-bit Timer/Counter1” on page 97, Table 51 on page 119 and Table 52 on page 120.
8. Updated “Enter Programming Mode” on page 184, “Chip Erase” on page 184, Figure 77 on page 187, and Figure 78 on page 188.
9. Updated “Electrical Characteristics” on page 197, “External Clock Drive” on page 199, Table 96 on page 199 and Table 97 on page 200, “SPI Timing Characteristics” on page 200 and Table 98 on page 202.
10. Added “Errata” on page 18.

**Rev. 2512B-09/02**

1. Changed the Endurance on the Flash to 10,000 Write/Erase Cycles.

**Rev. 2512A-04/02**

1. Initial.



## Atmel Corporation

2325 Orchard Parkway  
San Jose, CA 95131, USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 487-2600

## Regional Headquarters

### Europe

Atmel Sarl  
Route des Arsenalux 41  
Case Postale 80  
CH-1705 Fribourg  
Switzerland  
Tel: (41) 26-426-5555  
Fax: (41) 26-426-5500

### Asia

Room 1219  
Chinachem Golden Plaza  
77 Mody Road Tsimshatsui  
East Kowloon  
Hong Kong  
Tel: (852) 2721-9778  
Fax: (852) 2722-1369

### Japan

9F, Tonetsu Shinkawa Bldg.  
1-24-8 Shinkawa  
Chuo-ku, Tokyo 104-0033  
Japan  
Tel: (81) 3-3523-3551  
Fax: (81) 3-3523-7581

## Atmel Operations

### Memory

2325 Orchard Parkway  
San Jose, CA 95131, USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 436-4314

### Microcontrollers

2325 Orchard Parkway  
San Jose, CA 95131, USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 436-4314

La Chantrerie  
BP 70602  
44306 Nantes Cedex 3, France  
Tel: (33) 2-40-18-18-18  
Fax: (33) 2-40-18-19-60

### ASIC/ASSP/Smart Cards

Zone Industrielle  
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Tel: (33) 4-42-53-60-00  
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.  
Colorado Springs, CO 80906, USA  
Tel: 1(719) 576-3300  
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park  
Maxwell Building  
East Kilbride G75 0QR, Scotland  
Tel: (44) 1355-803-000  
Fax: (44) 1355-242-743

### RF/Automotive

Theresienstrasse 2  
Postfach 3535  
74025 Heilbronn, Germany  
Tel: (49) 71-31-67-0  
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.  
Colorado Springs, CO 80906, USA  
Tel: 1(719) 576-3300  
Fax: 1(719) 540-1759

### Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom

Avenue de Rochepleine  
BP 123  
38521 Saint-Egreve Cedex, France  
Tel: (33) 4-76-58-30-00  
Fax: (33) 4-76-58-34-80

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