

DS90LV011AQ Automotive LVDS Differential Driver

Check for Samples: [DS90LV011AQ](#)

FEATURES

- AECQ-100 Grade 1
- Conforms to TIA/EIA-644-A Standard
- >400Mbps (200MHz) Switching Rates
- 700 ps (100 ps typical) Maximum Differential Skew
- 1.5 ns Maximum Propagation Delay
- Single 3.3V Power Supply
- ± 350 mV Differential Signaling
- Power Off Protection (Outputs in TRI-STATE)
- Pinout Simplifies PCB Layout
- Low Power Dissipation (23 mW @ 3.3V Typical)
- SOT-23 5-Lead Package
- Pin Compatible with SN65LVDS1

DESCRIPTION

The DS90LV011AQ is an LVDS driver optimized for high data rate and low power applications. The DS90LV011AQ is a current mode driver allowing power dissipation to remain low even at high frequency. In addition, the short circuit fault current is also minimized. The device is designed to support data rates in excess of 400Mbps (200MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The device is offered in a 5-lead SOT-23 package. The LVDS outputs have been arranged for easy PCB layout. The differential driver outputs provide low EMI with its typical low output swing of 350 mV. The DS90LV011AQ can be paired with its companion single line receiver, the DS90LT012AQ, or with any of TI's LVDS receivers, to provide a high-speed LVDS interface.

Connection Diagram

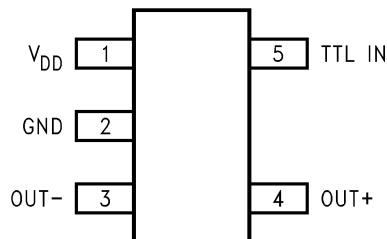
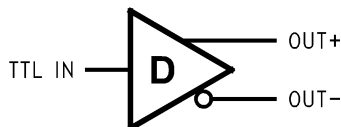


Figure 1. Top View
See Package Number MF05A

Functional Diagram



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾⁽²⁾

Supply Voltage (V_{DD})	-0.3V to 4.0V
LVCMOS input voltage (TTL IN)	-0.3V to to ($V_{DD} + 0.3V$)
LVDS output voltage (OUT_{\pm})	-0.3V to +3.9V
LVDS output short circuit current	24mA
Maximum Package Power Dissipation @ +25°C	
DBV Package	794 mW
Derate DBV Package	7.22 mW/°C above +25°C
Package Thermal Resistance (4-Layer, 2 oz. Cu, JEDEC)	
θ_{JA}	138.5°C/Watt
θ_{JC}	107.0°C/Watt
Storage Temperature	-65°C to +150°C
Lead Temperature Range Soldering	
(4 sec.)	+260°C
Maximum Junction Temperature	+135°C
ESD Ratings	
HBM ⁽³⁾	≥ 8kV
MM ⁽⁴⁾	≥ 250V
CDM ⁽⁵⁾	≥ 1250V

- (1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. Electrical Characteristics specifies conditions of device operation.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) Human Body Model, applicable std. JESD22-A114C
- (4) Machine Model, applicable std. JESD22-A115-A
- (5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{DD})	3.0	3.3	3.6	V
Temperature (T_A)	-40	+25	+125	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. ⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
$ V_{OD} $	Output Differential Voltage	$R_L = 100\Omega$ (Figure 2 and Figure 3)	OUT+, OUT-	250	350	450	mV
ΔV_{OD}	V_{OD} Magnitude Change				3	35	mV
V_{OS}	Offset Voltage	$R_L = 100\Omega$ (Figure 2)		1.125	1.22	1.375	V
ΔV_{OS}	Offset Magnitude Change			0	1	25	mV
I_{OFF}	Power-off Leakage	$V_{OUT} = 3.6V$ or GND, $V_{DD} = 0V$			±1	±10	µA
I_{OS}	Output Short Circuit Current ⁽⁴⁾	V_{OUT+} and $V_{OUT-} = 0V$			-6	-24	mA
I_{OSD}	Differential Output Short Circuit Current ⁽⁴⁾	$V_{OD} = 0V$			-5	-12	mA
C_{OUT}	Output Capacitance				3		pF

- (1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} .
- (2) All typicals are given for: $V_{DD} = +3.3V$ and $T_A = +25°C$.
- (3) The DS90LV011AQ is a current mode device and only function with datasheet specification when a resistive load is applied to the drivers outputs.
- (4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

Electrical Characteristics (continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. ⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units	
V _{IH}	Input High Voltage			TTL IN	2.0		V _{DD}	V	
V _{IL}	Input Low Voltage				GND		0.8	V	
I _{IH}	Input High Current	V _{IN} = 3.3V or 2.4V					±2	±10	µA
I _{IL}	Input Low Current	V _{IN} = GND or 0.5V					±1	±10	µA
V _{CL}	Input Clamp Voltage	I _{CL} = -18 mA				-1.5	-0.6		V
C _{IN}	Input Capacitance						3		pF
I _{DD}	Power Supply Current	No Load	V _{IN} = V _{DD} or GND	V _{DD}		5	8	mA	
		R _L = 100Ω				7	10	mA	

Switching Characteristics

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified. ⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t _{PHLD}	Differential Propagation Delay High to Low	R _L = 100Ω, C _L = 15 pF (Figure 4 and Figure 5)	0.3	1.0	1.5	ns
t _{PLHD}	Differential Propagation Delay Low to High		0.3	1.1	1.5	ns
t _{SKD1}	Differential Pulse Skew t _{PHLD} - t _{PLHD} ⁽⁵⁾		0	0.1	0.7	ns
t _{SKD3}	Differential Part to Part Skew ⁽⁶⁾		0	0.2	1.0	ns
t _{SKD4}	Differential Part to Part Skew ⁽⁷⁾		0	0.4	1.2	ns
t _{TLH}	Transition Low to High Time		0.2	0.5	1.0	ns
t _{THL}	Transition High to Low Time		0.2	0.5	1.0	ns
f _{MAX}	Maximum Operating Frequency ⁽⁸⁾				250	

- (1) All typicals are given for: V_{DD} = +3.3V and T_A = +25°C.
- (2) These parameters are ensured by design. The limits are based on statistical analysis of the device performance over PVT (process, voltage, temperature) ranges.
- (3) C_L includes probe and fixture capacitance.
- (4) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r ≤ 1 ns, t_f ≤ 1 ns (10%-90%).
- (5) t_{SKD1}, |t_{PHLD} - t_{PLHD}|, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
- (6) t_{SKD3}, Differential Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{DD} and within 5°C of each other within the operating temperature range.
- (7) t_{SKD4}, part to part skew, is the differential channel to channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max - Min| differential propagation delay.
- (8) f_{MAX} generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, 0V to 3V. Output criteria: duty cycle = 45%/55%, V_{OD} > 250mV.

Parameter Measurement Information

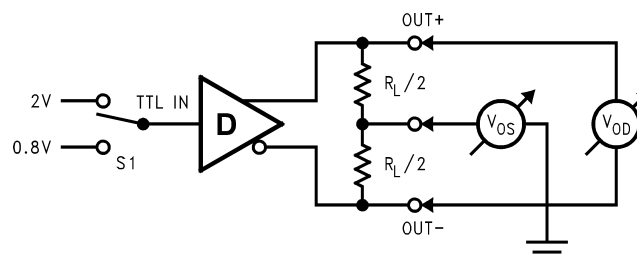


Figure 2. Differential Driver DC Test Circuit

Parameter Measurement Information (continued)

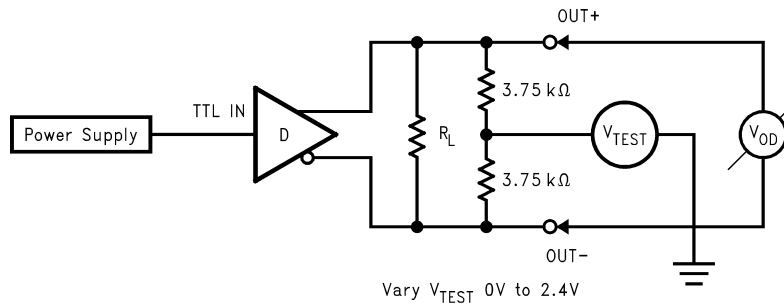


Figure 3. Differential Driver Full Load DC Test Circuit

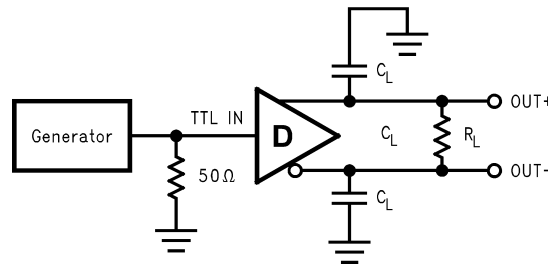


Figure 4. Differential Driver Propagation Delay and Transition Time Test Circuit

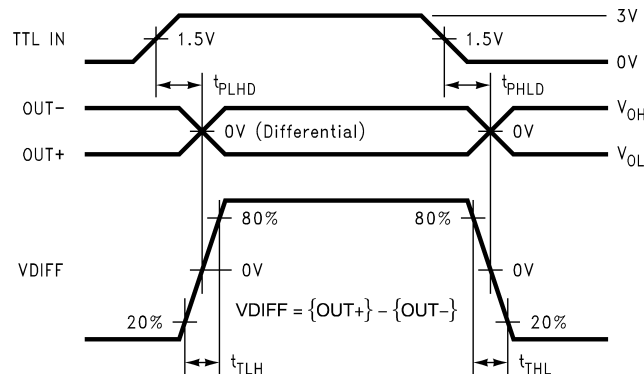


Figure 5. Differential Driver Propagation Delay and Transition Time Waveforms

APPLICATION INFORMATION

DEVICE PIN DESCRIPTIONS

Package Pin Number	Pin Name	Description
SOT-23		
5	TTL IN	LVTTTL/LVCMOS driver input pins
4	OUT+	Non-inverting driver output pin
3	OUT-	Inverting driver output pin
2	GND	Ground pin
1	V _{DD}	Power supply pin, +3.3V ± 0.3V

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
<hr/> <ul style="list-style-type: none">• Changed layout of National Data Sheet to TI format <hr/>	<hr/> 4 <hr/>

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90LV011AQMFB/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	N01Q	Samples
DS90LV011AQMFE/NOPB	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	N01Q	Samples
DS90LV011AQMFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	N01Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV011AQM/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
DS90LV011AQMFE/NOPB	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
DS90LV011AQMFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

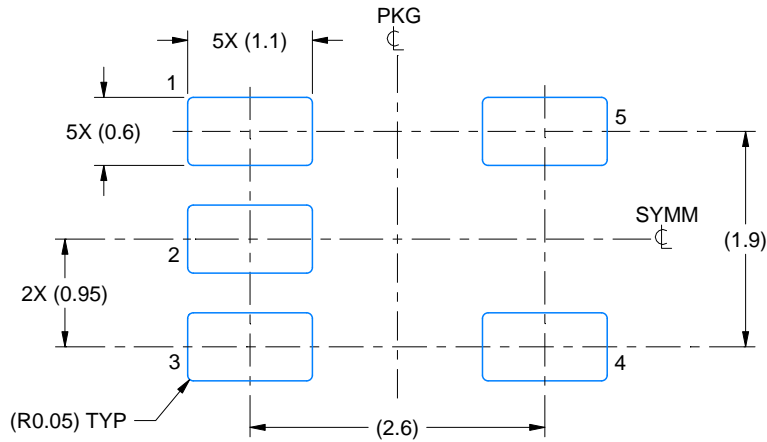
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV011AQMF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
DS90LV011AQMFE/NOPB	SOT-23	DBV	5	250	210.0	185.0	35.0
DS90LV011AQMFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

EXAMPLE BOARD LAYOUT

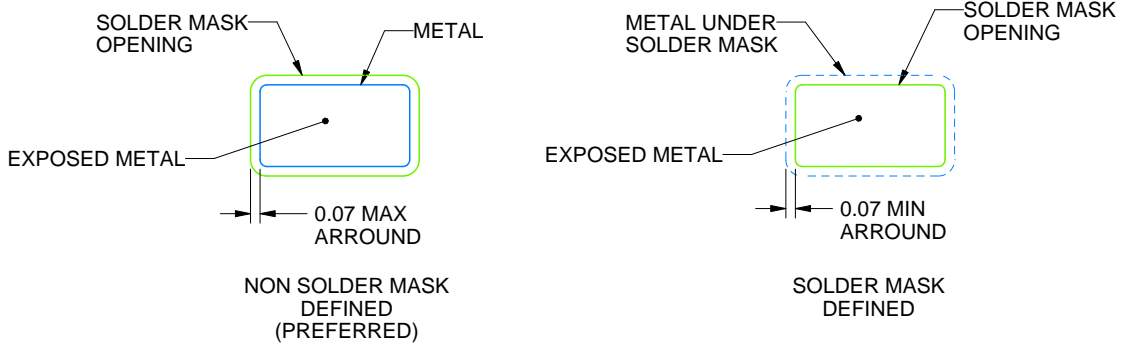
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

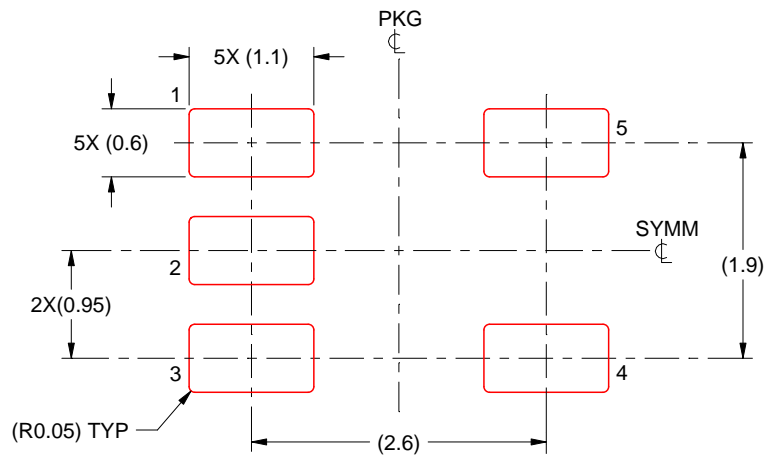
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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