THE DATASHEET OF

DS8024-RJX+T&R

DS8024

Smart Card Interface

General Description

The DS8024 smart card interface IC is a low-cost, analog front-end for a smart card reader, designed for all ISO 7816, EMV®, and GSM11-11 applications. The DS8024 is a pin-for-pin drop-in replacement for the NXP TDA8024 and is offered in 28-pin TSSOP and SO packages.

Applications requiring support for 1.8V smart cards or requiring low power should consider the DS8113, which achieves lower active- and stop-mode power with minimal changes to application hardware and software.

Applications

Set-Top Box Conditional Access
Access Control
Banking Applications
POS Terminals
Debit/Credit Payment Terminals
PIN Pads
Automated Teller Machines
Telecommunications
Pay/Premium Television

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS8024-RJX+	-40°C to +85°C	28 TSSOP
DS8024-RJX/V+	-40°C to +85°C	28 TSSOP
DS8024-RRX+	-40°C to +85°C	28 SO

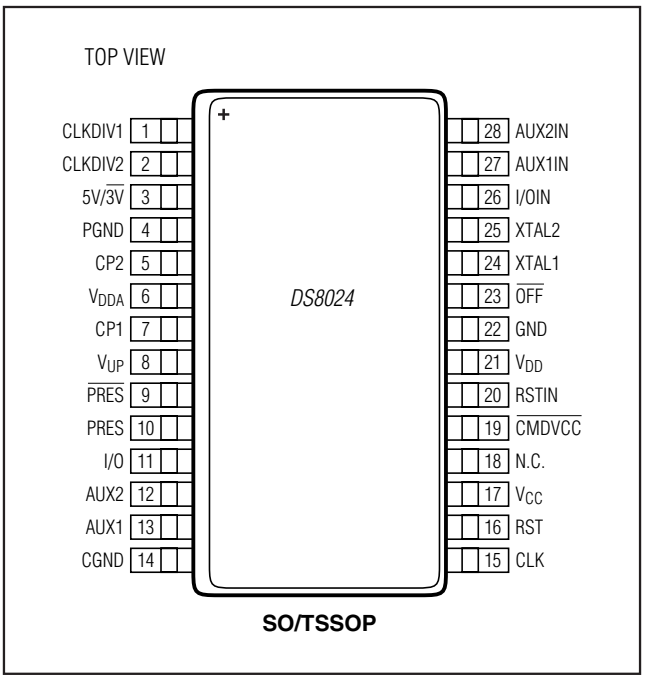
Note: *Contact the factory for availability of other variants and package options.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive-qualified part.

Selector Guide appears at end of data sheet.

Features

- **Analog Interface and Level Shifting for IC Card Communication**
- **±8kV (min) ESD (IEC) Protection on Card Interfaces**
- **Internal IC Card Supply-Voltage Generation:**
  5.0V ±5%, 80mA (max)
  3.0V ±8%, 65mA (max)
- **Automatic Card Activation and Deactivation Controlled by Dedicated Internal Sequencer**
- **I/O Lines from Host Directly Level Shifted for Smart Card Communication**
- **Flexible Card Clock Generation, Supporting External Crystal Frequency Divided by 1, 2, 4, or 8**
- **High-Current, Short-Circuit and High-Temperature Protection**

Pin Configuration



EMV is a registered trademark of EMVCo LLC. EMV Level 1 library and hardware reference design available. Contact factory for details.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to:* ***www.maximintegrated.com/errata****.*

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-6220; Rev 4; 4/13

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{DD} Relative to GND .....-0.5V to +6.5V
Voltage Range on V_{DDA} Relative to PGND .....-0.5V to +6.5V
Voltage Range on CP1, CP2, and V_{UP}
Relative to PGND.....-0.5V to +7.5V
Voltage Range on All Other Pins
Relative to GND.....-0.5V to (V_{DD} + 0.5V)
Maximum Junction Temperature .....+125°C

Continuous Power Dissipation (multilayer board, T_A = +70°C)
TSSOP (derate 14mW/°C above +70°C) 1117.3mW
SO (derate 16.7mW/°C above +70°C).....1355.9mW
Storage Temperature Range .....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(V_{DD} = +3.3V, V_{DDA} = +5.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Digital Supply Voltage	V_{DD}		2.7		6.0	V
Card Voltage-Generator Supply Voltage	V_{DDA}	V_{CC} = 5V, $\|I_{CC}\|$ < 80mA	4.0		6.0	V
		V_{CC} = 5V, $\|I_{CC}\|$ < 30mA	3.0		6.0	
Reset Voltage Thresholds	V_{TH2}	Threshold voltage (falling)	2.30	2.45	2.60	V
	V_{HYS2}	Hysteresis	50	100	150	mV
CURRENT CONSUMPTION						
Active V_{DD} Current 5V Cards (Including 80mA Draw from 5V Card)	I_{DD_50V}	I_{CC} = 80mA, f_{XTAL} = 20MHz, f_{CLK} = 10MHz, V_{DDA} = 5.0V			215	mA
Active V_{DD} Current 5V Cards (Current Consumed by DS8024 Only)	I_{DD_IC}	I_{CC} = 80mA, f_{XTAL} = 20MHz, f_{CLK} = 10MHz, V_{DDA} = 5.0V (Note 2)			135	mA
Active V_{DD} Current 3V Cards (Including 65mA Draw from 3V Card)	I_{DD_30V}	I_{CC} = 65mA, f_{XTAL} = 20MHz, f_{CLK} = 10MHz, V_{DDA} = 5.0V			100	mA
Active V_{DD} Current 3V Cards (Current Consumed by DS8024 Only)	I_{DD_IC}	I_{CC} = 65mA, f_{XTAL} = 20MHz, f_{CLK} = 10MHz, V_{DDA} = 5.0V (Note 2)			35	mA
Inactive-Mode Current	I_{DD}	Card inactive			500	µA
CLOCK SOURCE						
Crystal Frequency	f_{XTAL}	External crystal	0		20	MHz
XTAL1 Operating Conditions	f_{XTAL1}		0		20	MHz
	V_{IL_XTAL1}	Low-level input on XTAL1 (Note 3)	-0.3		0.3 x V_{DD}	V
	V_{IH_XTAL1}	High-level input on XTAL1 (Note 3)	0.7 x V_{DD}		V_{DD} + 0.3	
External Capacitance for Crystal	C_{XTAL1}, C_{XTAL2}	(Note 3)			15	pF
Internal Oscillator	f_{INT}			2.7		MHz
SHUTDOWN TEMPERATURE						
Shutdown Temperature	T_{SD}	(Note 3)		+150		°C

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DD} = +3.3V, V_{DDA} = +5.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RST PIN							
Card-Inactive Mode	Output Low Voltage	V_{OL_RST1}	I_{OL_RST} = 1mA	0		0.3	V
	Output Current	I_{OL_RST1}	V_{O_LRST} = 0V	0		-1	mA
Card-Active Mode	Output Low Voltage	V_{OL_RST2}	I_{OL_RST} = 200µA	0		0.3	V
	Output High Voltage	V_{OH_RST2}	I_{OH_RST} = -200µA	V_{CC} - 0.5		V_{CC}	V
	Rise Time	t_{R_RST}	C_L = 30pF (Note 3)			0.1	µs
	Fall Time	t_{F_RST}	C_L = 30pF (Note 3)			0.1	µs
	Shutdown Current Threshold	$I_{RST(SD)}$			-20		mA
	Current Limitation	$I_{RST(LIMIT)}$		-20		+20	mA
	RSTIN to RST Delay	$t_{D(RSTIN-RST)}$				2	µs
CLK PIN							
Card-Inactive Mode	Output Low Voltage	V_{OL_CLK1}	I_{OLCLK} = 1mA	0		0.3	V
	Output Current	I_{OL_CLK1}	V_{OLCLK} = 0V	0		-1	mA
Card-Active Mode	Output Low Voltage	V_{OL_CLK2}	I_{OLCLK} = 200µA	0		0.3	V
	Output High Voltage	V_{OH_CLK2}	I_{OHCLK} = -200µA	V_{CC} - 0.5		V_{CC}	V
	Rise Time	t_{R_CLK}	C_L = 30pF (Note 3)			8	ns
	Fall Time	t_{F_CLK}	C_L = 30pF (Note 3)			8	ns
	Current Limitation	$I_{CLK(LIMIT)}$		-70		+70	mA
	Clock Frequency	f_{CLK}	Operational (Note 3)	0		10	MHz
	Duty Factor	δ	C_L = 30pF (Note 3)	45		55	%
	Slew Rate	SR	C_L = 30pF (Note 3)	0.2			V/ns
V_{CC} PIN							
Card-Inactive Mode	Output Low Voltage	V_{CC1}	I_{CC} = 1mA	0		0.3	V
	Output Current	I_{CC1}	V_{CC} = 0V	0		-1	mA
Card-Active Mode	Output Low Voltage	V_{CC2}	$I_{CC(5V)}$ < 80mA	4.75	5.00	5.25	V
			$I_{CC(3V)}$ < 65mA	2.78	3.00	3.22	
			5V card: current pulses of 40nC with I < 200mA, t < 400ns, f < 20MHz (Note 3)	4.6		5.4	
			3V card: current pulses of 24nC with I < 200mA, t < 400ns, f < 20MHz (Note 3)	2.75		3.25	
	Output Current	I_{CC2}	$V_{CC(5V)}$ = 0 to 5V			-80	mA
			$V_{CC(3V)}$ = 0 to 3V			-65	
	Shutdown Current Threshold	$I_{CC(SD)}$			120		mA
	Slew Rate	V_{CCSR}	Up/down, C < 300nF	0.05	0.16	0.22	V/µs

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DD} = +3.3V, V_{DDA} = +5.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DATA LINES (I/O AND I/OIN)							
I/O ⇔ I/OIN Falling Edge Delay		$t_{D(IO-IOIN)}$	(Note 3)			200	ns
Pullup Pulse Active Time		t_{PU}	(Note 3)			100	ns
Maximum Frequency		f_{IOMAX}				1	MHz
Input Capacitance		C_I	(Note 3)			10	pF
I/O, AUX1, AUX2 PINS							
Card-Inactive Mode	Output Low Voltage	V_{OL_IO1}	I_{OL_IO} = 1mA	0		0.3	V
	Output Current	I_{OL_IO1}	V_{OL_IO} = 0V	0		-1	mA
	Internal Pullup Resistor	R_{PU_IO}	To V_{CC}	9	11	19	kΩ
Card-Active Mode	Output Low Voltage	V_{OL_IO2}	I_{OL_IO} = 1mA	0		0.3	V
	Output High Voltage	V_{OH_IO2}	I_{OH_IO} = < -40µA (3V/5V)	0.75 x V_{CC}		V_{CC}	V
	Output Rise/Fall Time	t_{OT}	C_L = 30pF (Note 3)			0.1	µs
	Input Low Voltage	V_{IL_IO}		-0.3		+0.8	V
	Input High Voltage	V_{IH_IO}		1.5		V_{CC}	
	Input Low Current	I_{IL_IO}	V_{IL_IO} = 0V			700	µA
	Input High Current	I_{IH_IO}	V_{IH_IO} = V_{CC}			20	µA
	Input Rise/Fall Time	t_{IT}	(Note 3)			1.2	µs
	Current Limitation	$I_{IO(LIMIT)}$	C_L = 30pF	-15		+15	mA
	Current When Pullup Active	I_{PU}	C_L = 80pF, V_{OH} = 0.9 x V_{DD} (Note 3)	-1			mA
I/OIN, AUX1IN, AUX2IN PINS							
Output Low Voltage		V_{OL}	I_{OL} = 1mA	0		0.3	V
Output High Voltage		V_{OH}	I_{OH} < -40µA	0.75 x V_{DD}		V_{DD} + 0.1	V
Output Rise/Fall Time		t_{OT}	C_L = 30pF, 10% to 90% (Note 3)			0.1	µs
Input Low Voltage		V_{IL}		-0.3		0.3 x V_{DD}	V
Input High Voltage		V_{IH}		0.7 x V_{DD}		V_{DD} + 0.3	V
Input Low Current		I_{IL_IO}	V_{IL} = 0V			600	µA
Input High Current		I_{IH_IO}	V_{IH} = V_{DD}			10	µA
Input Rise/Fall Time		t_{IT}	V_{IL} to V_{IH} (Note 3)			1.2	µs
Integrated Pullup Resistor		R_{PU}	Pullup to V_{DD}	9	11	13	kΩ
Current When Pullup Active		I_{PU}	C_L = 30pF, V_{OH} = 0.9 x V_{DD} (Note 3)	-1			mA

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DD} = +3.3V, V_{DDA} = +5.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL PINS (CLKDIV1, CLKDIV2, $\overline{CMDVCC}$, RSTIN, 5V/$\overline{3V}$)							
Input Low Voltage		V_{IL}		-0.3		0.3 x V_{DD}	V
Input High Voltage		V_{IH}		0.7 x V_{DD}		V_{DD} + 0.3	V
Input Low Current		I_{IL_IO}	0 < V_{IL} < V_{DD}			5	µA
Input High Current		I_{IH_IO}	0 < V_{IH} < V_{DD}			5	µA
Integrated Pullup Resistor		R_{PU}	Pullup to V_{DD}, 5V/$\overline{3V}$ only	50	85	120	kΩ
INTERRUPT OUTPUT PIN ($\overline{OFF}$)							
Output Low Voltage		V_{OL}	I_{OL} = 2mA	0		0.3	V
Output High Voltage		V_{OH}	I_{OH} = -15µA	0.75 x V_{DD}			V
Integrated Pullup Resistor		R_{PU}	Pullup to V_{DD}	12	20	28	kΩ
PRES, $\overline{PRES}$ PINS							
Input Low Voltage		V_{IL_PRES}				0.3 x V_{DD}	V
Input High Voltage		V_{IH_PRES}		0.7 x V_{DD}			V
Input Low Current		I_{IL_PRES}	V_{IL_PRES} = 0V			40	µA
Input High Current		I_{IH_PRES}	V_{IH_PRES} = V_{DD}			40	µA
TIMING							
Activation Time		t_{ACT}			160		µs
Deactivation Time		t_{DEACT}			80		µs
CLK to Card Start Time	Window Start	t_3			95		µs
	Window End	t_5			160		
PRES/$\overline{PRES}$ Debounce Time		$t_{DEBOUNCE}$			8		ms

Note 1: Operation guaranteed at T_A = -40°C and T_A = +85°C, but not tested.
Note 2: IDD_IC measures the amount of current used by the DS8024 to provide the smart card current minus the load.
Note 3: Guaranteed by design, but not production tested.

Pin Description

PIN	NAME	FUNCTION
1, 2	CLKDIV1, CLKDIV2	Clock Divider. Determines the divided-down input clock frequency (presented at XTAL1 or from a crystal at XTAL1 and XTAL2) on the CLK output pin. Dividers of 1, 2, 4, and 8 are available.
3	5V/$\overline{3V}$	5V/3V Selection Pin. Allows selection of 5V or 3V for communication with an IC card. Logic-high selects 5V operation; logic-low selects 3V operation. See Table 3 for a complete description of choosing card voltages.
4	PGND	Analog Ground
5, 7	CP2, CP1	Step-Up Converter Contact. Charge-pump capacitor. Connect a 100nF capacitor (ESR < 100mÃ) between CP1 and CP2.
6	V_{DDA}	Charge-Pump Supply. Must be equal to or higher than V_{DD}. Connect a supply of at least 3.3V.
8	V_{UP}	Charge-Pump Output. Connect a 100nF capacitor (ESR < 100mÃ) between V_{UP} and GND.
9	$\overline{PRES}$	Card Presence Indicator. Active-low card presence inputs. When the presence indicator becomes active, a debounce timeout begins. After 8ms (typ) the $\overline{OFF}$ signal becomes active.
10	PRES	Card Presence Indicator. Active-high card presence inputs. When the presence indicator becomes active, a debounce timeout begins. After 8ms (typ) the $\overline{OFF}$ signal becomes active.
11	I/O	Smart Card Data-Line Output. Card data communication line, contact C7.
12, 13	AUX2, AUX1	Smart Card Auxiliary Line (C4, C8) Output. Data line connected to card reader contacts C4 (AUX1) and C8 (AUX2).
14	CGND	Smart Card Ground
15	CLK	Smart Card Clock. Card clock, contact C3.
16	RST	Smart Card Reset. Card reset output from contact C2.
17	V_{CC}	Smart Card Supply Voltage. Decouple to CGND (card ground) with 2 x 100nF or 100 + 220nF capacitors (ESR < 100mΩ).
18	N.C.	No Connection. Unused on the DS8024.
19	$\overline{CMDVCC}$	Activation Sequence Initiate. Active-low input from host.
20	RSTIN	Card Reset Input. Reset input from the host.
21	V_{DD}	Supply Voltage
22	GND	Digital Ground
23	$\overline{OFF}$	Status Output. Active-low interrupt output to the host. Use a 20kΩ integrated pullup resistor to V_{DD}.
24, 25	XTAL1, XTAL2	Crystal/Clock Input. Connect an input from an external clock to XTAL1 or connect a crystal across XTAL1 and XTAL2. For the low idle-mode current variant, an external clock must be driven on XTAL1.
26	I/OIN	I/O Input. Host-to-interface chip data I/O line.
27, 28	AUX1IN, AUX2IN	C4/C8 Input. Host-to-interface I/O line for auxiliary connections to C4 and C8.

Detailed Description

The DS8024 is an analog front-end for communicating with 3V and 5V smart cards. Using an integrated charge pump, the DS8024 can operate from a single input voltage. The device translates all communication lines to the correct voltage level and provides power for smart card operation. It can operate from a wide input voltage range (3.3V to 6.0V). The DS8024 is compatible with the NXP TDA8024 and is provided in the same packages. (Note that the PORADJ pin is not present in the DS8024. Most applications do not make use of this input pin, instead using the DS8024's default reset threshold.)

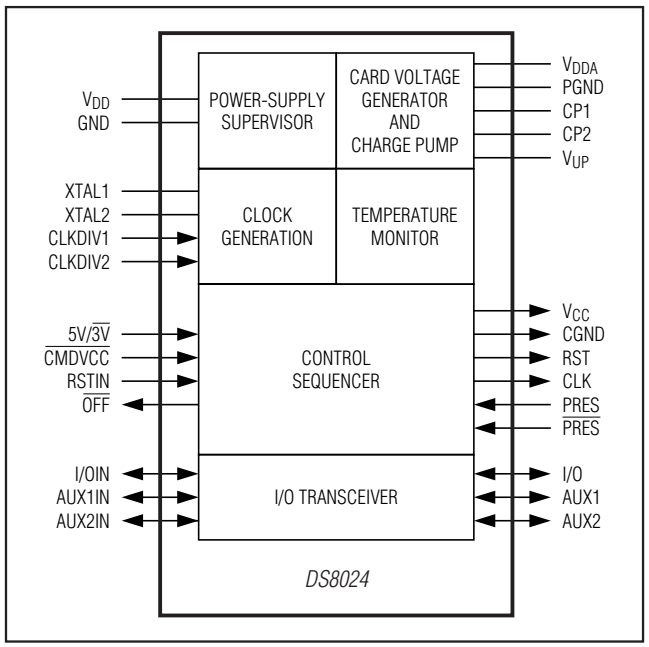


Figure 1. Functional Diagram

Power Supply

The DS8024 can operate from a single supply or a dual supply. The supply pins for the device are V_{DD}, GND, V_{DDA}, and PGND. V_{DD} should be in the range of 2.7V to 6.0V, and is the supply for signals that interface with the host controller. It should, therefore, be the same supply as used by the host controller. All smart card contacts remain inactive during power on or power off. The internal circuits are kept in the reset state until V_{DD} reaches V_{TH2} + V_{HYS2} and for the duration of the internal power-on reset pulse, t_W. A deactivation sequence is executed when V_{DD} falls below V_{TH2}.

An internal charge pump and regulator generate the 3V or 5V card supply voltage (V_{CC}). The charge pump and regulator are supplied by V_{DDA} and PGND. V_{DDA} should be connected to a minimum 3.3V (maximum 6.0V) supply and should be at a potential that is equal to or higher than V_{DD}.

The charge pump operates in a 1x (voltage follower) or 2x (voltage doubler) mode depending on the input V_{DDA} and the selected card voltage (5V or 3V).

- For 5V cards, the DS8024 operates in a 1x mode for V_{DDA} > 5.8V and in a 2x mode for V_{DDA} < 5.8V.
- For 3V cards, the DS8024 operates in a 1x mode for V_{DDA} > 4.1V and in a 2x mode for V_{DDA} < 4.0V.

Voltage Supervisor

The voltage supervisor monitors the V_{DD} supply. A 220µs reset pulse (t_W) is used internally to keep the device inactive during power on or power off of the V_{DD} supply. See Figure 2.

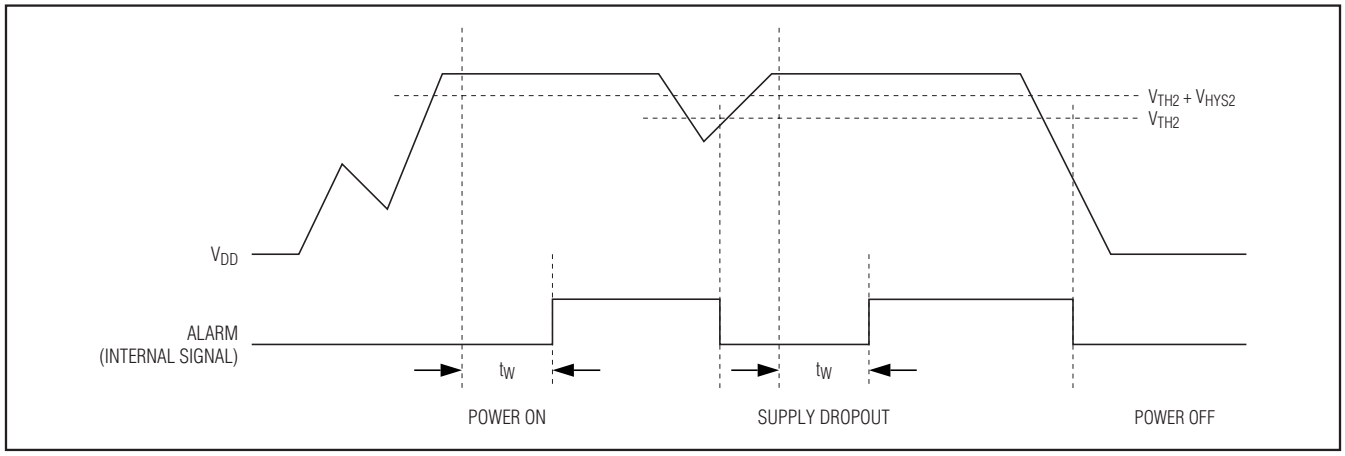


Figure 2. Voltage Supervisor Behavior

The DS8024 card interface remains inactive no matter the levels on the command lines until duration t_W after V_{DD} has reached a level higher than $V_{TH2} + V_{HYS2}$. When V_{DD} falls below V_{TH2}, the DS8024 executes a card deactivation sequence if its card interface is active.

Clock Circuitry

The clock signal from the DS8024 to the smart card (CLK) is generated from the clock input on XTAL1 or from a crystal operating at up to 20MHz connected between pins XTAL1 and XTAL2. The inputs CLKDIV1 and CLKDIV2 determine the frequency of the CLK signal, which can be f_{XTAL}, $f_{XTAL}/2$, $f_{XTAL}/4$, or $f_{XTAL}/8$. Table 1 shows the relationship between CLKDIV1 and CLKDIV2 and the frequency of CLK.

Do not change the state of pins CLKDIV1 and CLKDIV2 simultaneously; a delay of 10ns minimum between changes is required. The minimum duration of any state of CLK is 8 periods of XTAL1.

The hardware in the DS8024 guarantees that the frequency change is synchronous. During a transition of the clock divider, no pulse is shorter than 45% of the smallest period, and the clock pulses before and after the instant of change have the correct width.

To achieve a 45% to 55% duty factor on pin CLK when no crystal is present, the input signal on XTAL1 should have a 48% to 52% duty factor. Transition time on XTAL1 should be less than 5% of the period.

With a crystal, the duty factor on pin CLK may be 45% to 55% depending on the circuit layout and on the crystal characteristics and frequency.

The DS8024 crystal oscillator runs when the device is powered up. If the crystal oscillator is used or the clock pulse on pin XTAL1 is permanent, the clock pulse is applied to the card at time t_4 (see Figures 7 and 8). If the signal applied to XTAL1 is controlled by the host microcontroller, the clock pulse is applied to the card when it is sent by the system microcontroller (after completion of the activation sequence).

Table 1. Clock Frequency Selection

CLKDIV1	CLKDIV2	f_{CLK}
0	0	$f_{XTAL}/8$
0	1	$f_{XTAL}/4$
1	1	$f_{XTAL}/2$
1	0	f_{XTAL}

I/O Transceivers

The three data lines I/O, AUX1, and AUX2 are identical. This section describes the characteristics of I/O and I/OIN but also applies to AUX1, AUX1IN, AUX2, and AUX2IN.

I/O and I/OIN are pulled high with an 11kΩ resistor (I/O to V_{CC} and I/OIN to V_{DD}) in the inactive state. The first side of the transceiver to receive a falling edge becomes the master. When the master is decided, the opposite side switches to slave mode, ignoring subsequent edges until the master releases. After a time delay $t_{D(EDGE)}$, an n transistor on the slave side is turned on, thus transmitting the logic 0 present on the master side.

When the master side asserts a logic 1, a p transistor on the slave side is activated during the time delay t_{PU} and then both sides return to their inactive (pulled up) states. This active pullup provides fast low-to-high transitions. After the duration of t_{PU}, the output voltage depends only on the internal pullup resistor and the load current. Current to and from the card I/O lines is limited internally to 15mA. The maximum frequency on these lines is 1MHz.

Inactive Mode

The DS8024 powers up with the card interface in the inactive mode. Minimal circuitry is active while waiting for the host to initiate a smart card session.

- All card contacts are inactive (approximately 200Ω to GND).
- Pins I/OIN, AUX1IN, and AUX2IN are in the high-impedance state (11kΩ pullup resistor to V_{DD}).
- Voltage generators are stopped.
- XTAL oscillator is running (if included in the device).
- Voltage supervisor is active.
- The internal oscillator is running at its low frequency.

Activation Sequence

After power-on and the reset delay, the host microcontroller can monitor card presence with signals $\overline{OFF}$ and $\overline{CMDVCC}$, as shown in Table 2.

Table 2. Card Presence Indication

$\overline{OFF}$	$\overline{CMDVCC}$	STATUS
High	High	Card present.
Low	High	Card **not** present.

When a card is inserted into the reader (if PRES is active), the host microcontroller can begin an activation sequence (start a card session) by pulling $\overline{CMDVCC}$ low. The following events form an activation sequence (Figure 3):

1) Host: $\overline{CMDVCC}$ is pulled low.
2) DS8024: The internal oscillator changes to high frequency (t_0).
3) DS8024: The voltage generator is started simultaneously ($t_0 = t_1$).
4) DS8024: V_{CC} rises from 0 to 5V or 3V with a controlled slope ($t_2 = t_1 + 1.5 \times T$). T is 64 times the internal oscillator period (approximately 25µs).
5) DS8024: I/O, AUX1, and AUX2 are enabled ($t_3 = t_1 + 4T$).
6) DS8024: The CLK signal is applied to the C3 contact (t_4).
7) DS8024: RST is enabled simultaneously ($t_5 = t_4 = t_1 + 7T$).

An alternate sequence allows the application to control when the clock is applied to the card.

1) Host: Set RSTIN high.
2) Host: Set $\overline{CMDVCC}$ low.
3) Host: Set RSTIN low between t_3 and t_5; CLK will now start.
4) DS8024: RST stays low until t_5, then RST becomes the copy of RSTIN.
5) DS8024: RSTIN has no further effect on CLK after t_5.

If the applied clock is not needed, set $\overline{CMDVCC}$ low with RSTIN low. In this case, CLK starts at t_3 (minimum 200ns after the transition on I/O, see Figure 4); after t_5, RSTIN can be set high to obtain an answer to request (ATR) from an inserted smart card. Do not perform activation with RSTIN held permanently high.

Active Mode

When the activation sequence is completed, the DS8024 card interface is in active mode. The host microcontroller and the smart card exchange data on the I/O lines.

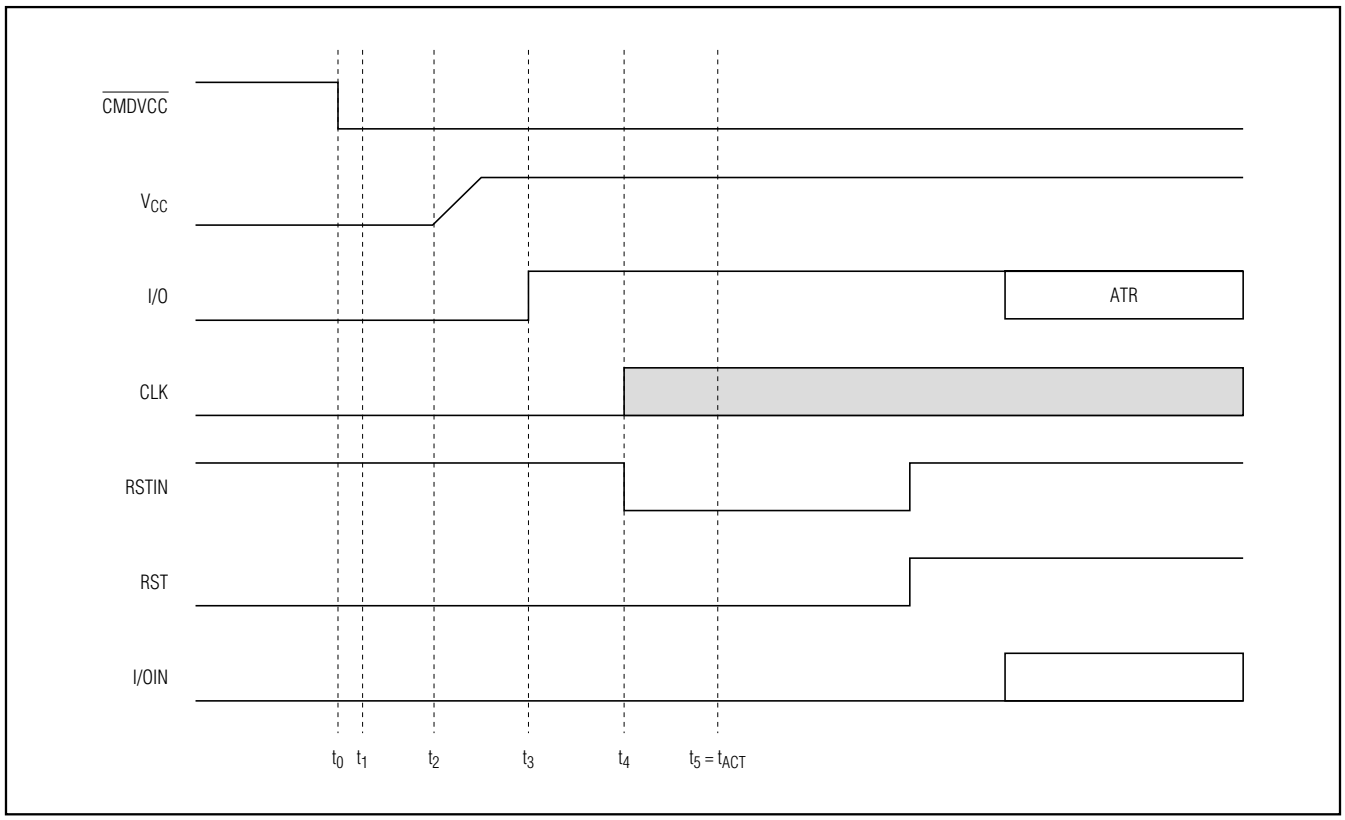


Figure 3. Activation Sequence Using RSTIN and $\overline{CMDVCC}$

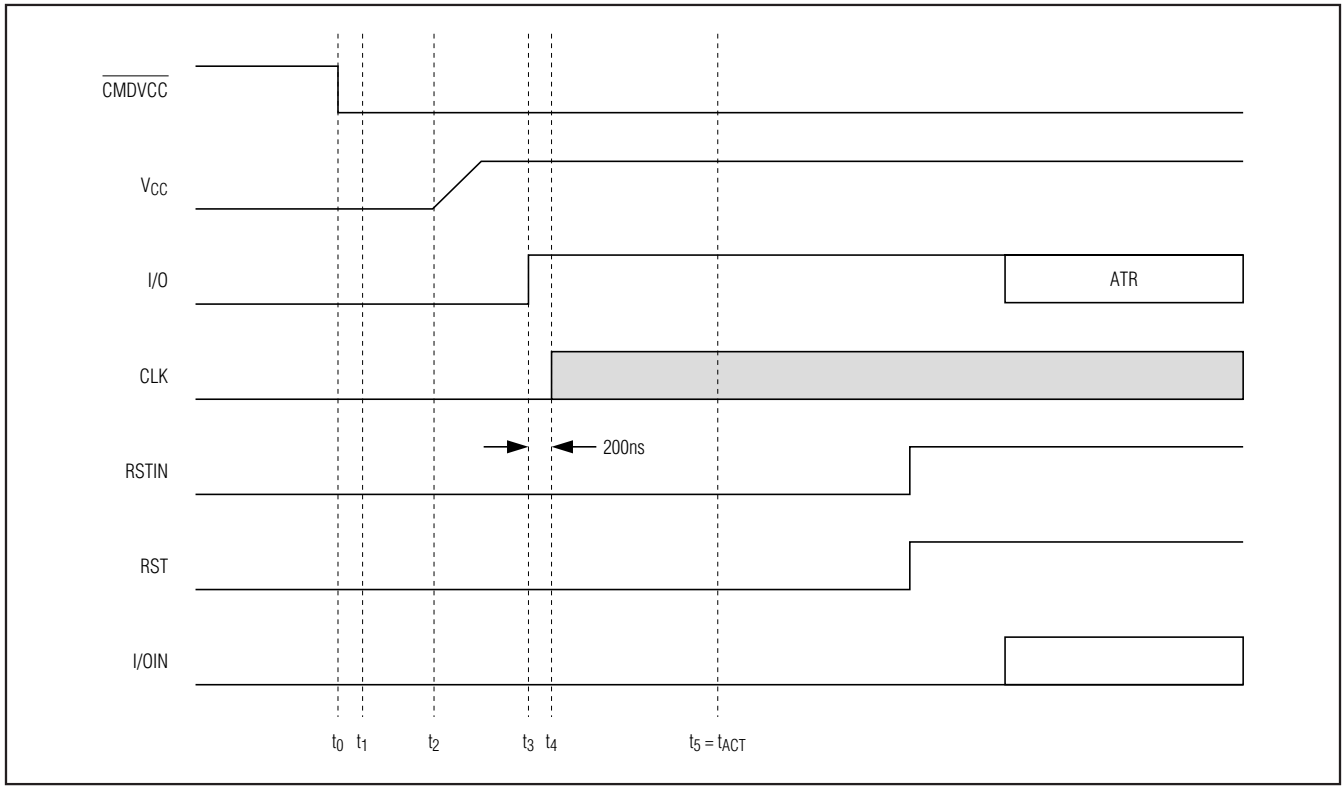


Figure 4. Activation Sequence at t_3

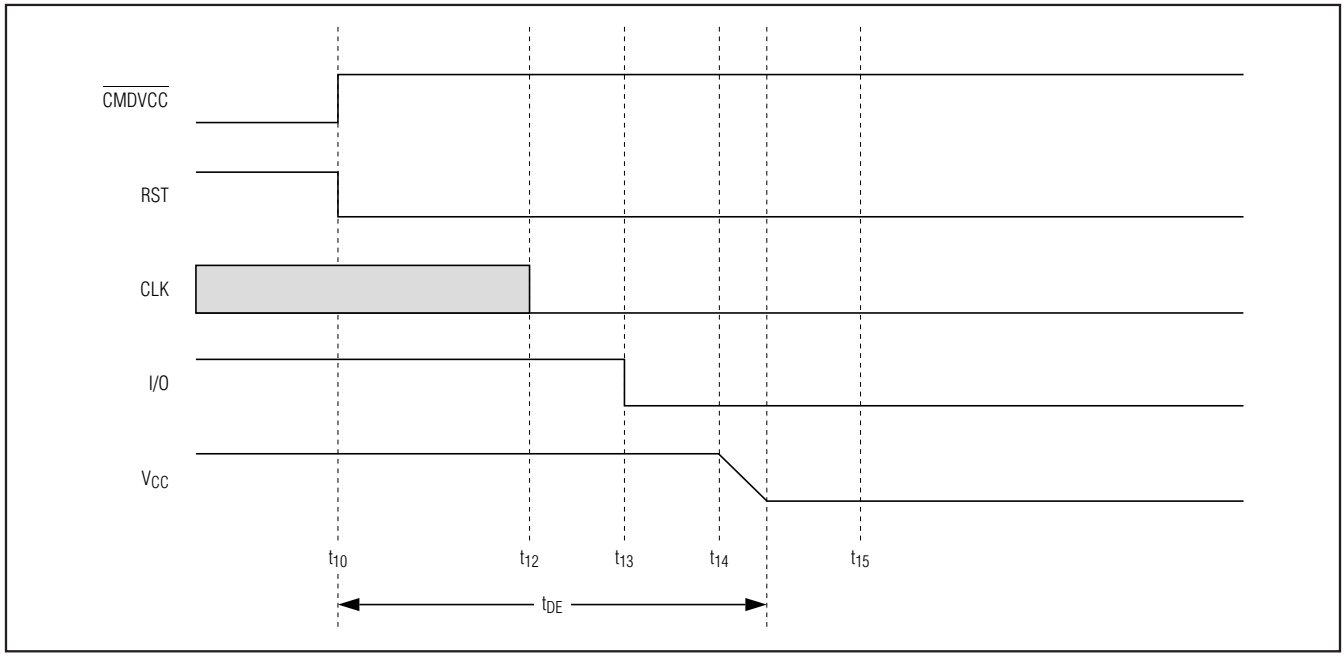


Figure 5. Deactivation Sequence

Deactivation Sequence

When the host microcontroller is done communicating with the smart card, it sets the $\overline{CMDVCC}$ line high to execute an automatic deactivation sequence and returns the card interface to the inactive mode.

The following sequence of events occurs during a deactivation sequence (Figure 5):

1) RST goes low (t_{10}).
2) CLK is held low ($t_{12} = t_{10} + 0.5 \times T$), where T is 64 times the period of the internal oscillator (approximately 25µs).
3) I/O, AUX1, and AUX2 are pulled low ($t_{13} = t_{10} + T$).
4) V_{CC} starts to fall ($t_{14} = t_{10} + 3T$).
5) When V_{CC} reaches its inactive state, the deactivation sequence is complete (at t_{DE}).
6) All card contacts become low impedance to GND; I/OIN, AUX1IN, and AUX2IN remain at V_{DD} (pulled up through an internal 11kΩ resistor).
7) The internal oscillator returns to its lower frequency.

VCC Generator

The card voltage (V_{CC}) generator can supply up to 80mA continuously at 5V or 65mA at 3V. An internal overload detector triggers at approximately 120mA. Current samples to the detector are filtered. This allows spurious current pulses (with a duration of a few µs) up to 200mA to be drawn without causing deactivation. The average current must stay below the specified maximum current value.

See the *Applications Information* section for recommendations to help maintain V_{CC} voltage accuracy.

Fault Detection

The DS8024 integrates circuitry to monitor the following fault conditions:

- Short-circuit or high current on V_{CC}
- Card removal while the interface is activated
- V_{DD} dropping below threshold
- Card voltage generator operating out of the specified values (V_{DDA} too low or current consumption too high)
- Overheating

There are two different cases for how the DS8024 reacts to fault detection (Figure 6):

- **Outside a Card Session ($\overline{CMDVCC}$ High).** Output $\overline{OFF}$ is low if a card is not in the card reader and high if a card is in the reader. The V_{DD} supply is monitored—a decrease in input voltage generates an internal power-on reset pulse but does not affect the $\overline{OFF}$ signal. Short-circuit and temperature detection are disabled because the card is not powered up.
- **Within a Card Session ($\overline{CMDVCC}$ Low).** Output $\overline{OFF}$ goes low when a fault condition is detected, and an emergency deactivation is performed automatically (Figure 7). When the system controller resets $\overline{CMDVCC}$ to high, it may sense the $\overline{OFF}$ level again after completing the deactivation sequence. This distinguishes between a card extraction and a hardware problem ($\overline{OFF}$ goes high again if a card is present). Depending on the connector's card-present switch (normally closed or normally open) and the mechanical characteristics of the switch, bouncing can occur on the PRES signals at card insertion or withdrawal.

The DS8024 has a debounce feature with an 8ms typical duration (Figure 6). When a card is inserted, output $\overline{OFF}$ goes high after the debounce time delay. When the card is extracted, an automatic deactivation sequence of the card is performed on the first true/false transition on PRES and output $\overline{OFF}$ goes low.

Stop Mode (Low-Power Mode)

The DS8024 (like the TDA8024) does not support a low-power stop mode. For applications requiring low-power support, refer to the DS8113.

Smart Card Power Select

The DS8024 supports two smart card V_{CC} voltages: 3V and 5V. The power select is controlled by the 5V/$\overline{3V}$ signal as shown in Table 3. V_{CC} is 5V if 5V/$\overline{3V}$ is asserted to a logic-high state, and V_{CC} is 3V if 5V/$\overline{3V}$ is pulled to a logic-low state.

Table 3. VCC Select and Operation Mode

5V/$\overline{3V}$	$\overline{CMDVCC}$	VCC SELECT (V)	CARD INTERFACE STATUS
0	0	3	Activated
0	1	3	Inactivated
1	0	5	Activated
1	1	5	Inactivated

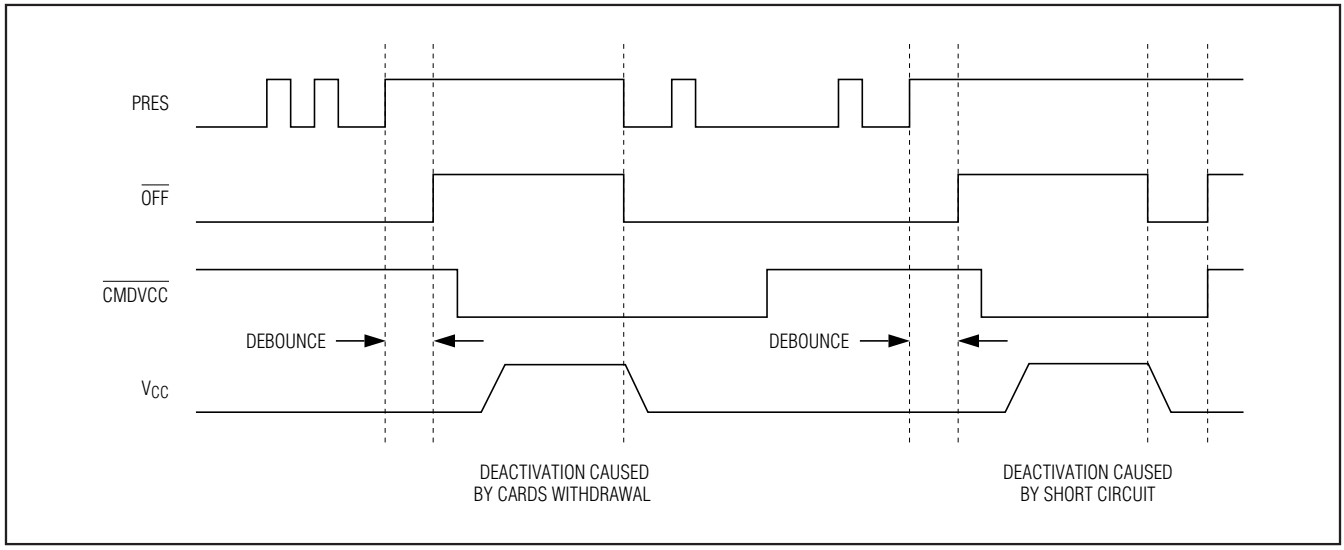


Figure 6. Behavior of PRES, $\overline{OFF}$, $\overline{CMDVCC}$, and V_{CC}

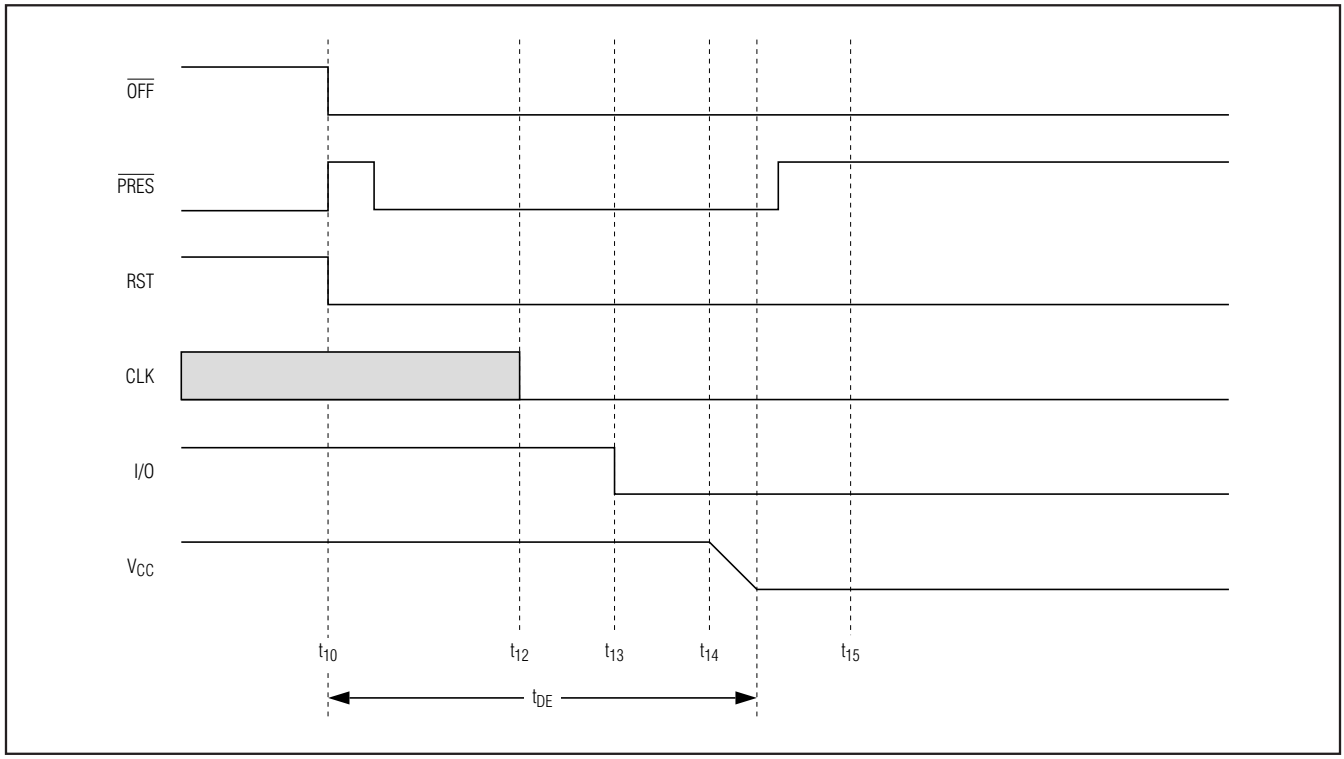
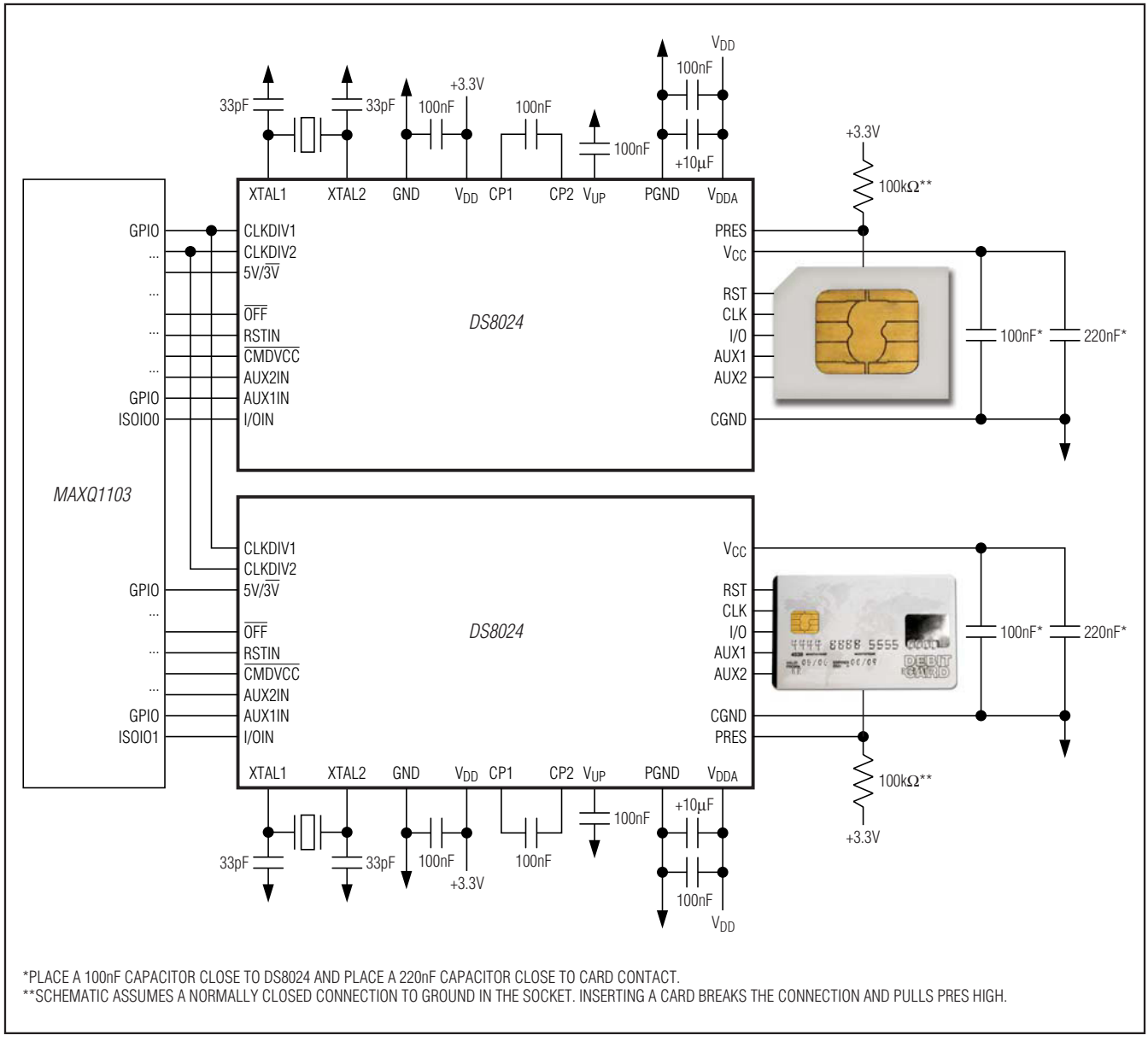


Figure 7. Emergency Deactivation Sequence (Card Extraction)



*PLACE A 100nF CAPACITOR CLOSE TO DS8024 AND PLACE A 220nF CAPACITOR CLOSE TO CARD CONTACT.
**SCHEMATIC ASSUMES A NORMALLY CLOSED CONNECTION TO GROUND IN THE SOCKET. INSERTING A CARD BREAKS THE CONNECTION AND PULLS PRES HIGH.

Figure 8. Typical Application Diagram

Applications Information

Performance can be affected by the layout of the application. For example, an additional cross-capacitance of 1pF between card reader contacts C2 (RST) and C3 (CLK) or C2 (RST) and C7 (I/O) can cause contact C2 to be polluted with high-frequency noise from C3 (or C7). In this case, include a 100pF capacitor between contacts C2 and CGND.

Application recommendations include the following:

- Ensure there is ample ground area around the DS8024 and the connector; place the DS8024 very near to the connector; decouple the V_{DD} and V_{DDA} lines separately. These lines are best positioned under the connector.
- The DS8024 and the host microcontroller must use the same V_{DD} supply. Pins CLKDIV1, CLKDIV2, RSTIN, PRES, AUX1IN, I/OIN, AUX2IN, 5V/3V, CMDVCC, and OFF are referenced to V_{DD}; if pin XTAL1 is to be driven by an external clock, also reference this pin to V_{DD}.
- Trace C3 (CLK) should be placed as far as possible from the other traces.
- The trace connecting CGND to C5 (GND) should be straight (the two capacitors on C1 (V_{CC}) should be connected to this ground trace).
- Avoid ground loops among CGND, PGND, and GND.
- Decouple V_{DDA} and V_{DD} separately; if the two supplies are the same in the application, they should be connected in a star on the main trace.
- Connect a 100nF capacitor (ESR < 100mΩ) between V_{CC} and CGND and place near the DS8024's V_{CC} pin.
- Connect a 100nF or 220nF capacitor (220nF preferred, ESR < 100mΩ) between V_{CC} and CGND and place near the smart card socket's C1 contact.

With all these layout precautions, noise should be kept to an acceptable level and jitter on C3 (CLK) should be less than 100ps.

Technical Support

For technical support, go to **https://support.maxim-integrated.com/micro**.

Selector Guide

PART	CURRENT VOLTAGES SUPPORTED (V)	SUPPORTS STOP MODE?	PIN-PACKAGE
DS8024-RJX+	3.0, 5.0	No	28 TSSOP
DS8024-RJX/V+	3.0, 5.0	No	28 TSSOP
DS8024-RRX+	3.0, 5.0	No	28 SO

Note: *Contact the factory for availability of other variants and package options.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive qualified part.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 SO (300 mils)	W28+6	21-0042	90-0109
28 TSSOP	U28+1	21-0066	90-0171

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/08	Initial release	—
1	8/08	Clarified the V_{DDA} specification in the *Recommended DC Operating Conditions* table	2
2	2/12	Added the automotive TSSOP version to the *Ordering Information* and *Selector Guide*; updated the *Absolute Maximum Ratings*	1, 2, 14
3	7/12	Added footnote to the resistor value on the PRES pin in Figure 8	13
4	4/13	Clarified t_1, t_5, and t_{14}	9, 11

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- Excess Inventory Management