THE DATASHEET OF

DS4422N+T&R

DS4422/DS4424

Two-/Four-Channel, I²C, 7-Bit Sink/Source Current DAC

General Description

The DS4422 and DS4424 contain two or four I²C programmable current DACs that are each capable of sinking and sourcing current up to 200µA. Each DAC output has 127 sink and 127 source settings that are programmed using the I²C interface. The current DAC outputs power up in a high-impedance state.

Applications

- Power-Supply Adjustment
- Power-Supply Margining
- Adjustable Current Sink or Source

Ordering Information

PART	OUTPUTS	TEMP RANGE	PIN-PACKAGE
DS4422N+	2	-40°C to +85°C	14 TDFN-EP
DS4422N+T&R	2	-40°C to +85°C	14 TDFN-EP
DS4424N+	4	-40°C to +85°C	14 TDFN-EP
DS4424N+T&R	4	-40°C to +85°C	14 TDFN-EP

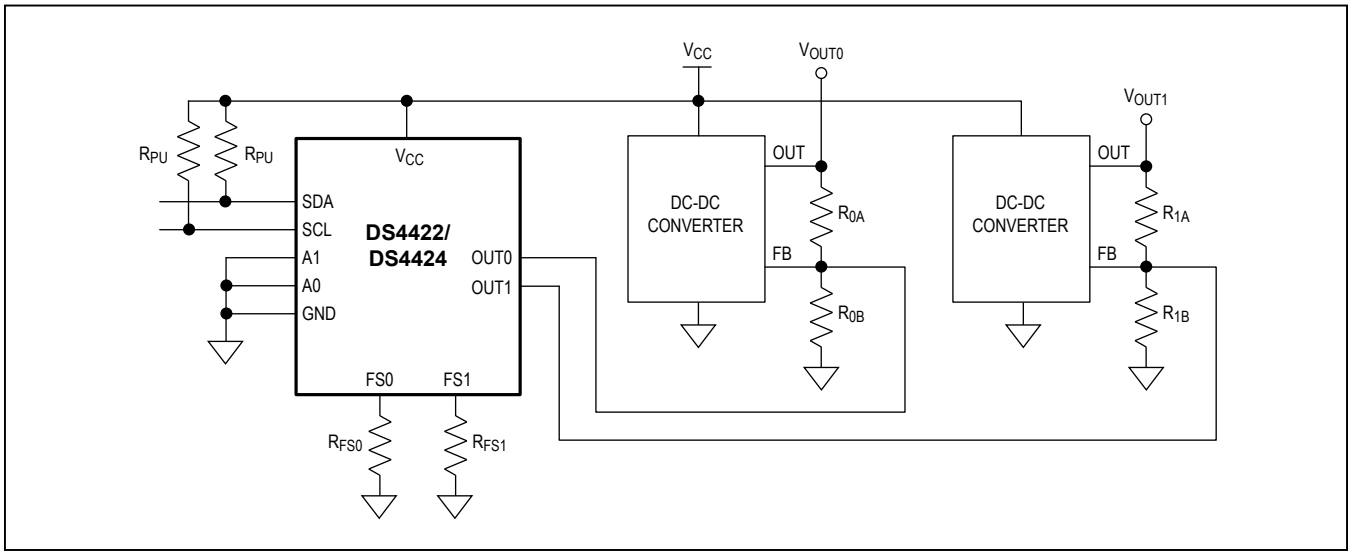
+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.
EP = Exposed pad.

Benefits and Features

- Two (DS4422) or Four (DS4424) Current DACs
- Full-Scale Current 50µA to 200µA
- Full-Scale Range for Each DAC Determined by External Resistors
- 127 Settings Each for Sink and Source Modes
- I²C-Compatible Serial Interface
- Two Address Pins Allow Four Devices on Same I²C Bus
- Low Cost
- Small Package (14-Pin, 3mm x 3mm TDFN)
- -40°C to +85°C Temperature Range
- 2.7V to 5.5V Operating Range

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



Absolute Maximum Ratings

Voltage Range on V_{CC}, SDA, and SCL Relative to Ground ..... -0.5V to +6.0V
Voltage Range on A0, A1, FS0, FS1, FS2, FS3, OUT0, OUT1, OUT2, and OUT3 Relative to Ground ..... -0.5V to (V_{CC} + 0.5V) (Not to exceed 6.0V.)
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Soldering Temperature ..... Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

(T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	2.7		5.5	V
Input Logic 1 (SDA, SCL, A0, A1)	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0 (SDA, SCL, A0, A1)	V_{IL}		-0.3		0.3 x V_{CC}	V
Full-Scale Resistor Values	R_{FS0}, R_{FS1}, R_{FS2}, R_{FS3}	(Note 2)	40		160	kΩ

DC Electrical Characteristics

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	V_{CC} = 5.5V (Note 3)	DS4422			250	µA
			DS4424			250	
Input Leakage (SDA, SCL)	I_{IL}	V_{CC} = 5.5V				1	µA
Output Leakage (SDA)	I_L					1	µA
Output Current Low (SDA)	I_{OL}	V_{OL} = 0.4V		3			mA
		V_{OL} = 0.6V		6			
RFS Voltage	V_{RFS}				0.976		V
I/O Capacitance	$C_{I/O}$					10	pF

Output Current Source Characteristics

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage for Sinking Current	$V_{OUT:SINK}$	(Note 4)	0.5		3.5	V
Output Voltage for Sourcing Current	$V_{OUT:SOURCE}$	(Note 4)	0		V_{CC} - 0.75	V
Full-Scale Sink Output Current	$I_{OUT:SINK}$	(Notes 1, 4)	50		200	µA
Full-Scale Source Output Current	$I_{OUT:SOURCE}$	(Notes 1, 4)	-200		-50	µA
Output Current Full-Scale Accuracy	$I_{OUT:FS}$	+25°C, V_{CC} = 3.3V; using 0.1% R_{FS} resistor (Note 2), V_{OUT0} = V_{OUT1} = 1.2V			±6	%
Output Current Temperature Coefficient	$I_{OUT:TC}$	(Note 5)		±75		ppm/°C

Output Current Source Characteristics (continued)

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Current Variation Due to Power-Supply Change		DC source		0.32		%/V
		DC sink		0.42		
Output Current Variation Due to Output-Voltage Change		DC source, V_{OUT} measure at 1.2V		0.16		%/V
		DC sink, V_{OUT} measure at 1.2V		0.16		
Output Leakage Current at Zero Current Setting	I_{ZERO}		-1		+1	µA
Output Current Differential Linearity	DNL	(Notes 6, 7)	-0.5		+0.5	LSB
Output Current Integral Linearity	INL	(Notes 7, 8)	-1		+1	LSB

AC Electrical Characteristics

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C.)

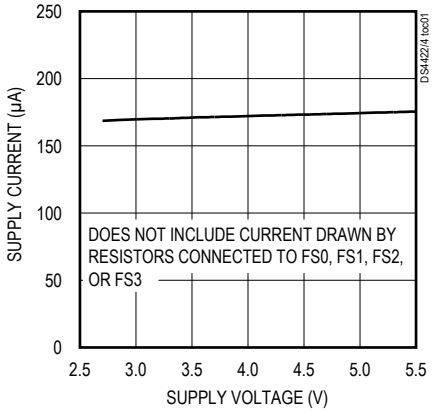
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 9)	0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{DH:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
START Setup Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 10)	20 + 0.1C_B		300	ns
SDA and SCL Fall Time	t_F	(Note 10)	20 + 0.1C_B		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitive Loading	C_B	(Note 10)			400	pF

Note 1: All voltages with respect to ground. Currents entering the IC are specified positive, and currents exiting the IC are negative.
Note 2: Input resistors (R_{FS}) must be between the speciifed values to ensure the device meets its accuracy and linearity specifications.
Note 3: Supply current specified with all outputs set to zero current setting. A0 and A1 are connected to GND. SDA and SCL are connected to V_{CC}. Excludes current through R_{FS} resistors (I_{RFS}). Total current including I_{RFS} is I_{CC} + (2 x I_{RFS}).
Note 4: The output-voltage range must be satisfied to ensure the device meets its accuracy and linearity specifications.
Note 5: Temperature drift excludes drift caused by external resistor.
Note 6: Differential linearity is defined as the difference between the expected incremental current increase with respect to position and the actual increase. The expected incremental increase is the full-scale range divided by 127.
Note 7: Guaranteed by design.
Note 8: Integral linearity is defined as the difference between the expected value as a function of the setting and the actual value. The expected value is a straight line between the zero and the full-scale values proportional to the setting.
Note 9: Timing shown is for fast-mode (400kHz) operation. This device is also backward compatible with I²C standard-mode timing.
Note 10: C_B—total capacitance of one bus line in pF.

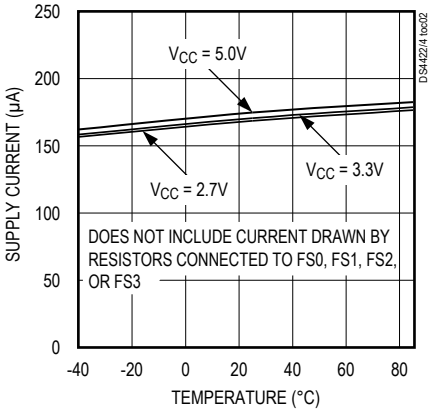
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

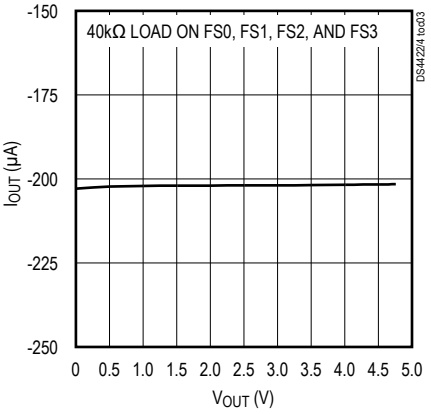
SUPPLY CURRENT vs. SUPPLY VOLTAGE



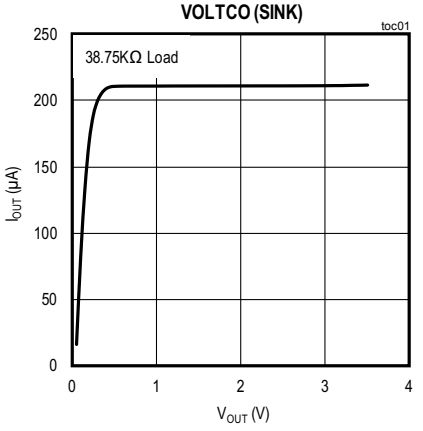
SUPPLY CURRENT vs. TEMPERATURE



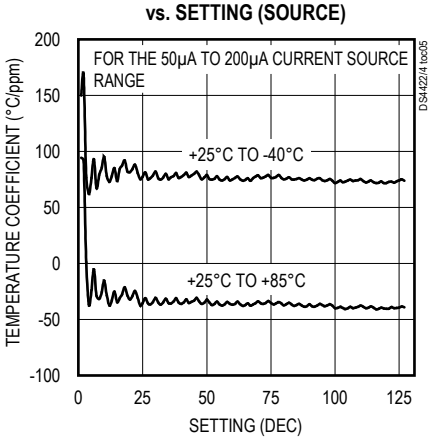
VOLTCO (SOURCE)



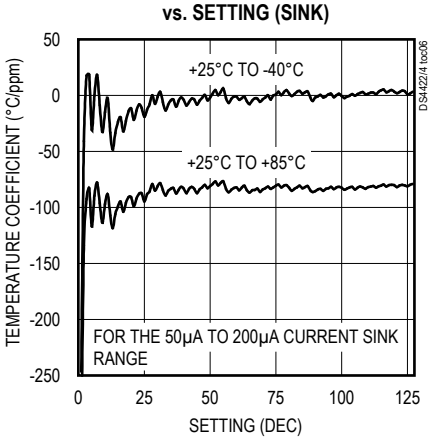
VOLTCO (SINK)



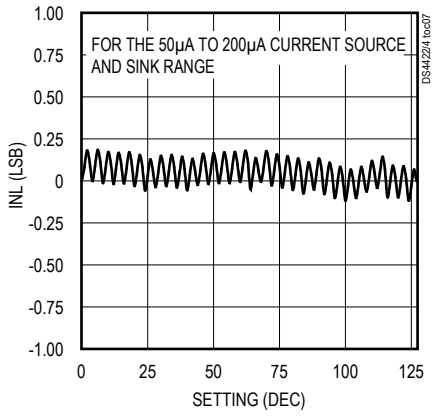
TEMPERATURE COEFFICIENT vs. SETTING (SOURCE)



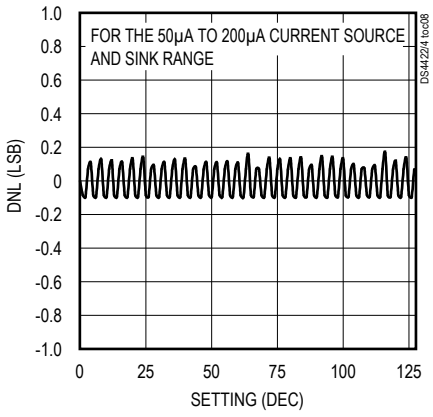
TEMPERATURE COEFFICIENT vs. SETTING (SINK)



INTEGRAL LINEARITY



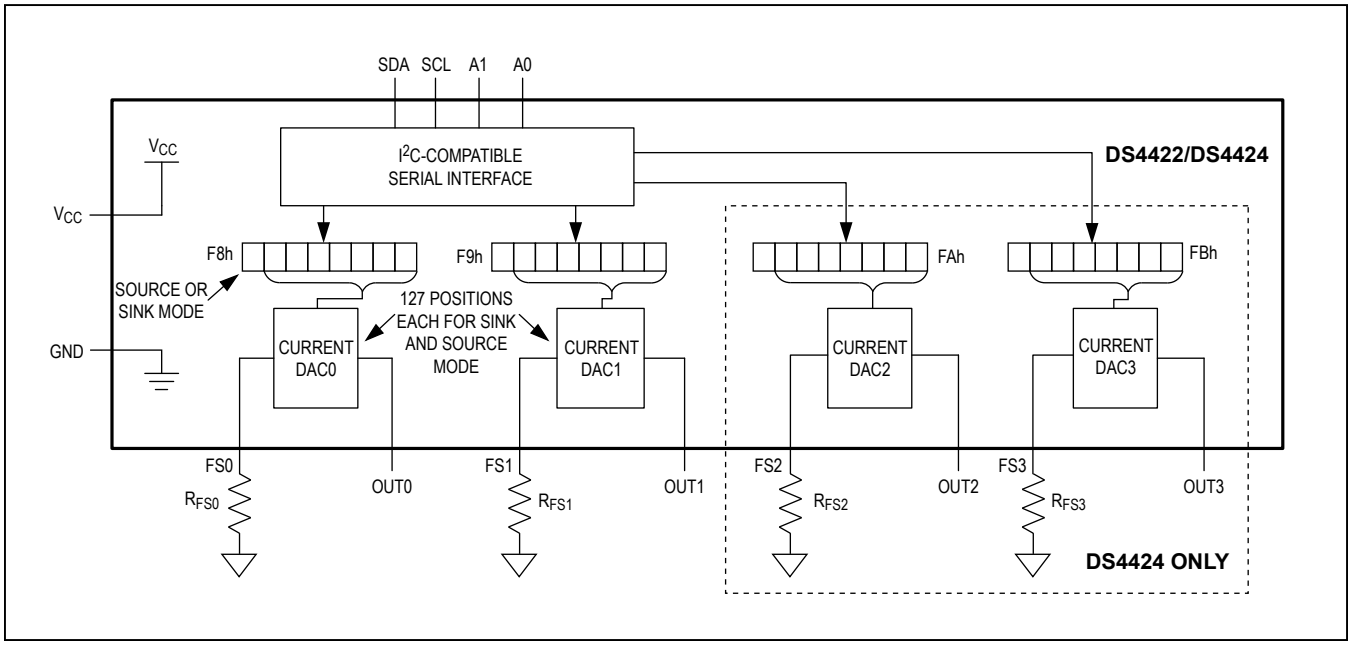
DIFFERENTIAL LINEARITY



Pin Description

PIN		NAME	FUNCTION
DS4424	DS4422		
1	1	SDA	I²C Serial Data. Input/output for I²C data.
2	2	SCL	I²C Serial Clock. Input for I²C clock.
3	3	GND	Ground
4	—	FS3	Full-Scale Calibration Input. A resistor to ground on these pins determines the full-scale current for each output. FS0 controls OUT0, FS1 controls OUT1, etc. (The DS4422 has only two inputs: FS0 and FS1.)
5	—	FS2	
6	6	FS1	
7	7	FS0	
8	8	OUT0	Current Output. Sinks or sources the current determined by the I²C interface and the resistance connected to FSx. (The DS4422 has only two outputs: OUT0 and OUT1.)
10	10	OUT1	
12	—	OUT2	
14	—	OUT3	
9, 11	9, 11	A0, A1	Address Select Inputs. Determines the I²C slave address by connecting V_{CC} or GND. See the Detailed Description section for the available device addresses.
13	13	V_{CC}	Power Supply
—	4, 5, 12, 14	N.C.	No Connection
—	—	EP	Exposed Pad. Connect to GND or leave unconnected.

Block Diagram



Detailed Description

The DS4422/DS4424 contain two or four I²C adjustable current sources that are each capable of sinking and sourcing current. Each output (OUT0, OUT1, OUT2, and OUT3) has 127 sink and 127 source settings that can be controlled by the I²C interface. The full-scale ranges and corresponding step sizes of the outputs are determined by external resistors, connected to pins FS0, FS1, FS2, and FS3, that can adjust the output current over a 4:1 range. Pins OUT2, OUT3, FS2, and FS3 are only available on the DS4424.

The formula to determine R_{FS} (connected to the FSx pins) to attain the desired full-scale current range is:

Equation 1:

$$R_{FS} = \frac{V_{RFS}}{16 \times I_{FS}} \times 127$$

Where I_{FS} is the desired full-scale current value, V_{RFS} is the R_{FS} voltage (see the *DC Electrical Characteristics* table), and R_{FS} is the external resistor value.

To calculate the output current value (I_{OUT}) based on the corresponding DAC value (see Table 1 for corresponding memory addresses), use equation 2.

Equation 2:

$$I_{OUT} = \frac{DAC\,Value(dec)}{127} \times I_{FS}$$

On power-up the DS4422/DS4424 output zero current. This is done to prevent them from sinking or sourcing an incorrect amount of current before the system host controller has had a chance to modify the device's setting.

As a source for biasing instrumentation or other circuits, the DS4422/DS4424 provide a simple and inexpensive current source with an I²C interface for control. The adjustable full-scale range allows the application to get the most out of its 7-bit sink or source resolution.

When used in adjustable power-supply applications (see *Typical Operating Circuit*), the DS4422/DS4424 do not affect the initial power-up voltage of the supply because they default to providing zero output current on power-up. As the devices source or sink current into the feedback-voltage node, they change the amount of output voltage required by the regulator to reach its steadystate operating point. Using the external resistor, R_{FS}, to set the output current range, the DS4422/DS4424 provide some flexibility for adjusting the impedances of the feedback network or the range over which the power supply can be controlled or margined.

I²C Slave Address

The DS4422/DS4424 respond to one of four I²C slave addresses determined by the two address inputs, A0 and A1. The address inputs should be connected to either V_{CC} or ground. Table 1 lists the slave addresses determined by the address input combinations.

Table 1. Slave Addresses

A1	A0	SLAVE ADDRESS (HEX)
GND	GND	20h
GND	V_{CC}	60h
V_{CC}	GND	A0h
V_{CC}	V_{CC}	E0h

Memory Organization

To control the DS4422/DS4424's current sources, write to the memory addresses listed in Table 2.

Table 2. Memory Addresses

MEMORY ADDRESS (HEX)	CURRENT SOURCE
F8h	OUT0
F9h	OUT1
FAh*	OUT2*
FBh*	OUT3*

**Only for DS4424.*

The format of each output control register is given by:

MSB							LSB
S	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Where:

BIT	NAME	FUNCTION	POWER-ON DEFAULT
S	Sign Bit	Determines if DAC sources or sinks current. For sink S = 0; for source S = 1.	0b
D_X	Data	7-Bit Data Controlling DAC Output. Setting 0000000b outputs zero current regardless of the state of the sign bit.	0000000b

Example: R_{FS0} = 80kΩ and register 0xF8h is written to a value of 0xAAh. Calculate the output current.

$$I_{FS} = (0.976V/80k\Omega) \times (127/16) = 96.838\mu A$$

The MSB of the output register is 1, so the output is sourcing the value corresponding to position 2Ah (42 decimal). The magnitude of the output current is equal to:

$$96.838\mu A \times (42/127) = 32.025\mu A$$

I²C Serial Interface Description

I²C Definitions

The following terminology is commonly used to describe I²C data transfers:

I²C Slave Address: The slave address of the DS4422/DS4424 is determined by the state of the A0 and A1 pins (see Table 1).

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states. When the bus is idle it often initiates a low-power mode for slave devices.

START Condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. See Figure 1 for applicable timing.

STOP Condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition. See Figure 1 for applicable timing.

Repeated START Condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated STARTs are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition. See Figure 1 for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL, plus the setup and hold time requirements (Figure 1). Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time (Figure 1) before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses, including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An Acknowledgement (ACK) or Not Acknowledge (NACK) is always the ninth bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the ninth bit. A device performs a

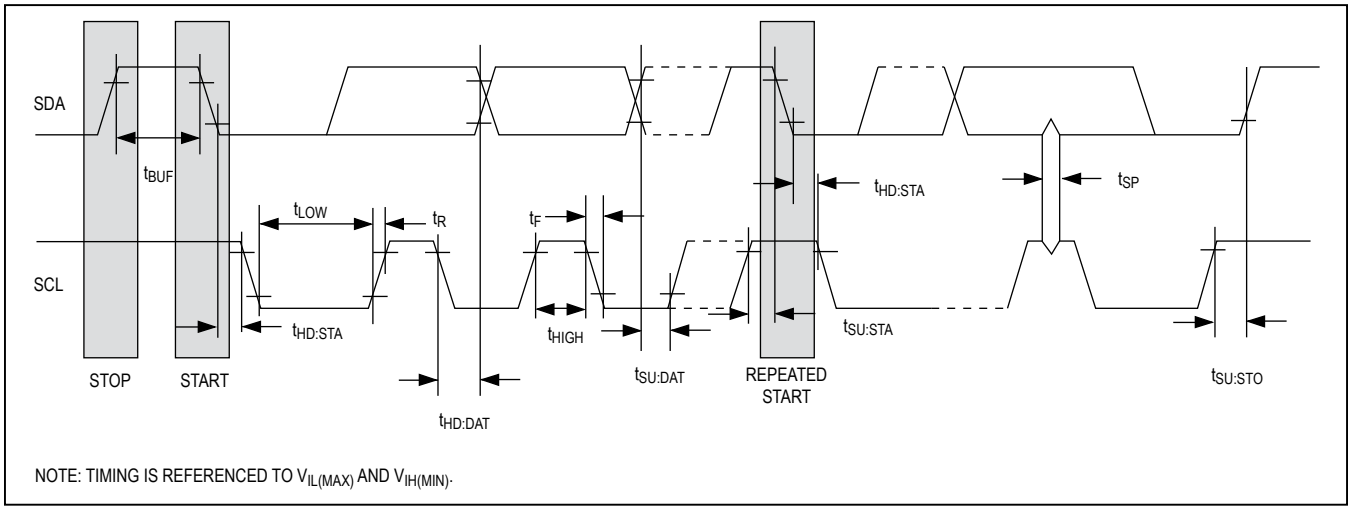


Figure 1. I²C Timing Diagram

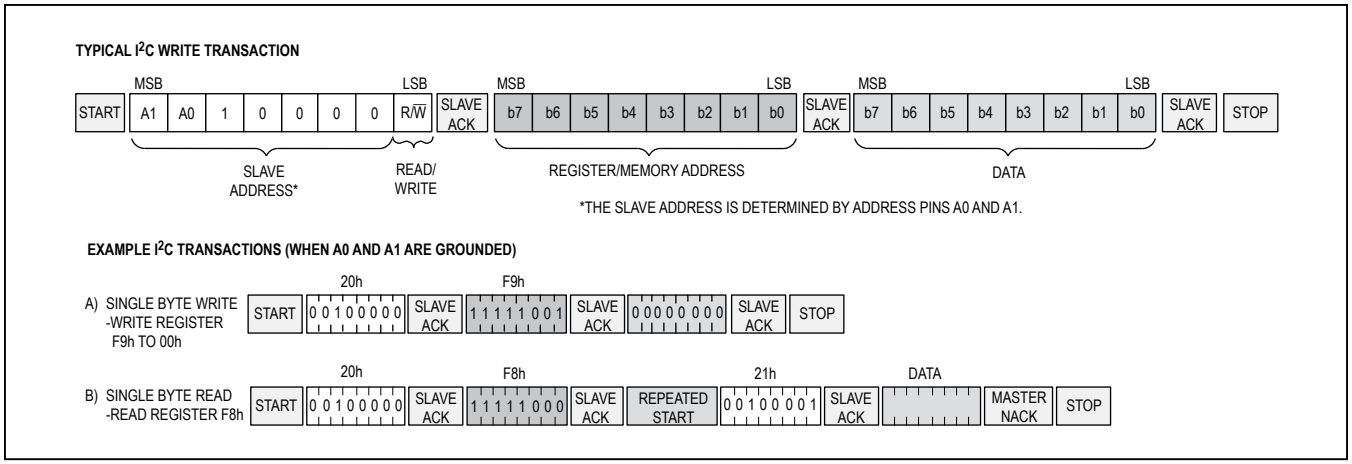


Figure 2. I2C Communication Examples

NACK by transmitting a one during the ninth bit. Timing for the ACK and NACK is identical to all other bit writes (Figure 2). An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit-write definition, and the acknowledgement is read using the bit-read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit-read definition above, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminated communication so the slave will return control of SDA to the master.

Slave Address Byte: Each slave on the I2C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit. The DS4422/DS4424 slave address is determined by the state of the A0 and A1 address pins. Table 1 describes the addresses corresponding to the state of A0 and A1.

When the R/$\overline{W}$ bit is 0 (such as in A0h), the master is indicating that it will write data to the slave. If R/$\overline{W}$ = 1 (A1h in this case), the master is indicating that it wants to read from the slave. If an incorrect slave address is written, the DS4422/DS4424 assume the master is communicating with another I2C device and ignore the communication until the next START condition is sent.

Memory Address: During an I2C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I2C Communication

Writing to a Slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember that the master must read the slave's acknowledgement during all byte-write operations.

Reading from a Slave: To read from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition.

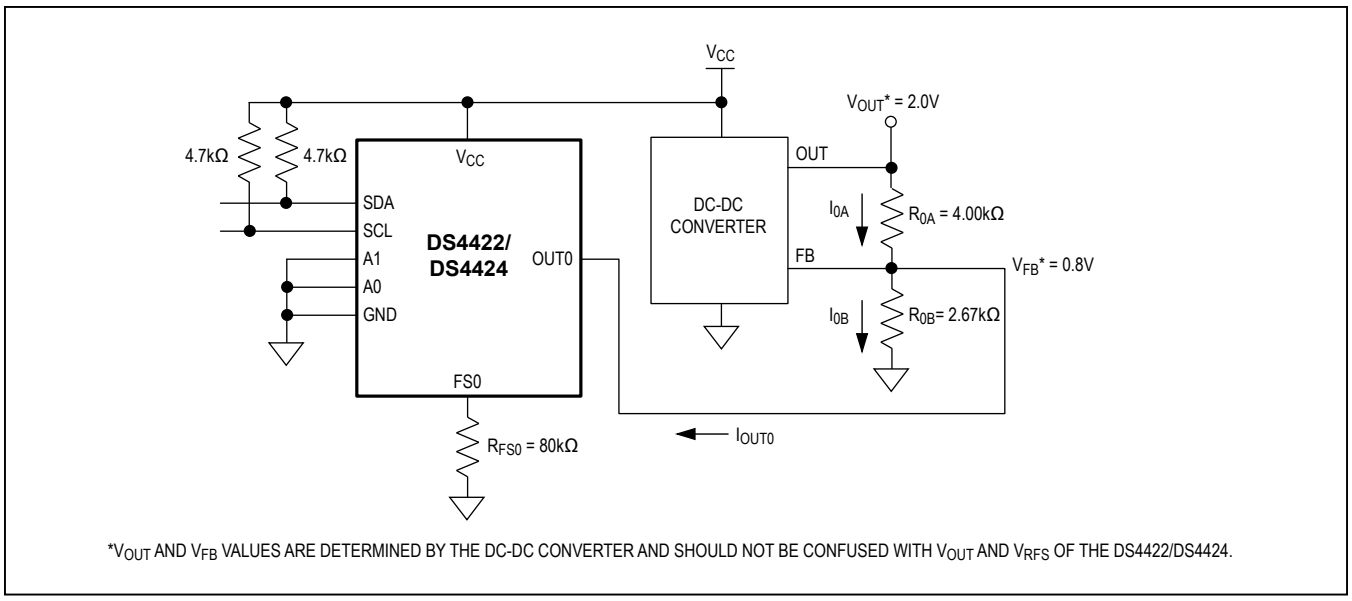


Figure 3. Example Application Circuit

Applications Information

Example Calculations for an Adjustable Power Supply

In this example, the *Typical Operating Circuit* is used as a base to create Figure 3, a DC-DC output voltage of 2.0V with ±20% margin. The adjustable power supply has a DC-DC converter output voltage, V_{OUT}, of 2.0V and a DC-DC converter feedback voltage, V_{FB}, of 0.8V. To determine the relationship of R_{0A} and R_{0B}, start with the equation:

$$V_{FB} = \frac{R_{0B}}{R_{0A} + R_{0B}} \times V_{OUT}$$

Substituting V_{FB} = 0.8V and V_{OUT} = 2.0V, the relationship between R_{0A} and R_{0B} is determined to be:

$$R_{0A} \approx 1.5 \times R_{0B}$$

I_{OUT0} is chosen to be 100µA (midrange source/sink current for the DS4422/DS4424). Summing the currents into the feedback node produces the following:

$$I_{OUT0} = I_{R0B} - I_{R0A}$$

Where:

$$I_{R0B} = \frac{V_{FB}}{R_{0B}}$$

And:

$$I_{R0A} = \frac{V_{OUT} - V_{FB}}{R_{0A}}$$

To create a 20% margin in the supply voltage, the value of V_{OUT} is set to 2.4V. With these values in place, R_{0B} is calculated to be 2.67kΩ, and R_{0A} is calculated to be 4.00kΩ. The current DAC in this configuration allows the output voltage to be moved linearly from 1.6V to 2.4V using 127 settings. This corresponds to a resolution of 6.3mV/step.

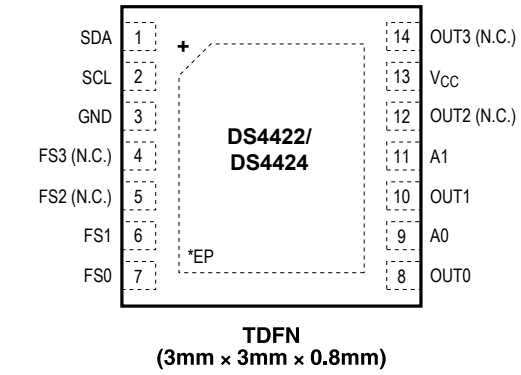
V_{CC} Decoupling

To achieve the best results when using the DS4422/DS4424, decouple the power supply with a 0.01µF or 0.1µF capacitor. Use a high-quality ceramic surfacemount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

Power Rail Considerations

Given that the absolute maximum rating for the OUT pins is V_{CC} + 0.5V, it is recommended that the DS4424 power rail be brought up before or at the same time as the power rail of the source it is controlling.

Pin Configuration



TDFN
(3mm × 3mm × 0.8mm)

( ) INDICATES DS4422 ONLY.
*EXPOSED PAD

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
14 TDFN-EP	T1433+2	21-0137

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/08	Initial release.	—
1	7/09	Added the *Power Rail Considerations* section.	9
2	9/17	Replaced TOC04 in *Typical Operating Characteristics* section	4

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