THE DATASHEET OF

DS3930E+T&R

Rev 0; 4/03

DALLAS SEMICONDUCTOR MAXIM

Hex Nonvolatile Potentiometer with I/O and Memory

General Description

The DS3930 contains six 256-position nonvolatile (NV) potentiometers, 64 bytes of NV user EEPROM memory, and four programmable NV I/O pins. The six potentiometers all share a common low side. The potentiometers are separated into two groups of three 50kΩ potentiometers in parallel. Each group of three potentiometers shares a common high side and forms an equivalent resistance of 16.6kΩ (three 50kΩ potentiometers in parallel).

Applications

RF Transceivers

Voltage References

Power Supply Calibration

Mobile Phones and PDAs

Fiber Optic Transceiver Modules

Portable Electronics

Radio Tuners

Small, Low-Cost Replacement for Mechanical Potentiometers

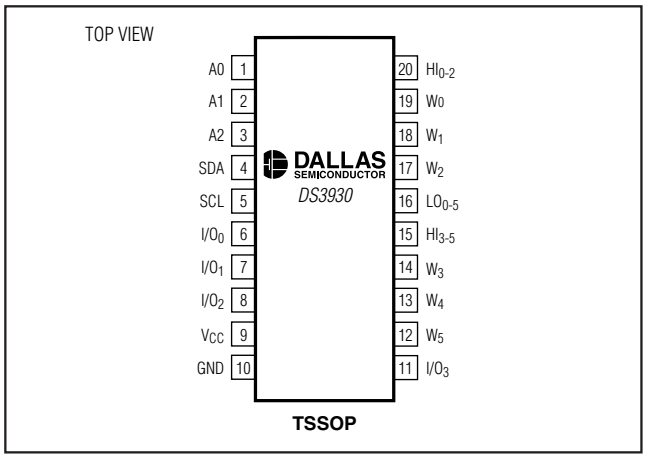
Features

- **Six 256-Position NV Potentiometers**
- **Four General-Purpose NV I/O Pins**
- **64 Bytes of User EEPROM Memory**
- **0 to 5.5V on Any Potentiometer Terminal, Independent of V_{CC}**
- **All Six Potentiometers Share a Common Low Side**
- **Potentiometers Separated into Two Groups of Three Potentiometers, Each Sharing a Common High Side**
- **2-Wire Serial Interface**
- **Wide Supply Range (2.7V to 5.5V)**
- **Up to Eight DS3930s Can Share the Same 2-Wire Bus**

Ordering Information

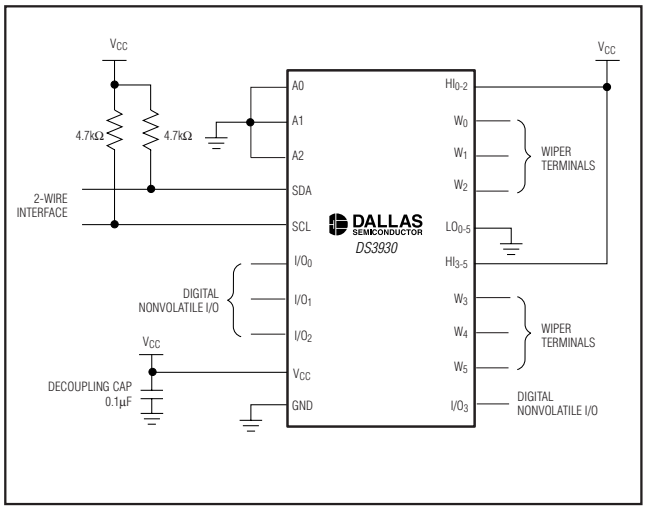
PART	PIN-PACKAGE
DS3930E	20 TSSOP

Pin Configuration



TSSOP

Typical Operating Circuit



Hex Nonvolatile Potentiometer with I/O and Memory

ABSOLUTE MAXIMUM RATINGS

Voltage on V_{CC} Relative to Ground ..... -0.5V to +6.0V
Voltage on I/O_0, I/O_1, I/O_2, I/O_3, SDA, SCL, A0, A1, and A2 Relative to Ground* ..... -0.5V to (V_{CC} + 0.5V)
Voltage on LO_{0-5}, W_{0-5}, HI_{0-2}, and HI_{3-5} Relative to Ground .....-0.5V to +6.0V
Current Through W_{0-5}..... ±1mA

Operating Temperature Range ..... -40°C to +85°C
Programming Temperature Range .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature..... See IPC/JEDEC J-STD-020A

**This voltage must not exceed 6.0V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -40° to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	+2.7		+5.5	V
Input Logic 1 (SDA, SCL, A0, A1, A2, I/O_0, I/O_1, I/O_2, I/O_3)	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0 (SDA, SCL, A0, A1, A2, I/O_0, I/O_1, I/O_2, I/O_3)	V_{IL}		-0.3		0.3 x V_{CC}	V
Wiper Current	I_W		-1		+1	mA
Potentiometer Terminals (LO_{0-5}, W_{0-5}, HI_{0-2}, and HI_{3-5})		V_{CC} = +2.7V to +5.5V	-0.3		+5.5	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V; T_A = -40°C to +85°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage	I_{IL}		-1		+1	µA
Low-Level Output Voltage (SDA, I/O_0, I/O_1, I/O_2, I/O_3)	V_{OL1}	3mA sink current	0		0.4	V
	V_{OL2}	6mA sink current	0		0.6	V
I/O Capacitance	$C_{I/O}$				10	pF
I/O Pullup Resistor Value	$R_{I/O}$		3.5	5	7.0	kΩ
Standby Current	I_{STBY}	3V (Note 2)		160	300	µA
		5V (Note 2)		195	350	

ANALOG RESISTOR CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V; T_A = -40°C to +85°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
End-to-End Resistance		T_A = +25°C (three 50kΩ pots in parallel)	13.2	16.5	19.8	kΩ
Wiper Resistance	R_W			400	1000	Ω
Factory Default Wiper Setting				FF		Hex
Factory Default I/O Setting				0F		Hex
POT-to-POT Matching			-1		+1	LSB
Differential Linearity			-0.5		+0.5	LSB
Integral Linearity			-1		+1	LSB
End-to-End Temperature Coefficient		3 potentiometers in parallel	-250	0	+250	ppm/°C
Ratiometric Temperature Coefficient				2		ppm/°C

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V; T_A = -40°C to +85°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency (Note 3)	f_{SCL}	Fast mode	0		400	kHz
		Standard mode	0		100	
Bus Free Time Between STOP and START Condition (Note 3)	t_{BUF}	Fast mode	1.3			µs
		Standard mode	4.7			
Hold Time (Repeated) START Condition (Notes 3 and 4)	$t_{HD:STA}$	Fast mode	0.6			µs
		Standard mode	4.0			
Low Period of SCL Clock (Note 3)	t_{LOW}	Fast mode	1.3			µs
		Standard mode	4.7			
High Period of SCL Clock (Note 3)	t_{HIGH}	Fast mode	0.6			µs
		Standard mode	4.0			

Hex Nonvolatile Potentiometer with I/O and Memory

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.5V; T_A = -40°C to +85°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Hold Time (Notes 3, 5, 7)	$t_{HD:DAT}$	Fast mode	0		0.9	µs
		Standard mode	0		0.9	
Data Setup Time (Note 3)	$t_{SU:DAT}$	Fast mode	100			ns
		Standard mode	250			
Start Setup Time (Note 3)	$t_{SU:STA}$	Fast mode	0.6			µs
		Standard mode	4.7			
Rise Time of Both SDA and SCL Signals (Note 7)	t_R	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		1000	
Fall Time of Both SDA and SCL Signals (Note 7)	t_F	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		300	
Setup Time for STOP Condition	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.0			
Capacitive Load for Each Bus	C_B	(Note 7)			400	pF
EEPROM Write Time	t_W	(Note 8)		5	20	ms

EEPROM CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V; T_A = -40°C to +85°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Writes		+70°C	50,000			

Note 1: All voltages are referenced to ground.

Note 2: I_{STBY} specified for V_{CC} equal 3.0V and 5.0V, SDA = SCL = V_{CC}, and $I/O_0 = I/O_1 = I/O_2 = I/O_3 = A0 = A1 = A2 = GND$.

Note 3: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} > 250ns$ must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT} = 1000ns + 250ns = 1250ns$ before the SCL line is released.

Note 4: After this period, the first clock pulse is generated.

Note 5: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

Note 6: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH\ MIN}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

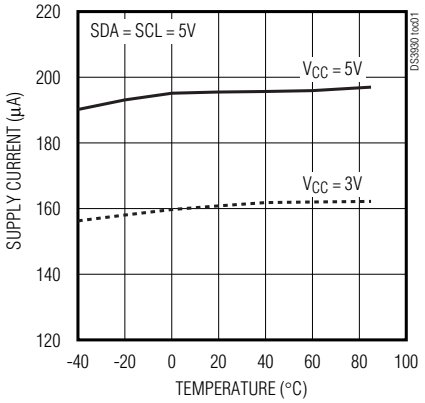
Note 7: C_B—total capacitance of one bus line in picofarads, timing referenced to $0.9V_{CC}$ and $0.1V_{CC}$.

Note 8: EEPROM write begins after a STOP condition occurs.

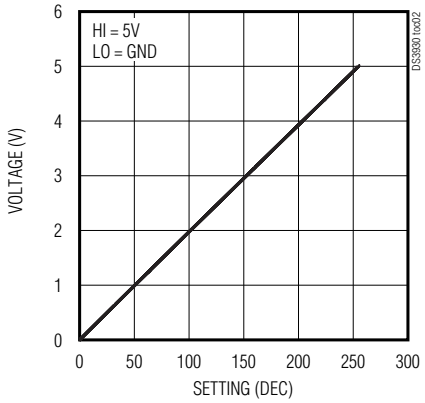
Typical Operating Characteristics

(V_{CC} = 5.0V; T_A = +25°C, unless otherwise specified.)

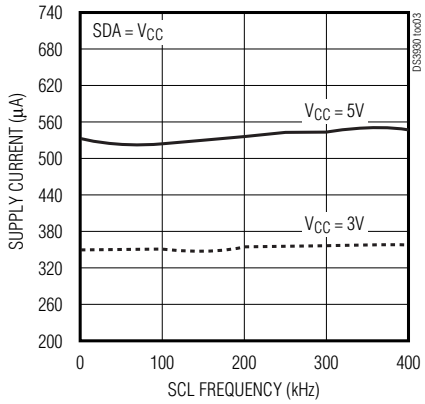
SUPPLY CURRENT vs. TEMPERATURE



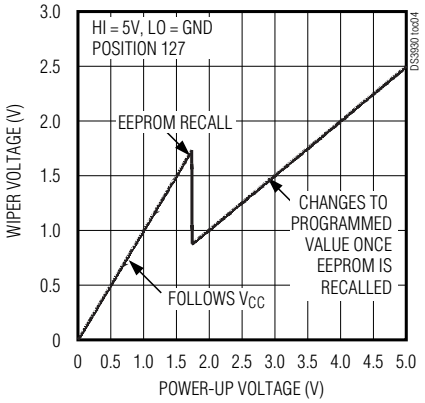
WIPER VOLTAGE vs. WIPER SETTING



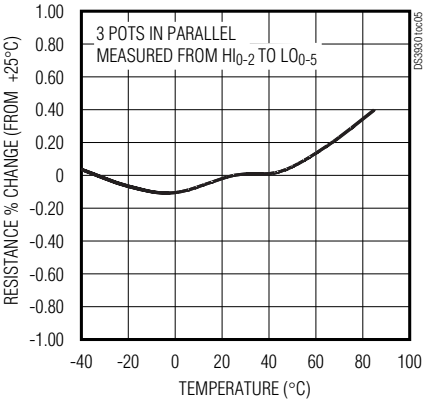
ACTIVE SUPPLY CURRENT vs. SCL FREQUENCY



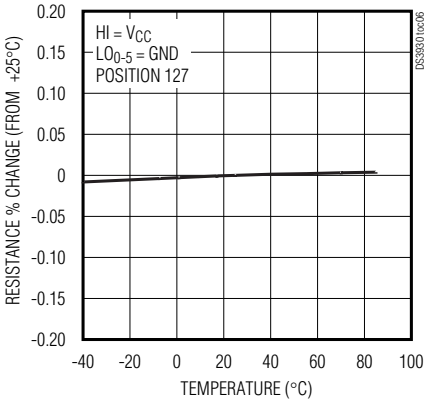
WIPER VOLTAGE vs. POWER-UP VOLTAGE



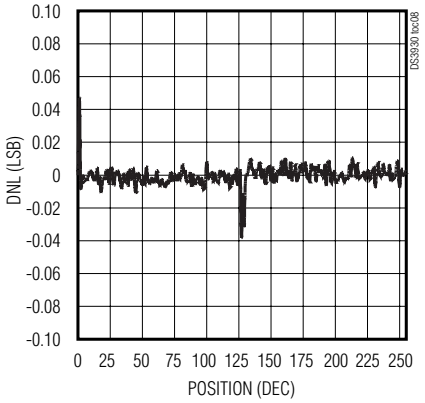
END-TO-END RESISTANCE % CHANGE FROM +25°C vs. TEMPERATURE



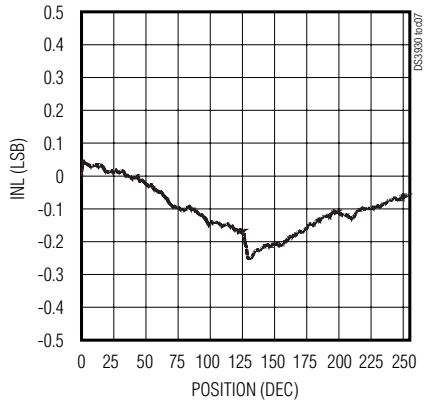
VOLTAGE DIVIDER % CHANGE FROM +25°C vs. TEMPERATURE



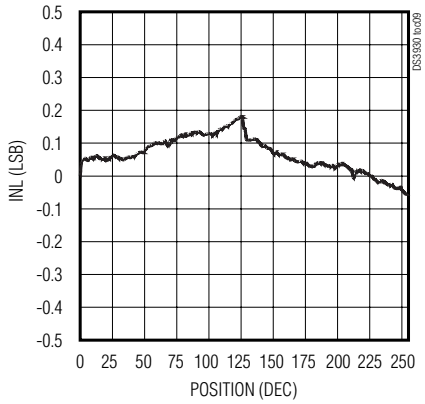
ALL POTS DNL (LSB)



POTS 0, 2, 4, INL (LSB)



POTS 1, 3, 5 INL (LSB)



Hex Nonvolatile Potentiometer with I/O and Memory

Pin Description

PIN	NAME	FUNCTION
1	A0	Address Input. The address input pins determine the 2-wire address of the device.
2	A1	Address Input
3	A2	Address Input
4	SDA	2-Wire Serial Data I/O. This pin is for serial data transfer to and from the device.
5	SCL	2-Wire Serial Clock Input. The serial clock input is used to clock data into and out of the device.
6	I/O_0	General-Purpose NV I/O Pin
7	I/O_1	General-Purpose NV I/O Pin
8	I/O_2	General-Purpose NV I/O Pin
9	V_{CC}	Supply Voltage
10	GND	Ground
11	I/O_3	General-Purpose NV I/O Pin
12	W_5	Wiper Terminal of Potentiometer 5
13	W_4	Wiper Terminal of Potentiometer 4
14	W_3	Wiper Terminal of Potentiometer 3
15	HI_{3-5}	High-End Terminal of Potentiometers 3 to 5. This is the common high-side terminal of potentiometers 3, 4, and 5.
16	LO_{0-5}	Low-End Terminal of the Potentiometers. This is the common low-side terminal of all six potentiometers.
17	W_2	Wiper Terminal of Potentiometer 2
18	W_1	Wiper Terminal of Potentiometer 1
19	W_0	Wiper Terminal of Potentiometer 0
20	HI_{0-2}	High-End Terminal of Potentiometers 0 to 2. This is the common high-side terminal of potentiometers 0, 1, and 2.

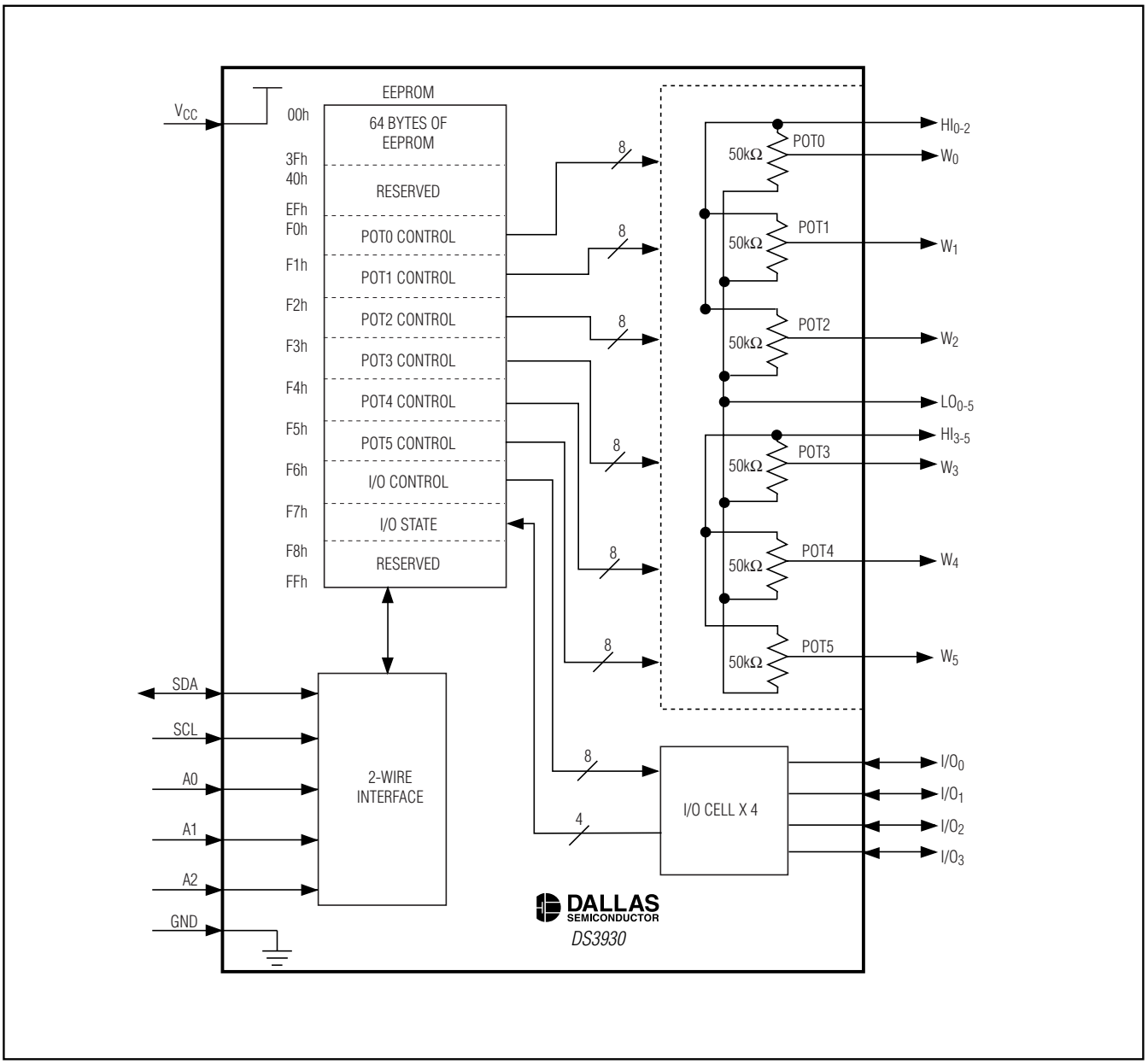


Figure 1. DS3930 Functional Diagram

Detailed Description

The DS3930 contains six NV potentiometers with 64 bytes of NV user memory (EEPROM), and four programmable NV I/O pins. Figure 1 is a functional diagram of the DS3930.

Potentiometers

The six potentiometers share a common low side and are separated into two groups of three potentiometers, each group sharing a common high side. The six 256-position potentiometers are controllable using six 8-bit EEPROM registers through the 2-wire interface.

Hex Nonvolatile Potentiometer with I/O and Memory

I/O Signals

The I/O pins can be used as general-purpose digital I/O signals. The I/O pins have CMOS outputs with an internal pullup resistor (see Figure 2). The I/O pins are configured with the I/O Control register (F6h) and monitored with the I/O State register (F7h). The I/O Control register controls the state of the internal pullup resistor ($R_{I/O}$) with bits 7 to 4 and the I/O pin setting with bits 3 to 0 (see Table 1). The read-only values of the I/O State register contains the values of the I/O pin setting bits of the I/O Control register unless the I/O output is tri-stated. When the I/O is tri-stated the I/O State register will read high or low depending on the external source on the I/O pin. Since the I/O pins are controlled by EEPROM, the number of writes is limited.

Table 1. I/O Pin Truth Table

PULLUP CTRL (I/O CONTROL REGISTER) (BITS 7 TO 4)	I/O PIN SETTING (I/O CONTROL REGISTER) (BITS 3 TO 0)	I/O PIN OUTPUT
0	0	0
0	1	1
1	0	0
1	1	Pullup disabled (HI-Z)

Memory

The memory map is shown in Table 2.

Table 2. Memory Map

ADDRESS	BIT	DEFAULT (HEX)	FUNCTION
00h to 3Fh		FF	64 bytes of general-purpose EEPROM
40h to EFh		FF	Reserved
F0h		FF	Controls potentiometer 0
F1h		FF	Controls potentiometer 1
F2h		FF	Controls potentiometer 2
F3h		FF	Controls potentiometer 3
F4h		FF	Controls potentiometer 4
F5h		FF	Controls potentiometer 5
F6h		0F	I/O Control
	Bit 7		Set to 0 to enable I/O_3 pullup, set to 1 to disable pullup
	Bit 6		Set to 0 to enable I/O_2 pullup, set to 1 to disable pullup
	Bit 5		Set to 0 to enable I/O_1 pullup, set to 1 to disable pullup
	Bit 4		Set to 0 to enable I/O_0 pullup, set to 1 to disable pullup
	Bit 3		Sets I/O_3 to 0 or 1
	Bit 2		Sets I/O_2 to 0 or 1
	Bit 1		Sets I/O_1 to 0 or 1
	Bit 0		Sets I/O_0 to 0 or 1
F7h		0X	I/O State
	Bit 7		0
	Bit 6		0
	Bit 5		0
	Bit 4		0
	Bit 3		Contains state of I/O_3 pin (read only)
	Bit 2		Contains state of I/O_2 pin (read only)
	Bit 1		Contains state of I/O_1 pin (read only)
	Bit 0		Contains state of I/O_0 pin (read only)
F8h to FFh		FF	Reserved

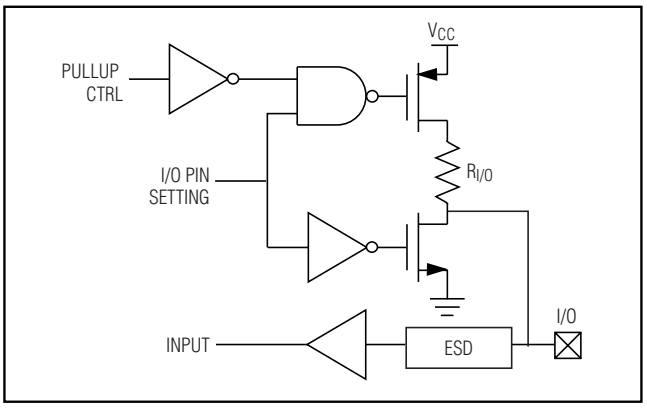


Figure 2. I/O Cell

2-Wire Serial Port Operation

The 2-wire serial port interface supports a bidirectional data transmission protocol with device addressing. A device that sends data on the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master." The devices that are controlled by the master are "slaves." The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the start and stop conditions. The DS3930 operates as a slave on the 2-wire bus. Connections to the bus are made through the open-drain I/O lines, SDA and SCL. The following I/O terminals control the 2-wire serial port: SDA, SCL, and A0. Timing diagrams for the 2-wire serial port can be found in Figures 3 and 5. Timing information for the 2-wire serial port is provided in the *AC Electrical Characteristics* table for 2-wire serial communications.

The following bus protocol has been defined:

- Data transfer can be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy: Both data and clock lines remain high.

Start Data Transfer: A change in the state of the data line from high to low while the clock is high defines a start condition.

Stop Data Transfer: A change in the state of the data line from low to high while the clock line is high defines the stop condition.

Data Valid: The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line can be changed during the low period of the clock signal. There is one clock pulse per bit of data. Figures 3 and 5 detail how data transfer is accomplished on the 2-wire bus. Depending upon the state of the R/W bit, two types of data transfer are possible.

Each data transfer is initiated with a start condition and

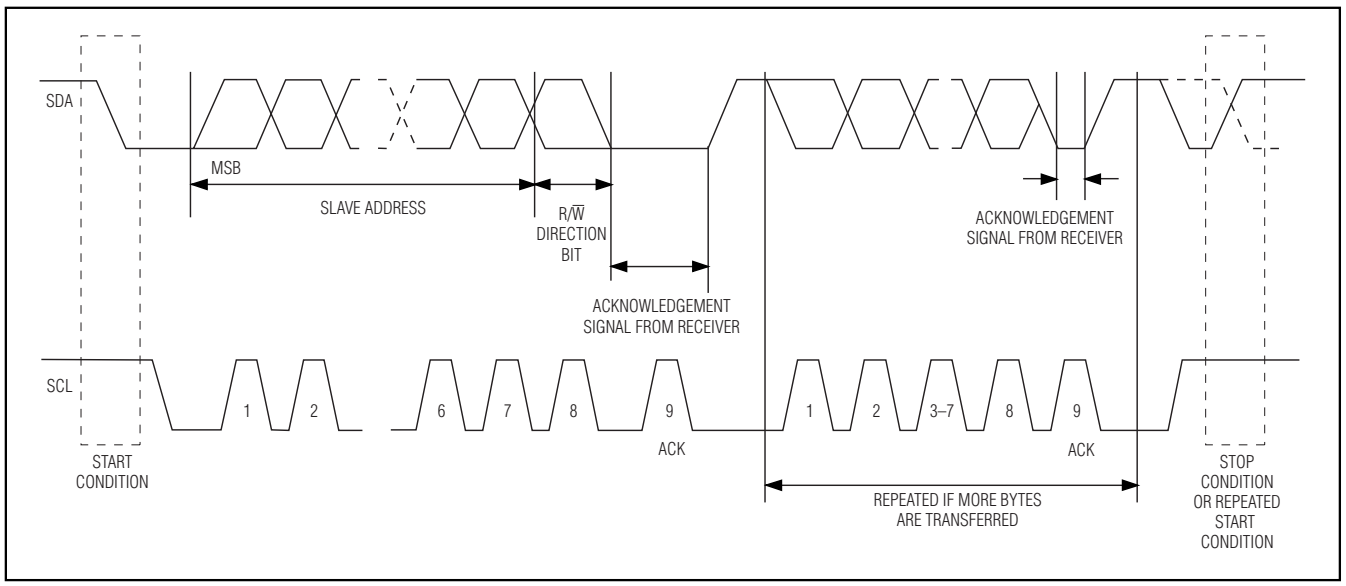


Figure 3. 2-Wire Data Transfer Protocol

Hex Nonvolatile Potentiometer with I/O and Memory

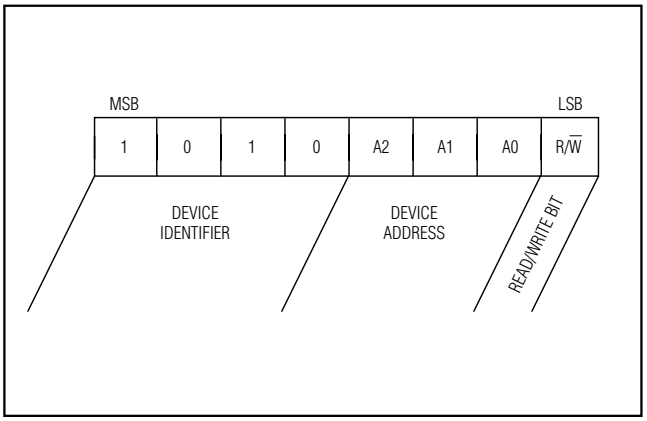


Figure 4. Slave Address

terminated with a stop condition. The number of data bytes transferred between start and stop conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Within the bus specifications, a regular mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined. The DS3930 works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the byte has been received. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the stop condition.

Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the command/control byte. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.

Data transfer from a slave transmitter to a master receiver. The master transmits the first byte (the command/control byte) to the slave. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not acknowledge can be returned.

The master device generates all serial clock pulses and the start and stop conditions. A transfer is ended with a stop condition or with a repeated start condition. Since a repeated start condition is also the beginning of the next serial transfer, the bus is not released.

The DS3930 can operate in the following three modes:

1) **Slave Receiver Mode:** Serial data and clock are received through SDA and SCL, respectively. After each byte is received, an acknowledge bit is transmitted. Start and stop conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after the slave (device) address and direction bit have been received.
2) **Slave Transmitter Mode:** The first byte is received and handled as in the slave receiver mode. However, in this mode the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS3930 while the serial clock is input on SCL. Start and stop conditions are recognized as the beginning and end of a serial transfer.
3) **Slave Address:** This is the first byte received following the start condition from the master device. The slave address consists of a 4-bit control code. For the DS3930, this is set as 1010 binary for read/write operations. The next bits of the slave address are the device address (A2–A0). The last bit of the slave address (R/W) defines the operation to be performed. When set to a '1,' a read operation is selected, and when set to a '0,' a write operation is selected (see Figure 4).

Following the start condition, the DS3930 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the 1010 device identifier, the appropriate device address bit, and the read/write bit, the slave device outputs an acknowledge signal on the SDA line.

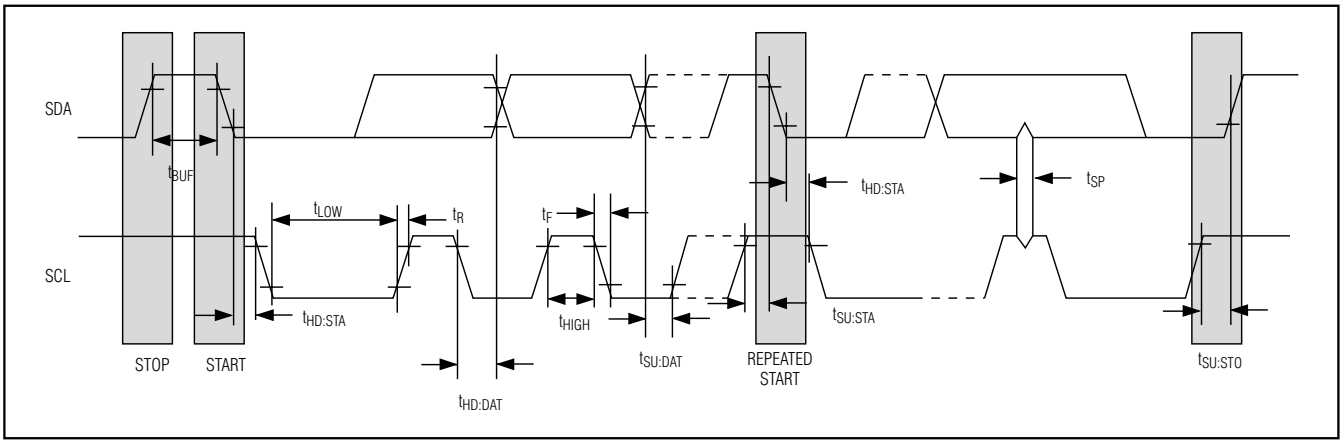


Figure 5. 2-Wire AC Characteristics

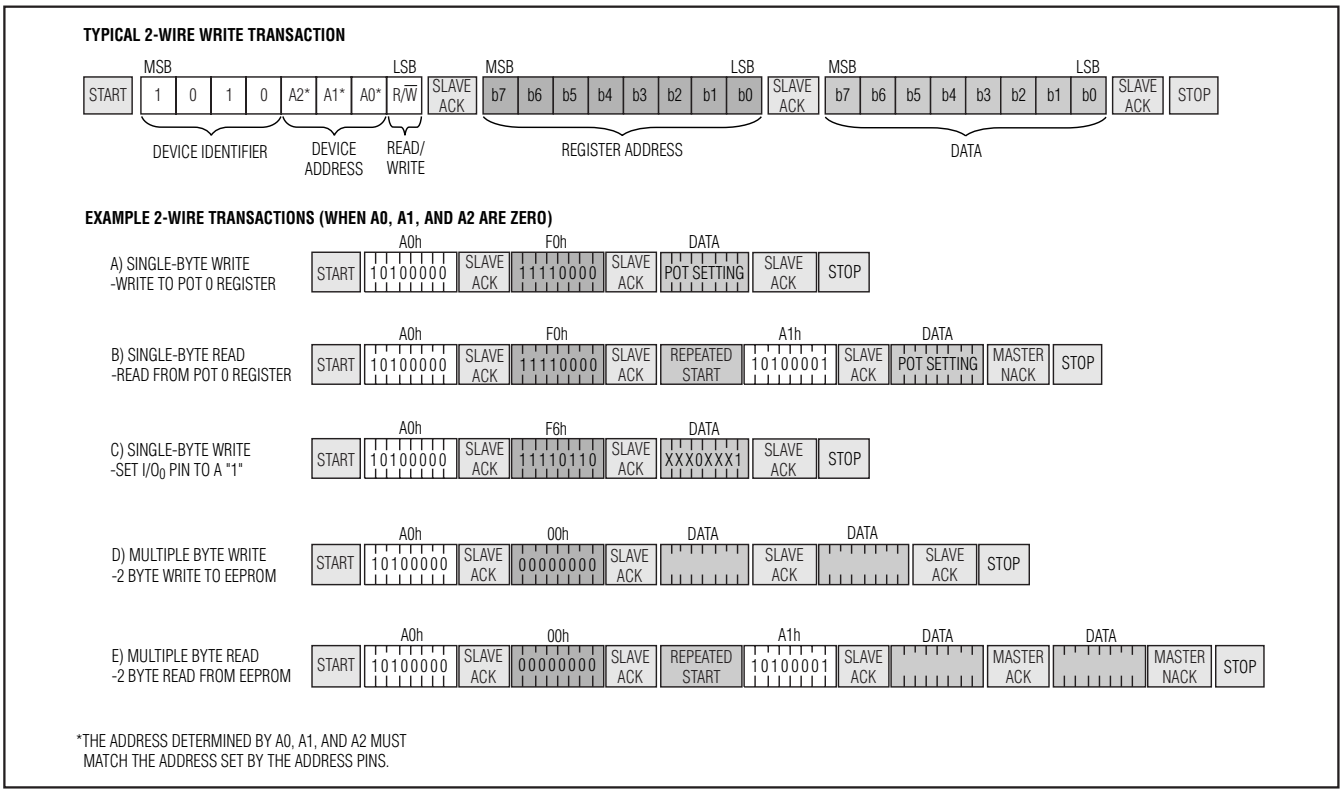


Figure 6. Example 2-Wire Transactions

Applications Information

Power Supply Decoupling

To achieve the best results when using the DS3930, decouple the power supply with a 0.1µF high-quality, ceramic, surface-mount capacitor. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications. The capacitor should be placed as close as possible to the V_{CC} and GND pins.

Hex Nonvolatile Potentiometer with I/O and Memory

Wiper Resistance

One difference between digital potentiometers and mechanical potentiometers is the wiper resistance. The wiper resistance (R_W) is a result of the interconnecting materials on the IC between the internal resistive elements and the wiper pin. This can be modeled by using an ideal potentiometer, with a resistance of R_W connected between the ideal wiper and wiper terminal of the digital potentiometer.

Chip Information

TRANSISTOR COUNT: 27,000

SUBSTRATE CONNECTED TO GROUND.

Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View DS3930E+T&R on WIN SOURCE
- Maxim Integrated Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management