



**THE DATASHEET OF
DS26521DK**



GENERAL DESCRIPTION

The DS26521DK is an easy-to-use evaluation kit for the DS26521 T1/E1/J1 single-chip transceiver (SCT). The DS26521DK is intended to be used as a stand-alone system. The board comes complete with a transceiver, transformer, termination resistors, configuration switches, network connectors, microprocessor, and RS-232 connector. The on-board processor and Dallas' ChipView software give point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal and interrupt status, as well as multiple clock and signal routing configurations.

Windows is a registered trademark of Microsoft Corp.

DESIGN KIT CONTENTS

DS26521DK PC Board

CD_ROM Including:

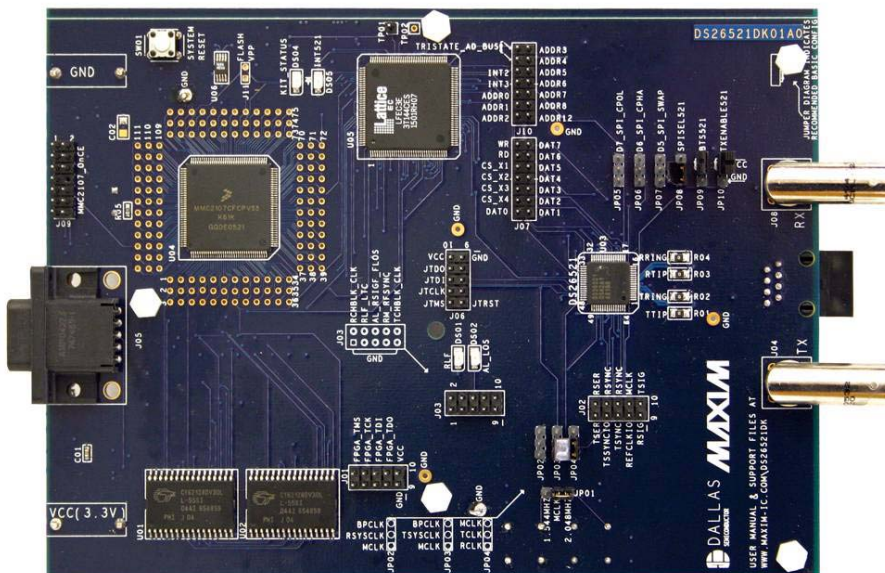
- ChipView Software
- DS26521 Definition Files
- DS26521 Initialization Files
- DS26521DK Data Sheet
- DS26521 Data Sheet
- DS26521 Errata Sheet (if applicable)

FEATURES

- Demonstrates Key Functions of DS26521 T1/E1/J1 SCT
- Includes Transceiver, Transformers, and Termination Passives
- BNC Connections for 75Ω E1
- RJ48 Connector for 120Ω E1 and 100Ω T1
- On-Board Processor and ChipView Software Provide Point-and-Click Access to the DS26521 Register Set
- Accessible Address/Data Bus with Tri-State Control to Allow Interface for External Processor
- All Equipment-Side Framer Pins are Easily Accessible for External Data Source/Sink
- LEDs for Loss-of-Signal and Interrupt Status
- Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs

ORDERING INFORMATION

PART	DESCRIPTION
DS26521DK	Design Kit for DS26521



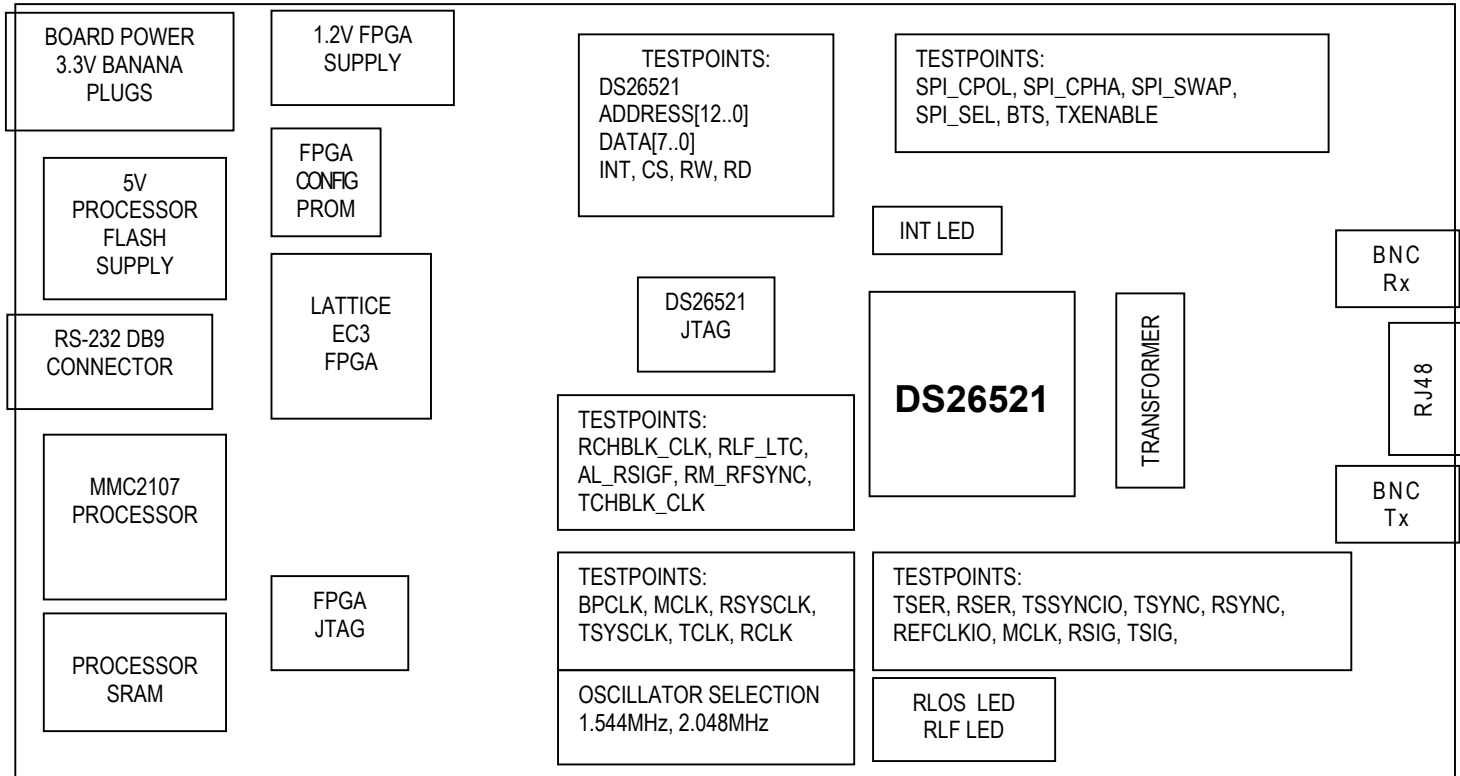
COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER/PART
C01, CB07, CB08, CB10, CB12, CB16, CB18, CB19, CB21, CB23, CB26, CB32, CB39–CB41	15	0.1 μ F \pm 10%, 16V ceramic capacitors (0603)	Phycomp 06032R104K7B20D
C02	1	1 μ F \pm 10%, 16V ceramic capacitor (1206)	Panasonic ECJ-3YB1C105K
CB01, CB02, CB05, CB06, CB11, CB14, CB20, CB28, CB31, CB34, CB36, CB37	12	10 μ F \pm 20%, 10V ceramic capacitors (1206)	Panasonic ECJ-3YB1A106M
CB03, CB04, CB13, CB17, CB24, CB25, CB29, CB38	8	4.7 μ F, 6.3V multilayer ceramic capacitors (0603)	Digi-Key ECJ-1VB0J475M
CB09	1	560pF \pm 5%, 50V ceramic capacitor (1206)	Digi-Key 478-1489-2-ND
CB15, CB22, CB27, CB33, CB35	5	0.1 μ F \pm 20%, 16V X7R ceramic capacitors (0603)	Arrow 0603YC104MAT2
CB30	1	470 μ F \pm 20%, 6.3V tantalum capacitor (D case)	Digi-Key 399-3002-1-ND
DB01	1	1A 40V Schottky diode	International Rectifier 10BQ040
DS01, DS02, DS05	3	Red LEDs, SMD	Panasonic LN1251C
DS04	1	Green LED, SMD	Panasonic LN1351C
GND_TP01–GND_TP06	6	Standard ground clips	Keystone 4954
H1–H5, H10	6	Kit, 4-40 hardware, 0.50 nylon standoff and nylon hex-nut	Lab Stock 4-40KIT4
J01–J03, J06	4	10-pin, dual-row, vertical terminal strips	Samtec TSW-105-07-T-D
J04, J08	2	5-pin right-angle BNC connectors	Trompetor UCBJR220
J05	1	DB9 right-angle connector (long case)	AMP 747459-1
J07, J10	2	Nonpopulated 14-pin, dual-row, vertical headers	Samtec NOPOP-HDR-TSW-107-14-T-D
J09	1	100-mil, 2 x 7-position jumper	Lab Stock
J11	1	100-mil, 2-position jumper	Lab Stock
JB01	1	Red banana plug socket, horizontal	Mouser Electronics 164-6219
JB02	1	8-pin single-port RJ48 connector	Molex 15-43-8588
JB03	1	Black banana plug socket, horizontal	Mouser Electronics 164-6218
JP01–JP09, JP10	10	100-mil, 3-position jumpers	Lab Stock
R01–R04, RB47	5	0 Ω \pm 5%, 1/8W resistors (1206)	Panasonic ERJ-8GEYJ0R00V
R05, RB35–RB40, RB45, RB46	9	1.0k Ω \pm 5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ102V

DESIGNATION	QTY	DESCRIPTION	SUPPLIER/PART
R06, R07, RB06, RB07, RB44, RB54, RB55	7	10k Ω \pm 5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ103V
RB01–RB05, RB11, RB23–RB26, RB28, RB29	12	30 Ω \pm 5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ300V
RB08, RB09, RB10, RB14–RB22, RB27, RB32, RB33, RB43, RB48	17	10k Ω \pm 5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ103V
RB12, RB13, RB50	3	330 Ω \pm 5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ331V
RB30, RB31	2	61.9 Ω \pm 1%, 1/10W resistors (0805)	Panasonic ERJ-6ENF61R9V
RB34	1	1.0M Ω \pm 5%, 1/16W resistor (0603)	Panasonic ERJ-3GEYJ105V
RB41	1	51.1 Ω \pm 1%, 1/10W resistor (0805)	Panasonic ERJ-6ENF51R1V
RB42	1	10k Ω \pm 1%, 1/10W resistor (0805)	Panasonic ERJ-6ENF1002V
RB51	1	0 Ω \pm 5%, 1/16W resistor (0603)	Panasonic ERJ-3GEY0R00V
RB52	1	330 Ω \pm 5%, 1/16W resistor (0603)	Panasonic ERJ-3GEYJ331V
RB53	1	1.0k Ω \pm 5%, 1/16W resistor (0603)	Panasonic ERJ-3GEYJ102V
SW01	1	4-pin single-pole switch	Panasonic EVQPAE04M
TB01	1	16-pin SMT transformer	Pulse Engineering TX1099
TP01, TP02	2	Testpoints, one plated hole DO NOT STUFF	Lab Stock
U01, U02	2	Cypress SRAM	Lab Stock
U03	1	Single T1/E1/J1 transceiver, 64-pin, 10mm x 10mm LQFP	Dallas Semiconductor DS26521
U04	1	MMC2107 processor	Motorola MMC2107
U05	1	1.2V FPGA 144-pin, 20mm x 20mm TQFP	Lattice LFEC3E-3T144C
U06	1	3V to 5V regulating charge pump	Maxim MAX1686HEUA
UB01	1	Dual RS-232 transceivers with 3.3V/5V internal capacitors	MAXIM NA
UB02	1	Microprocessor voltage monitor, 2.93V reset, 4-pin SOT143	Maxim MAX811SEUS-T
UB04	1	SPI serial EEPROM, 2M, 2.7V to 3.6V, 8-pin SO	Atmel AT25F2048N-10SU-2.7
UB05	1	LDO regulator with reset, 1.20V output, 300mA, 6-pin SOT23	Maxim MAX1963EZT120-T
YB01	1	Oscillator, crystal clock 3.3V, 1.544MHz	SaRonix NTH039A3-1.5440

DESIGNATION	QTY	DESCRIPTION	SUPPLIER/PART
YB02	1	Oscillator, crystal clock 3.3V, 2.048MHz	SaRonix NTH039A3-2.0480
XB01	1	8.0MHz low-profile crystal	PEI Sales Inc. EC1-8.000M

BOARD FLOORPLAN



PC BOARD ERRATA

DS26521DK01A0 10/10/2005:

There is no errata for the DS26521DK01A0 design.

DS26521DK02A0 11/22/2005:

There is no errata for the DS26521DK02A0 design.

BASIC OPERATION

This design kit relies upon several supporting files, which are available for downloading on our website at www.maxim-ic.com/DS26521DK QuickView page.

Hardware Configuration

- Supply 3.3V to the banana-plug receptacles marked GND and VCC_3.3V.
- Install the following jumpers (detailed in Table 2):
 - JP01—Connect MCLK to 2.048MHz (for both T1 and E1).
 - Connect JP02 MCLK to RSYSCLK, JP03 MCLK to TSYCLK, JP04 TCLK to RCLK.
 - JP08 SPI_SEL to GND, JP09 BTS to VCC, TXENABLE to VCC.
- From the **Programs** menu, launch the host application named *ChipView.exe*. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select **Programs** → **ChipView** → **ChipView**.

General:

- Upon power-up, the RLF and AL_LOS LEDs (red) will be lit, and the INT LED (red) will not be lit. The board will draw approximately 200mA at power-up.

Quick Setup (Register View)

- The PC will load ChipView, offering a choice among DEMO MODE, REGISTER VIEW, and TERMINAL MODE. Select REGISTER VIEW.
- The program will request a definition file. Navigate to the .def files in the T1 or E1 folder, then select the file named *DS26521_GLOBAL_T1.def* (T1 mode) or *DS26521_GLOBAL_E1.def* (E1 mode). Note: Through the “links” section this will also load the LIU def file and framer def file.
- The *Register View Screen* will appear, showing the register names, acronyms, and values for the DS26521.
- Predefined register settings for several functions are available as initialization files.
 - .ini files are loaded by selecting the menu **File**→**Reg Ini File**→**Load Ini File**.
 - Load the .ini file *Load_T1_LBO0_0_133_impMatchOn.ini* (T1 mode) or *Load_E1_75_impMatchOn.ini* (E1 mode).
 - After loading the .ini file, the following may be observed:
 - The DS26521 begins transmitting AIS with impedance match.
 - The AL_LOS LEDs extinguishes upon external loopback.

Miscellaneous:

- The DS26521 uses three register definition files. All three files are loaded when the *DS26521_GLOBAL*.def* file is loaded. Individual files are selected from the **Def File Selection** menu in ChipView.

ADDRESS MAP

The on-board microcontroller is configured to start the user address space at 0x8100000. All offsets given below are relative to the beginning of the user address space.

Table 1. Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0087	FPGA	Board Identification and FPGA Test Registers
0X1000 to 0X2FFF	DS26521	DS26521 Framer, LIU, and BERT Registers

TESTPOINTS AND CONNECTORS

The DS26521DK has several connectors, testpoints, oscillators, and jumpers. Table 2 provides a description of these signals, given in order of appearance on the PC board, from left to right then top to bottom (with the board held so that the RS-232 connector is on the top edge).

Table 2. Main Board PC Board Configuration

SILKSCREEN REFERENCE	FUNCTION	DEFAULT SETTING	SCHEMATIC PAGE	DESCRIPTION
VCC 3.3V (banana plug)	Power supply VDD	3.3V	2	System VDD. Always connected to power supply.
GND (banana plug)	Power supply Ground	GND	2	System Ground. Always connected to power supply.
J05	RS232 Connector	Connected to Host PC	8	Used for Communication with Host PC. Basic setting is 57.6k baud, 8 bits, no stop bit, 1 parity bit (57.6, 8, N, 1).
J09	OnCE BDM Connector	—	8	OnCE Debug Connector for MMC2107 Processor
SW01	System Reset	—	6	System Reset. Connects to all device reset pins.
J11	Flash VPP Jumper	Not Installed	8	Provides Flash Programming Voltage (5V) to Processor
J01	FPGA, JTAG	—	11	JTAG Connector for Lattice EC3 FPGA
TP01, TP02	FPGA, Testpoint	—	11	FPGA Init and Done Pins
J03	DS26521 Testpoints	—	5	Testpoints for DS26521 Pins: RCHBLK_CLK, RLF_LTC, AL_RSIGF, RM_RFSYNC, TCHBLK_CLK
J06	DS26521 JTAG	—	3	JTAG Connector for DS26521
YB01, YB02 (Bottom side of PC Board)	Oscillators	—	5	Oscillators for 2.048MHz and 1.544MHz
J07, J10	Testpoints	—	10	Testpoints for DS26521 Address/Data Bus and Control Lines
J10.12 + J10.14	Bus Tri-State	Not Jumpered	10	—
JP01	MCLK Selection	Jumpered pins 2+3	5	MCLK Selection: 1.544MHz, 2.048MHz (default)
JP02	RSYSCLK Selection	Jumpered Pins 1+2	5	RSYSCLK Selection: MCLK (default), BPCLK
JP03	TSYSCLK Selection	Jumpered Pins 1+2	5	TSYSCLK Selection: MCLK (default), BPCLK
JP04	TCLK Selection	Jumpered Pins 1.2	5	TCLK Selection: RCLK (default), MCLK
J02	DS26521 Testpoints	—	5	Testpoints for DS26521 Pins: TSER, RSER, TSSYNCIO, TSYNC, RSYNC, REFCLKIO, MCLK, RSIG, TSIG
JP05	SPI_CPOL bias	Not Jumpered	3	SPI_CPOL Selection: Pulldown, Pullup
JP06	SPI_CPHA bias	Not Jumpered	3	SPI_CPHA Selection: Pulldown, Pullup
JP07	SPI_SWAP bias	Not Jumpered	3	SPI_SWAP Selection: Pulldown, Pullup
JP08	SPI_SEL bias	Jumpered Pins 1+2	3	SPI_SEL Selection: Pulldown (default), Pullup
JP09	BTS bias	Jumpered Pins 2+3	3	BTS Selection: Pulldown, Pullup (default)
JP10	TXENABLE bias	Jumpered Pins 2+3	3	TXENABLE Selection: Pulldown, Pullup (default)
J04, J08	Network BNC	—	4	BNC for 75Ω Network Connection
JB02	Network RJ48	—	4	RJ48 Network Connection

DS26521 INFORMATION

For more information about the DS26521, consult the DS26521 data sheet available on our website at www.maxim-ic.com/DS26521. Software downloads are also available for this design kit.

DS26521DK INFORMATION

For more information about the DS26521DK, including software downloads, consult the DS26521DK data sheet available on our website at www.maxim-ic.com/DS26521DK.

TECHNICAL SUPPORT

For additional technical support, please e-mail your questions to telecom.support@dalsemi.com.

SCHEMATICS

The DS26521DK schematics are featured in the following pages.

B 7 6 5 4 3 2 1

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D

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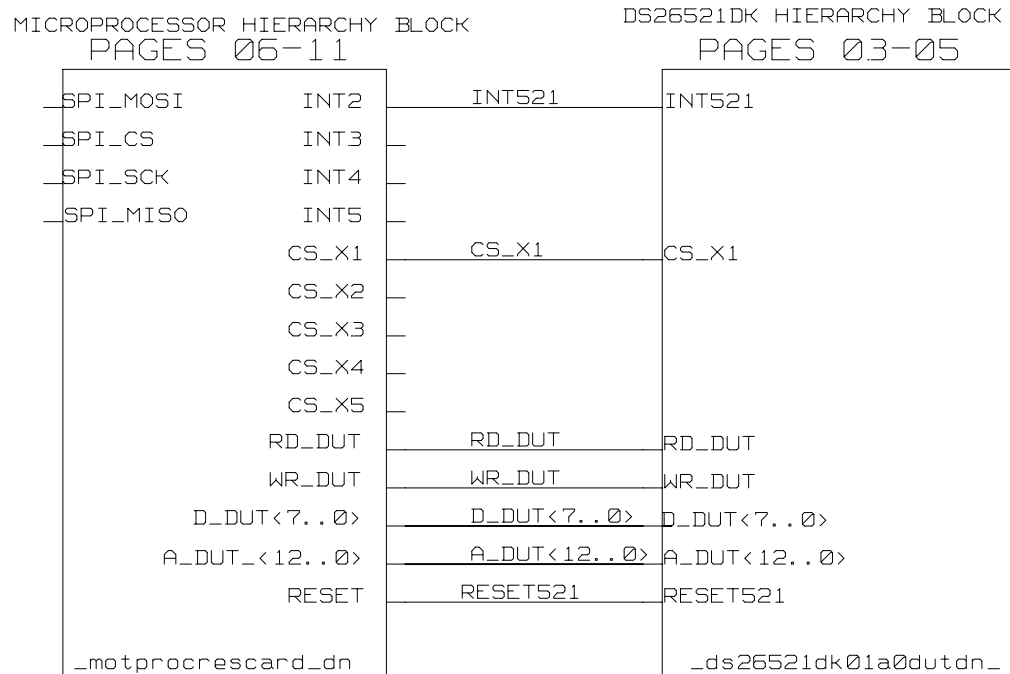
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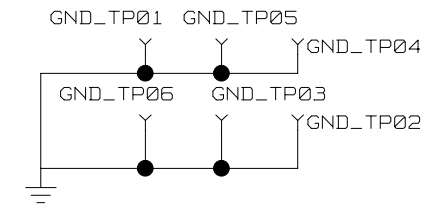
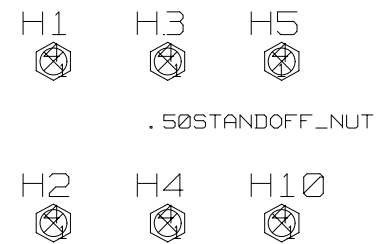
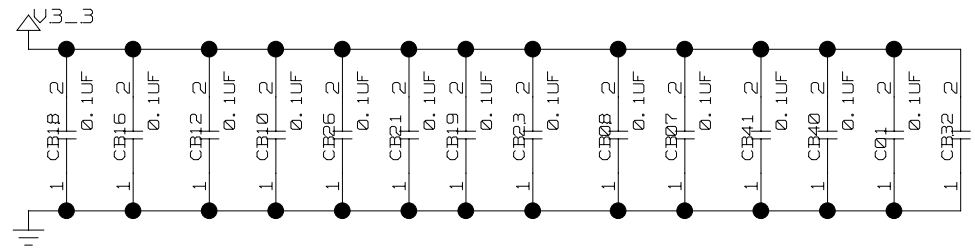
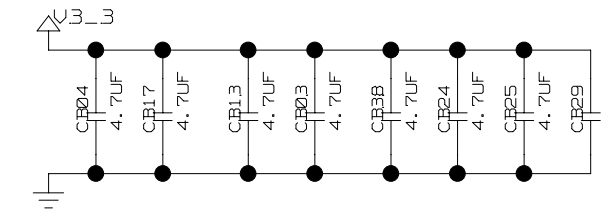
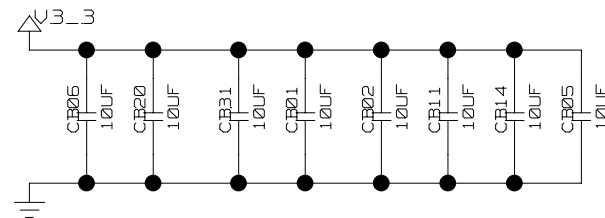
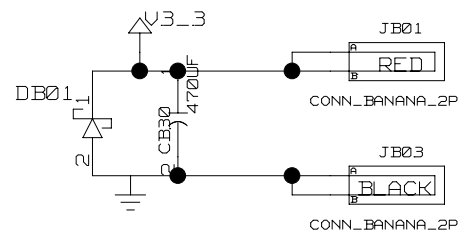
CONTENTS

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PAGE 02:	DECOUPLING / MOUNTING HOLES
DS26521 DESIGN KIT	
PAGES 03-05:	DS26521 DEVICE, LINE BUILDOUT AND TESTPOINTS
PAGES 06-11:	MICROPROCESSOR AND INTERFACE

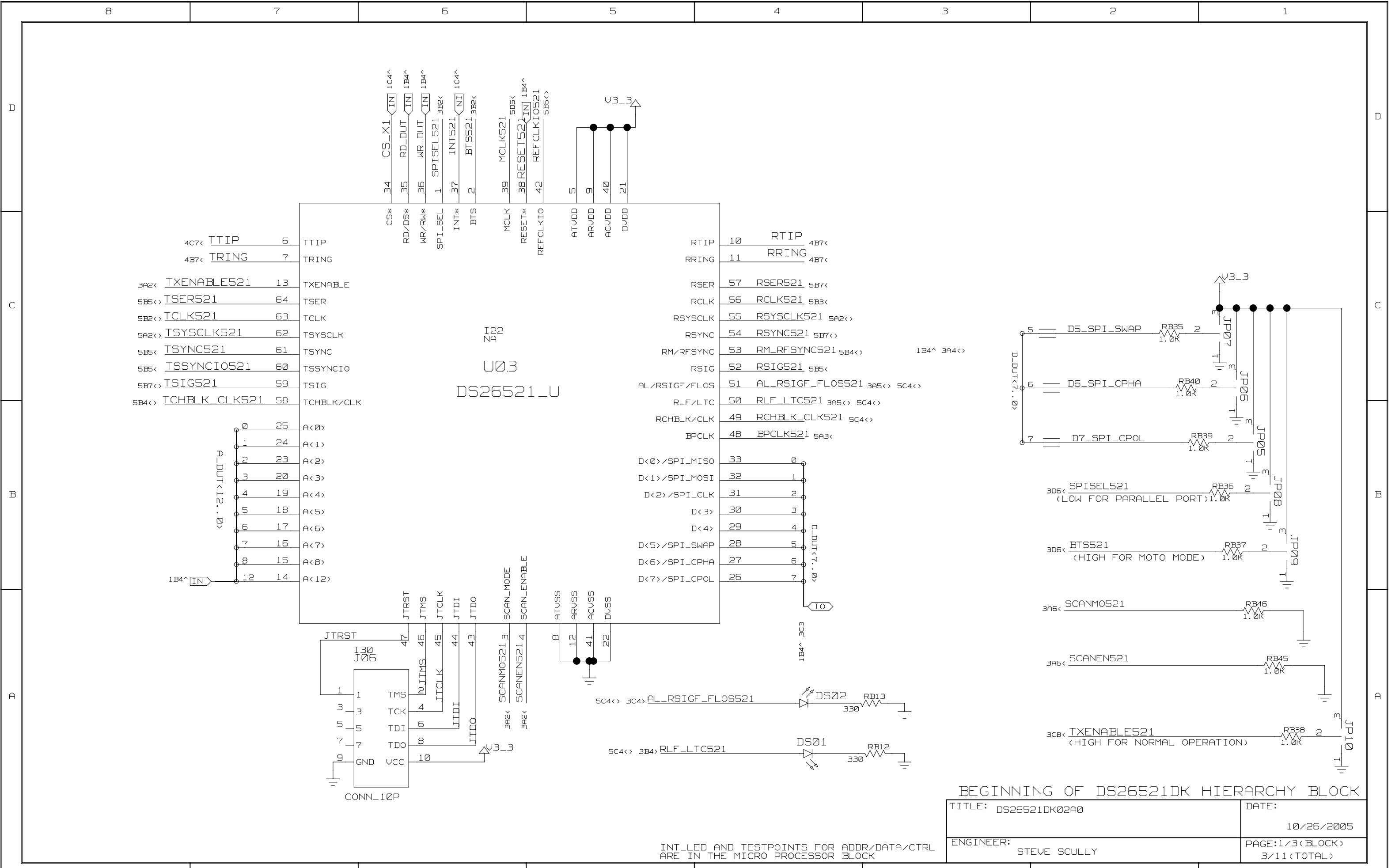
NOTES: EACH HIERARCHY BLOCK IS INDEPENDENT OF THE NEXT.
 ONLY SIGNALS WITH IMPORT/OUTPORT CONNECTORS HAVE CONNECTION OUTSIDE THE HIERARCHY BLOCK. THESE SIGNALS APPEAR AS PINS ON THE HIERARCHY BLOCK CONNECTOR

TITLE: DS26521DK02A0	DATE: 10/26/2005
DS26521DK TOP LEVEL	
ENGINEER: STEVE SCULLY	PAGE: 1/2 (BLOCK) 1/11 (TOTAL)

B 7 6 5 4 3 2 1



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ENGINEER: STEVE SCULLY	PAGE:2/2 (BLOCK) 2/11 (TOTAL)

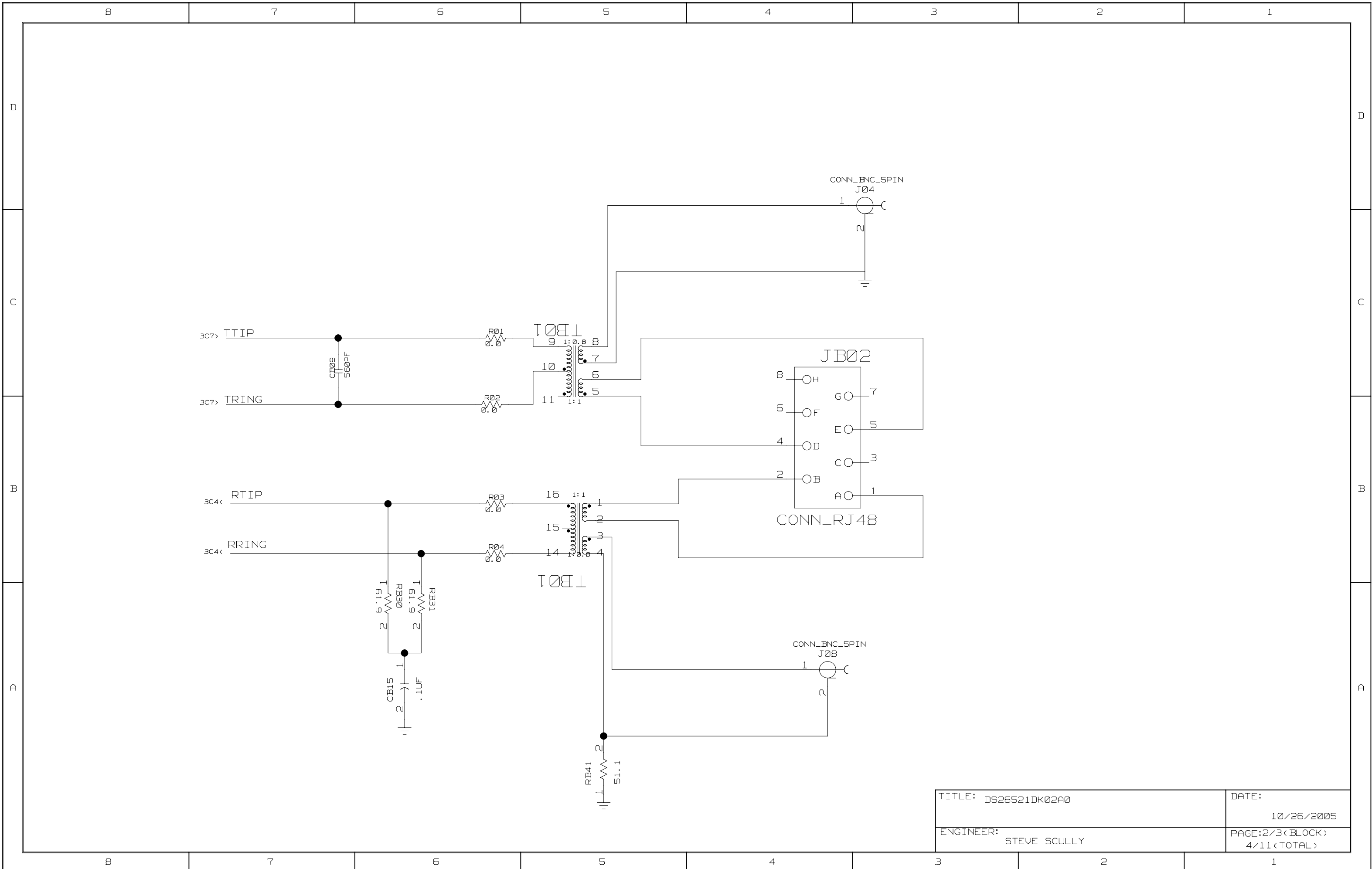


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U03
DS26521-U

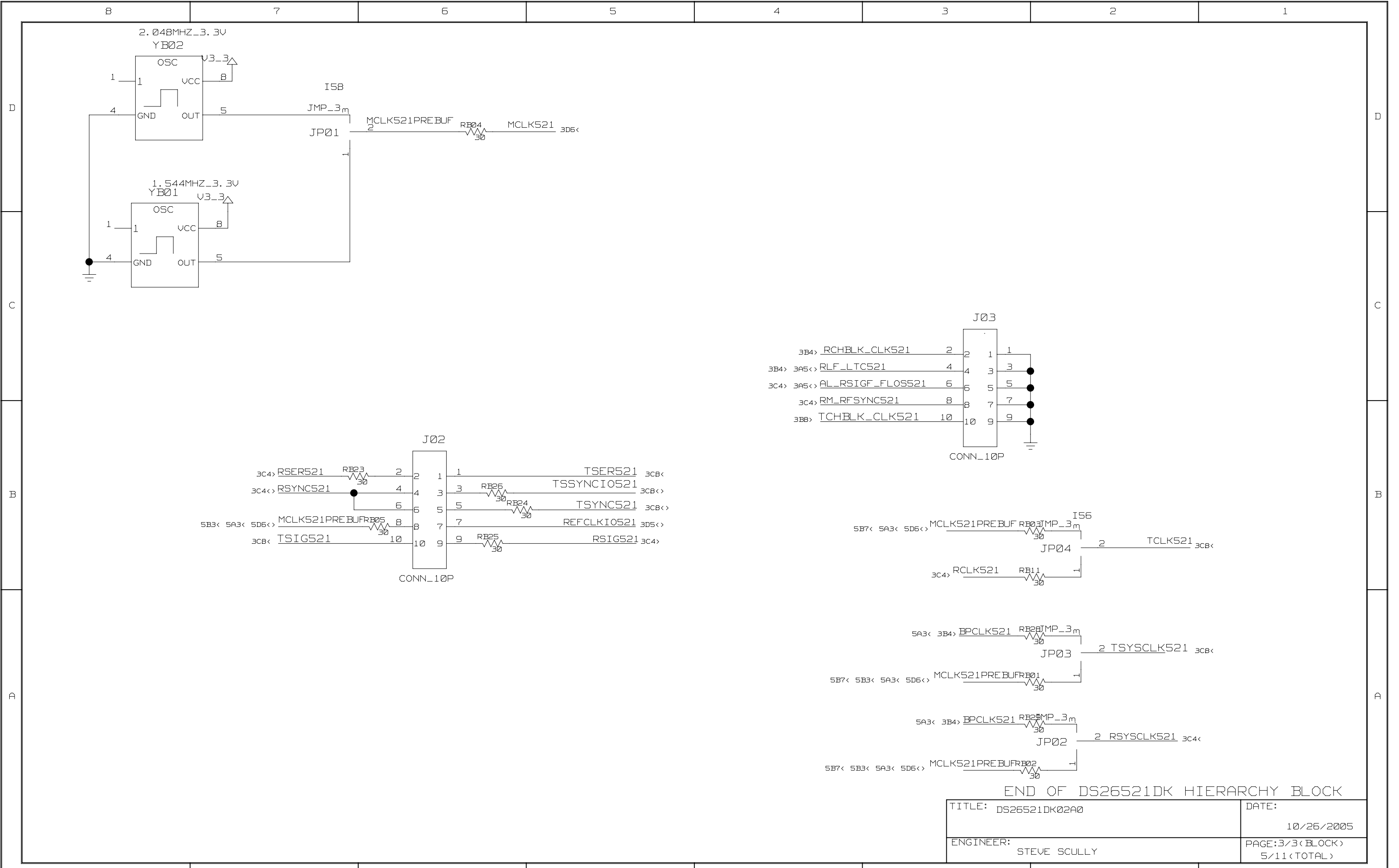
BEGINNING OF DS26521DK HIERARCHY BLOCK

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ENGINEER: STEVE SCULLY	PAGE: 1/3 (BLOCK) 3/11 (TOTAL)

INT_LED AND TESTPOINTS FOR ADDR/DATA/CTRL ARE IN THE MICRO PROCESSOR BLOCK



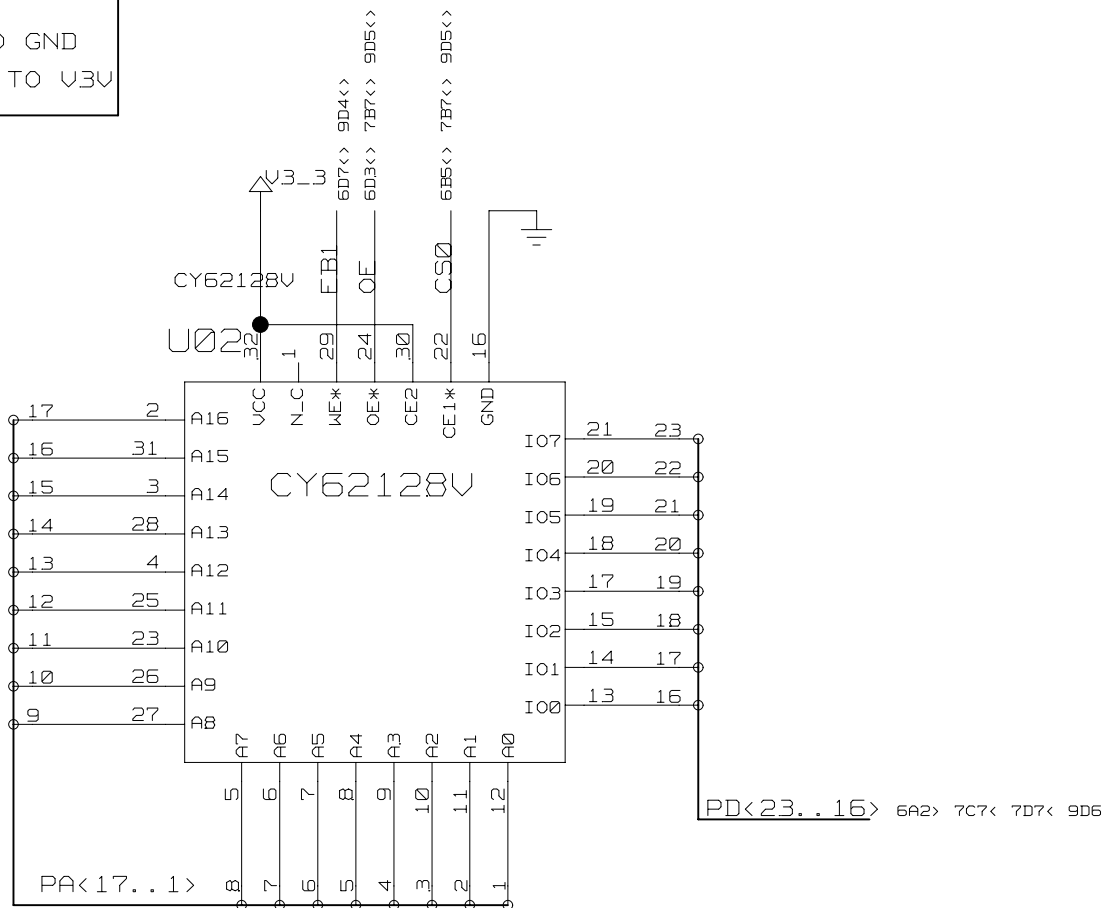
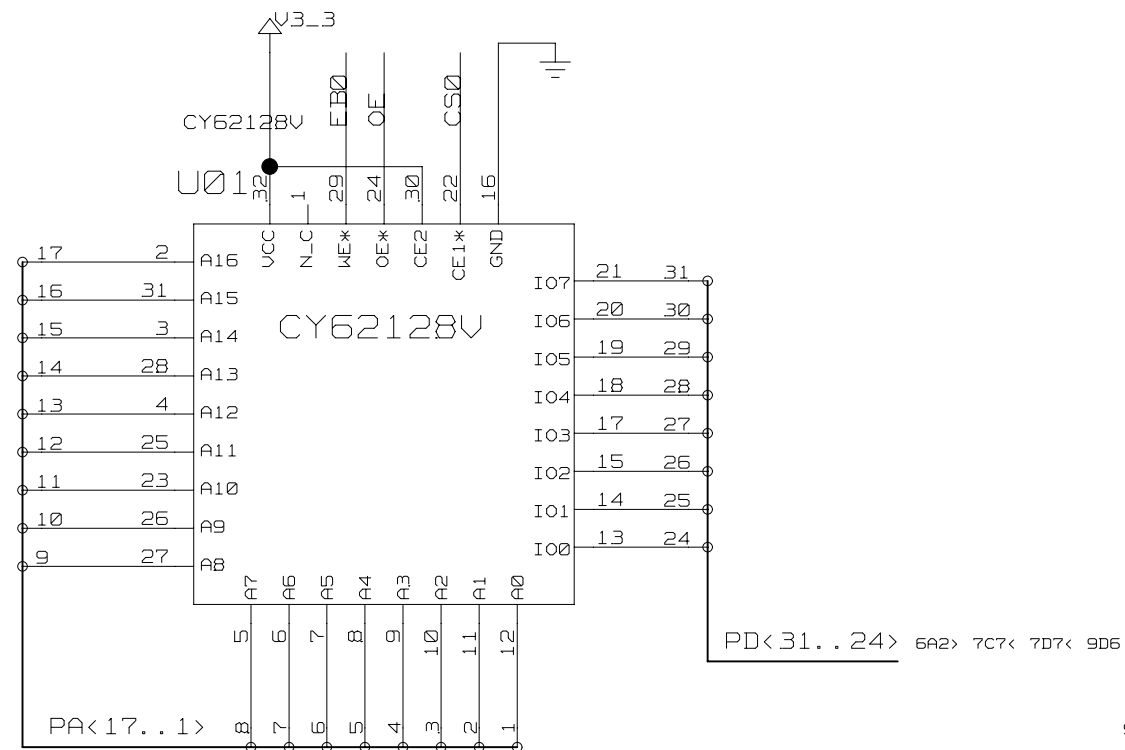
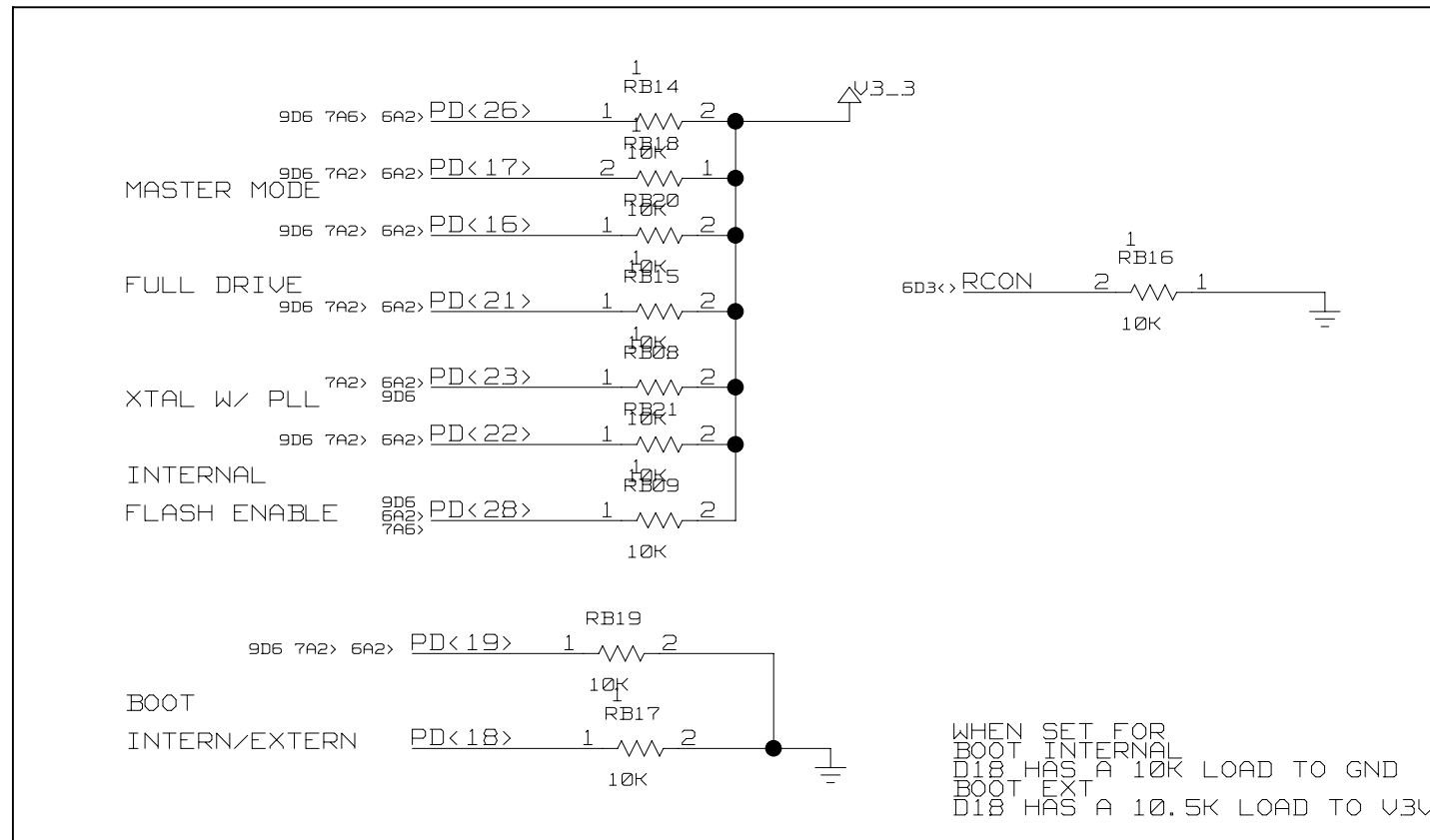
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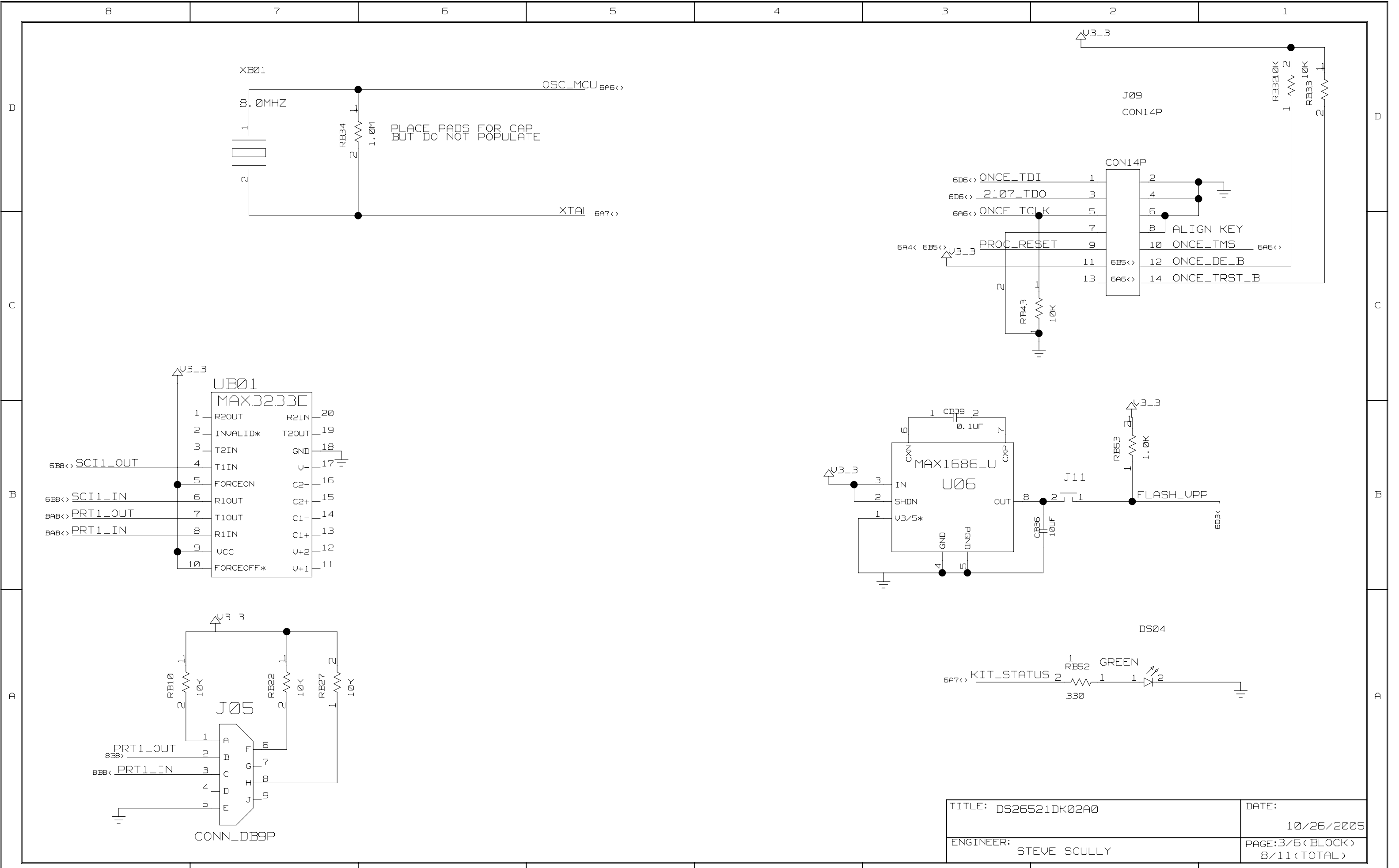
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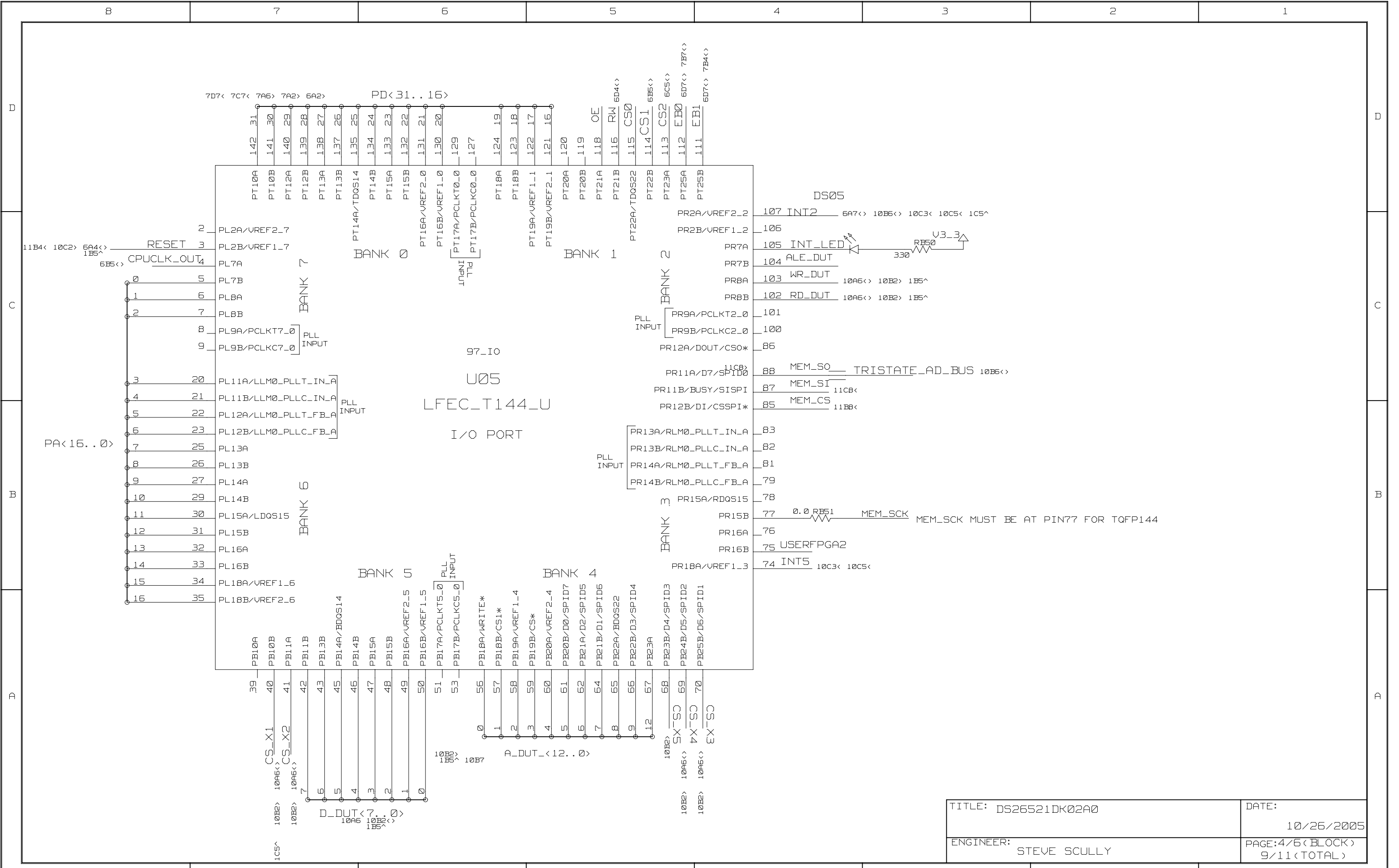
RESET CONFIGURATION



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ENGINEER: STEVE SCULLY	PAGE: 3/6 (BLOCK) 8/11 (TOTAL)



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ENGINEER: STEVE SCULLY	PAGE:4/6 (BLOCK) 9/11 (TOTAL)

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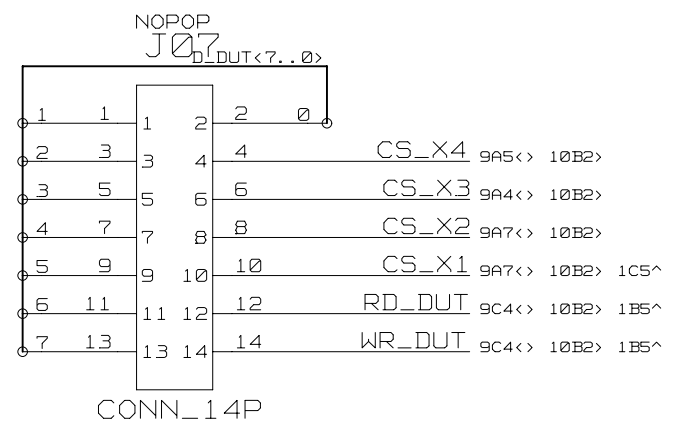
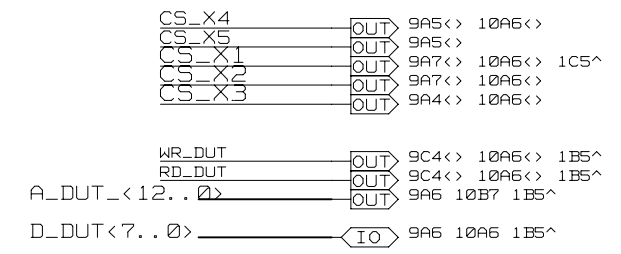
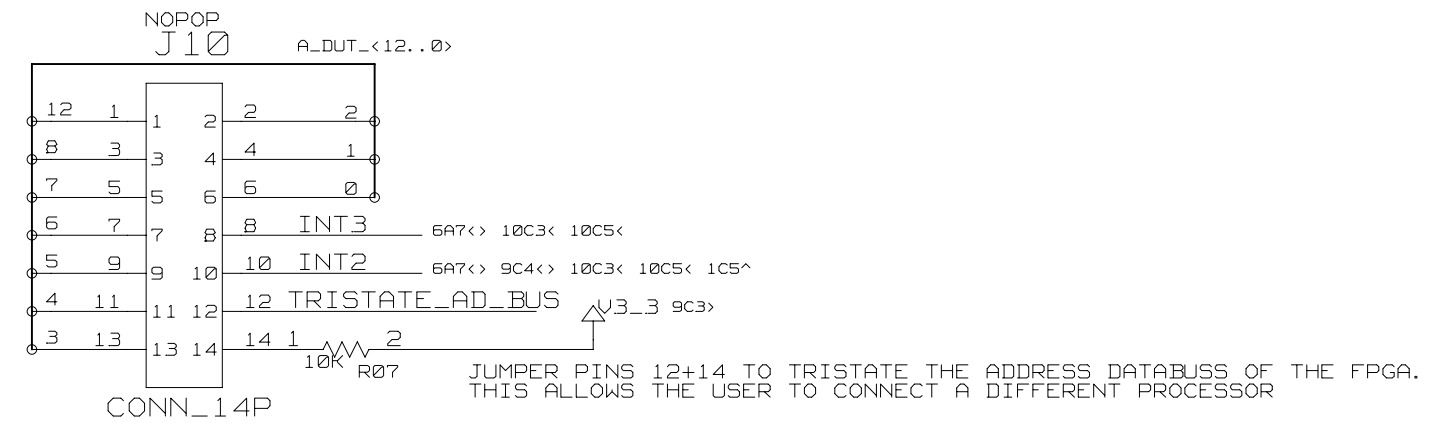
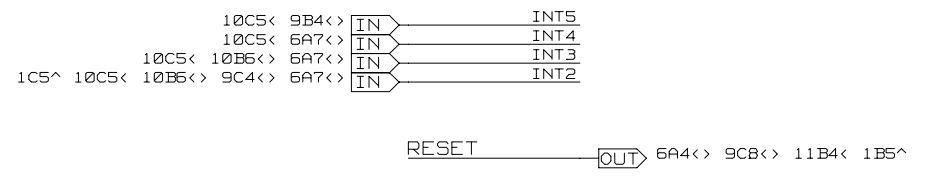
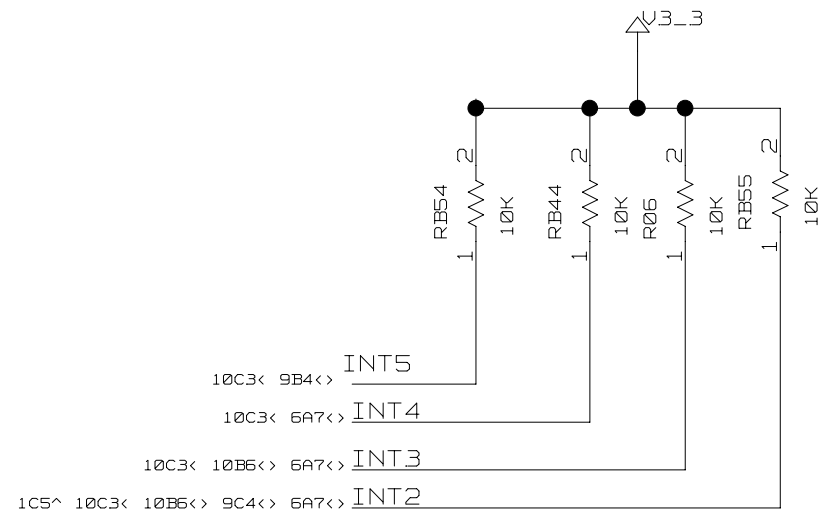
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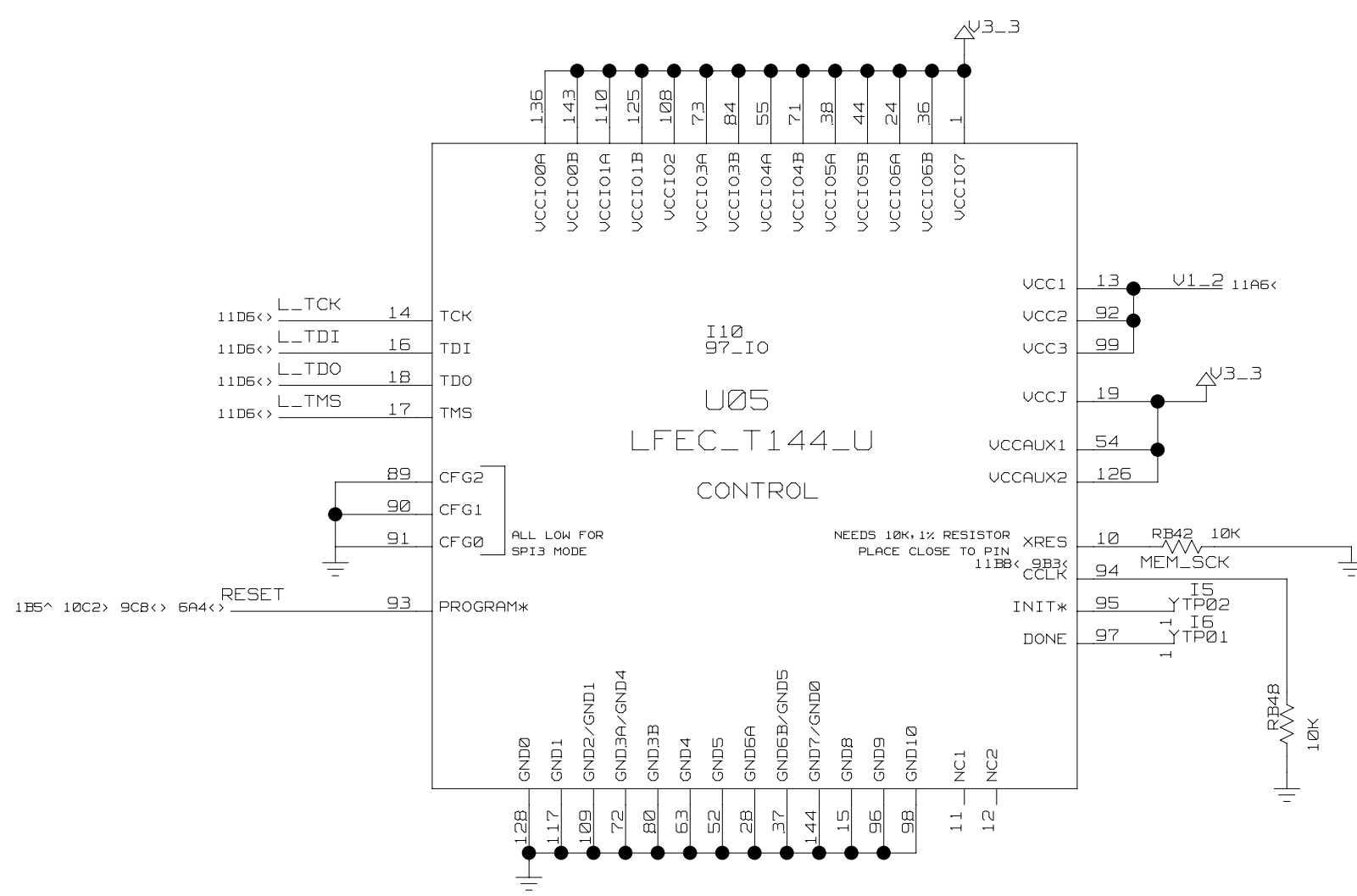
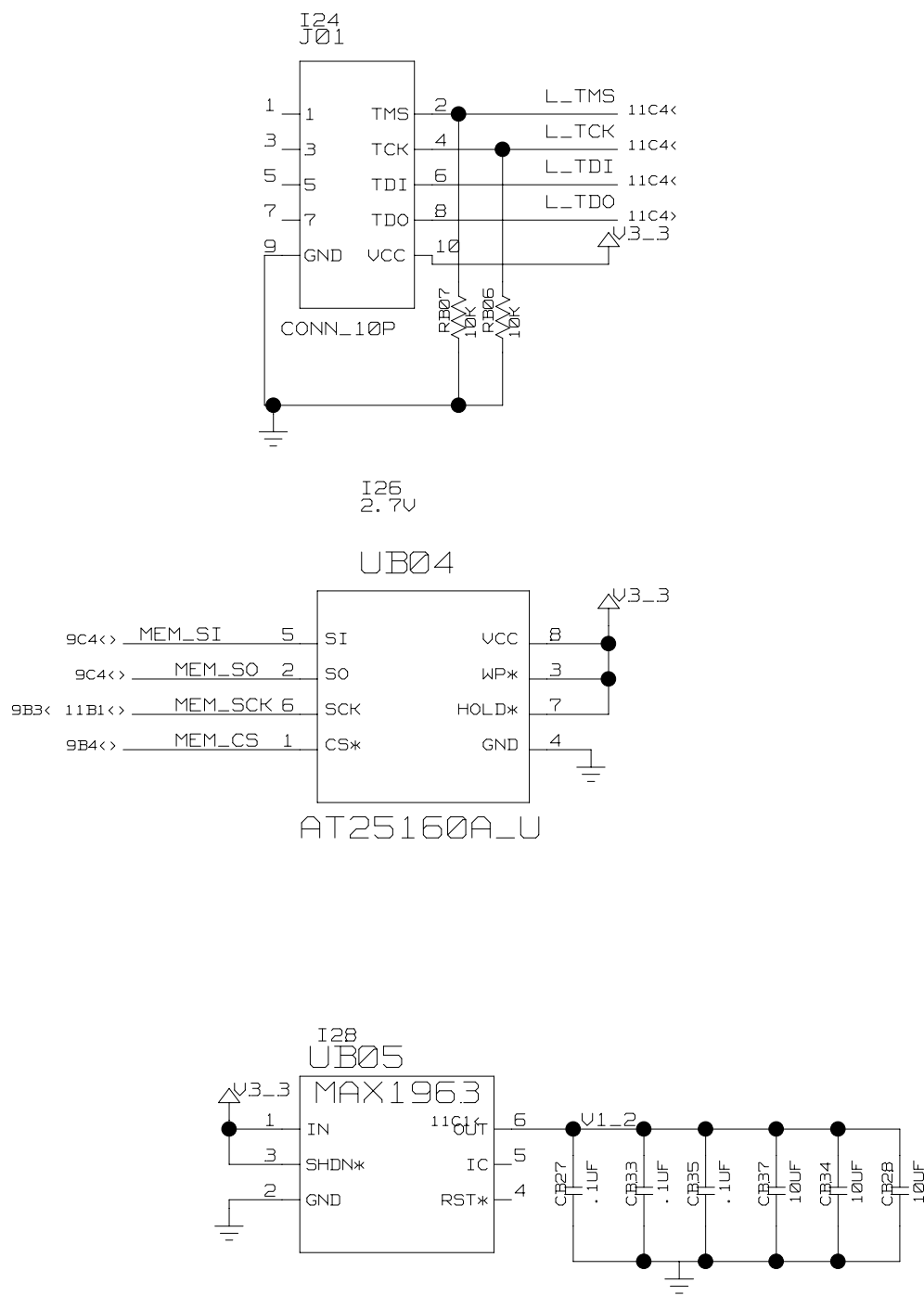
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ENGINEER: STEVE SCULLY	PAGE:5/6 (BLOCK) 10/11 (TOTAL)

B 7 6 5 4 3 2 1



END OF PROCESSOR HIERARCHY BLOCK

TITLE: DS26521DK02A0	DATE: 10/26/2005
ENGINEER: STEVE SCULLY	PAGE: 6/6 (BLOCK) 11/11 (TOTAL)

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