



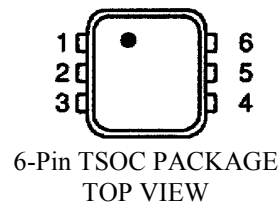
**THE DATASHEET OF
DS2415P+T&R**



FEATURES

- Real-time clock with fully compatible 1-Wire[®] MicroLAN interface
- Uses the same binary time/date representation as the DS2404 but with 1 second resolution
- Clock accuracy ± 2 minutes per month at 25°C
- Communicates at 16.3kbits per second
- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester) assures absolute traceability because no two parts are alike
- 8-bit family code specifies device communication requirements to bus master
- Built-in multidrop controller ensures compatibility with other MicroLAN products
- Operates over a wide V_{DD} voltage range of 2.5V to 5.5V from -40°C to +85°C
- Low power, 200nA typically with oscillator running
- Compact, low cost 6-pin TSOC surface mount package

PIN ASSIGNMENT



PIN DESCRIPTION

Pin 1	- GND
Pin 2	- 1-Wire
Pin 3	- V_{DD}
Pin 4	- V_{BAT}
Pin 5	- X1
Pin 6	- X2

ORDERING INFORMATION

DS2415P	6-pin TSOC package
DS2415P/T&R	Tape & Reel of DS2415P
DS2415X	Chip Scale Pkg., Tape & Reel

DESCRIPTION

The DS2415 1-Wire time chip offers a simple solution for storing and retrieving vital time information with minimal hardware. The DS2415 contains a unique, lasered ROM and a real-time clock/calendar implemented as a binary counter. Only one pin is required for communication with the device. Utilizing a backup energy source, the data is nonvolatile and allows for stand-alone operation. The DS2415 features can be used to add functions such as calendar, time and date stamp, and logbook to any type of electronic device or embedded application that uses a microcontroller.

OVERVIEW

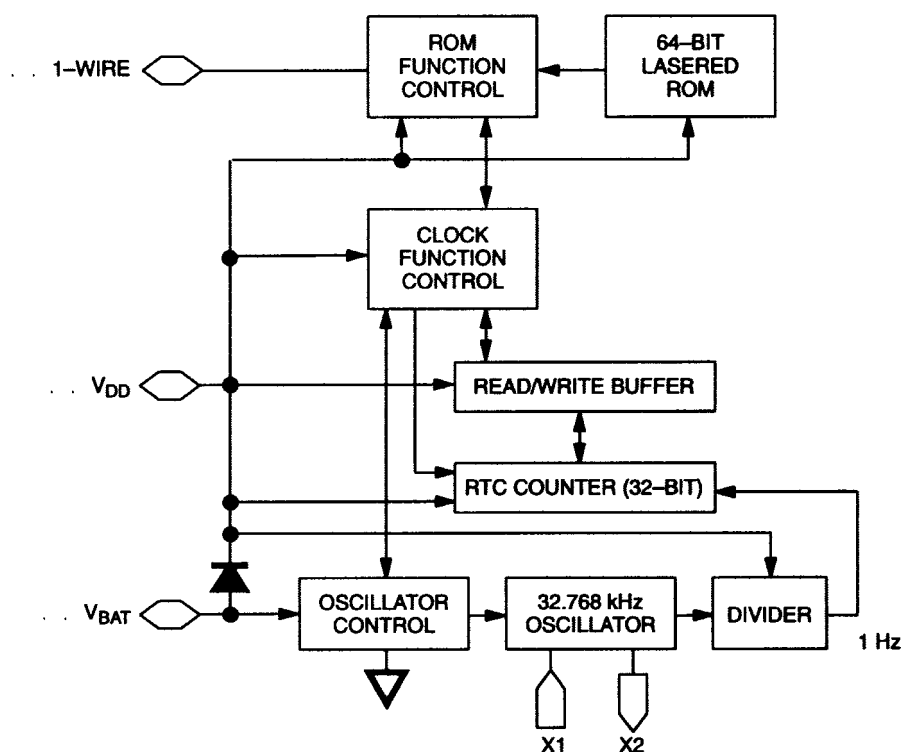
The DS2415 has two main data components: 1) 64-bit lasered ROM, and 2) real-time clock counter (Figure 1). The real-time clock utilizes an on-chip oscillator that is connected to an external 32.768kHz crystal. All data is read and written least significant bit first. The real-time clock functions will not be

available until the ROM function protocol has been established. This protocol is described in the ROM functions flow chart (Figure 7). The master must first provide one of four ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM. After a ROM function sequence has been successfully executed, the real-time clock functions are accessible and the master may then provide a real time clock function command (Figure 5).

DETAILED PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	GND	Ground pin.
2	1-Wire	Data input/output. Open drain.
3	V _{DD}	Internal power line. Connect a capacitor
4	V _{BAT}	Power input pin. 2.5V to 5.5V.
5, 6	X1, X2	Crystal pins. Connections for a standard 32.768kHz quartz crystal, EPSON part number C-002RX or C-004R (be sure to request 6pF load capacitance). NOTE: X1 and X2 are very high-impedance nodes. It is recommended that they and the crystal be guard-ringed with ground and that high frequency signals be kept away from the crystal area. See Figure 10 and Application Note 58 for details.

BLOCK DIAGRAM Figure 1

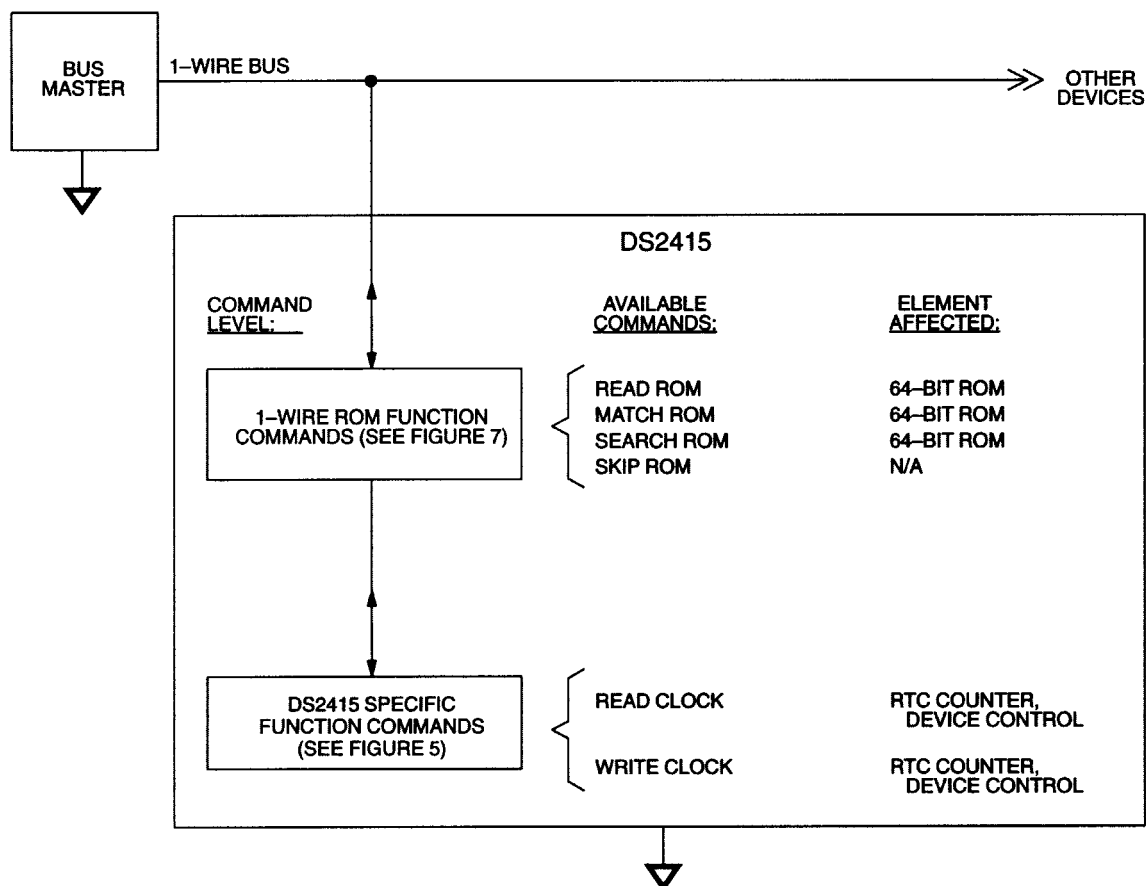


64-BIT LASERED ROM

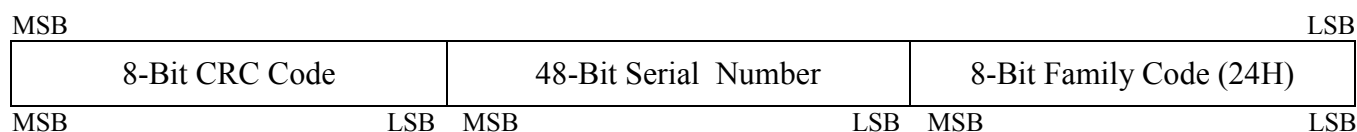
Each DS2415 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits. (See Figure 3.) The 1-Wire CRC of the lasered ROM is generated using the polynomial $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas Semiconductor 1-Wire Cyclic Redundancy Check is available in the Book of DS19xx iButton Standards[®]. The 64-bit ROM and ROM Function Control section allow the DS2415 to operate as a 1-Wire device and follow the 1-Wire protocol detailed in the section "1-Wire Bus System."

The functions required to exercise the control functions of the DS2415 are not accessible until the ROM function protocol has been satisfied. This protocol is described in the ROM functions flow chart (Figure 7). The 1-Wire bus master must first provide one of the four ROM function commands. After a ROM function sequence has been successfully executed, the bus master may then provide one of the function commands specific to the DS2415 (Figure 5).

HIERARCHICAL STRUCTURE FOR 1-WIRE PROTOCOL Figure 2

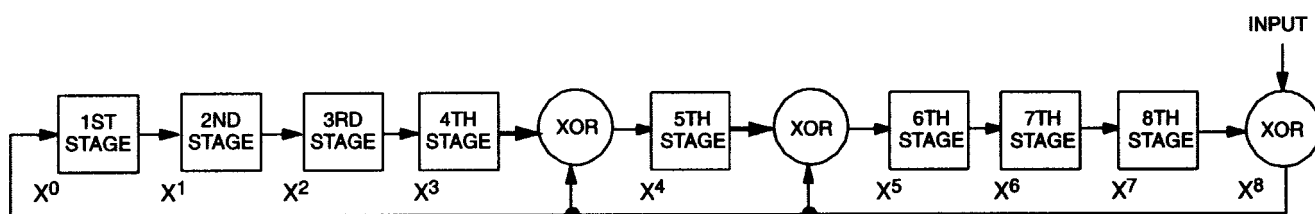


64-BIT LASERED ROM Figure 3



1-WIRE CRC GENERATOR Figure 4

$$\text{Polynomial} = X^8 + X^5 + X^4 + 1$$



TIMEKEEPING

A 32.768kHz crystal oscillator is used as the time base for the real-time clock counter. The oscillator can be turned on or off under software control. The oscillator must be on for the real-time clock to function. The real-time clock counter is double-buffered. This allows the master to read time without the data changing while it is being read. To accomplish this, a snapshot of the counter data is transferred to a read/write buffer, which the user accesses.

DEVICE CONTROL BYTE

The on/off control of the 32.768kHz crystal oscillator is done through the device control byte. This byte can be read and written through the Clock Function commands.

Device Control Byte

7	6	5	4	3	2	1	0
U4	U3	U2	U1	OSC	OSC	0	0

Bit 0 - 1 No function

Bits 0 and 1 are hard-wired to read all 0s.

Bit 2 - 3 Oscillator Enable/Disable

These bits control/report whether the 32.768kHz crystal oscillator is running. If the oscillator is running, both OSC bits will read 1. If the oscillator is turned off these bits will read 0. When writing the device control byte both occurrences of the OSC bit should have identical data. Otherwise, the value in bit address 3 (bold) takes precedence.

Bit 4 - 7 General-purpose user flags

These bits have no particular function within the chip. They can be read and written under the control of the application software and remain non-volatile as long as there is sufficient voltage at the V_{DD} pin. If the DS2415 is located inside a battery pack, for example, these bits could convey data on the charging status from the charging station to the equipment that uses the battery.

Real-Time Clock

The real-time clock is a 32-bit binary counter. It is incremented once per second. The real-time clock can accumulate 136 years of seconds before rolling over. Time/date is represented by the number of seconds since a reference point, which is determined by the user. For example, 12:00 a.m., January 1, 1970 could be a reference point.

CLOCK FUNCTION COMMANDS

The “Clock Function Flow Chart” (Figure 5) describes the protocols necessary for accessing the real-time clock. With only four bytes of real-time clock and one control byte the DS2415 does not provide random access. Reading and writing always starts with the device control byte followed by the least significant byte (LSB) of the time data.

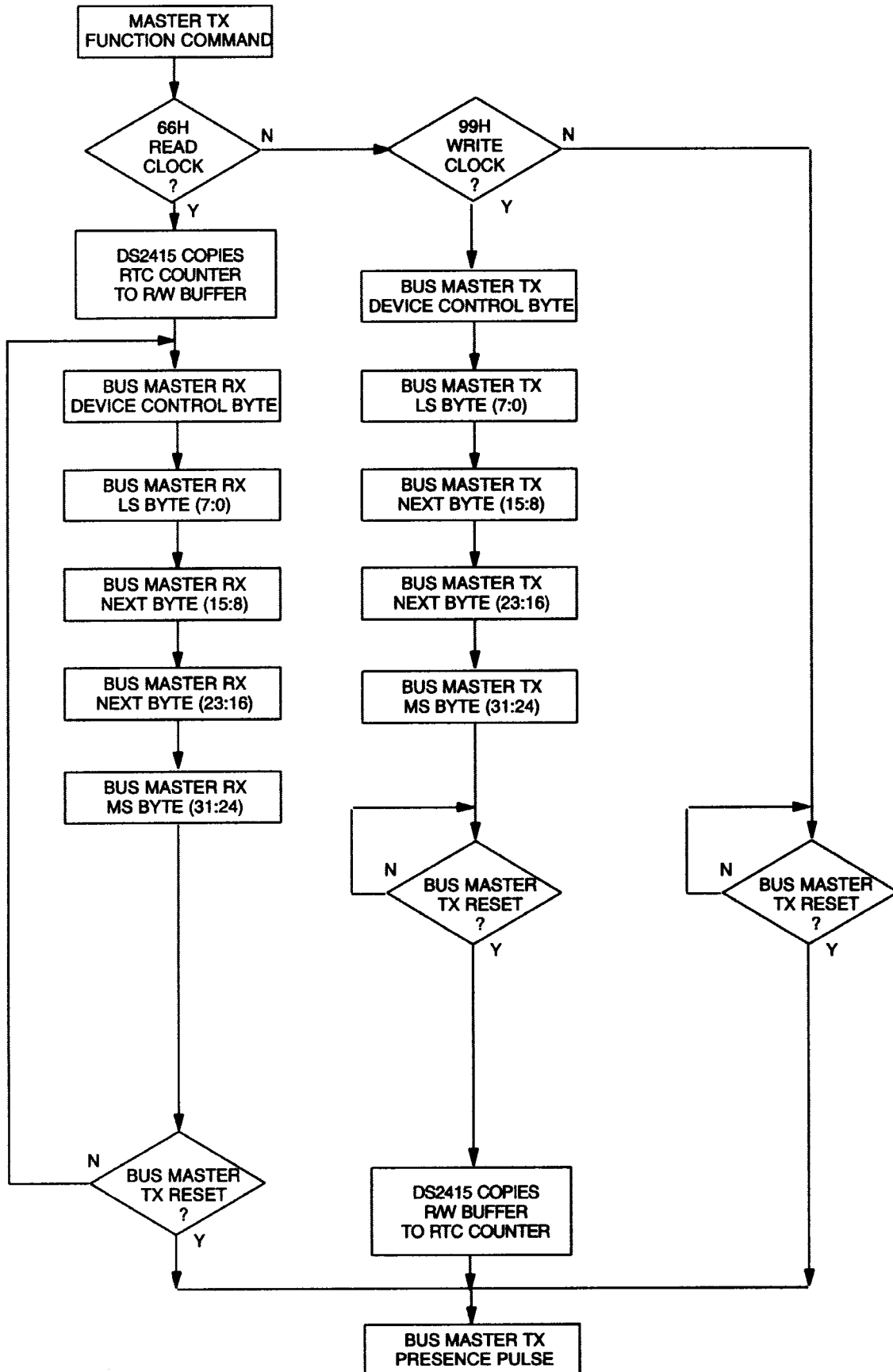
READ CLOCK [66h]

The Read Clock command is used to read the device control byte and the contents of the real-time clock counter. After having received the most significant bit of the command code the device copies the actual contents of the real-time clock counter to the read/write buffer. Now the bus master reads data beginning with the device control byte followed by the least significant byte through the most significant byte of the real-time clock. After this the bus master may continue reading from the DS2415. The data received will be the same as in the first pass through the command flow. The Read Clock command can be ended at any point by issuing a Reset Pulse.

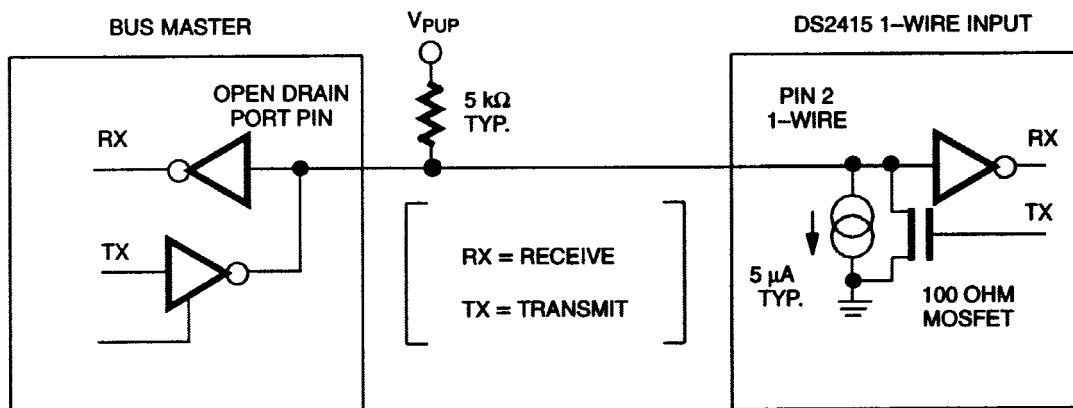
WRITE CLOCK [99h]

The Write Clock command is used to set the real-time clock counter and to write the device control byte. After issuing the command, the bus master writes first the device control byte, which becomes immediately effective. After this the bus master sends the least significant byte through the most significant byte to be written to the real time clock counter. The new time data is copied from the read/write buffer to the real time clock counter and becomes effective as the bus master generates a Reset Pulse. If the oscillator is intentionally stopped the real time clock counter behaves as a 4-byte nonvolatile memory.

CLOCK FUNCTION COMMAND FLOW CHART Figure 5



HARDWARE CONFIGURATION Figure 6



1-WIRE BUS SYSTEM

The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances the DS2415 behaves as a slave. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). A 1-Wire protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx iButton Standards.

Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open drain or 3-state outputs. The 1-Wire input of the DS2415 is open drain with an internal circuit equivalent to that shown in Figure 6. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The 1-Wire bus has a maximum data rate of 16.3kbits per second and requires a pullup resistor of approximately 5kΩ.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus must be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120μs, one or more of the devices on the bus may be reset. Since the DS2415 gets all its energy for operation through its V_{BAT} pin it will not perform a power-on reset if the 1-Wire bus is low for an extended time period.

Transaction Sequence

The protocol for accessing the DS2415 via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Clock Function Command

INITIALIZATION

All transactions on the 1-wire bus begin with an initialization sequence. The initialization sequence consists of a Reset Pulse transmitted by the bus master followed by Presence Pulse(s) transmitted by the slave(s).

The Presence Pulse lets the bus master know that the DS2415 is on the bus and is ready to operate. For more details, see the “1-Wire Signaling” section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are 8 bits long. A list of these commands follows (refer to flowchart in Figure 7):

Read ROM [33h]

This command allows the bus master to read the DS2415’s 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS2415 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The resultant family code and 48-bit serial number will usually result in a mismatch of the CRC.

Match ROM [55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS2415 on a multidrop bus. Only the DS2415 that exactly matches the 64-bit ROM sequence will respond to the following clock function command. All slaves that do not match the 64-bit ROM sequence will wait for a Reset Pulse. This command can be used with a single or multiple devices on the bus.

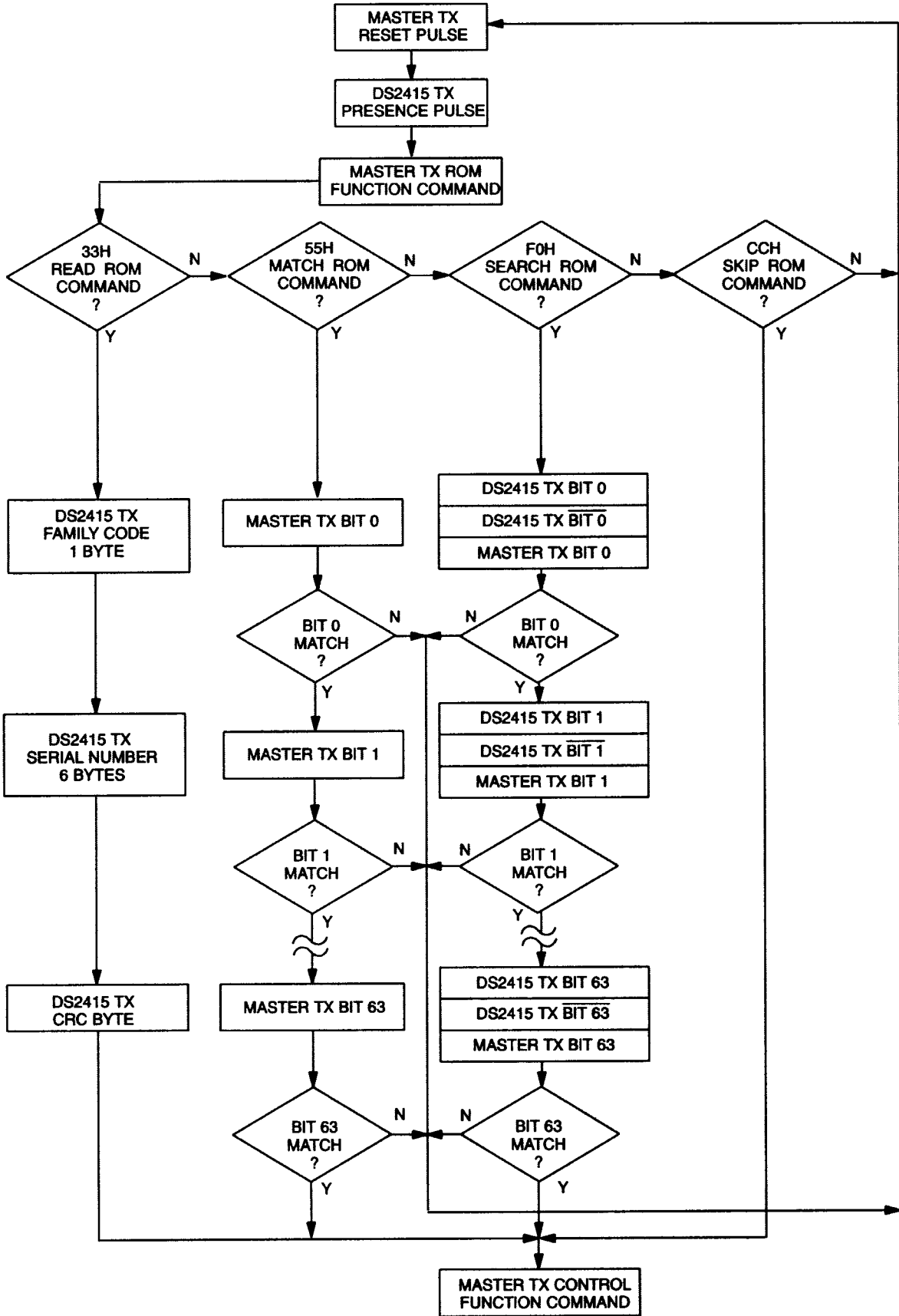
Skip ROM [CCh]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wired-AND result).

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The Search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The Search ROM process is the repetition of a simple, three-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, three-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the Book of DS19xx 1-Wire Standards for a comprehensive discussion of a search ROM, including an actual example.

ROM FUNCTIONS FLOW CHART Figure 7

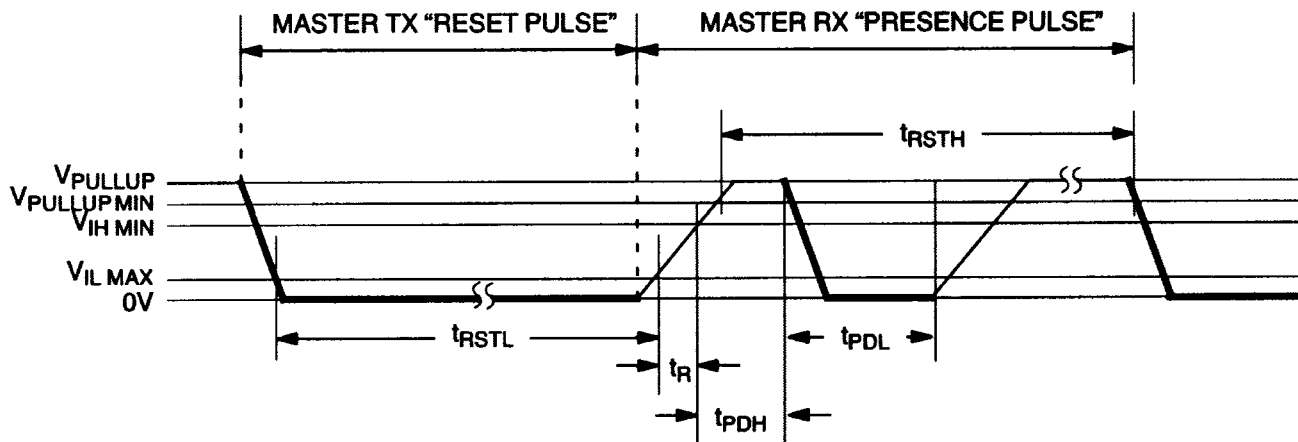


(SEE FIGURE 5)

1-WIRE SIGNALING

The DS2415 requires strict protocols to insure data integrity. The protocol consists of four types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1, and Read Data. The bus master initiates all these signals, except Presence Pulse. The initialization sequence required to begin any communication with the DS2415 is shown in Figure 8. A Reset Pulse followed by a Presence Pulse indicates the DS2415 is ready to send or receive data given the correct ROM command and control function command. The bus master transmits (TX) a Reset Pulse (t_{RSTL} , minimum 480 μ s). The bus master then releases the line and goes into receive mode (RX). The 1-Wire bus is pulled to a high state via the pullup resistor. After detecting the rising edge on the data line, the DS2415 waits (t_{PDH} , 15 μ s to 60 μ s) and then transmits the Presence Pulse (t_{PDL} , 60 μ s to 240 μ s).

INITIALIZATION PROCEDURE “RESET AND PRESENCE PULSES” Figure 8



—	RESISTOR
—	MASTER
—	DS2415

$$480\mu\text{s} \leq t_{RSTL} < \infty *$$

$$480\mu\text{s} \leq t_{RSTH} < \infty \text{ (INCLUDES RECOVERY TIME)}$$

$$15\mu\text{s} \leq t_{PDH} < 60\mu\text{s}$$

$$60\mu\text{s} \leq t_{PDL} < 240\mu\text{s}$$

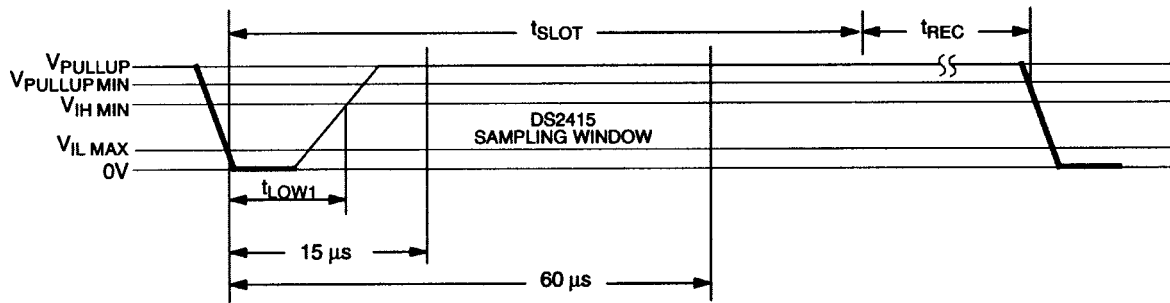
* In order not to mask interrupt signaling by other devices on the 1-Wire bus, $t_{RSTL} + t_R$ should always be less than 960 μ s.

READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 9. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS2415 to the master by triggering a delay circuit in the DS2415. During write time slots, the delay circuit determines when the DS2415 will sample the data line. For a read data time slot, if a 0 is to be transmitted, the delay circuit determines how long the DS2415 will hold the data line low overriding the 1 generated by the master. If the data bit is a 1, the device will leave the read data time slot unchanged.

READ/WRITE TIMING DIAGRAM Figure 9

Write-1 Time Slot

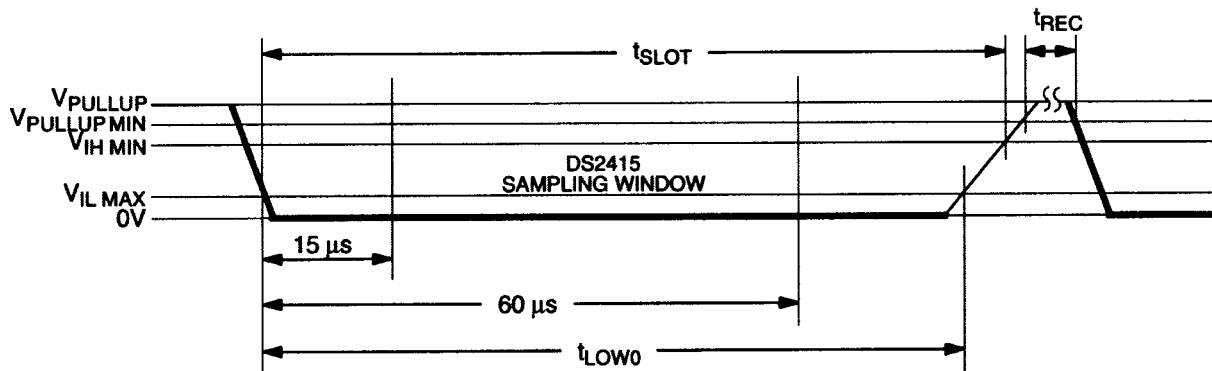


$$60\mu\text{s} \leq t_{\text{SLOT}} < 120\mu\text{s}$$

$$1\mu\text{s} \leq t_{\text{LOW1}} < 15\mu\text{s}$$

$$1\mu\text{s} \leq t_{\text{REC}} < \infty$$

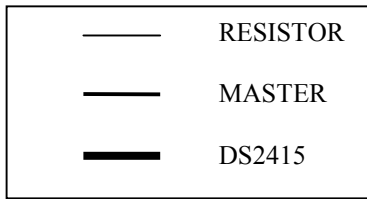
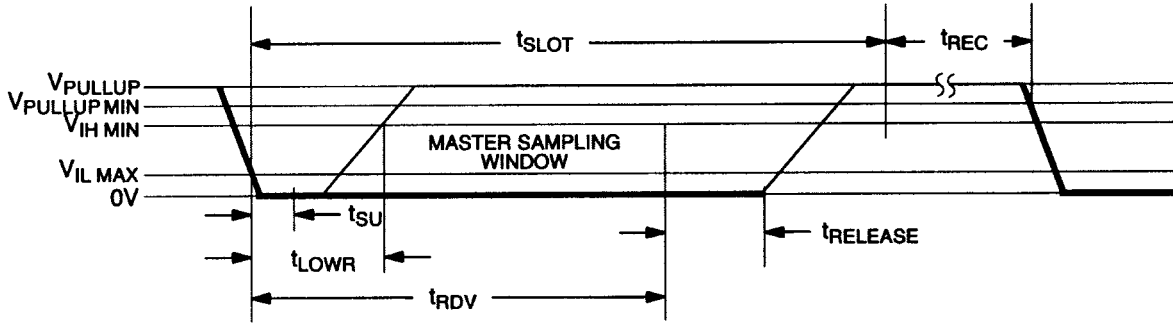
Write-0 Time Slot



$$60\mu\text{s} \leq t_{\text{LOW0}} < t_{\text{SLOT}} < 120\mu\text{s}$$

$$1\mu\text{s} \leq t_{\text{REC}} < \infty$$

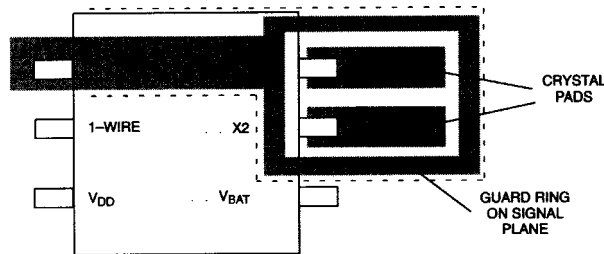
Read-data Time Slot



$60\mu s \leq t_{SLOT} < 120\mu s$
 $1\mu s \leq t_{LOWR} < 15\mu s$
 $0 \leq t_{RELEASE} < 45\mu s$
 $1\mu s \leq t_{REC} < \infty$
 $t_{RDV} = 15\mu s$
 $t_{SU} < 1\mu s$

CRYSTAL PLACEMENT ON PCB Figure 10

LOCAL GROUND PLANE BENEATH SIGNAL PLANE OR ON OTHER SIDE OF PCB



ABSOLUTE MAXIMUM RATINGS*

Voltage on 1-Wire to Ground	-0.5V to +7.0V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See J-STD-020A Specification

- * This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

The Dallas Semiconductor DS2415 is built to the highest quality standards and manufactured for long term reliability. All Dallas Semiconductor devices are made using the same quality materials and manufacturing methods. However, the DS2415 is not exposed to environmental stresses, such as burn-in, that some industrial applications require. For specific reliability information on this product, please contact the factory in Dallas at (972) 371-4448.

DC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C, $V_{PUP} = 2.5V$ to 6.0V, $V_{BAT} = 2.5V$ to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH1}	2.2		6.0	V	1,12
Logic 0	V_{IL1}	-0.3		+0.8	V	1,7
Output Logic Low @ 4mA	V_{OL1}			0.4	V	1
Output Logic High	V_{OH1}			V_{PUP}	V	1,3
Input Load Current	I_{L1}		5		μA	4
Operating Current (Osc. On)	I_{BAT3}			250	nA	2,10
Quiescent Current (Osc. Off)	I_{BATQ3}			50	nA	2,9,10
Operating Current (Osc. On)	I_{BAT5}			450	nA	2,11
Quiescent Current (Osc. Off)	I_{BATQ5}			100	nA	2,9,11

CAPACITANCE

($T_A = 25^\circ C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance 1-Wire	C_{IN}			50	pF	

AC ELECTRICAL CHARACTERISTICS(-40°C to +85°C, $V_{PUP} = 2.5V$ to $6.0V$, $V_{BAT} = 2.5V$ to $5.5V$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	μs	
Write 1 Low Time	t_{LOW1}	1		15	μs	14
Write 0 Low Time	t_{LOW0}	60		120	μs	
Read Low Time	t_{LOWR}	1		15	μs	14
Read Data Valid	t_{RDV}		15		μs	13
Release Time	$t_{RELEASE}$	0	15	45	μs	
Read Data Setup	t_{SU}			1	μs	6
Recovery Time	t_{REC}	1			μs	
Reset Time High	t_{RSTH}	480			μs	5
Reset Time Low	t_{RSTL}	480		960	μs	8
Presence Detect High	t_{PDH}	15		60	μs	
Presence Detect Low	t_{PDL}	60		240	μs	

NOTES:

- All voltages are referenced to ground.
- Measured with outputs open.
- V_{PUP} = external pullup voltage.
- Input load is to ground.
- An additional reset or communication sequence cannot begin until the reset high time has expired.
- Read data setup time refers to the time the bus master must pull the I/O line low to read a bit. Data is guaranteed to be valid within $1\mu s$ of this falling edge.
- Under certain low voltage conditions V_{ILIMAX} may have to be reduced to as much as $0.5V$ to always guarantee a Presence Pulse.
- The reset low time (t_{RSTL}) should be restricted to a maximum of $960\mu s$, to allow interrupt signaling, otherwise, it could mask or conceal interrupt pulses.
- When V_{BAT} ramps up, the oscillator is always off.
- At $V_{BAT} = 3V \pm 10\%$
- At $V_{BAT} = 5V \pm 10\%$
- V_{IHI} has to be $V_{BAT} - 0.3V$ or higher.
- The optimal sampling point for the master is as close as possible to the end time of the $15\mu s$ t_{RDV} period without exceeding t_{RDV} . For the case of a Read-One Time Slot, this maximizes the amount of time for the pull-up resistor to recover to a high level. For a Read-Zero Time Slot, it ensures that a read will occur before the fastest 1-Wire device(s) release the line.
- The duration of the low pulse sent by the master should be a minimum of $1\mu s$ with a maximum value as short as possible to allow time for the pull-up resistor to recover the line to a high level before the 1-Wire device samples in the case of a Write-One Time or before the master samples in the case of a Read-One Time.

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