



**THE DATASHEET OF
DS2045L-100#**





DS2045L 3.3V Single-Piece 1Mb Nonvolatile SRAM

DS2045L

General Description

The DS2045L is a 1Mb reflowable nonvolatile (NV) SRAM, which consists of a static RAM (SRAM), an NV controller, and an internal rechargeable manganese lithium (ML) battery. These components are encased in a surface-mount module with a 256-ball BGA footprint. Whenever V_{CC} is applied to the module, it recharges the ML battery, powers the SRAM from the external power source, and allows the contents of the SRAM to be modified. When V_{CC} is powered down or out-of-tolerance, the controller write-protects the SRAM's contents and powers the SRAM from the battery. The DS2045L also contains a power-supply monitor output, RST, which can be used as a CPU supervisor for a microprocessor.

Features

- ◆ Single-Piece, Reflowable, 27mm² BGA Package Footprint
- ◆ Internal ML Battery and Charger
- ◆ Unconditionally Write-Protects SRAM when V_{CC} is Out-of-Tolerance
- ◆ Automatically Switches to Battery Supply when V_{CC} Power Failures Occur
- ◆ Internal Power-Supply Monitor Detects Power Fail Below Nominal V_{CC} (3.3V)
- ◆ Reset Output can be used as a CPU Supervisor for a Microprocessor
- ◆ Industrial Temperature Range (-40°C to +85°C)
- ◆ UL Recognized

Applications

| | |
|--------------------------|--------------------------|
| RAID Systems and Servers | POS Terminals |
| Industrial Controllers | Data-Acquisition Systems |
| Gaming | Fire Alarms |
| Router/Switches | PLCs |

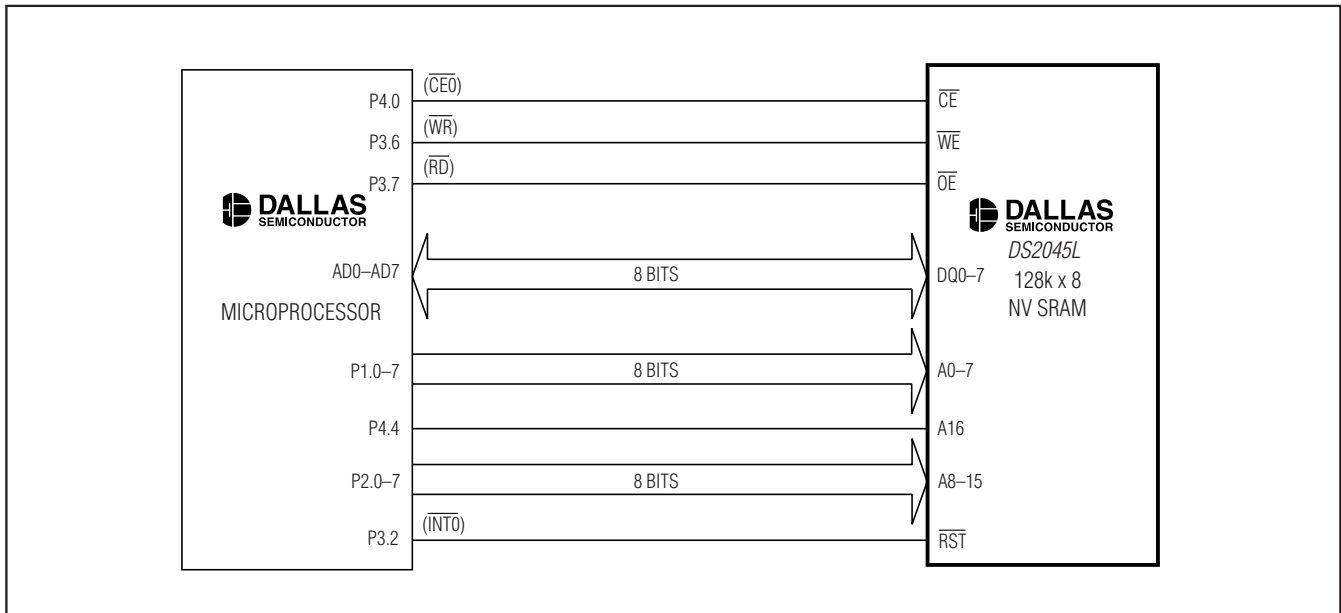
Pin Configuration appears at end of data sheet.

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | SPEED (ns) | SUPPLY TOLERANCE |
|--------------|----------------|---------------------------------------|------------|------------------|
| DS2045L-100# | -40°C to +85°C | 256 Ball 27mm ² BGA Module | 100 | 3.3V ±0.3V |

#Denotes a RoHS-compliant device that may include lead that is exempt under the RoHS requirements.

Typical Operating Circuit



DS2045L 3.3V Single-Piece 1Mb Nonvolatile SRAM

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin Relative to Ground-0.3V to +4.6V
 Operating Temperature Range-40°C to +85°C

Storage Temperature Range-40°C to +85°C
 Soldering TemperatureSee IPC/JEDEC J-STD-020

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------|----------|------------|-----|-----|----------|-------|
| Supply Voltage | V_{CC} | | 3.0 | 3.3 | 3.6 | V |
| Input Logic 1 | V_{IH} | | 2.2 | | V_{CC} | V |
| Input Logic 0 | V_{IL} | | 0 | | 0.4 | V |

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|-------------------------|--|------|-----|------|---------------|
| Input Leakage Current | I_{IL} | | -1.0 | | +1.0 | μA |
| I/O Leakage Current | I_{IO} | $\overline{CE} = V_{CC}$ | -1.0 | | +1.0 | μA |
| Output-Current High | I_{OH} | At 2.4V | -1.0 | | | mA |
| Output-Current Low | I_{OL} | At 0.4V | 2.0 | | | mA |
| Output-Current Low \overline{RST} | $I_{OL} \overline{RST}$ | At 0.4V (Note 1) | 10.0 | | | mA |
| Standby Current | I_{CCS1} | $\overline{CE} = 2.2\text{V}$ | | 0.5 | 2 | mA |
| | I_{CCS2} | $\overline{CE} = V_{CC} - 0.2\text{V}$ | | 0.2 | 1 | |
| Operating Current | I_{CCO1} | $t_{RC} = 200\text{ns}$, outputs open | | | 50 | mA |
| Write Protection Voltage | V_{TP} | | 2.8 | 2.9 | 3.0 | V |

CAPACITANCE

($T_A = +25^\circ\text{C}$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------|-----------|------------|-----|-----|-----|-------|
| Input Capacitance | C_{IN} | Not tested | | 7 | | pF |
| Input/Output Capacitance | C_{OUT} | Not tested | | 7 | | pF |

DS2045L 3.3V Single-Piece 1Mb Nonvolatile SRAM

DS2045L

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = 3.3V \pm 0.3V$, $T_A = -40^\circ C$ to $+85^\circ C$.)

| PARAMETER | SYMBOL | CONDITIONS | DS2045L-100 | | UNITS |
|---|--|------------|-------------|-----|-------|
| | | | MIN | MAX | |
| Read Cycle Time | t _{RC} | | 100 | | ns |
| Access Time | t _{ACC} | | | 100 | ns |
| \overline{OE} to Output Valid | t _{OE} | | | 50 | ns |
| \overline{CE} to Output Valid | t _{CO} | | | 100 | ns |
| \overline{OE} or \overline{CE} to Output Active | t _{COE} | (Note 2) | 5 | | ns |
| Output High Impedance from Deselection | t _{OD} | (Note 2) | | 35 | ns |
| Output Hold from Address Change | t _{OH} | | 5 | | ns |
| Write Cycle Time | t _{WC} | | 100 | | ns |
| Write Pulse Width | t _{WP} | (Note 3) | 75 | | ns |
| Address Setup Time | t _{AW} | | 0 | | ns |
| Write Recovery Time | t _{WR1} | (Note 4) | 5 | | ns |
| | t _{WR2} | (Note 5) | 20 | | |
| Output High Impedance from \overline{WE} | t _{ODW} | (Note 2) | | 35 | ns |
| Output Active from \overline{WE} | t _{OE\overline{W}} | (Note 2) | 5 | | ns |
| Data Setup Time | t _{DS} | (Note 6) | 40 | | ns |
| Data Hold Time | t _{DH1} | (Note 4) | 0 | | ns |
| | t _{DH2} | (Note 5) | 20 | | |

POWER-DOWN/POWER-UP TIMING

($T_A = -40^\circ C$ to $+85^\circ C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|------------------|------------|-----|-----|-----|---------|
| V_{CC} Fail Detect to \overline{CE} and \overline{WE} Inactive | t _{PD} | (Note 7) | | | 1.5 | μs |
| V_{CC} Slew from V_{TP} to 0V | t _F | | 150 | | | μs |
| V_{CC} Slew from 0V to V_{TP} | t _R | | 150 | | | μs |
| V_{CC} Valid to \overline{CE} and \overline{WE} Inactive | t _{PU} | | | | 2 | ms |
| V_{CC} Valid to End of Write Protection | t _{REC} | | | | 125 | ms |
| V_{CC} Fail Detect to \overline{RST} Active | t _{RPD} | (Note 1) | | | 3.0 | μs |
| V_{CC} Valid to \overline{RST} Inactive | t _{RPU} | (Note 1) | 225 | 350 | 525 | ms |

DATA RETENTION

($T_A = +25^\circ C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-----------------|------------|-----|-----|-----|-------|
| Expected Data-Retention Time (Per Charge) | t _{DR} | (Note 8) | 11 | 16 | | Weeks |

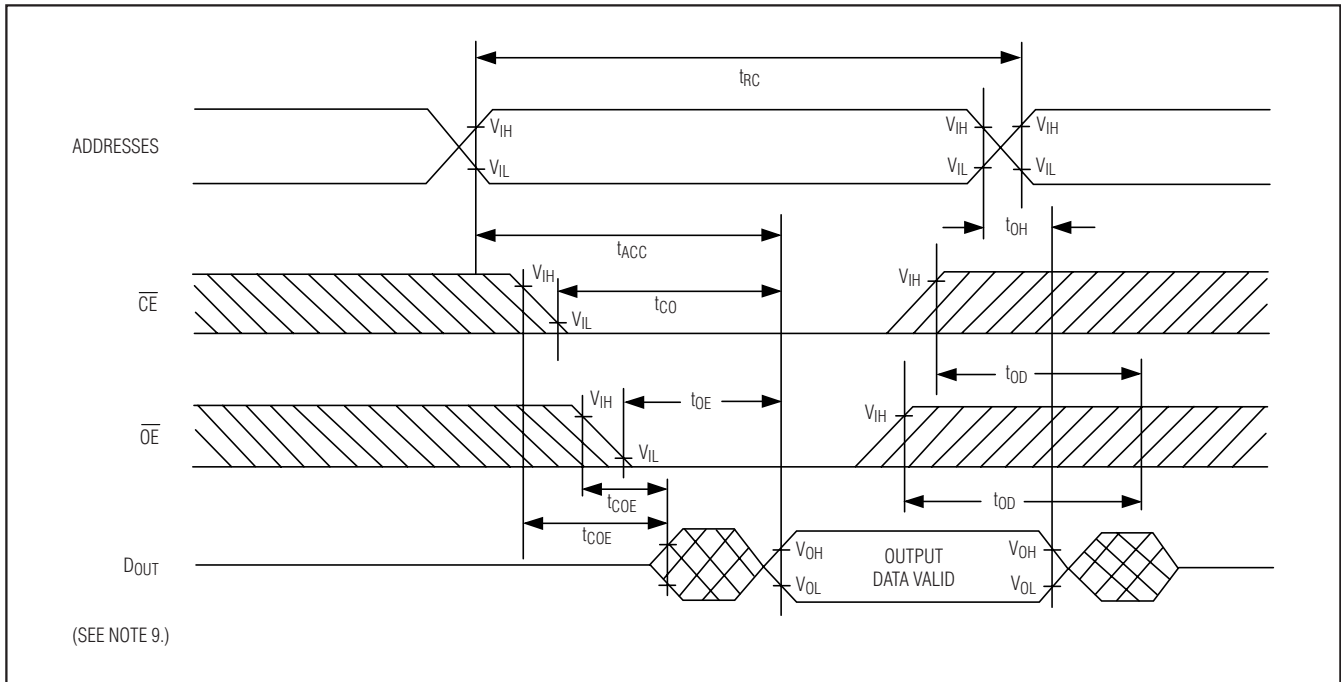
AC TEST CONDITIONS

- Input Pulse Levels: $V_{IL} = 0.0V$, $V_{IH} = 2.7V$
- Input Pulse Rise and Fall Times: 5ns
- Input and Output Timing Reference Level: 1.5V
- Output Load: 1 TTL Gate + C_L (100pF) including scope and jig

DS2045L 3.3V Single-Piece 1Mb Nonvolatile SRAM

DS2045L

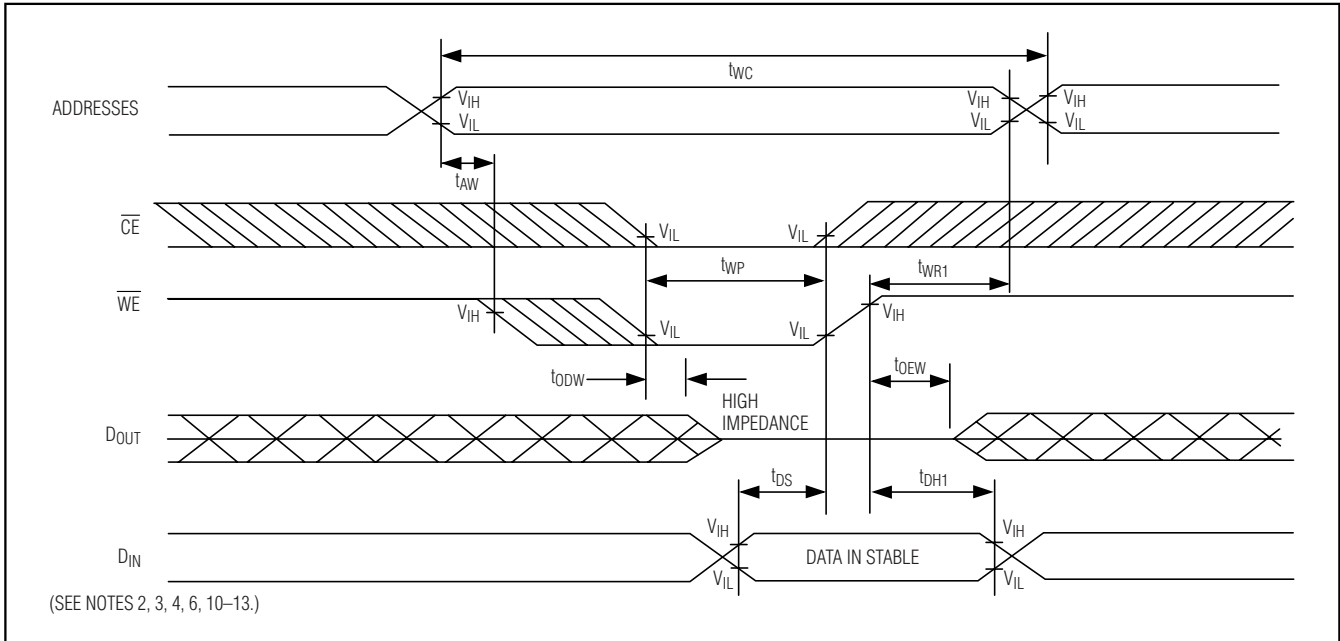
Read Cycle



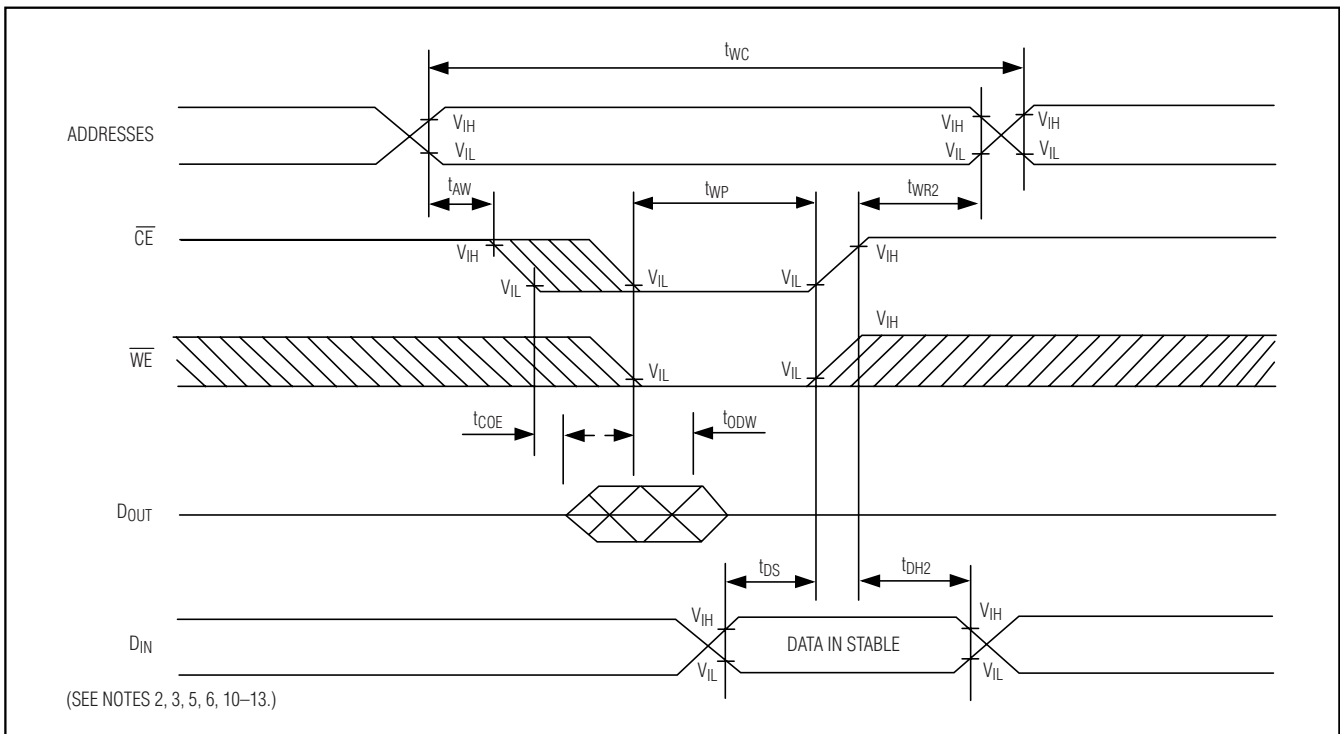
DS2045L 3.3V Single-Piece 1Mb Nonvolatile SRAM

DS2045L

Write Cycle 1

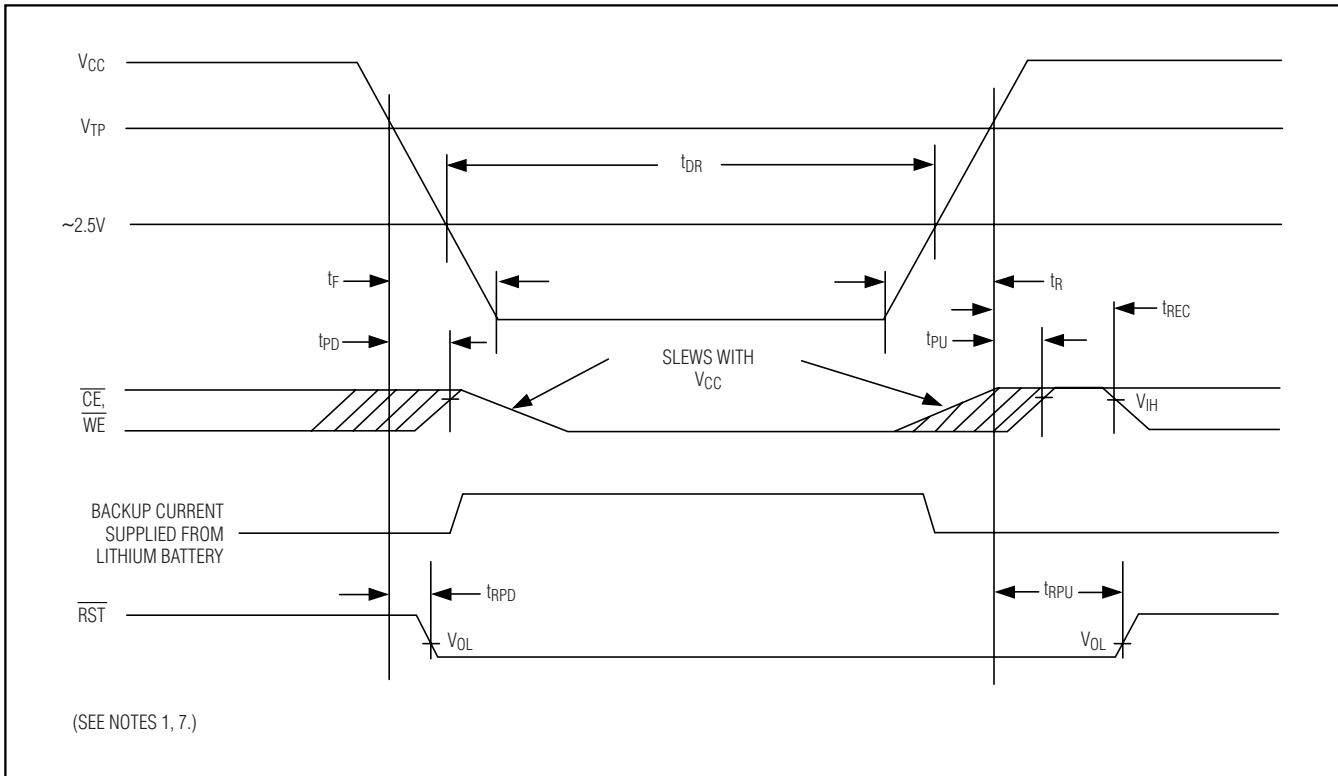


Write Cycle 2



DS2045L 3.3V Single-Piece 1Mb Nonvolatile SRAM

Power-Down/Power-Up Condition



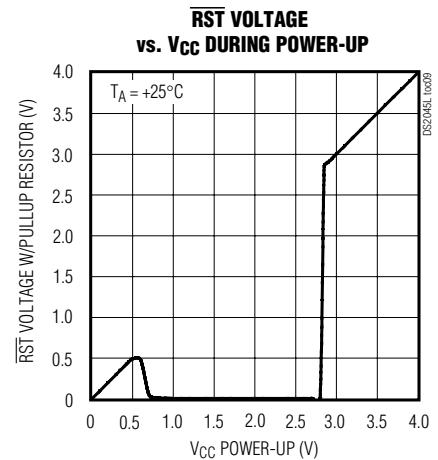
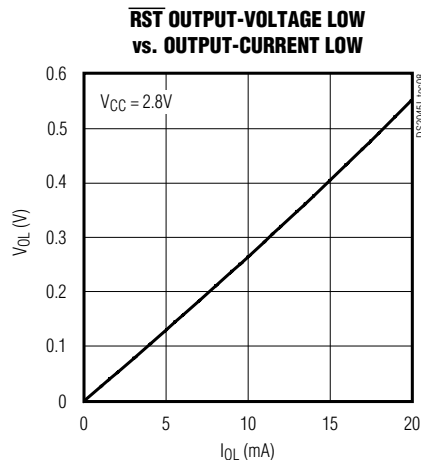
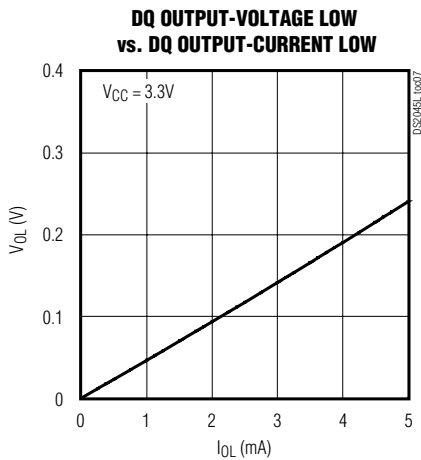
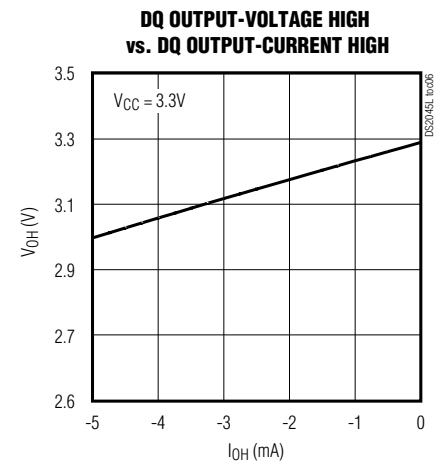
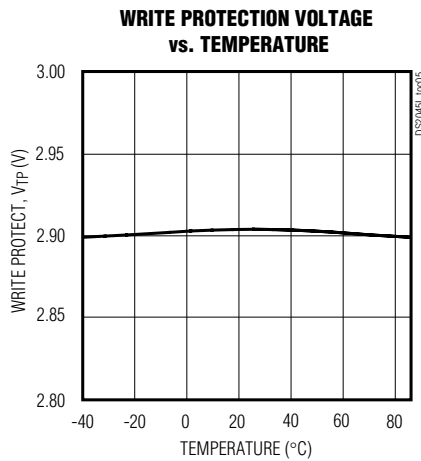
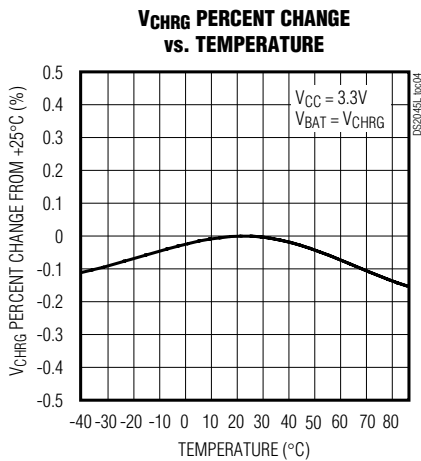
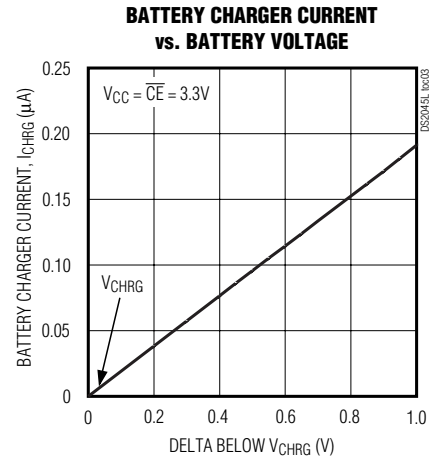
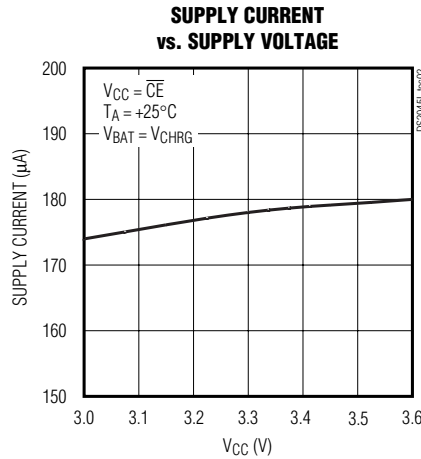
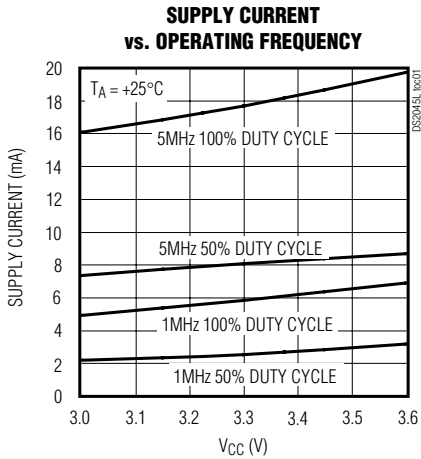
- Note 1:** $\overline{\text{RST}}$ is an open-drain output and cannot source current. An external pullup resistor should be connected to this pin to realize a logic-high level.
- Note 2:** These parameters are sampled with a 5pF load and are not 100% tested.
- Note 3:** t_{WP} is specified as the logical AND of $\overline{\text{CE}}$ and $\overline{\text{WE}}$. t_{WP} is measured from the latter of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ going low to the earlier of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ going high.
- Note 4:** t_{WR1} and t_{DH1} are measured from $\overline{\text{WE}}$ going high.
- Note 5:** t_{WR2} and t_{DH2} are measured from $\overline{\text{CE}}$ going high.
- Note 6:** t_{DS} is measured from the earlier of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ going high.
- Note 7:** In a power-down condition, the voltage on any pin can not exceed the voltage on V_{CC} .
- Note 8:** The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user. Minimum expected data-retention time is based on a maximum of two +230°C convection solder reflow exposures, followed by a fully charged cell. Full charge occurs with the initial application of V_{CC} for a minimum of 96 hours. This parameter is assured by component selection, process control, and design. It is not measured directly in production testing.
- Note 9:** $\overline{\text{WE}}$ is high for a read cycle.
- Note 10:** $\overline{\text{OE}} = V_{IH}$ or V_{IL} . If $\overline{\text{OE}} = V_{IH}$ during write cycle, the output buffers remain in a high-impedance state.
- Note 11:** If the $\overline{\text{CE}}$ low transition occurs simultaneously with or later than the $\overline{\text{WE}}$ low transition, the output buffers remain in a high-impedance state during this period.
- Note 12:** If the $\overline{\text{CE}}$ high transition occurs prior to or simultaneously with the $\overline{\text{WE}}$ high transition, the output buffers remain in a high-impedance state during this period.
- Note 13:** If $\overline{\text{WE}}$ is low or the $\overline{\text{WE}}$ low transition occurs prior to or simultaneously with the $\overline{\text{CE}}$ low transition, the output buffers remain in a high-impedance state during this period.
- Note 14:** DS2045L BGA modules are recognized by Underwriters Laboratory (UL) under file E99151.

DS2045L 3.3V Single-Piece 1Mb Nonvolatile SRAM

Typical Operating Characteristics

($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)

DS2045L



DS2045L 3.3V Single-Piece 1Mb Nonvolatile SRAM

DS2045L

Pin Description

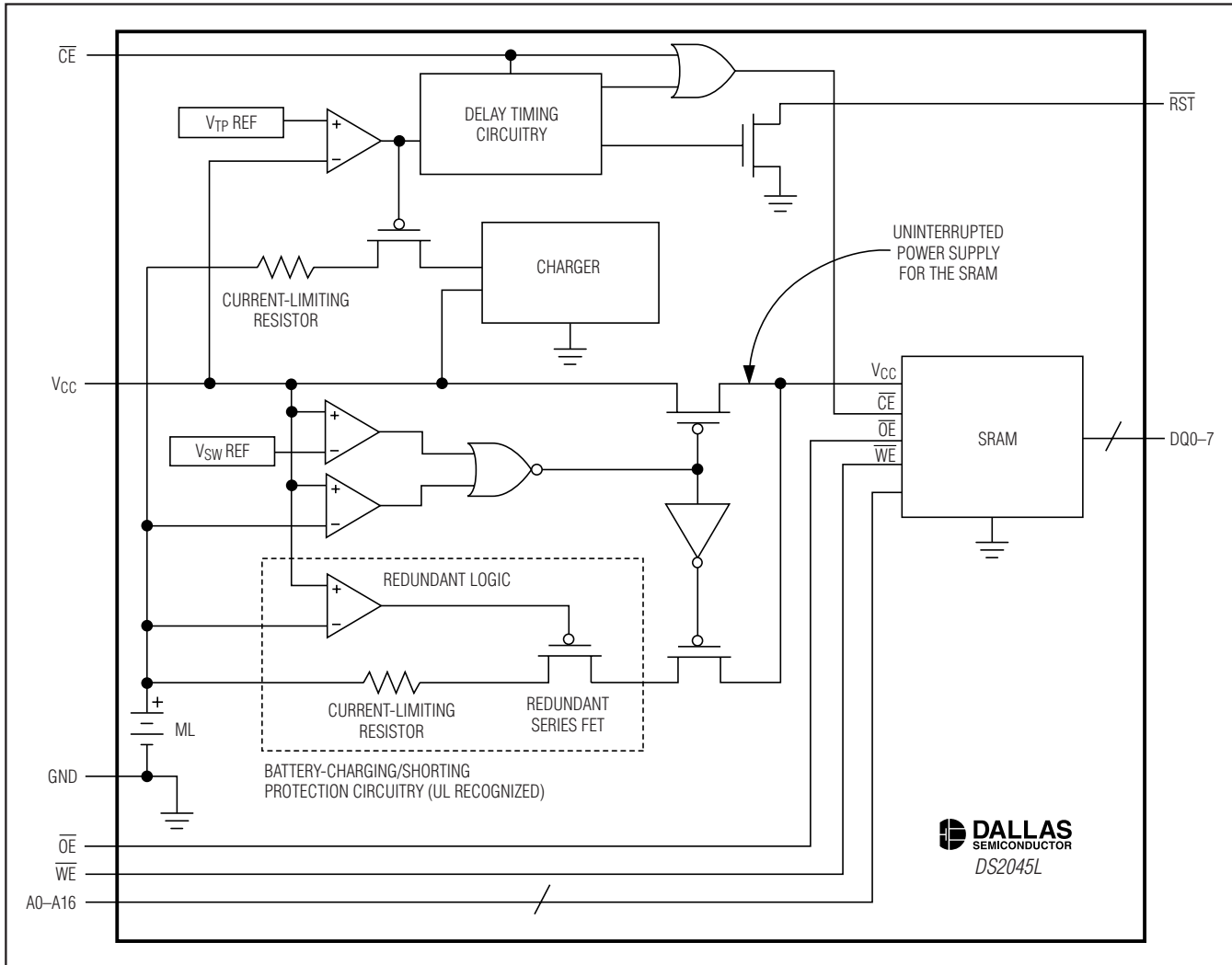
| BALLS | NAME | DESCRIPTION |
|--------------------|-------------------------|-------------------------|
| A1, A2, A3, A4 | GND | Ground |
| B1, B2, B3, B4 | N.C. | No Connection |
| C1, C2, C3, C4 | A15 | Address Input 15 |
| D1, D2, D3, D4 | A16 | Address Input 16 |
| E1, E2, E3, E4 | $\overline{\text{RST}}$ | Open-Drain Reset Output |
| F1, F2, F3, F4 | VCC | Supply Voltage |
| G1, G2, G3, G4 | $\overline{\text{WE}}$ | Write Enable Input |
| H1, H2, H3, H4 | $\overline{\text{OE}}$ | Output Enable Input |
| J1, J2, J3, J4 | $\overline{\text{CE}}$ | Chip Enable Input |
| K1, K2, K3, K4 | DQ7 | Data Input/Output 7 |
| L1, L2, L3, L4 | DQ6 | Data Input/Output 6 |
| M1, M2, M3, M4 | DQ5 | Data Input/Output 5 |
| N1, N2, N3, N4 | DQ4 | Data Input/Output 4 |
| P1, P2, P3, P4 | DQ3 | Data Input/Output 3 |
| R1, R2, R3, R4 | DQ2 | Data Input/Output 2 |
| T1, T2, T3, T4 | DQ1 | Data Input/Output 1 |
| U1, U2, U3, U4 | DQ0 | Data Input/Output 0 |
| V1, V2, V3, V4 | GND | Ground |
| W1, W2, W3, W4 | GND | Ground |
| Y1, Y2, Y3, Y4 | GND | Ground |
| A17, A18, A19, A20 | GND | Ground |
| B17, B18, B19, B20 | N.C. | No Connection |
| C17, C18, C19, C20 | N.C. | No Connection |
| D17, D18, D19, D20 | A14 | Address Input 14 |
| E17, E18, E19, E20 | A13 | Address Input 13 |
| F17, F18, F19, F20 | A12 | Address Input 12 |
| G17, G18, G19, G20 | A11 | Address Input 11 |
| H17, H18, H19, H20 | A10 | Address Input 10 |
| J17, J18, J19, J20 | A9 | Address Input 9 |
| K17, K18, K19, K20 | A8 | Address Input 8 |
| L17, L18, L19, L20 | A7 | Address Input 7 |
| M17, M18, M19, M20 | A6 | Address Input 6 |

| BALLS | NAME | DESCRIPTION |
|--------------------|------|-----------------|
| N17, N18, N19, N20 | A5 | Address Input 5 |
| P17, P18, P19, P20 | A4 | Address Input 4 |
| R17, R18, R19, R20 | A3 | Address Input 3 |
| T17, T18, T19, T20 | A2 | Address Input 2 |
| U17, U18, U19, U20 | A1 | Address Input 1 |
| V17, V18, V19, V20 | A0 | Address Input 0 |
| W17, W18, W19, W20 | GND | Ground |
| Y17, Y18, Y19, Y20 | GND | Ground |
| A5, B5, C5, D5 | N.C. | No Connection |
| A6, B6, C6, D6 | N.C. | No Connection |
| A7, B7, C7, D7 | N.C. | No Connection |
| A8, B8, C8, D8 | N.C. | No Connection |
| A9, B9, C9, D9 | N.C. | No Connection |
| A10, B10, C10, D10 | N.C. | No Connection |
| A11, B11, C11, D11 | N.C. | No Connection |
| A12, B12, C12, D12 | N.C. | No Connection |
| A13, B13, C13, D13 | N.C. | No Connection |
| A14, B14, C14, D14 | N.C. | No Connection |
| A15, B15, C15, D15 | N.C. | No Connection |
| A16, B16, C16, D16 | N.C. | No Connection |
| U5, V5, W5, Y5 | N.C. | No Connection |
| U6, V6, W6, Y6 | N.C. | No Connection |
| U7, V7, W7, Y7 | N.C. | No Connection |
| U8, V8, W8, Y8 | N.C. | No Connection |
| U9, V9, W9, Y9 | N.C. | No Connection |
| U10, V10, W10, Y10 | N.C. | No Connection |
| U11, V11, W11, Y11 | N.C. | No Connection |
| U12, V12, W12, Y12 | N.C. | No Connection |
| U13, V13, W13, Y13 | N.C. | No Connection |
| U14, V14, W14, Y14 | N.C. | No Connection |
| U15, V15, W15, Y15 | N.C. | No Connection |
| U16, V16, W16, Y16 | N.C. | No Connection |

DS2045L 3.3V Single-Piece 1Mb Nonvolatile SRAM

Functional Diagram

DS2045L



Detailed Description

The DS2045L is a 1Mb (128kb x 8 bits) fully static, NV memory similar in function and organization to the DS1245W NV SRAM, but containing a rechargeable ML battery. The DS2045L NV SRAM constantly monitors VCC for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. There is no limit to the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing. This device can be used in place of SRAM, EEPROM, or flash components.

The DS2045L assembly consists of a low-power SRAM, an ML battery, and an NV controller with a battery charger, integrated on a standard 256-ball, 27mm² BGA substrate. Unlike other surface-mount NV memory modules that require the battery to be removable for soldering, the internal ML battery can tolerate exposure to convection reflow soldering temperatures allowing this single-piece component to be handled with standard BGA assembly techniques.

The DS2045L also contains a power-supply monitor output, $\overline{\text{RST}}$, which can be used as a CPU supervisor for a microprocessor.

DS2045L 3.3V Single-Piece 1Mb Nonvolatile SRAM

Memory Operation Truth Table

| \overline{WE} | \overline{CE} | \overline{OE} | MODE | I _{CC} | OUTPUTS |
|-----------------|-----------------|-----------------|---------|-----------------|----------------|
| 1 | 0 | 0 | Read | Active | Active |
| 1 | 0 | 1 | Read | Active | High Impedance |
| 0 | 0 | X | Write | Active | High Impedance |
| X | 1 | X | Standby | Standby | High Impedance |

X = Don't care.

Read Mode

The DS2045L executes a read cycle whenever \overline{WE} (write enable) is inactive (high) and \overline{CE} (chip enable) is active (low). The unique address specified by the 17 address inputs (A0 to A16) defines which of the 131,072 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (access time) after the last address input signal is stable, providing that \overline{CE} and \overline{OE} (output enable) access times are also satisfied. If \overline{CE} and \overline{OE} access times are not satisfied, then data access must be measured from the later occurring signal (\overline{CE} or \overline{OE}) and the limiting parameter is either t_{CO} for \overline{CE} or t_{OE} for \overline{OE} rather than address access.

Write Mode

The DS2045L executes a write cycle whenever the \overline{CE} and \overline{WE} signals are active (low) after address inputs are stable. The later-occurring falling edge of \overline{CE} or \overline{WE} will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of \overline{CE} or \overline{WE} . All address inputs must be kept valid throughout the write cycle. \overline{WE} must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The \overline{OE} control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers have been enabled (\overline{CE} and \overline{OE} active) then \overline{WE} will disable the outputs in t_{ODW} from its falling edge.

Data-Retention Mode

The DS2045L provides full functional capability for V_{CC} greater than 3.0V and write-protects by 2.8V. Data is maintained in the absence of V_{CC} without additional support circuitry. The NV static RAM constantly monitors V_{CC} . Should the supply voltage decay, the NV SRAM automatically write-protects itself. All inputs become "don't care", and all data outputs become high impedance. As V_{CC} falls below approximately 2.5V (V_{SW}), the power-switching circuit connects the lithium

energy source to the RAM to retain data. During power-up, when V_{CC} rises above V_{SW} , the power-switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds V_{TP} for a minimum duration of t_{REC} .

Battery Charging

When V_{CC} is greater than V_{TP} , an internal regulator charges the battery. The UL-approved charger circuit includes short-circuit protection and a temperature-stabilized voltage reference for on-demand charging of the internal battery. Typical data-retention expectations of 16 weeks *per charge cycle* are achievable.

A maximum of 96 hours of charging time is required to fully charge a depleted battery.

System Power Monitoring

When the external V_{CC} supply falls below the selected out-of-tolerance trip point, the output \overline{RST} is forced active (low). Once active, the \overline{RST} is held active until the V_{CC} supply has fallen below that of the internal battery. On power-up, the \overline{RST} output is held active until the external supply is greater than the selected trip point and one reset timeout period (t_{RPU}) has elapsed. This is sufficiently longer than t_{REC} to ensure that the SRAM is ready for access by the microprocessor.

Freshness Seal and Shipping

The DS2045L is shipped from Dallas Semiconductor with the lithium battery electrically disconnected, guaranteeing that no battery capacity has been consumed during transit or storage. As shipped, the lithium battery is ~60% charged, and no preassembly charging operations should be attempted.

When V_{CC} is first applied at a level greater than V_{TP} , the lithium battery is enabled for backup operation. A 96 hour initial battery charge time is recommended for new system installations.

DS2045L 3.3V Single-Piece 1Mb Nonvolatile SRAM

DS2045L

Recommended Reflow Temperature Profile

| PROFILE FEATURE | Sn-Pb EUTECTIC ASSEMBLY |
|---|-------------------------------------|
| Average ramp-up rate (T _L to T _P) | 3°C/second max |
| Preheat - Temperature min (T _{Smin}) - Temperature max (T _{Smax}) - Time (min to max) (ts) | 100°C 150°C 60 to 120 seconds |
| T _{Smax} to T _L - Ramp-up rate | |
| Time maintained above: - Temperature (T _L) - Time (t _L) | 183°C 60 to 150 seconds |
| Peak temperature (T _P) | 225 +0/-5°C |
| Time within 5°C of actual peak temperature (T _P) | 10 to 30 seconds |
| Ramp-down rate | 6°C/second max |
| Time 25°C to peak temperature | 6 minutes max |

Note: All temperatures refer to top side of the package, measured on the package body surface.

Recommended Cleaning Procedures

The DS2045L may be cleaned using aqueous-based cleaning solutions. No special precautions are needed when cleaning boards containing a DS2045L module.

Removal of the topside label violates the environmental integrity of the package and voids the warranty of the product.

Applications Information

Power-Supply Decoupling

To achieve the best results when using the DS2045L, decouple the power supply with a 0.1µF capacitor. Use a high-quality, ceramic surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, while ceramic capacitors have adequately high frequency response for decoupling applications.

Using the Open-Drain \overline{RST} Output

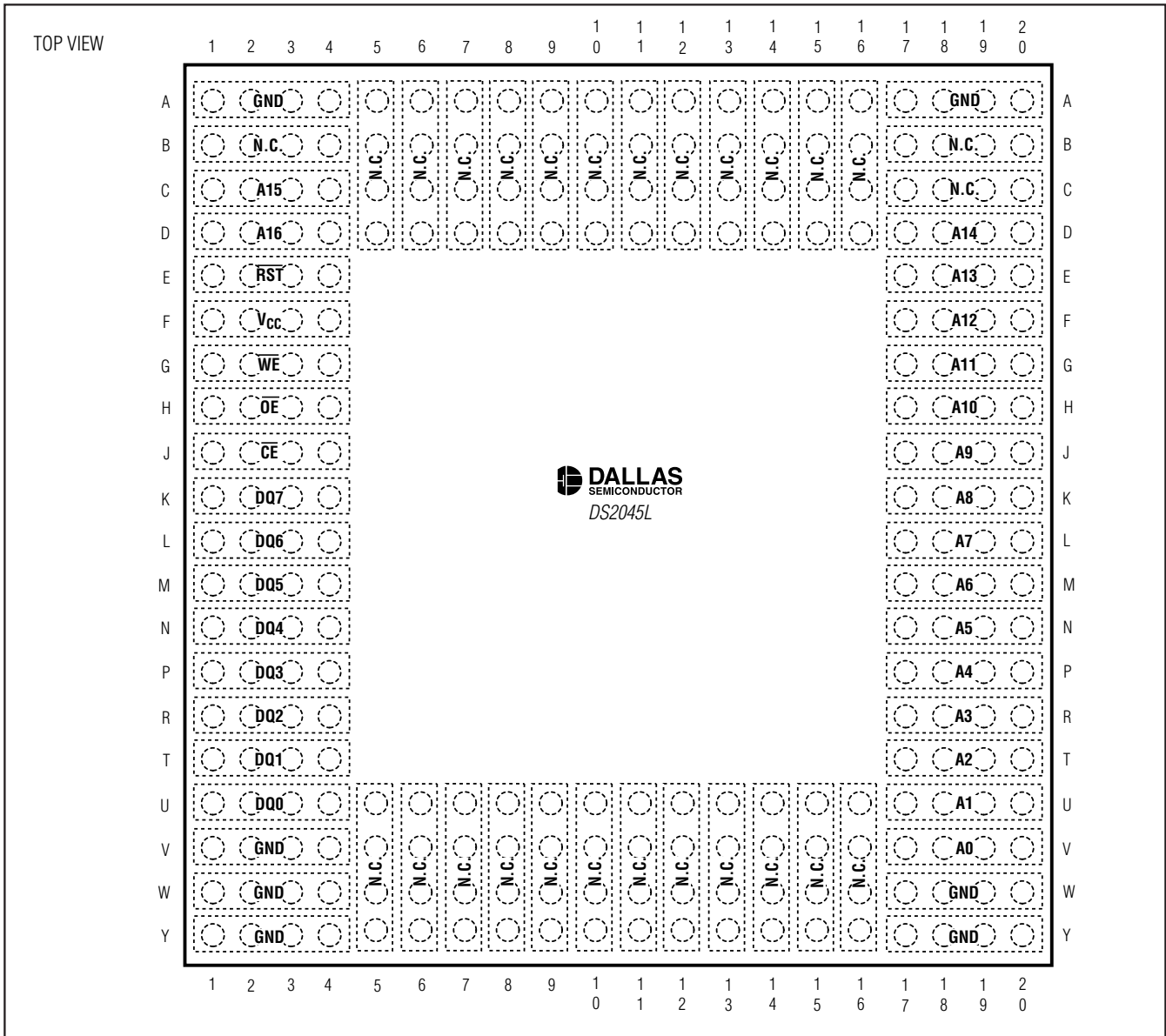
The \overline{RST} output is open drain, and therefore requires a pullup resistor to realize a high logic output level. Pullup resistor values between 1kΩ and 10kΩ are typical.

Battery Charging/Lifetime

The DS2045L charges an ML battery to maximum capacity in approximately 96 hours of operation when V_{CC} is greater than V_{TP}. Once the battery is charged, its lifetime depends primarily on the V_{CC} duty cycle. The DS2045L can maintain data from a single, initial charge for up to 16 weeks. Once recharged, this deep-discharge cycle can be repeated up to 20 times, producing a worst-case service life of 6 years. More typical duty cycles are of shorter duration, enabling the DS2045L to be charged hundreds of times, therefore extending the service life well beyond 6 years.

DS2045L 3.3V Single-Piece 1Mb Nonvolatile SRAM

Pin Configuration



Revision History

Pages changed at Rev 3: 1, 3, 12

Package Information



For the latest package outline information, go to www.maxim-ic.com/DallasPackInfo.

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

12 Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View DS2045L-100#](#) on WIN SOURCE
-  [Maxim Integrated](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management