THE DATASHEET OF

DS1743P-100IND+

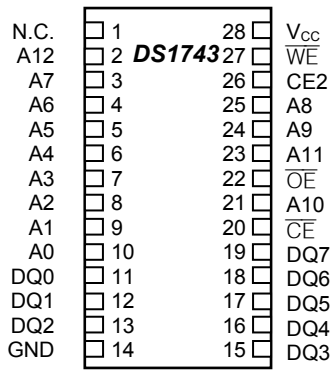
DS1743/DS1743P
Y2K-Compliant, Nonvolatile Timekeeping RAMs

FEATURES

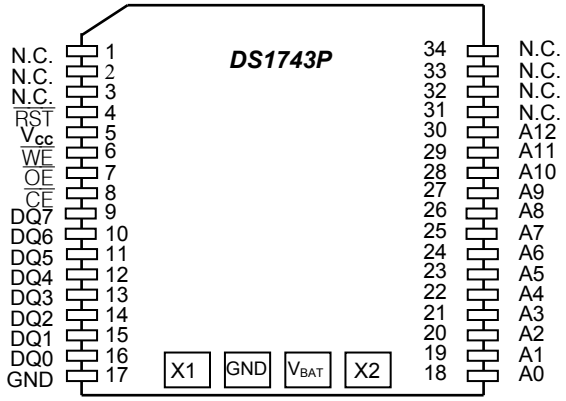
- Integrated NV SRAM, Real-Time Clock, Crystal, Power-Fail Control Circuit, and Lithium Energy Source
- Clock Registers are Accessed Identically to the Static RAM. These Registers Reside in the Eight Top RAM Locations.
- Century Byte Register
- Totally Nonvolatile with Over 10 Years of Operation in the Absence of Power
- BCD-Coded Century, Year, Month, Date, Day, Hours, Minutes, and Seconds with Automatic Leap Year Compensation Valid through 2099
- Low-Battery-Voltage Level Indicator Flag
- Power-Fail Write Protection Allows for ±10% V_{CC} Power-Supply Tolerance
- Lithium Energy Source is Electrically Disconnected to Retain Freshness Until Power is Applied for the First Time
- DIP Module Only
  Standard JEDEC Bytewide 8k x 8 Static RAM Pinout
- PowerCap Module Board Only
  Surface-Mountable Package for Direct Connection to PowerCap Containing Battery and Crystal
  Replaceable Battery (PowerCap)
  Power-On Reset Output
  Pin-for-Pin Compatible with Other Densities of DS174XP Timekeeping RAM
- Underwriters Laboratories (UL) Recognized to Prevent Charging of the Internal Lithium Battery

PIN CONFIGURATIONS

TOP VIEW



28-Pin Encapsulated Package
(28 PIN 740)



34-Pin PowerCap Module Board
(Uses DS9034PCX+ or DS9034I-PCX+ PowerCap)

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maximintegrated.com/errata.*

19-6719; Rev 9/13

PIN DESCRIPTION

PIN		NAME	FUNCTION
PDIP	PowerCap		
1	1, 2, 3, 31–34	N.C.	No Connection
2	30	A12	Address Input
3	25	A7	
4	24	A6	
5	23	A5	
6	22	A4	
7	21	A3	
8	20	A2	
9	19	A1	
10	18	A0	
11	16	DQ0	Data Input/ Output
12	15	DQ1	
13	14	DQ2	
14	17	GND	Ground
15	13	DQ3	Data Input/ Output
16	12	DQ4	
17	11	DQ5	
18	10	DQ6	
19	9	DQ7	

PIN		NAME	FUNCTION
PDIP	PowerCap		
20	8	$\overline{CE}$	Chip Enable, Active Low
21	28	A10	Address Input
22	7	$\overline{OE}$	Output Enable, Active Low
23	29	A11	Address Input
24	27	A9	
25	26	A8	
26	—	CE2	Chip Enable 2
27	6	$\overline{WE}$	Write Enable, Active Low
28	5	V_{CC}	Power-Supply Input
—	4	$\overline{RST}$	Power-On Reset Output, Active Low
—		X1, X2	Crystal Connection
—		V_{BAT}	Battery Connection

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE	VOLTAGE (V)	TOP MARK**
DS1743-85+	0°C to +70°C	28 EDIP Module	5	DS1743-85
DS1743-100+	0°C to +70°C	28 EDIP Module	5	DS1743-100
DS1743-100 IND+	-40°C to +85°C	28 EDIP Module	5	DS1743-100-IND
DS1743P-85+	0°C to +70°C	34 PowerCap*	5	DS1743P-85
DS1743P-100+	0°C to +70°C	34 PowerCap*	5	DS1743P-100
DS1743P-100IND+	-40°C to +85°C	34 PowerCap*	5	DS1743P-100 IND
DS1743W-120+	0°C to +70°C	28 EDIP Module	3.3	DS1743W-120
DS1743W-120 IND+	-40°C to +85°C	28 EDIP Module	3.3	DS1743W-120 IND
DS1743W-150+	0°C to +70°C	28 EDIP Module	3.3	DS1743W-150
DS1743W-150 IND+	-40°C to +85°C	28 EDIP Module	3.3	DS1743W-150 IND
DS1743WP-120+	0°C to +70°C	34 PowerCap*	3.3	DS1743WP-120
DS1743WP-120 IND+	-40°C to +85°C	34 PowerCap*	3.3	DS1743WP-120 IND
DS9034PCX+	0°C to +70°C	PowerCap	—	DS9034PC
DS9034I-PCX+	-40°C to +85°C	PowerCap IND	—	DS9034PCI

+Denotes a lead(Pb)-free/RoHS-compliant package.
**DS9034PCX+ or DS9034I-PCX+ required (must be ordered separately).*
***A '+' indicates lead(Pb)-free. The top mark will include a '+' symbol on lead(Pb)-free devices.*

DESCRIPTION

The DS1743 is a full-function, year-2000-compliant (Y2KC), real-time clock/calendar (RTC) and 8k x 8 nonvolatile static RAM. User access to all registers within the DS1743 is accomplished with a bytewide interface as shown in Figure 1. The RTC information and control bits reside in the eight uppermost RAM locations. The RTC registers contain century, year, month, date, day, hours, minutes, and seconds data in 24-hour binary-coded decimal (BCD) format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double buffered to avoid access of incorrect data that can occur during clock update cycles. The double-buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1743 also contains its own power-fail circuitry, which deselects the device when the V_{CC} supply is in an out-of-tolerance condition. When V_{CC} is above V_{PF}, the device is fully accessible. When V_{CC} is below V_{PF}, the internal $\overline{CE}$ signal is forced high, preventing any access. When V_{CC} rises above V_{PF}, access remains inhibited for T_{REC}, allowing time for the system to stabilize. These features prevent loss of data from unpredictable system operation brought on by low V_{CC} as errant access and update cycles are avoided.

PACKAGES

The DS1743 is available in two packages: the 28-pin DIP and the 34-pin PowerCap module. The 28-pin DIP-style module integrates the crystal, lithium energy source, and silicon all in one package. The 34-pin PowerCap Module Board is designed with contacts for connection to a separate PowerCap (DS9034PCX) that contains the crystal and battery. This design allows the PowerCap to be mounted on top of the DS1743P after the completion of the surface-mount process. Mounting the PowerCap after the surface-mount process prevents damage to the crystal and battery due to the high temperatures required for solder reflow. The PowerCap is keyed to prevent reverse insertion. The PowerCap Module Board and PowerCap are ordered separately and shipped in separate containers.

TIME AND DATE OPERATION

The time and date information is obtained by reading the appropriate register bytes. Table 2 shows the RTC registers. The time and date are set or initialized by writing the appropriate register bytes. The contents of the time and date registers are in the BCD format. The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined, but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday and so on). Illogical time and date entries result in undefined operation.

CLOCK OPERATIONS-READING THE CLOCK

While the double-buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1743 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a 1 is written into the read bit, bit 6 of the century register (see Table 2). As long as a 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the count that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double-buffered system continue to update so that the clock accuracy is not affected by the access of data. All the DS1743 registers are updated simultaneously after the internal clock register updating process has been re-enabled. Updating is within a second after the read bit is written to 0.

The READ bit must be a zero for a minimum of 500µs to ensure the external registers are updated.

Figure 1. Block Diagram

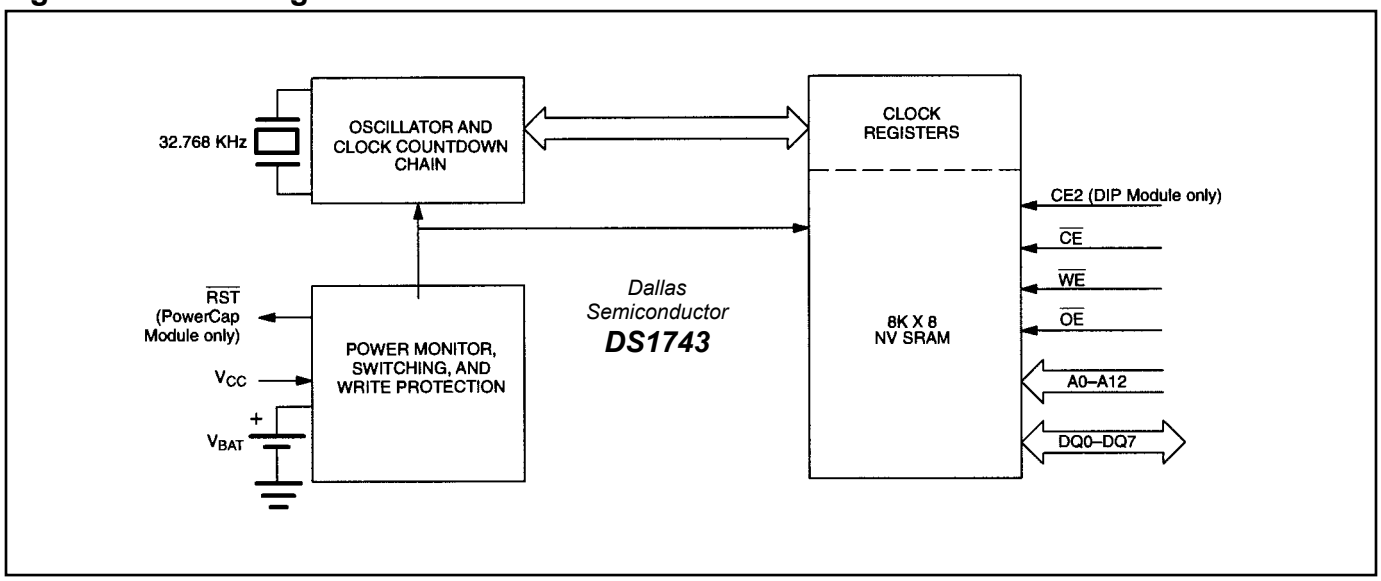


Table 1. Truth Table

V_{CC}	$\overline{CE}$	CE2	$\overline{OE}$	$\overline{WE}$	MODE	DQ	POWER
$V_{CC} > V_{PF}$	V_{IH}	X	X	X	Deselect	High-Z	Standby
	X	V_{IL}	X	X	Deselect	High-Z	Standby
	V_{IL}	V_{IH}	X	V_{IL}	Write	Data In	Active
	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Read	Data Out	Active
	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Read	High-Z	Active
$V_{SO} < V_{CC} < V_{PF}$	X	X	X	X	Deselect	High-Z	CMOS Standby
$V_{CC}<V_{SO}<V_{PF}$	X	X	X	X	Deselect	High-Z	Data-Retention Mode

SETTING THE CLOCK

As shown in Table 2, bit 7 of the Control register is the W (write) bit. Setting the W bit to 1 halts updates to the DS1743 registers. The user can subsequently load correct date and time values into all eight registers, followed by a write cycle of 00h to the Control register to clear the W bit and transfer those new settings into the clock, allowing timekeeping operations to resume from the new set-point.

Again referring to Table 2, bit 6 of the Control register is the R (read) bit. Setting the R bit to 1 halts updates to the DS1743 registers. The user can subsequently read the date and time values from the eight registers without those contents possibly changing during those I/O operations. A subsequent write cycle of 00h to the Control register to clear the R bit allows timekeeping operations to resume from the previous set-point.

The pre-existing contents of the Control register bits 0:5 (Century value) are ignored/unmodified by a write cycle to Control if either the W or R bits are being set to 1 in that write operation.

The pre-existing contents of the Control register bits 0:5 (Century value) will be modified by a write cycle to Control if the W bit is being cleared to 0 in that write operation.

The pre-existing contents of the Control register bits 0:5 (Century value) will not be modified by a write cycle to Control if the R bit is being cleared to 0 in that write operation.

STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB (bit 7) of the seconds registers, see Table 2. Setting it to a 1 stops the oscillator.

FREQUENCY TEST BIT

As shown in Table 2, bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic 1 and the oscillator is running, the LSB of the seconds register will toggle at 512Hz. When the seconds register is being read, the DQ0 line will toggle at the 512Hz frequency as long as conditions for access remain valid (i.e., $\overline{CE}$ low, $\overline{OE}$ low, $\overline{WE}$ high, and address for seconds register remain valid and stable).

CLOCK ACCURACY (DIP MODULE)

The DS1743 is guaranteed to keep time accuracy to within ±1 minute per month at +25°C. The RTC is calibrated at the factory by Dallas Semiconductor using nonvolatile tuning elements, and does not require additional calibration. For this reason, methods of field clock calibration are not available and not necessary. The electrical environment also affects clock accuracy, so caution should be taken to place the RTC in the lowest-level EMI section of the PC board layout. For additional information, please refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks*.

CLOCK ACCURACY (PowerCap MODULE)

The DS1743 and DS9034PCX are each individually tested for accuracy. Once mounted together, the module will typically keep time accuracy to within ±1.53 minutes per month (35ppm) at +25°C. The electrical environment also affects clock accuracy, so caution should be taken to place the RTC in the lowest-level EMI section of the PC board layout. For additional information, please refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks*.

Table 2. Register Map

ADDRESS	DATA								FUNCTION	RANGE
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1FFF	10 Year				Year				Year	00–99
1FFE	X	X	X	10 Month	Month				Month	01–12
1FFD	X	X	10 Date		Date				Date	01–31
1FFC	BF	FT	X	X	X	Day			Day	01–07
1FFB	X	X	10 Hour		Hour				Hour	00–23
1FFA	X	10 Minutes			Minutes				Minutes	00–59
1FF9	$\overline{OSC}$	10 Seconds			Seconds				Seconds	00–59
1FF8	W	R	10 Century		Century				Control	00–39

$\overline{OSC}$ = STOP BIT R = READ BIT FT = FREQUENCY TEST
W = WRITE BIT X = SEE NOTE BELOW BF = BATTERY FLAG

Note: *All indicated "X" bits must be set to "0" when written to ensure proper clock operation.*

RETRIEVING DATA FROM RAM OR CLOCK

The DS1743 is in the read mode whenever $\overline{OE}$ (output enable) is low, $\overline{WE}$ (write enable) is high, and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within t_{AA} after the last address input is stable, providing that the, $\overline{CE}$ and $\overline{OE}$ access times and states are satisfied. If $\overline{CE}$, or $\overline{OE}$ access times and states are not met, valid data will be available at the latter of chip enable access (t_{CEA}) or at output enable access time (t_{CEA}). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$ and $\overline{OE}$. If the outputs are activated before t_{AA}, the data lines are driven to an intermediate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data will remain valid for output data hold time (t_{OH}) but will then go indeterminate until the next address access.

WRITING DATA TO RAM OR CLOCK

The DS1743 is in the write mode whenever $\overline{WE}$, and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring transition of $\overline{WE}$, on $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return inactive for a minimum of t_{WR} prior to the initiation of another read or write cycle. Data in must be valid t_{DS} prior to the end of write and remain valid for t_{DH} afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs t_{WEZ} after $\overline{WE}$ goes active.

DATA-RETENTION MODE

The 5V device is fully accessible and data can be written or read only when V_{CC} is greater than V_{PF}. However, when V_{CC} is below the power-fail point, V_{PF}, (point at which write protection occurs) the internal clock registers and SRAM are blocked from any access. At this time (PowerCap only) the power-fail reset-output signal ($\overline{RST}$) is driven active and remains active until V_{CC} returns to nominal levels. When V_{CC} falls below the battery switch point V_{SO} (battery supply level), device power is switched from the V_{CC} in to the backup battery. RTC operation and SRAM data are maintained from the battery until V_{CC} is returned to nominal levels.

The 3.3V device is fully accessible and data can be written or read only when V_{CC} is greater than V_{PF}. When V_{CC} falls below the power-fail point, V_{PF}, access to the device is inhibited. At this time the power-fail reset-output signal ($\overline{RST}$) is driven active and remains active until V_{CC} returns to nominal levels. If V_{PF} is less than V_{SO}, the device power is switched from V_{CC} to the backup supply (V_{BAT}) when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{SO}, the device power is switched from V_{CC} to the backup supply (V_{BAT}) when V_{CC} drops below V_{SO}. RTC operation and SRAM data are maintained from the battery until V_{CC} is returned to nominal levels. The $\overline{RST}$ (PowerCap only) signal is an open-drain output and requires a pullup resistor. Except for $\overline{RST}$, all control, data, and address signals must be powered down when V_{CC} is powered down.

BATTERY LONGEVITY

The DS1743 has a lithium power source that is designed to provide energy for clock activity and clock and RAM data retention when the V_{CC} supply is not present. The capability of this internal power supply is sufficient to power the DS1743 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at +25°C with the internal clock oscillator running in the absence of V_{CC} power. Each DS1743 is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than V_{PF}, the lithium energy source is enabled for battery backup operation. Actual life expectancy of the DS1743 will be longer than 10 years since no lithium battery energy is consumed when V_{CC} is present.

BATTERY MONITOR

The DS1743 constantly monitors the battery voltage of the internal battery. The battery flag bit (bit 7) of the day register is used to indicate the voltage level range of the battery. This bit is not writeable and should always be a 1 when read. If a 0 is ever present, an exhausted lithium energy source is indicated and both the contents of the RTC and RAM are questionable.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……-0.3V to +6.0V
Storage Temperature Range……-40°C to +85°C
Soldering Temperature (EDIP) (leads, 10 seconds)……..…+260°C
Soldering Temperature……..….See J-STD-020 Specification (See Note 8)

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMP RANGE	V_{CC}
Commercial	0°C to +70°C	3.3V ±10% or 5V ±10%
Industrial	-40°C to +85°C	3.3V ±10% or 5V ±10%

RECOMMENDED DC OPERATING CONDITIONS

(T_A = Over the Operating Range.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Logic 1 Voltage All Inputs	V_{IH}	V_{CC} = 5V ±10%	2.2		V_{CC} +0.3V	V	1
		V_{CC} = 3.3V ±10%	2.0		V_{CC} +0.3V	V	1
Logic 0 Voltage All Inputs	V_{IL}	V_{CC} = 5V ±10%	-0.3		+0.8	V	1
		V_{CC} = 3.3V ±10%	-0.3		+0.6	V	1

DC ELECTRICAL CHARACTERISTICS (5V)

(V_{CC} = 5.0V ±10%, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{CC}		15	50	mA	2, 3
TTL Standby Current ($\overline{CE}$ = V_{IH}, CE2 = V_{IL})	I_{CC1}		1	3	mA	2, 3
CMOS Standby Current ($\overline{CE} \geq V_{CC}$ - 0.2V; CE2 = GND + 0.2V)	I_{CC2}		1	3	mA	2, 3
Input Leakage Current (Any Input)	I_{IL}	-1		+1	µA	
Output Leakage Current (Any Output)	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0mA)	V_{OH}	2.4				1
Output Logic 0 Voltage (I_{OUT} = 2.1mA)	V_{OL1}			0.4		1
Write-Protection Voltage	V_{PF}	4.20		4.50	V	1
Battery Switchover Voltage	V_{SO}		V_{BAT}			1, 4

DC ELECTRICAL CHARACTERISTICS (3.3V)

(V_{CC} = 3.3V ±10%, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{CC}		10	30	mA	2, 3
TTL Standby Current ($\overline{CE} = V_{IH}$)	I_{CC1}		0.7	2	mA	2, 3
CMOS Standby Current ($\overline{CE} \geq V_{CC}$ - 0.2V; CE2 = GND + 0.2V)	I_{CC2}		0.7	2	mA	2, 3
Input Leakage Current (Any Input)	I_{IL}	-1		+1	µA	
Output Leakage Current (Any Output)	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0mA)	V_{OH}	2.4				1
Output Logic 0 Voltage (I_{OUT} =2.1mA)	V_{OL1}			0.4		1
Write-Protection Voltage	V_{PF}	2.75		2.97	V	1
Battery Switchover Voltage	V_{SO}		V_{BAT} or V_{PF}		V	1, 4

AC CHARACTERISTICS—READ CYCLE (5V)

(V_{CC} = 5.0V ±10%, T_A = Over the Operating Range.)

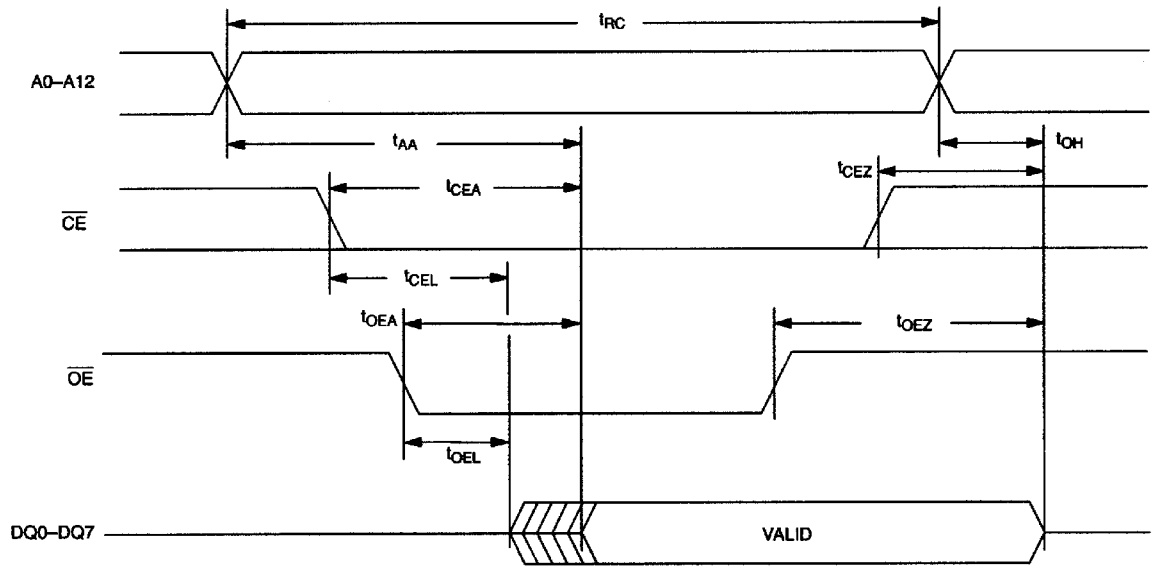
PARAMETER	SYMBOL	ACCESS						UNITS	NOTES
		70ns		85ns		100ns			
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		85		100		ns	
Address Access Time	t_{AA}		70		85		100	ns	
$\overline{CE}$ to CE2 to DQ Low-Z	t_{CEL}	5		5		5		ns	5
$\overline{CE}$ Access Time	t_{CEA}		70		85		100	ns	5
CE2 Access Time	t_{CE2A}		80		95		105	ns	5
$\overline{CE}$ and CE2 Data-Off Time	t_{CEZ}		25		30		35	ns	
$\overline{OE}$ to DQ Low-Z	t_{OEL}	5		5		5		ns	
$\overline{OE}$ Access Time	t_{OEA}		35		45		55	ns	
$\overline{OE}$ Data-Off Time	t_{OEZ}		25		30		35	ns	
Output Hold from Address	t_{OH}	5		5		5		ns	

AC CHARACTERISTICS—READ CYCLE (3.3V)

(V_{CC} = 3.3V ±10%, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	ACCESS				UNITS	NOTES
		120ns		150ns			
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		ns	
Address Access Time	t_{AA}		120		150	ns	
$\overline{CE}$ and CE2 Low to DQ Low-Z	t_{CEL}	5		5		ns	5
$\overline{CE}$ Access Time	t_{CEA}		120		150	ns	5
CE2 Access Time	t_{CE2A}		140		170	ns	5
$\overline{CE}$ and CE2 Data-Off time	t_{CEZ}		40		50	ns	5
$\overline{OE}$ Low to DQ Low-Z	t_{OEL}	5		5		ns	
$\overline{OE}$ Access Time	t_{OEA}		100		130	ns	
$\overline{OE}$ Data-Off Time	t_{OEZ}		35		35	ns	
Output Hold from Address	t_{OH}	5		5		ns	

READ CYCLE TIMING DIAGRAM



AC CHARACTERISTICS—WRITE CYCLE (5V)

(V_{CC} = 5.0V ±10%, T_A = Over the Operating Range.)

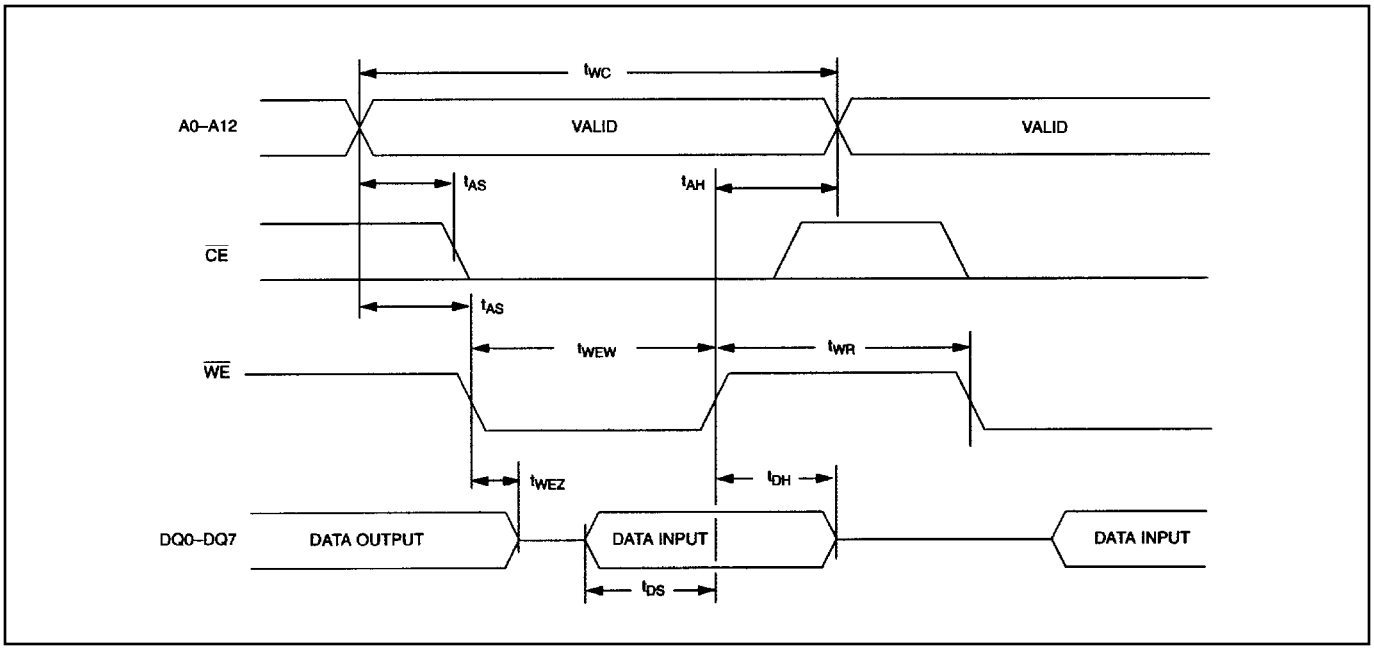
PARAMETER	SYMBOL	ACCESS						UNITS	NOTES
		70ns		85ns		100ns			
		MIN	MAX	MIN	MAX	MIN	MAX		
Write Cycle Time	t_{WC}	70		85		100		ns	
Address Setup Time	t_{AS}	0		0		0		ns	5
$\overline{WE}$ Pulse Width	t_{WEW}	50		65		70		ns	
$\overline{CE}$ Pulse Width	t_{CEW}	60		70		75		ns	5
CE2 Pulse Width	t_{CE2W}	65		75		85		ns	5
Data Setup Time	t_{DS}	30		35		40		ns	5
Data Hold Time $\overline{CE}$	t_{DH}	0		0		0		ns	5
Data Hold Time CE2	t_{DH}	8		8		8		ns	5
Address Hold Time	t_{AH}	5		5		5		ns	5
$\overline{WE}$ Data-Off Time	t_{WEZ}		25		30		35	ns	
Write Recovery Time	t_{WR}	10		10		10		ns	

AC CHARACTERISTICS—WRITE CYCLE (3.3V)

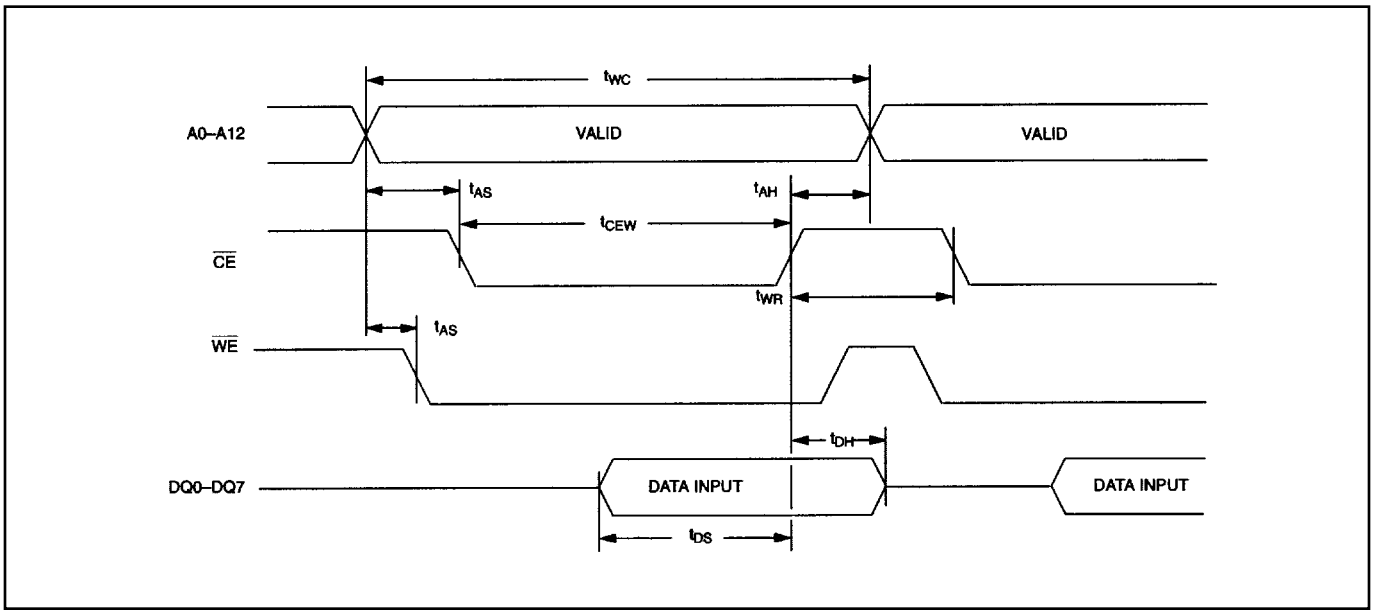
(**V_{CC} = 3.3V ±10%**, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	ACCESS				UNITS	NOTES
		120ns		150ns			
		MIN	MAX	MIN	MAX		
Write Cycle Time	t_{WC}	120		150		ns	
Address Setup Time	t_{AS}	0		0		ns	5
$\overline{WE}$ Pulse Width	t_{WEW}	100		130		ns	
$\overline{CE}$ and CE2 Pulse Width	t_{CEW}	110		140		ns	5
Data Setup Time	t_{DS}	80		90		ns	5
Data Hold Time $\overline{CE}$	t_{DH}	0		0		ns	5
Data Hold Time CE2	t_{DH}	10		10		ns	5
Address Hold Time	t_{AH}	0		0		ns	5
$\overline{WE}$ Data-Off Time	t_{WEZ}		40		50	ns	
Write Recovery Time	t_{WR}	10		10		ns	

WRITE CYCLE TIMING—WRITE-ENABLE CONTROLLED (See Note 5)



WRITE CYCLE TIMING—$\overline{CE}$/CE2-CONTROLLED (See Note 5)

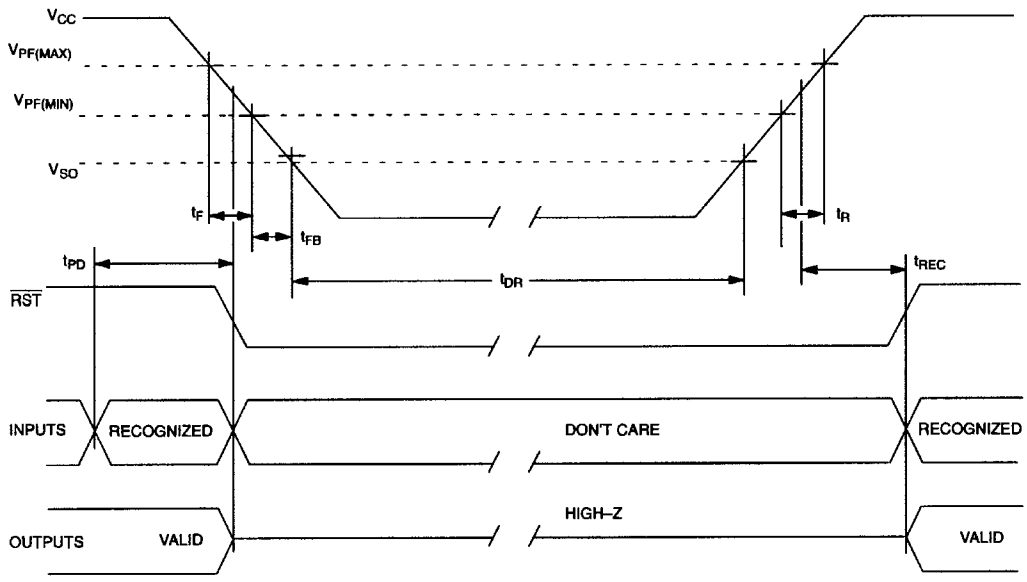


POWER-UP/DOWN CHARACTERISTICS—5V

(V_{CC} = 5.0V ±10%, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH}, CE2 at V_{IL}, Before Power-Down	t_{PD}	0			µs	
V_{CC} Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F	300			µs	
V_{CC} Fall Time: $V_{PF(MIN)}$ to V_{SO}	t_{FB}	10			µs	
V_{CC} Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R	0			µs	
Power-Up Recover Time	t_{REC}			35	ms	
Expected Data-Retention Time (Oscillator On)	t_{DR}	10			years	6, 7

POWER-UP/DOWN TIMING (5V DEVICE)

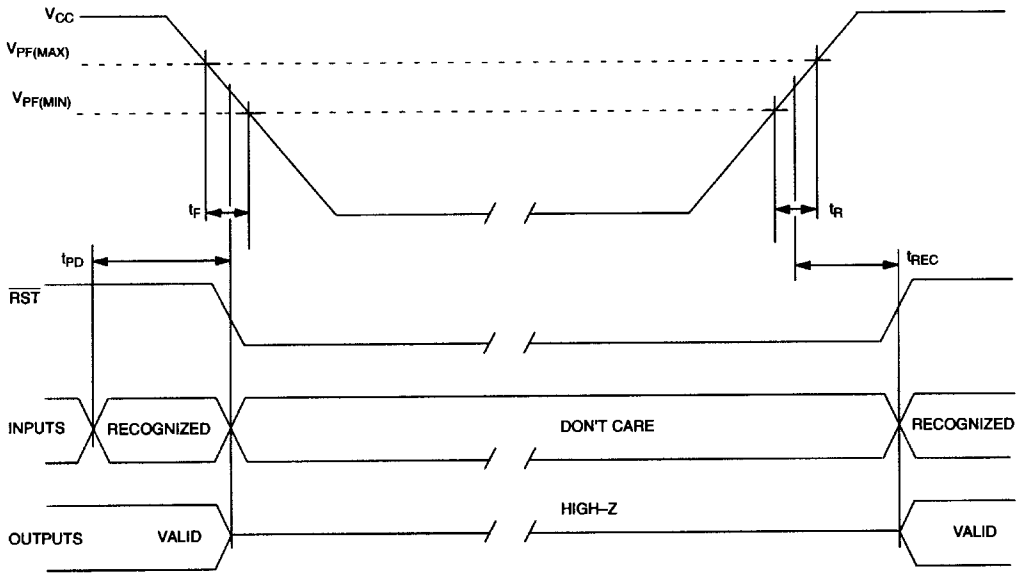


POWER-UP/DOWN CHARACTERISTICS—3.3V

(V_{CC} = 3.3V ±10%, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH}, Before Power-Down	t_{PD}	0			µs	
V_{CC} Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F	300			µs	
V_{CC} Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R	0			µs	
V_{PF} to $\overline{RST}$ High	t_{REC}			35	ms	
Expected Data-Retention Time (Oscillator On)	t_{DR}	10			years	6, 7

POWER-UP/DOWN WAVEFORM TIMING (3.3V DEVICE)



CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on All Input Pins	C_{IN}			7	pF	
Capacitance on All Output Pins	C_O			10	pF	

AC TEST CONDITIONS

Output Load: 50 pF + 1TTL Gate
Input Pulse Levels: 0 to 3.0V
Timing Measurement Reference Levels:
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

NOTES:

1) Voltages are referenced to ground.
2) Typical values are at +25°C and nominal supplies.
3) Outputs are open.
4) Battery switchover occurs at the lower of either the battery terminal voltage or V_{PF}.
5) The CE2 control signal functions the same as the $\overline{CE}$ signal except that the logic levels for active and inactive levels are opposite. If CE2 is used to terminate a write, the CE2 data hold time (t_{DH}) applies.
6) Data-retention time is at +25°C.
7) Each DS1743 has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined for DIP modules as a cumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
8) RTC Encapsulated DIP Modules (EDIP) can be successfully processed through conventional wave-soldering techniques as long as temperatures as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post-solder cleaning with water-washing techniques is acceptable, provided that ultrasonic vibration is not used. See the PowerCap package drawing for details regarding the PowerCap package.

PACKAGE INFORMATION

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 EDIP (740)	MDF28+2	21-0245	—
34 PWRCP	PC1+2	21-0246	—

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
9/13	Updated the *Ordering Information* table; updated the *Setting the Clock* section added the parameter t_{CE2A} for 3.3V read operation in the *AC Characteristics—Read Cycle (3.3V)* table	3, 4, 11

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