THE DATASHEET OF

DAC7311IDCKTG4

DACx311 2-V to 5.5-V, 80-µA, 8-, 10-, and 12-Bit, Low-Power, Single-Channel, Digital-to-Analog Converters in SC70 Package

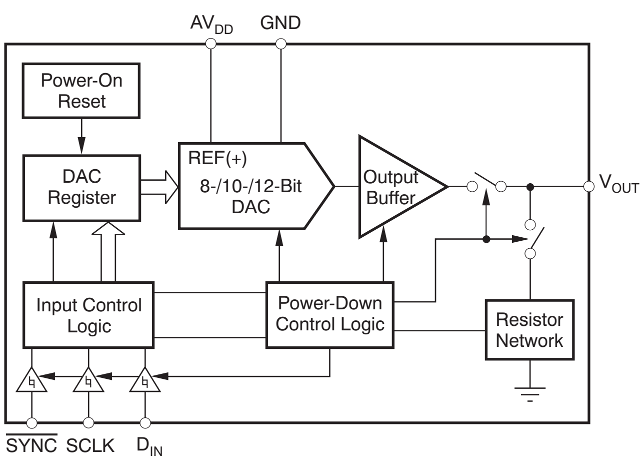
1 Features

- Relative Accuracy:
  - 0.25 LSB INL (DAC5311: 8-Bit)
  - 0.5 LSB INL (DAC6311: 10-Bit)
  - 1 LSB INL (DAC7311: 12-Bit)
- *micro*Power Operation: 80 µA at 2.0 V
- Power-Down: 0.5 µA at 5 V, 0.1 µA at 2.0 V
- Wide Power Supply: 2.0 V to 5.5 V
- Power-On Reset to Zero Scale
- Straight Binary Data Format
- Low Power Serial Interface With Schmitt-Triggered Inputs: up to 50 MHz
- On-Chip Output Buffer Amplifier, Rail-to-Rail Operation
- $\overline{\text{SYNC}}$ Interrupt Facility
- Extended Temperature Range –40°C to +125°C
- Pin-Compatible Family in a Tiny, 6-Pin SC70 Package

2 Applications

- Portable, Battery-Powered instruments
- Process Controls
- Digital Gain and Offset Adjustment
- Programmable Voltage and Current Sources

Simplified Schematic



3 Description

The DAC5311 (8-bit), DAC6311 (10-bit), and DAC7311 (12-bit) devices are low-power, single-channel, voltage output digital-to-analog converters (DACs). The low power consumption of these devices in normal operation (0.55 mW at 5 V, reducing to 2.5 µW in power-down mode) makes it ideally suited for portable, battery-operated applications.

These devices are monotonic by design, provide excellent linearity, and minimize undesired code-to-code transient voltages while offering an easy upgrade path within a pin-compatible family. All devices use a versatile, three-wire serial interface that operates at clock rates of up to 50 MHz and is compatible with standard SPI™, QSPI™, Microwire, and digital signal processor (DSP) interfaces.

All devices use an external power supply as a reference voltage to set the output range. The devices incorporate a power-on reset (POR) circuit that ensures the DAC output powers up at 0 V and remains there until a valid write to the device occurs. The DAC5311, DAC6311, and DAC7311 contain a power-down feature, accessed over the serial interface, that reduces current consumption of the device to 0.1 µA at 2.0 V in power-down mode.

These devices are pin-compatible with the DAC8311 and DAC8411, offering an easy upgrade path from 8-, 10-, and 12-bit resolution to 14- and 16-bit. All devices are available in a small, 6-pin, SC70 (SOT) package. This package offers a flexible, pin- and function-compatible, drop-in solution within the family over an extended temperature range of –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DACx311	SC70 (6)	2.00 mm × 1.25 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Device Comparison ... 3
6 Pin Configuration and Functions ... 3
7 Specifications ... 4
7.1 Absolute Maximum Ratings ... 4
7.2 ESD Ratings ... 4
7.3 Recommended Operating Conditions ... 4
7.4 Thermal Information ... 4
7.5 Electrical Characteristics ... 5
7.6 Timing Requirements ... 7
7.7 Typical Characteristics ... 8
8 Detailed Description ... 22
8.1 Overview ... 22
8.2 Functional Block Diagram ... 22
8.3 Feature Description ... 22
8.4 Device Functional Modes ... 24
8.5 Programming ... 25
9 Application and Implementation ... 26
9.1 Application Information ... 26
9.2 Typical Applications ... 27
10 Power Supply Recommendations ... 30
11 Layout ... 31
11.1 Layout Guidelines ... 31
11.2 Layout Example ... 31
12 Device and Documentation Support ... 32
12.1 Related Links ... 32
12.2 Community Resources ... 32
12.3 Trademarks ... 32
12.4 Electrostatic Discharge Caution ... 32
12.5 Glossary ... 32
13 Mechanical, Packaging, and Orderable Information ... 32

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2013) to Revision C — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added *Device Comparison* section and moved existing tables to this new section ... 3
- Moved *Operating Temperature* parameter from *Electrical Characteristics* table to *Recommended Operating Conditions* table ... 4
- Deleted *Parameter Definitions* section; definitions moved to new *Glossary* section ... 32

Changes from Revision A (August 2011) to Revision B — **Page**

- Changed all 1.8 V to 2.0 V throughout data sheet ... 1
- Deleted the 1.8-V Typical Characteristics section ... 8
- Changed X-axis for Figure 36 ... 12
- Changed X-axis for Figure 37 ... 12

Changes from Original (August, 2008) to Revision A — **Page**

- Changed specifications and test conditions for input low voltage parameter ... 6
- Changed specifications and test conditions for input high voltage parameter ... 6

5 Device Comparison

Table 1. Related Devices

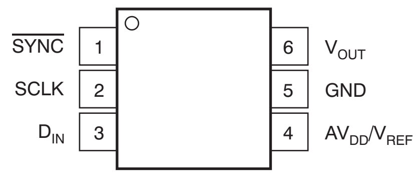
RELATED DEVICES	16-BIT	14-BIT	12-BIT	10-BIT	8-BIT
Pin and Function Compatible	DAC8411	DAC8311	DAC7311	DAC6311	DAC5311

Table 2. Relative Accuracy and Differential Nonlinearity

DEVICE	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM DIFFERENTIAL NONLINEARITY (LSB)
DAC5311	±0.25	±0.25
DAC6311	±0.5	±0.5
DAC7311	±1	±1

6 Pin Configuration and Functions

DCK Package
6-Pin SC70
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AV_{DD}/V_{REF}	4	I	Power supply input, +2.0 V to +5.5 V.
D_{IN}	3	I	Serial Data Input. Data are clocked into the 16-bit input shift register on the falling edge of the serial clock input.
GND	5	—	Ground reference point for all circuitry on the part.
SCLK	2	I	Serial clock input. Data are transferred at rates up to 50MHz.
SYNC	1	I	Level-triggered control input (active low). This is the frame sychronization signal for the input data. When SYNC goes low, it enables the input shift register and data are transferred in on the falling edges of the following clocks. The DAC is updated following 16th clock cycle, unless SYNC is taken high before this edge, in which case the rising edge of SYNC acts as an interrupt and the write sequence is ignored by the DACx311. See the *SYNC Interrupt* section for more details.
V_{OUT}	6	O	Analog output voltage from DAC. The output amplifier has rail-to-rail operation.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	AV_{DD} to GND	–0.3	+6	V
	Digital input voltage to GND	–0.3	$+AV_{DD}$ + 0.3	V
	V_{OUT} to GND	–0.3	$+AV_{DD}$ + 0.3	V
Temperature	Junction, T_J max		150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Operating temperature	–40		125	°C
AV_{DD}	Supply voltage	2		5.5	V

7.4 Thermal Information

THERMAL METRIC (1)		DACx311 DCK (SC70) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	216.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

at AV_{DD} = 2.0 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, and T_A = –40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE[1]						
DAC5311	Resolution		8			Bits
DAC6311	Resolution		10			Bits
DAC7311	Resolution		12			Bits
DAC5311	Relative accuracy	Measured by the line passing through codes 3 and 252		±0.01	±0.25	LSB
DAC6311	Relative accuracy	Measured by the line passing through codes 12 and 1012		±0.06	±0.5	LSB
DAC7311	Relative accuracy	Measured by the line passing through codes 30 and 4050		±0.3	±1	LSB
DAC5311	Differential nonlinearity			±0.01	±0.25	LSB
DAC6311	Differential nonlinearity			±0.03	±0.5	LSB
DAC7311	Differential nonlinearity			±0.2	±1	LSB
Offset error		Measured by the line passing through two codes[2]		±0.05	±4	mV
Offset error drift				3		μV/°C
Zero code error		All zeros loaded to the DAC register		0.2		mV
Full-scale error		All ones loaded to DAC register		0.04	0.2	% of FSR
Gain error				0.05	±0.15	% of FSR
Gain temperature coefficient		AV_{DD} = 5 V		±0.5		ppm of FSR/°C
		AV_{DD} = 2.0 V		±1.5		
OUTPUT CHARACTERISTICS						
Output voltage range			0		AV_{DD}	V
Output voltage settling time[3]		R_L = 2 kΩ, C_L = 200 pF, AV_{DD} = 5 V, 1/4 scale to 3/4 scale		6	10	μs
		R_L = 2 MΩ, C_L = 470 pF		12		μs
Slew rate				0.7		V/μs
Capacitive load stability		R_L = ∞		470		pF
		R_L = 2 kΩ		1000		pF
Code change glitch impulse		1 LSB change around major carry		0.5		nV-s
Digital feedthrough				0.5		nV-s
Power-on glitch impulse		R_L = 2 kΩ, C_L = 200 pF, AV_{DD} = 5 V		17		mV
DC output impedance				0.5		Ω
Short circuit current		AV_{DD} = 5 V		50		mA
		AV_{DD} = 3 V		20		mA
Power-up time		Coming out of power-down mode		50		μs

(1) Linearity calculated using a reduced code range of 3 to 252 for 8-bit, 12 to 1012 for 10bit, and 30 to 4050 for 12-bit, output unloaded.
(2) Straight line passing through codes 3 and 252 for 8-bit, 12 and 1012 for 10-bit, and 30 and 4050 for 12-bit, output unloaded.
(3) Specified by design and characterization, not production tested.

Electrical Characteristics (continued)

at AV_{DD} = 2.0 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, and T_A = –40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SNR		T_A = +25°C, BW = 20 kHz, 12-bit level, AV_{DD} = 5 V, f_{OUT} = 1 kHz, 1st 19 harmonics removed for SNR calculation			81		dB
THD					–65		dB
SFDR					65		dB
SINAD					65		dB
DAC output noise density(4)		T_A = +25°C, at zero-scale input, f_{OUT} = 1 kHz, AV_{DD} = 5 V			17		nV/√Hz
		T_A = +25°C, at mid-code input, f_{OUT} = 1 kHz, AV_{DD} = 5 V			110		nV/√Hz
DAC output noise(5)		T_A = +25°C, at mid-code input, 0.1 Hz to 10 Hz, AV_{DD} = 5 V			3		μV_{PP}
LOGIC INPUTS(6)							
Input current						±1	μA
$V_{IN}L$, Input low voltage		AV_{DD} = 2.7 V to 5.5 V				0.3 × AV_{DD}	V
		AV_{DD} = 2.0 V to 2.7 V				0.1 × AV_{DD}	V
$V_{IN}H$, Input high voltage		AV_{DD} = 2.7 V to 5.5 V		0.7 × AV_{DD}			V
		AV_{DD} = 2.0 V to 2.7 V		0.9 × AV_{DD}			V
Pin capacitance					1.5	3	pF
POWER REQUIREMENTS							
AV_{DD}				2.0		5.5	V
I_{DD}	Normal mode	$V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND, at midscale code(7)	AV_{DD} = 3.6 V to 5.5 V		110	160	μA
			AV_{DD} = 2.7 V to 3.6 V		95	150	μA
			AV_{DD} = 2.0 V to 2.7 V		80	140	μA
	All power-down mode	$V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND, at midscale code(7)	AV_{DD} = 3.6 V to 5.5 V		0.5	3.5	μA
			AV_{DD} = 2.7 V to 3.6 V		0.4	3	μA
			AV_{DD} = 2.0 V to 2.7 V		0.1	2	μA
Power dissipation	Normal mode	$V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND, at midscale code(7)	AV_{DD} = 3.6 V to 5.5 V		0.55	0.88	mW
			AV_{DD} = 2.7 V to 3.6 V		0.25	0.54	mW
			AV_{DD} = 2.0 V to 2.7 V		0.14	0.38	mW
	All power-down mode	$V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND, at midscale code(7)	AV_{DD} = 3.6 V to 5.5 V		2.50	19.2	μW
			AV_{DD} = 2.7 V to 3.6 V		1.08	10.8	μW
			AV_{DD} = 2.0 V to 2.7 V		0.72	8.1	μW

(4) For more details, see Figure 23.
(5) For more details, see Figure 24.
(6) Specified by design and characterization, not production tested.
(7) For more details, see Figure 16 and Figure 58.

7.6 Timing Requirements

at –40°C to 125°C, and AV_{DD} = 2 V to 5.5 V (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
$f_{(SCLK)}$	Serial clock frequency	AV_{DD} = 2.0 V to 3.6 V			20	MHz
		AV_{DD} = 3.6 V to 5.5 V			50	
t_1	SCLK cycle time	AV_{DD} = 2.0 V to 3.6 V	50			ns
		AV_{DD} = 3.6 V to 5.5 V	20			
t_2	SCLK high time	AV_{DD} = 2.0 V to 3.6 V	25			ns
		AV_{DD} = 3.6 V to 5.5 V	10			
t_3	SCLK low time	AV_{DD} = 2.0 V to 3.6 V	25			ns
		AV_{DD} = 3.6 V to 5.5 V	10			
t_4	$\overline{SYNC}$ to SCLK rising edge setup time	AV_{DD} = 2.0 V to 3.6 V	0			ns
		AV_{DD} = 3.6 V to 5.5 V	0			
t_5	Data setup time	AV_{DD} = 2.0 V to 3.6 V	5			ns
		AV_{DD} = 3.6 V to 5.5 V	5			
t_6	Data hold time	AV_{DD} = 2.0 V to 3.6 V	4.5			ns
		AV_{DD} = 3.6 V to 5.5 V	4.5			
t_7	SCLK falling edge to $\overline{SYNC}$ rising edge	AV_{DD} = 2.0 V to 3.6 V	0			ns
		AV_{DD} = 3.6 V to 5.5 V	0			
t_8	Minimum $\overline{SYNC}$ high time	AV_{DD} = 2.0 V to 3.6 V	50			ns
		AV_{DD} = 3.6 V to 5.5 V	20			
t_9	16th SCLK falling edge to $\overline{SYNC}$ falling edge	AV_{DD} = 2.0 V to 3.6 V	100			ns
		AV_{DD} = 3.6 V to 5.5 V	100			
t_{10}	$\overline{SYNC}$ rising edge to 16th SCLK falling edge (for successful $\overline{SYNC}$ interrupt)	AV_{DD} = 2.0 V to 3.6 V	15			ns
		AV_{DD} = 3.6 V to 5.5 V	15			

(1) All input signals are specified with $t_R = t_F$ = 3 ns (10% to 90% of AV_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH}) / 2$.

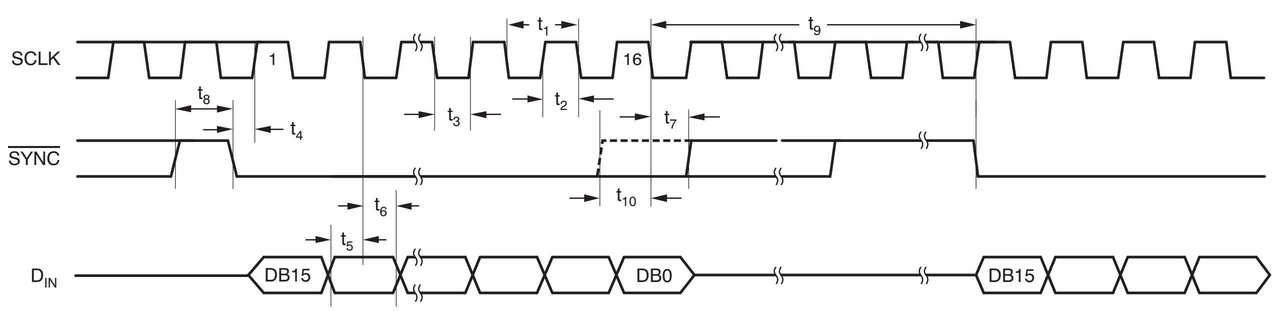


Figure 1. Serial Write Operation

7.7 Typical Characteristics

7.7.1 Typical Characteristics: AV_{DD} = 5 V

at T_A = 25°C, AV_{DD} = 5 V, and DAC loaded with midscale code (unless otherwise noted)

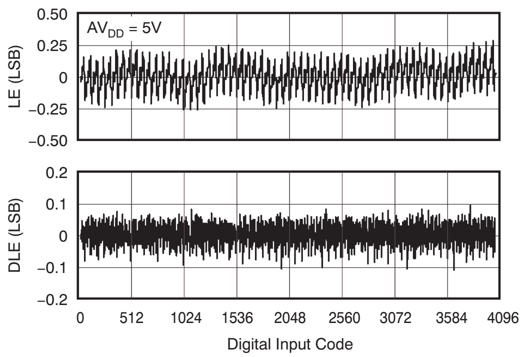


Figure 2. DAC7311 12-Bit Linearity Error and Differential Linearity Error vs Code (–40°C)

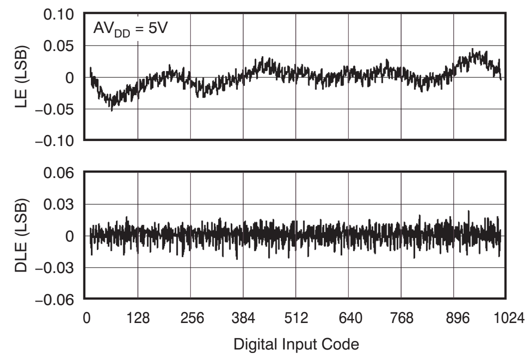


Figure 3. DAC6311 10-Bit Linearity Error and Differential Linearity Error vs Code (–40°C)

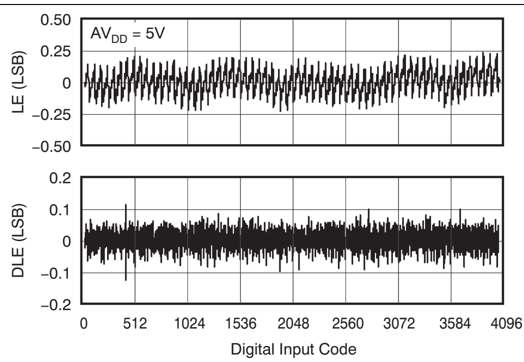


Figure 4. DAC7311 12-Bit Linearity Error and Differential Linearity Error vs Code (25°C)

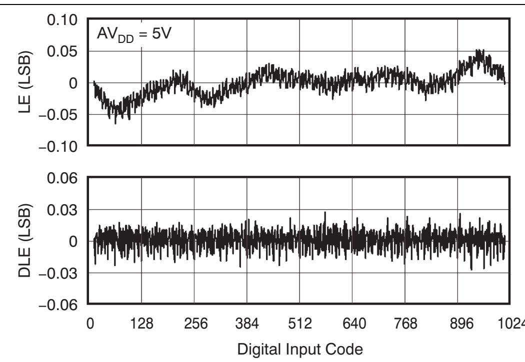


Figure 5. DAC6311 10-Bit Linearity Error and Differential Linearity Error vs Code (25°C)

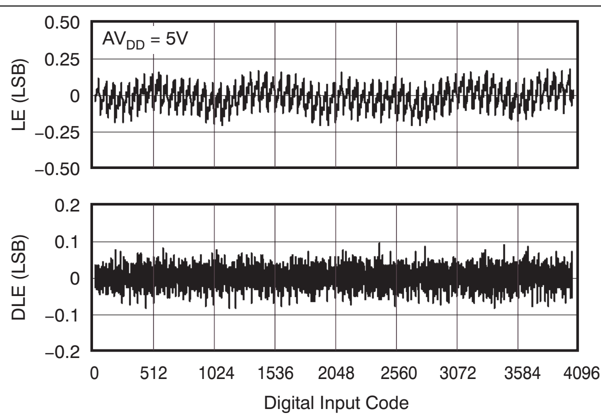


Figure 6. DAC7311 12-Bit Linearity Error and Differential Linearity Error vs Code (125°C)

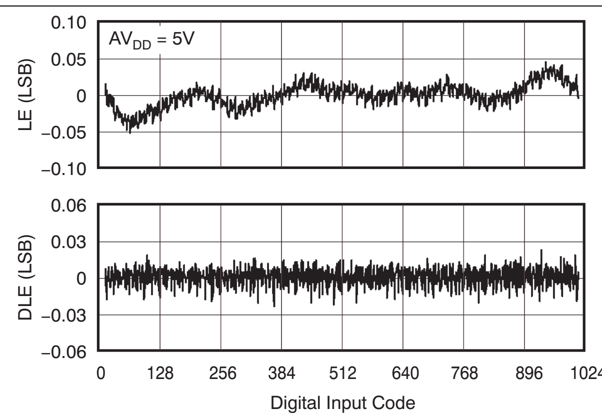


Figure 7. DAC6311 10-Bit Linearity Error and Differential Linearity Error vs Code (125°C)

Typical Characteristics: AV_{DD} = 5 V (continued)

at T_A = 25°C, AV_{DD} = 5 V, and DAC loaded with midscale code (unless otherwise noted)

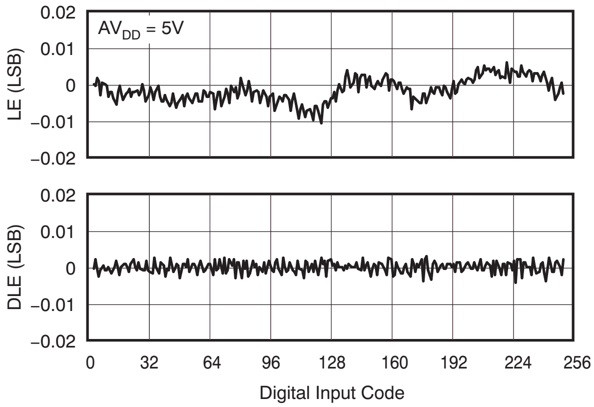


Figure 8. DAC5311 8-Bit Linearity Error and Differential Linearity Error vs Code (–40°C)

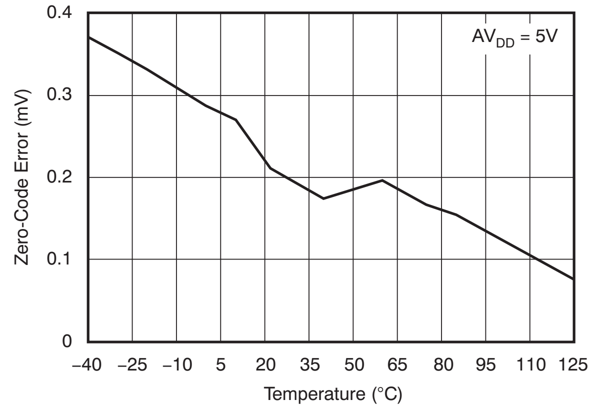


Figure 9. Zero-Code Error vs Temperature

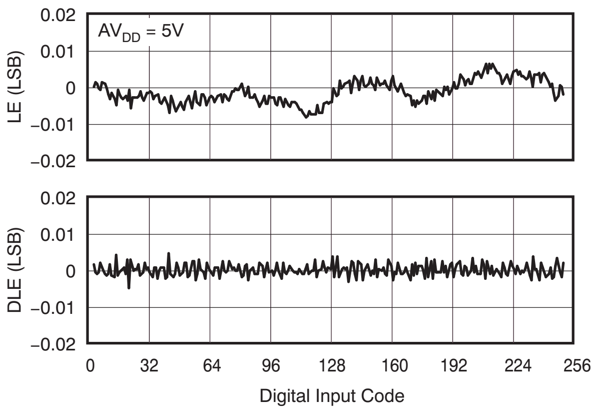


Figure 10. DAC5311 8-Bit Linearity Error and Differential Linearity Error vs Code (25°C)

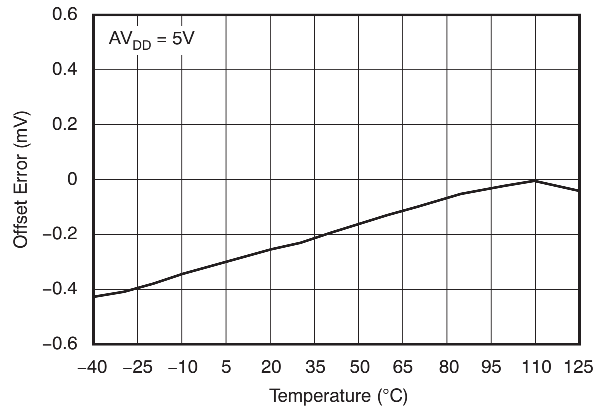


Figure 11. Offset Error vs Temperature

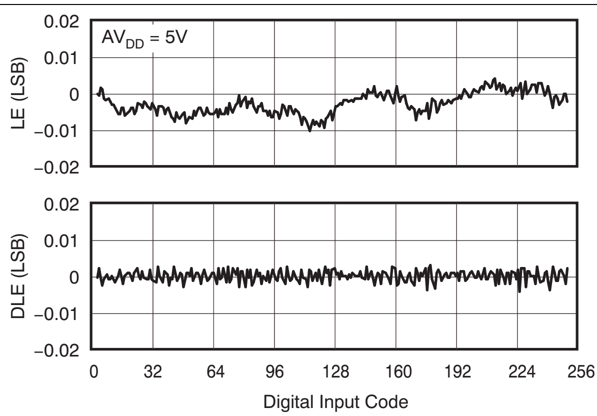


Figure 12. DAC5311 8-Bit Linearity Error and Differential Linearity Error vs Code (125°C)

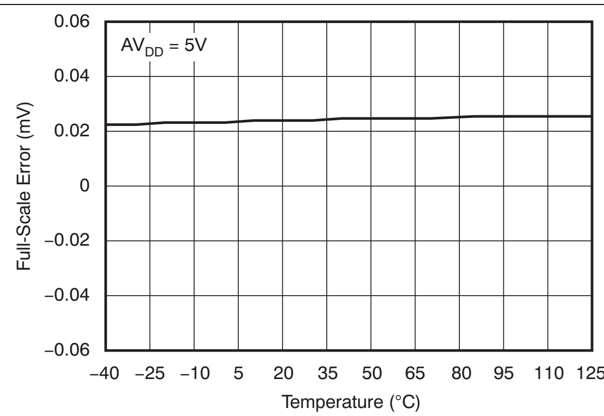


Figure 13. Full-Scale Error vs Temperature

Typical Characteristics: AV_{DD} = 5 V (continued)

at T_A = 25°C, AV_{DD} = 5 V, and DAC loaded with midscale code (unless otherwise noted)

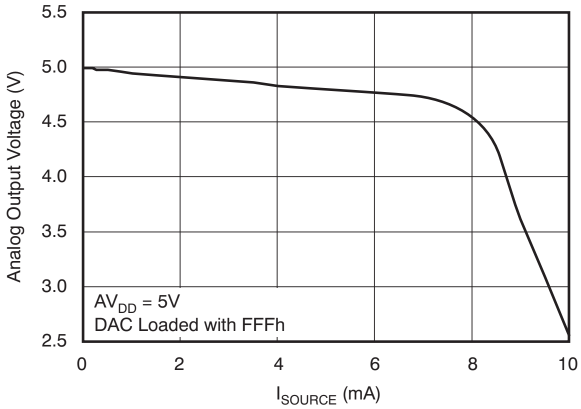


Figure 14. Source Current at Positive Rail

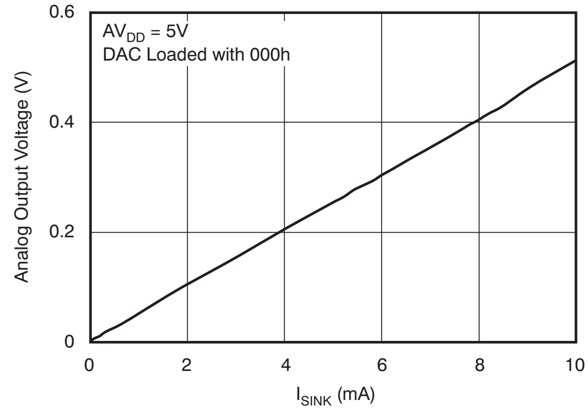


Figure 15. Sink Current at Negative Rail

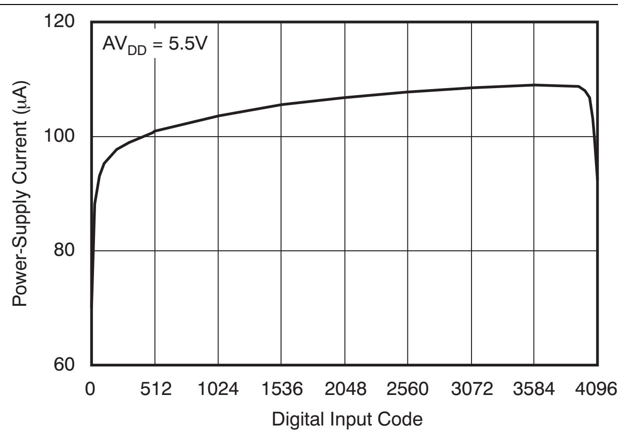


Figure 16. Power-Supply Current vs Digital Input Code

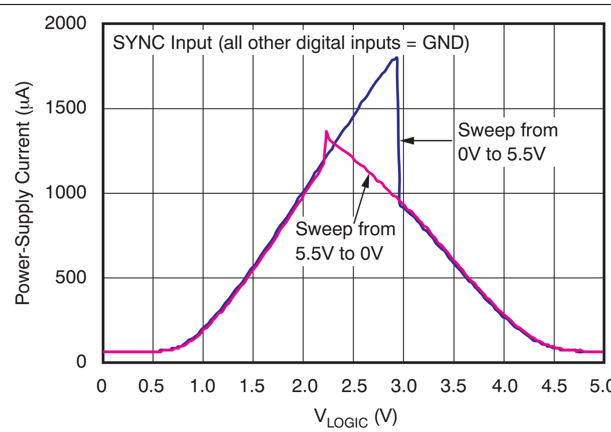


Figure 17. Power-Supply Current vs Logic Input Voltage

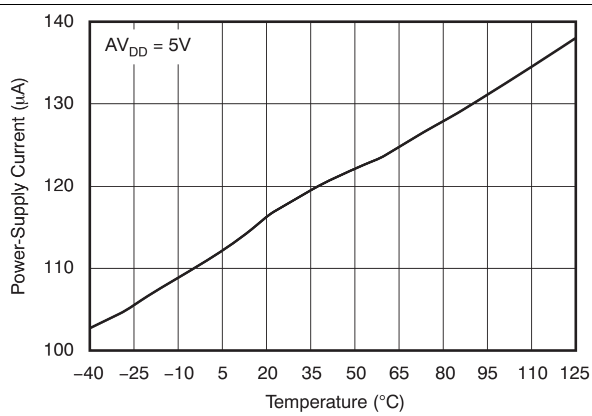


Figure 18. Power-Supply Current vs Temperature

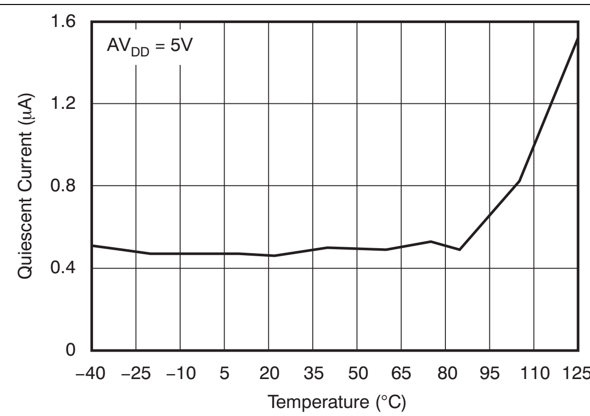


Figure 19. Power-Down Current vs Temperature

Typical Characteristics: AV_{DD} = 5 V (continued)

at T_A = 25°C, AV_{DD} = 5 V, and DAC loaded with midscale code (unless otherwise noted)

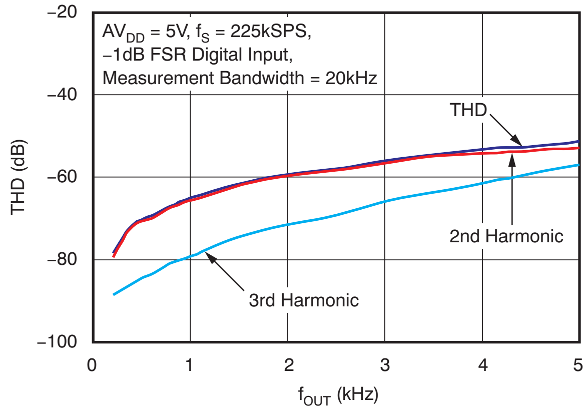


Figure 20. Total Harmonic Distortion vs Output Frequency

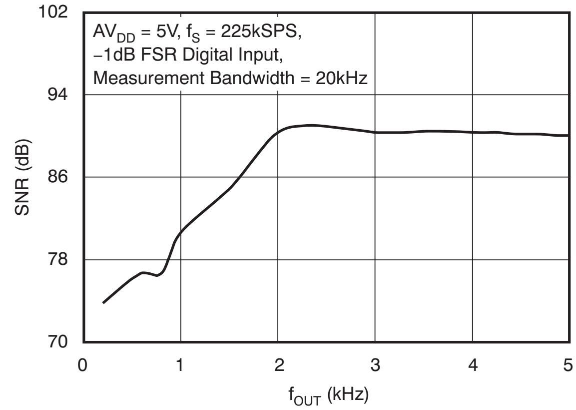


Figure 21. Signal-to-Noise Ratio vs Output Frequency

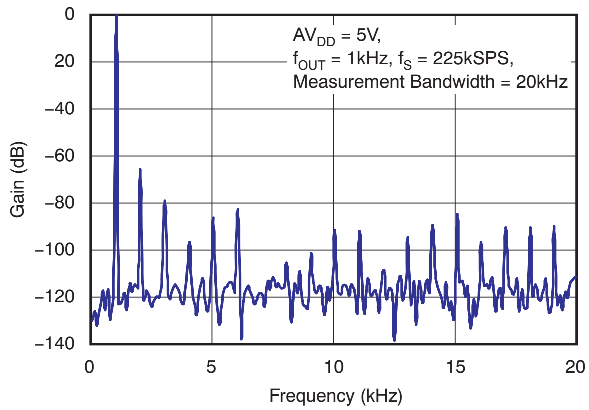


Figure 22. Power Spectral Density

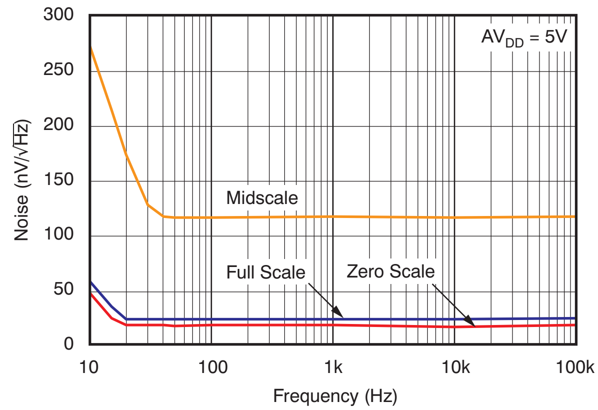


Figure 23. DAC Output Noise Density vs Frequency

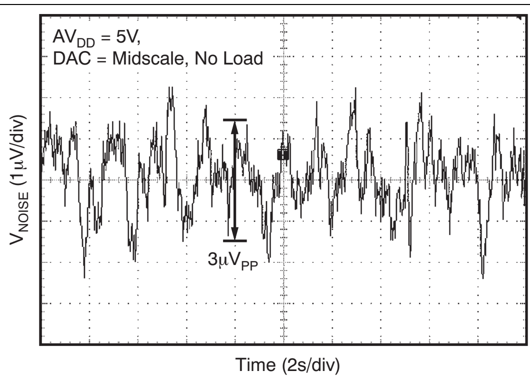


Figure 24. DAC Output Noise, 0.1-Hz to 10-Hz Bandwidth

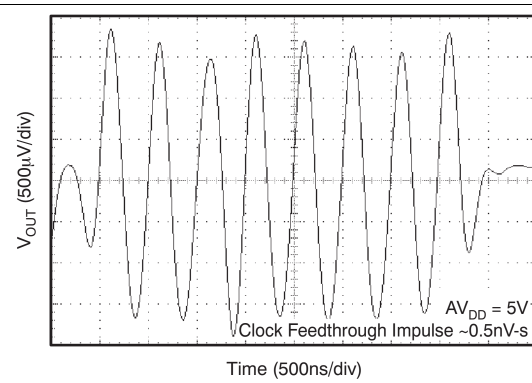


Figure 25. Clock Feedthrough, 5-V, 2-MHz, Midscale

Typical Characteristics: AV_{DD} = 5 V (continued)

at T_A = 25°C, AV_{DD} = 5 V, and DAC loaded with midscale code (unless otherwise noted)

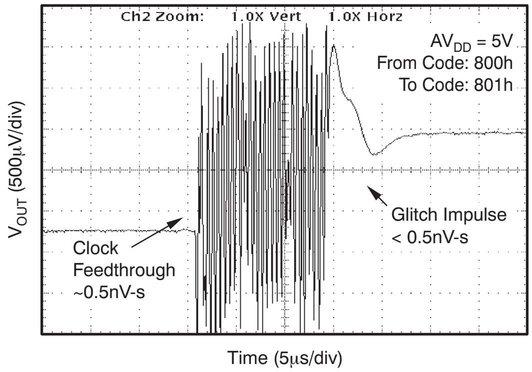


Figure 26. Glitch Energy, 5-V, 12-Bit, 1-LSB Step, Rising Edge

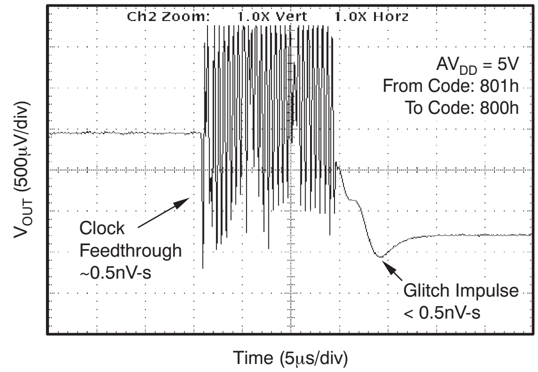


Figure 27. Glitch Energy, 5-V, 12-Bit, 1-LSB Step, Falling Edge

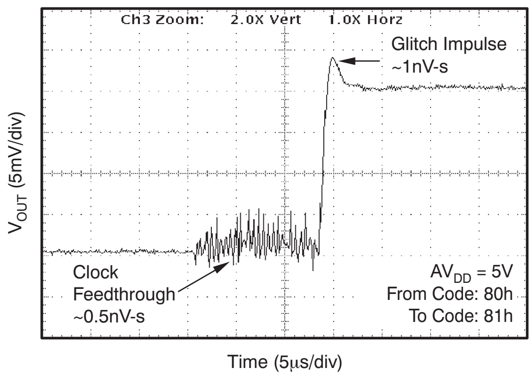


Figure 28. Glitch Energy, 5-V, 8-Bit, 1-LSB Step, Rising Edge

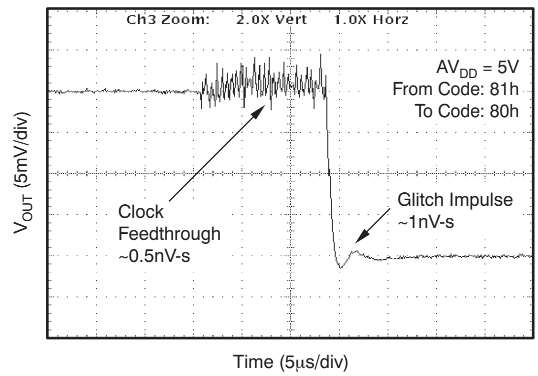


Figure 29. Glitch Energy, 5-V, 8-Bit, 1-LSB Step, Falling Edge

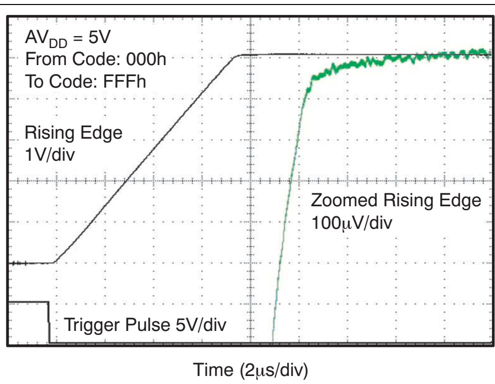


Figure 30. Full-Scale Settling Time, 5-V Rising Edge

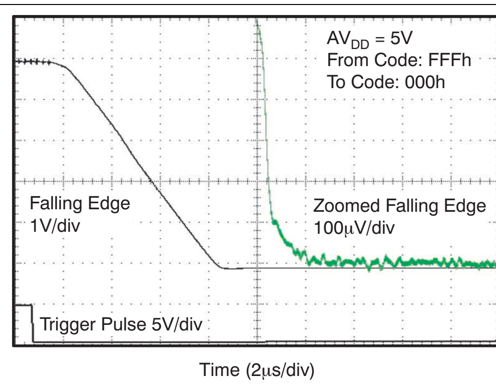


Figure 31. Full-Scale Settling Time, 5-V Falling Edge

Typical Characteristics: AV_{DD} = 5 V (continued)

at T_A = 25°C, AV_{DD} = 5 V, and DAC loaded with midscale code (unless otherwise noted)

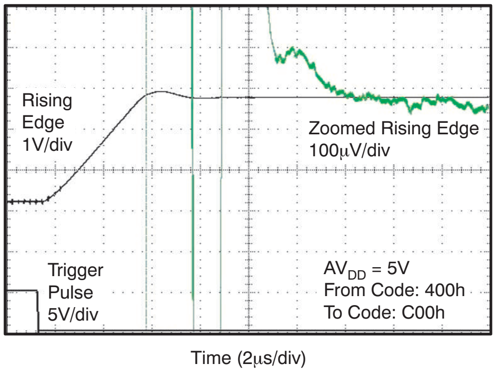


Figure 32. Half-Scale Settling Time, 5-V Rising Edge

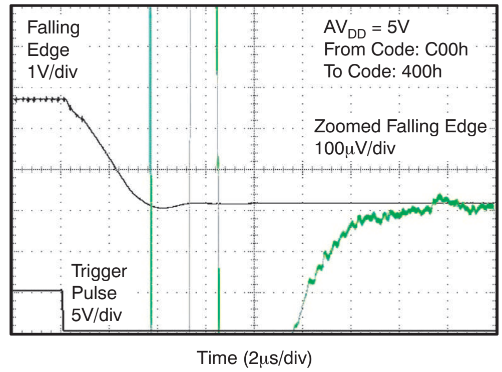


Figure 33. Half-Scale Settling Time 5-V Falling Edge

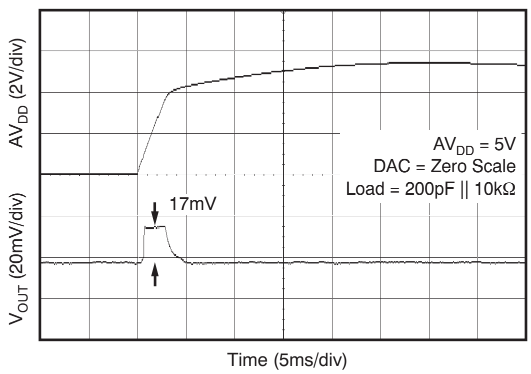


Figure 34. Power-On Reset to 0-V Power-On Glitch

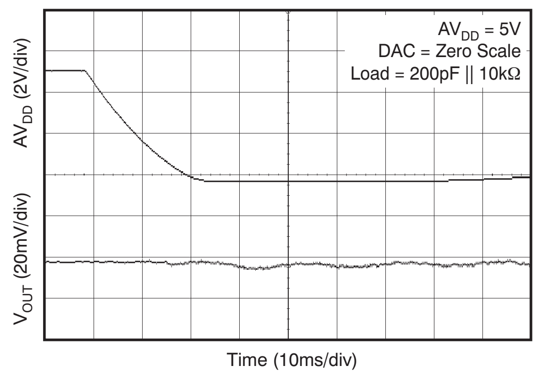


Figure 35. Power-Off Glitch

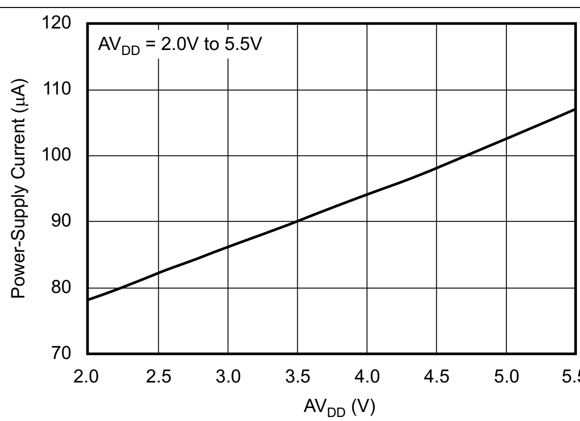


Figure 36. Power-Supply Current vs Power-Supply Voltage

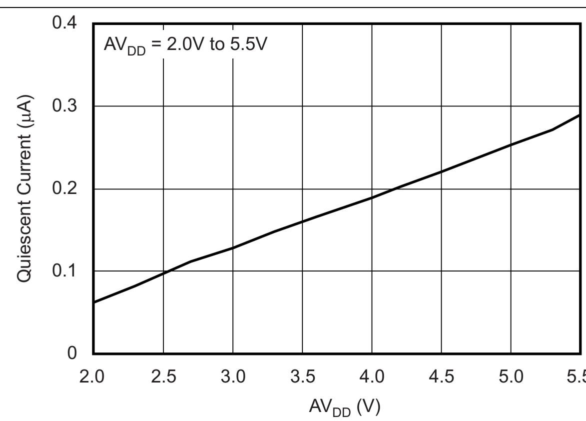


Figure 37. Power-Down Current vs Power-Supply Voltage

Typical Characteristics: AV_{DD} = 5 V (continued)

at T_A = 25°C, AV_{DD} = 5 V, and DAC loaded with midscale code (unless otherwise noted)

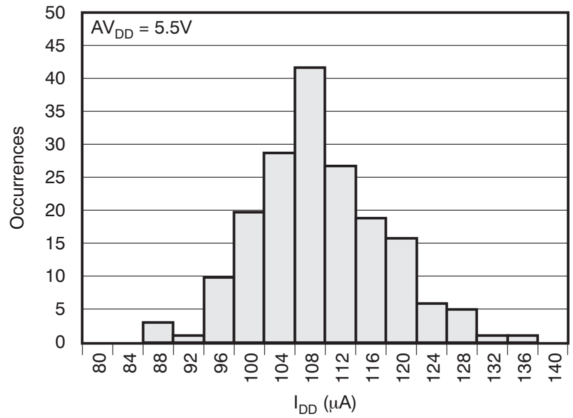


Figure 38. Power-Supply Current Histogram

7.7.2 Typical Characteristics: AV_{DD} = 3.6 V

at T_A = 25°C, AV_{DD} = 3.6 V, and DAC loaded with midscale code (unless otherwise noted)

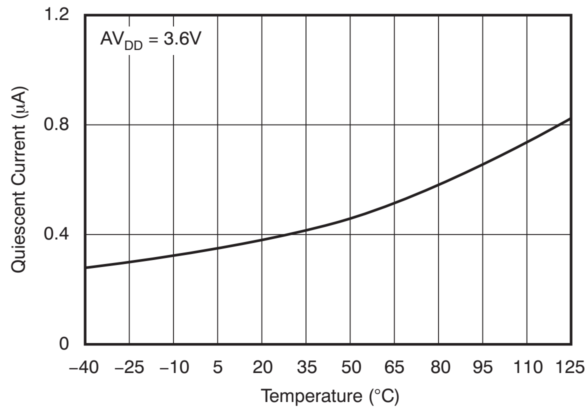


Figure 39. Power-Down Current vs Temperature

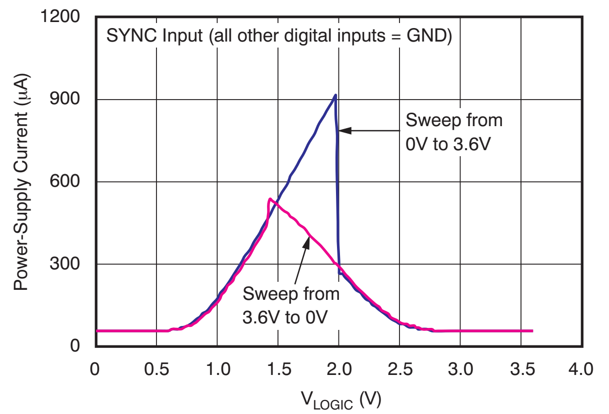


Figure 40. Power-Supply Current vs Logic Input Voltage

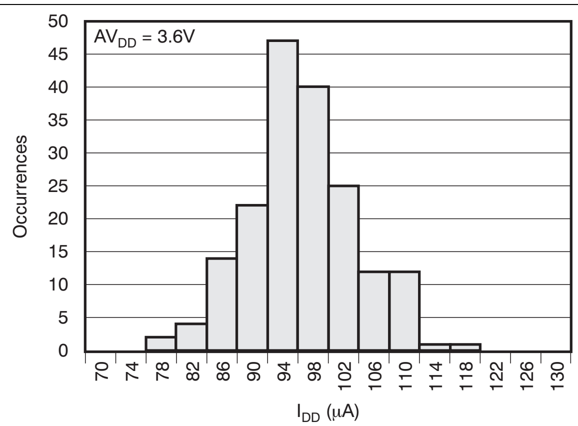


Figure 41. Power-Supply Current Histogram

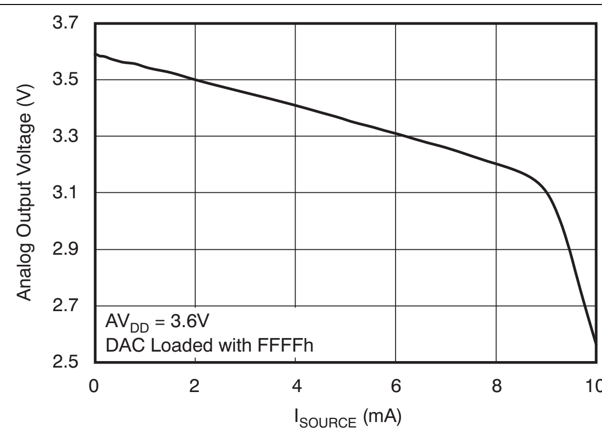


Figure 42. Source Current at Positive Rail

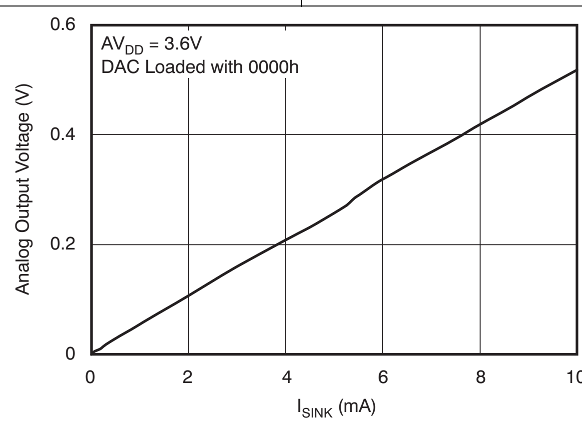


Figure 43. Sink Current at Negative Rail

7.7.3 Typical Characteristics: AV_{DD} = 2.7 V

at T_A = 25°C, AV_{DD} = 2.7 V, and DAC loaded with midscale code (unless otherwise noted)

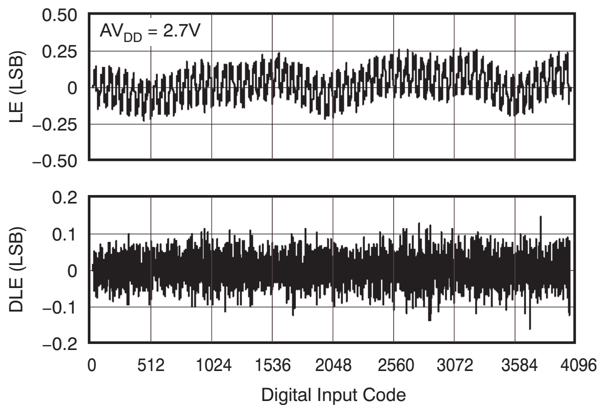


Figure 44. DAC7311 12-Bit Linearity Error and Differential Linearity Error vs Code (–40°C)

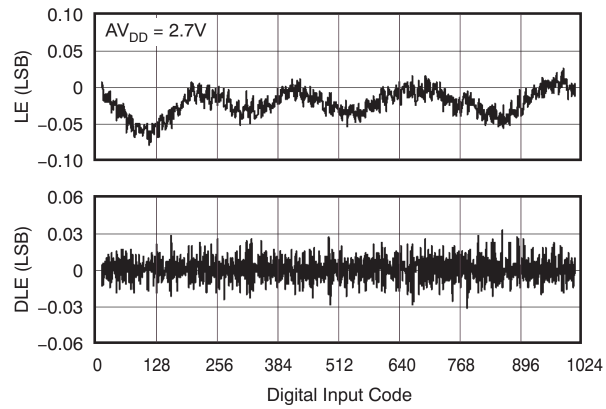


Figure 45. DAC6311 10-Bit Linearity Error and Differential Linearity Error vs Code (–40°C)

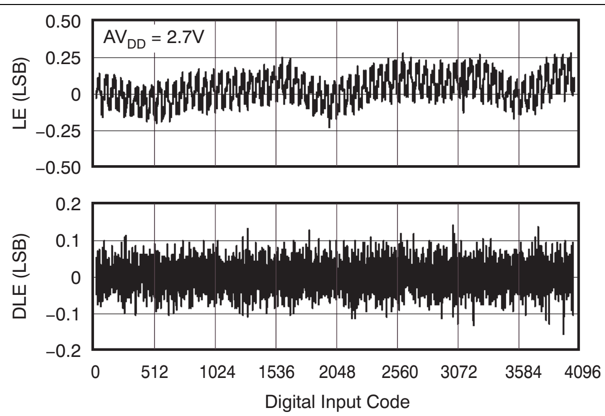


Figure 46. DAC7311 12-Bit Linearity Error and Differential Linearity Error vs Code (25°C)

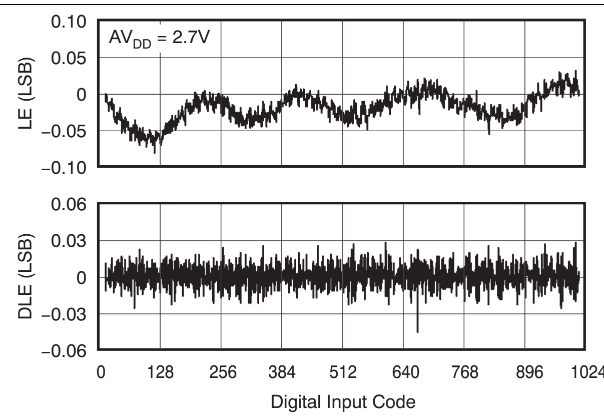


Figure 47. DAC6311 10-Bit Linearity Error and Differential Linearity Error vs Code (25°C)

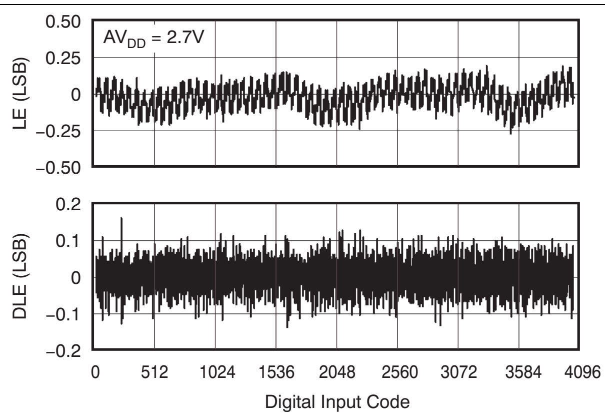


Figure 48. DAC7311 12-Bit Linearity Error and Differential Linearity Error vs Code (125°C)

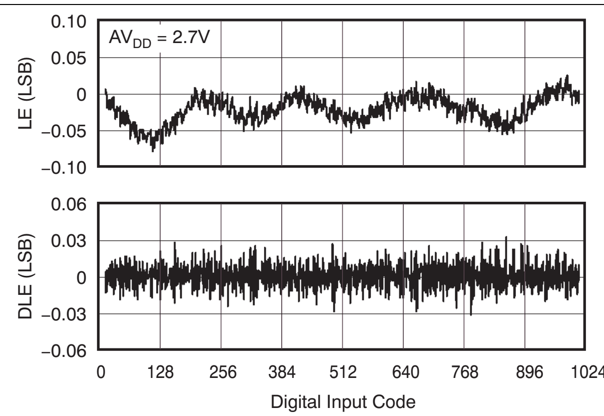


Figure 49. DAC6311 10-Bit Linearity Error and Differential Linearity Error vs Code (125°C)

Typical Characteristics: AV_{DD} = 2.7 V (continued)

at T_A = 25°C, AV_{DD} = 2.7 V, and DAC loaded with midscale code (unless otherwise noted)

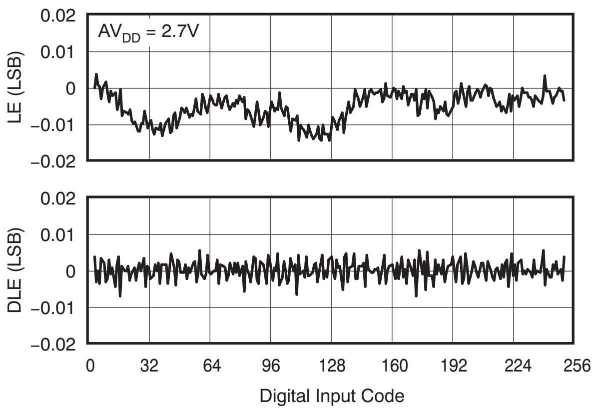


Figure 50. DAC5311 8-Bit Linearity Error and Differential Linearity Error vs Code (–40°C)

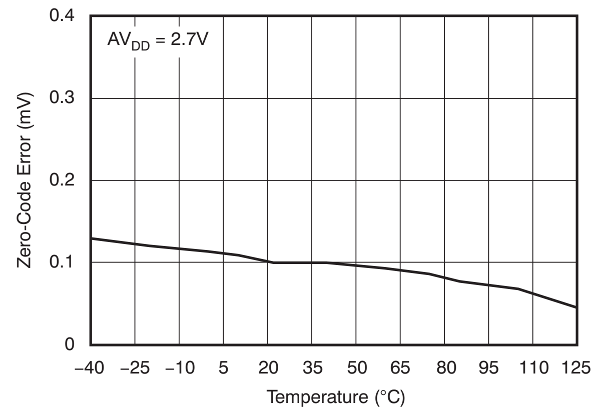


Figure 51. Zero-Code Error vs Temperature

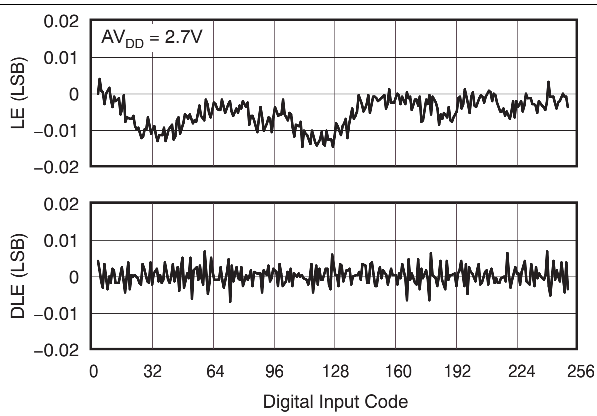


Figure 52. DAC5311 8-Bit Linearity Error and Differential Linearity Error vs Code (25°C)

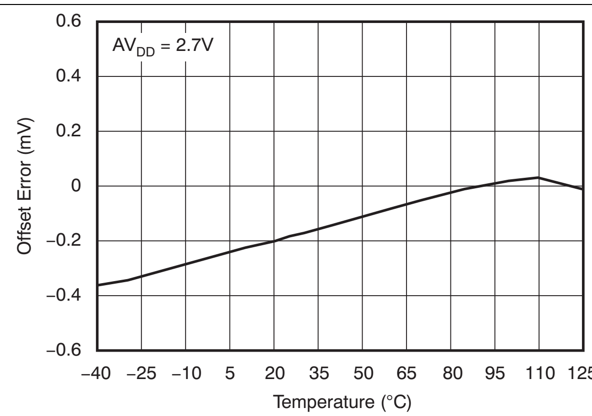


Figure 53. Offset Error vs Temperature

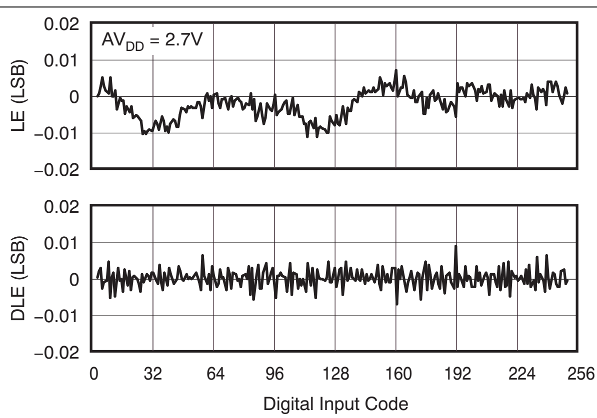


Figure 54. DAC5311 8-Bit Linearity Error and Differential Linearity Error vs Code (125°C)

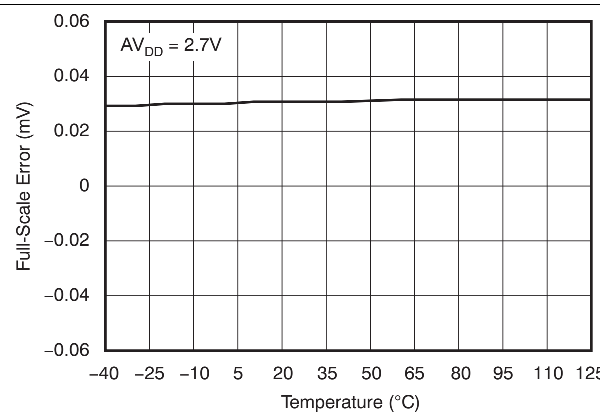


Figure 55. Full-Scale Error vs Temperature

Typical Characteristics: AV_{DD} = 2.7 V (continued)

at T_A = 25°C, AV_{DD} = 2.7 V, and DAC loaded with midscale code (unless otherwise noted)

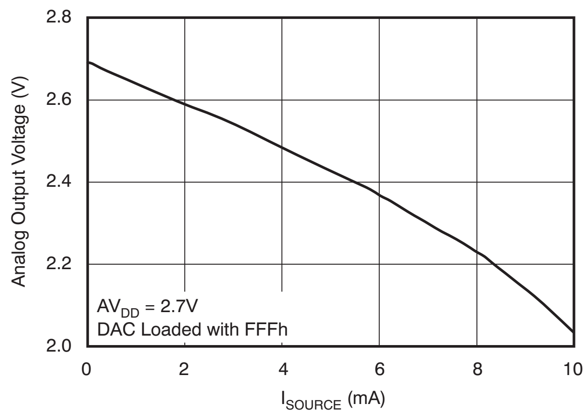


Figure 56. Source Current at Positive Rail

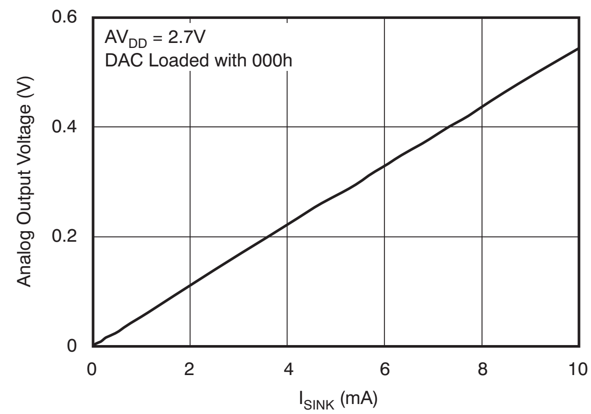


Figure 57. Sink Current at Negative Rail

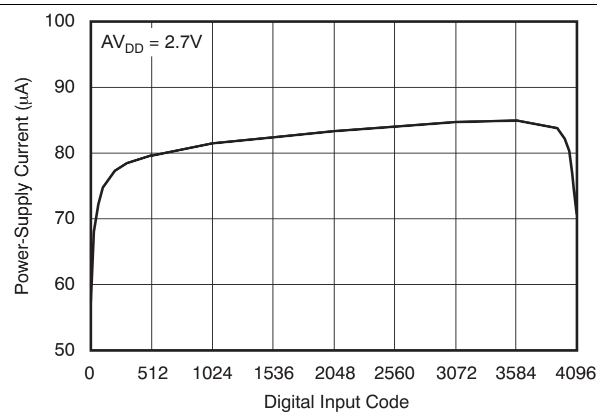


Figure 58. Power-Supply Current vs Digital Input Code

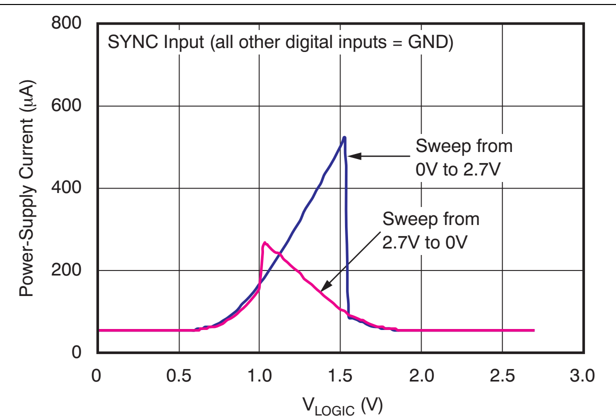


Figure 59. Power-Supply Current vs Logic Input Voltage

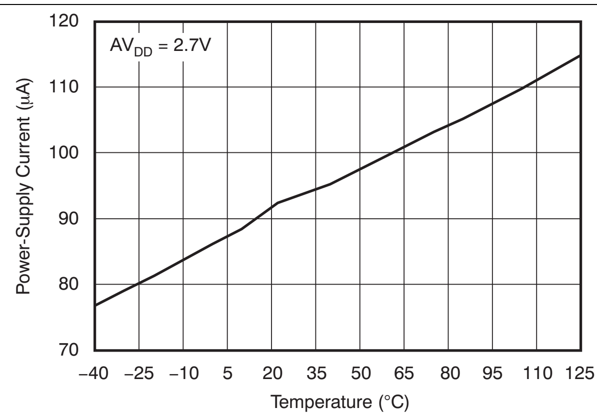


Figure 60. Power-Supply Current vs Temperature

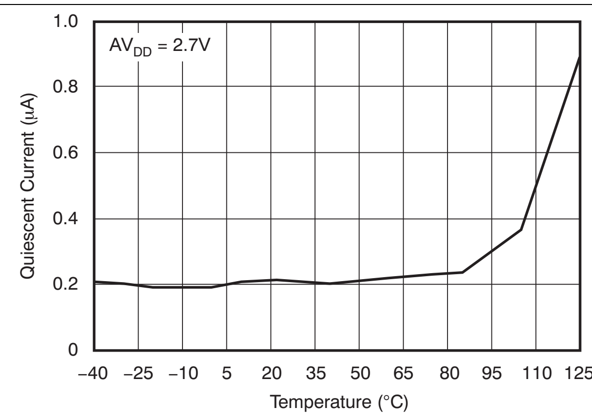


Figure 61. Power-Down Current vs Temperature

Typical Characteristics: AV_{DD} = 2.7 V (continued)

at T_A = 25°C, AV_{DD} = 2.7 V, and DAC loaded with midscale code (unless otherwise noted)

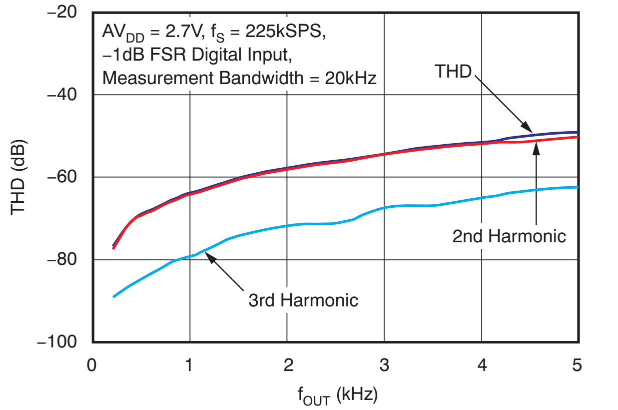


Figure 62. Total Harmonic Distortion vs Output Frequency

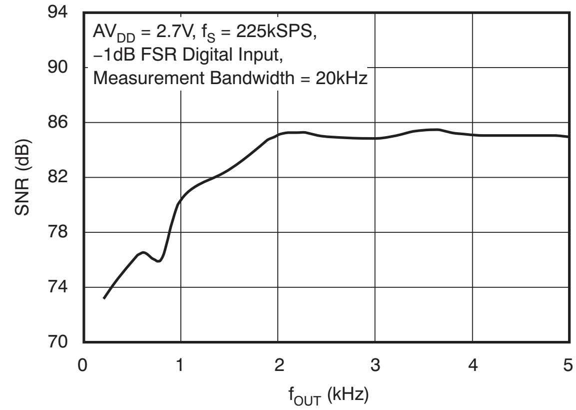


Figure 63. Signal-to-Noise Ratio vs Output Frequency

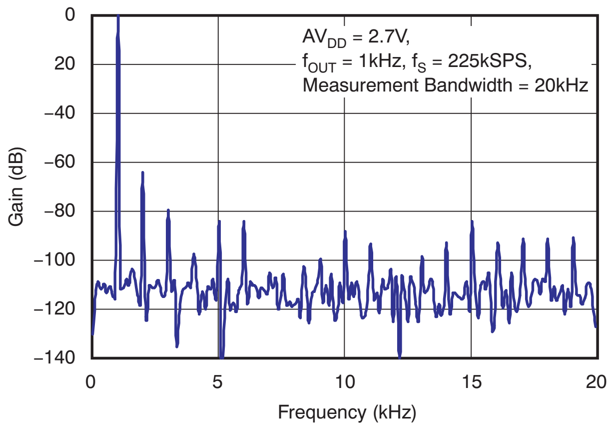


Figure 64. Power Spectral Density

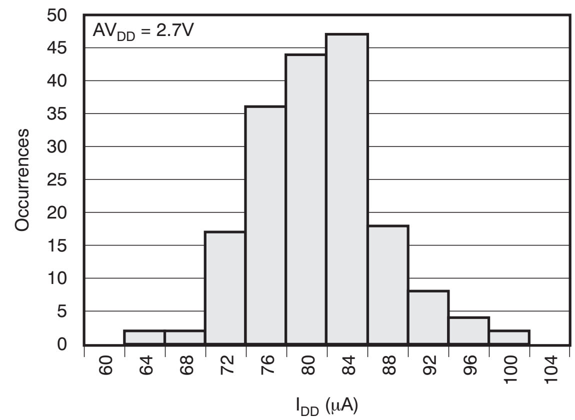


Figure 65. Power-Supply Current Histogram

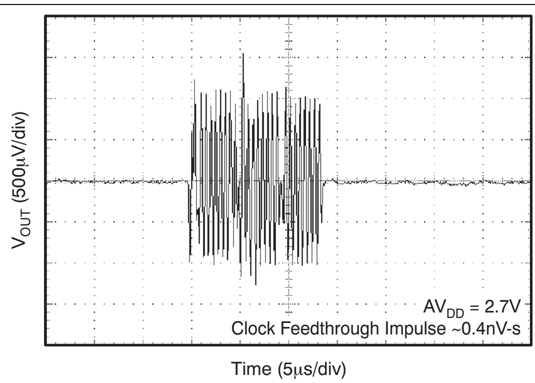


Figure 66. Clock Feedthrough 2.7-V, 20-MHz, Midscale

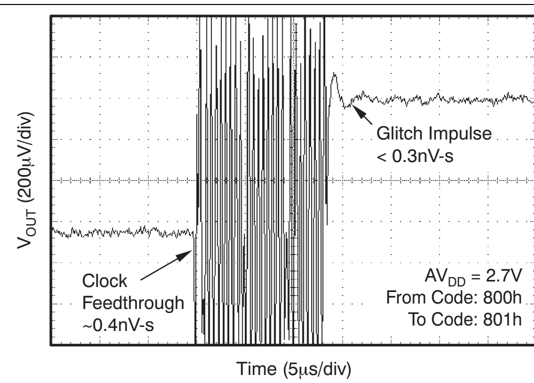


Figure 67. Glitch Energy, 2.7-V, 12-Bit, 1-LSB Step, Rising Edge

Typical Characteristics: AV_{DD} = 2.7 V (continued)

at T_A = 25°C, AV_{DD} = 2.7 V, and DAC loaded with midscale code (unless otherwise noted)

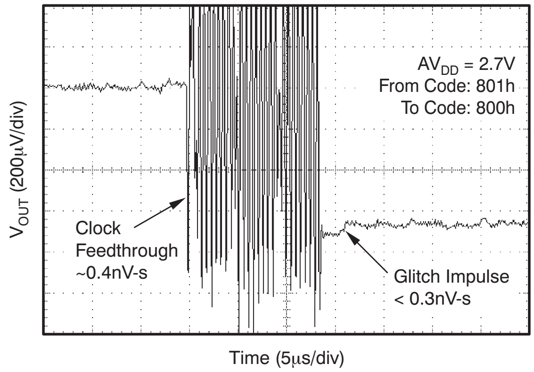


Figure 68. Glitch Energy, 2.7-V, 12-Bit, 1-LSB Step, Falling Edge

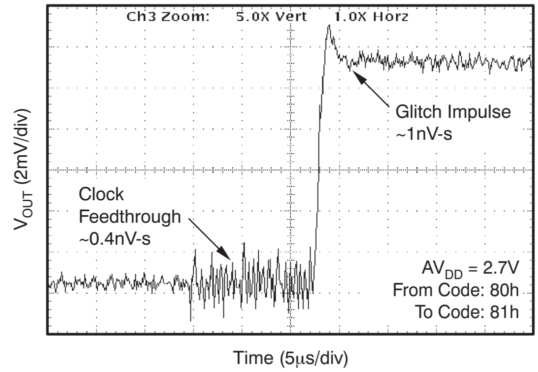


Figure 69. Glitch Energy, 2.7-V, 8-Bit, 1-LSB Step, Rising Edge

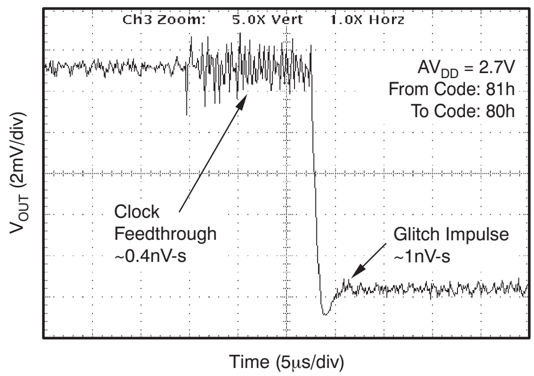


Figure 70. Glitch Energy, 2.7-V, 8-Bit, 1-LSB Step, Falling Edge

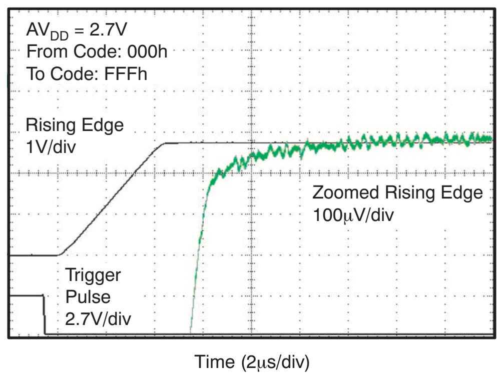


Figure 71. Full-Scale Settling Time, 2.7-V Rising Edge

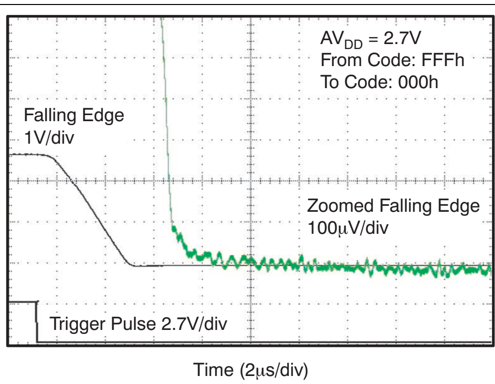


Figure 72. Full-Scale Settling Time, 2.7-V Falling Edge

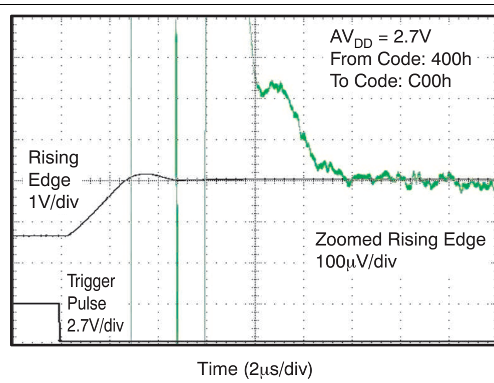


Figure 73. Half-Scale Settling Time, 2.7-V Rising Edge

Typical Characteristics: AV_{DD} = 2.7 V (continued)

at T_A = 25°C, AV_{DD} = 2.7 V, and DAC loaded with midscale code (unless otherwise noted)

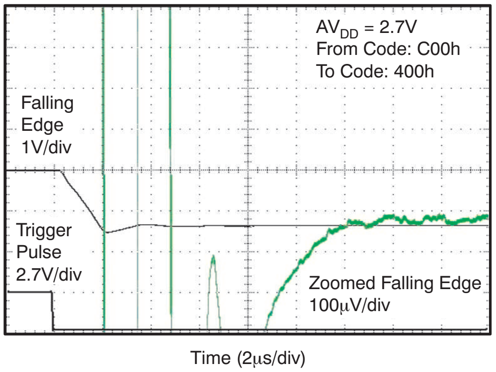


Figure 74. Half-Scale Settling Time, 2.7-V Falling Edge

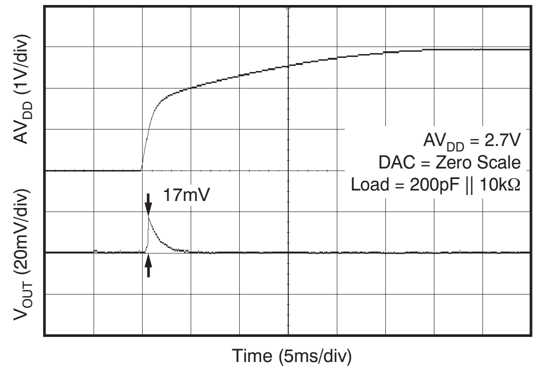


Figure 75. Power-On Reset to 0-V Power-On Glitch

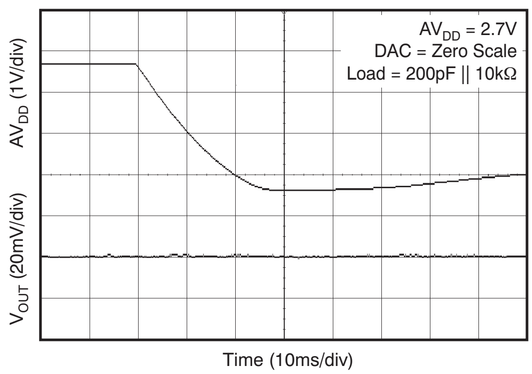


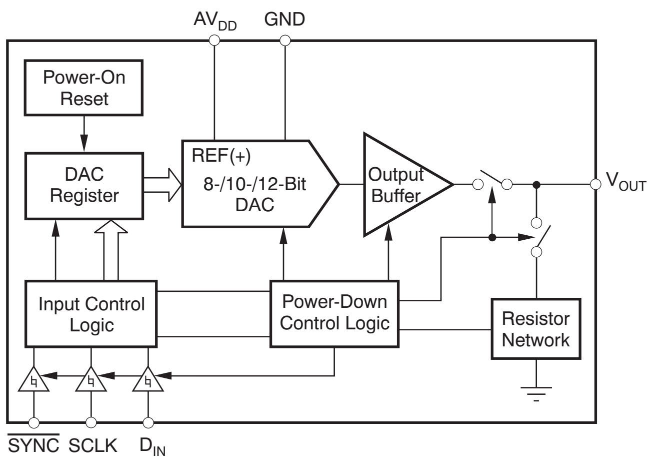
Figure 76. Power-Off Glitch

8 Detailed Description

8.1 Overview

The DAC5311 (8-bit), DAC6311 (10-bit), and DAC7311 (12-bit) are low-power, single-channel, voltage output DACs. These devices are monotonic by design, provide excellent linearity, and minimize undesired code-to-code transient voltages while offering an easy upgrade path within a pin-compatible family. All devices use a versatile, three-wire serial interface that operates at clock rates of up to 50 MHz and is compatible with standard SPI, QSPI, Microwire, and digital signal processor (DSP) interfaces.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DAC Section

The DAC5311, DAC6311, and DAC7311 are fabricated using Texas Instruments' proprietary HPA07 process technology. The architecture consists of a string DAC followed by an output buffer amplifier. Because there is no reference input pin, the power supply (AV_{DD}) acts as the reference. Figure 77 shows a block diagram of the DAC architecture.

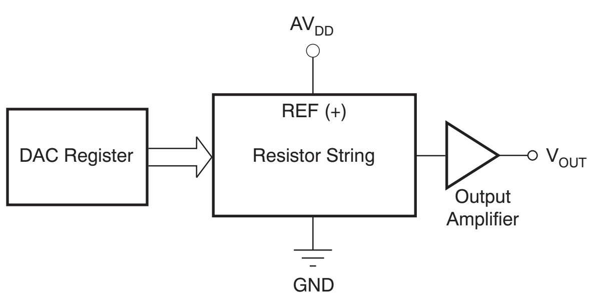


Figure 77. DACx311 Architecture

The input coding to the DACx311 is straight binary, so the ideal output voltage is given by:

$$V_{OUT} = AV_{DD} \times \frac{D}{2^n}$$

where

- n = resolution in bits; either 8 (DAC5311), 10 (DAC6311), or 12 (DAC7311).
- D = decimal equivalent of the binary code that is loaded to the DAC register. It ranges from 0 to 255 for 8-bit DAC5311; from 0 to 1023 for the 10-bit DAC6311; and 0 to 4095 for the 12-bit DAC7311. (1)

Feature Description (continued)

8.3.2 Resistor String

The resistor string section is shown in Figure 78. It is simply a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. The resistor string architecture is inherently monotonic.

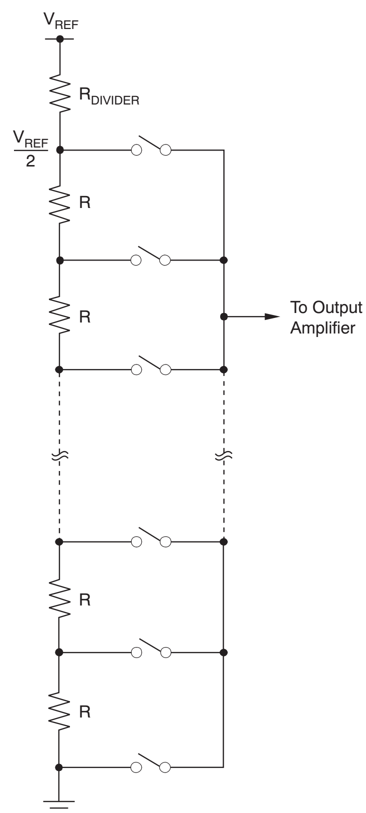


Figure 78. Resistor String

8.3.3 Output Amplifier

The output buffer amplifier is capable of generating rail-to-rail voltages on its output which gives an output range of 0 V to AV_{DD}. The output amplifier is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in the *Typical Characteristics* section for the given voltage input. The slew rate is 0.7 V/µs with a half-scale settling time of typically 6 µs with the output unloaded.

8.3.4 Power-On Reset

The DACx311 contains a power-on reset circuit that controls the output voltage during power up. On power up, the DAC register is filled with zeros and the output voltage is 0 V. The DAC register remains that way until a valid write sequence is made to the DAC. This design is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

The occurring power-on glitch impulse is only a few millivolts (typically, 17 mV; see Figure 34).

8.4 Device Functional Modes

8.4.1 Power-Down Modes

The DACx311 contains four separate modes of operation. These modes are programmable by setting two bits (PD1 and PD0) in the control register. Table 3 shows how the state of the bits corresponds to the mode of operation of the device.

Table 3. Modes of Operation for the DACx311

PD1	PD0	OPERATING MODE
NORMAL MODE		
0	0	Normal Operation
POWER-DOWN MODES		
0	1	Output 1 kΩ to GND
1	0	Output 100 kΩ to GND
1	1	High-Z

When both bits are set to 0, the device works normally with a standard power consumption of typically 80 µA at 2 V. However, for the three power-down modes, the typical supply current falls to 0.5 µA at 5 V, 0.4 µA at 3 V, and 0.1 µA at 2 V. Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. The advantage of this architecture is that the output impedance of the part is known while the part is in power-down mode. There are three different options: the output is connected internally to GND either through a 1-kΩ resistor or a 100-kΩ resistor, or is left open-circuited (High-Z). Figure 79 illustrates the output stage.

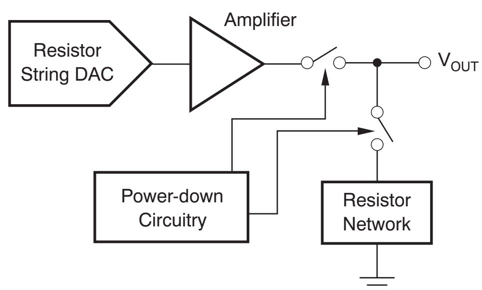


Figure 79. Output Stage During Power-Down

All linear circuitry is shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 50 µs for AV_{DD} = 5 V and AV_{DD} = 3 V.

8.5 Programming

8.5.1 Serial Interface

The DACx311 has a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and DIN) compatible with SPI, QSPI, and Microwire interface standards, as well as most DSPs. See Figure 1 for an example of a typical write sequence.

8.5.1.1 Input Shift Register

The input shift register is 16 bits wide, as shown in Figure 80. The first two bits (PD0 and PD1) are reserved control bits that set the desired mode of operation (normal mode or any one of three power-down modes) as indicated in Table 3.

The remaining data bits are either 12 (DAC7311), 10 (DAC6311), or 8 (DAC5311) data bits, followed by *don't care* bits, as shown in Figure 80, Figure 81, and Figure 82, respectively.

Figure 80. DAC5311 8-Bit Data Input Register

DB15	DB14								DB6	DB5					DB0
PD1	PD0	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X	X

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Figure 81. DAC6311 10-Bit Data Input Register

DB15	DB14										DB4	DB3			DB0
PD1	PD0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Figure 82. DAC7311 12-Bit Data Input Register

DB15	DB14												DB2	DB1	DB0
PD1	PD0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the DIN line are clocked into the 16-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 50 MHz, making

the DACx311 compatible with high-speed DSPs. On the 16th falling edge of the serial clock, the last data bit is clocked in and the programmed function is executed.

At this point, the $\overline{\text{SYNC}}$ line may be kept low or brought high. In either case, it must be brought high for a minimum of 20 ns before the next write sequence so that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence.

8.5.1.2 $\overline{\text{SYNC}}$ Interrupt

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th falling edge. However, bringing $\overline{\text{SYNC}}$ high before the 16th falling edge acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs, as shown in Figure 83.

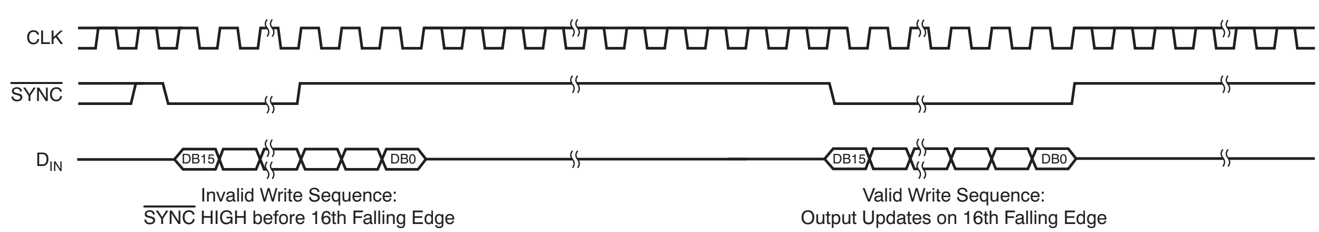


Figure 83. DACx311 $\overline{\text{SYNC}}$ Interrupt Facility

9 Application and Implementation

NOTE

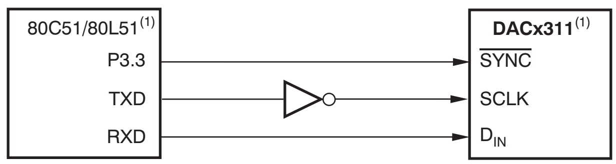
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Microprocessor Interfacing

9.1.1.1 DACx311 to 8051 Interface

Figure 84 shows a serial interface between the DACx311 and a typical 8051-type microcontroller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DACx311, while RXD drives the serial data line of the part. The SYNC signal is derived from a bit programmable pin on the port. In this case, port line P3.3 is used. When data are to be transmitted to the DACx311, P3.3 is taken low. The 8051 transmits data only in 8-bit bytes; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 remains low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 8051 outputs the serial data in a format which has the LSB first. The DACx311 requires its data with the MSB as the first bit received. Therefore, the 8051 transmit routine must take this requirement into account, and *mirror* the data as needed.

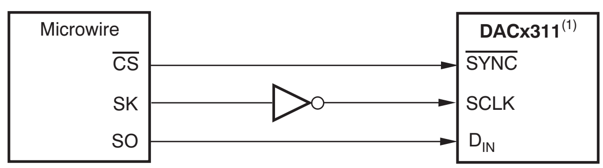


NOTE: (1) Additional pins omitted for clarity.

Figure 84. DACx311 to 80C51/80l51 Interfaces

9.1.1.2 DACx311 to Microwire Interface

Figure 85 shows an interface between the DACx311 and any Microwire-compatible device. Serial data are shifted out on the falling edge of the serial clock and are clocked into the DACx311 on the rising edge of the SK signal.



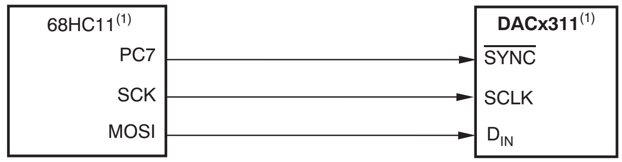
NOTE: (1) Additional pins omitted for clarity.

Figure 85. DACx311 to Microwire Interface

9.1.1.3 DACx311 to 68HC11 Interface

Figure 86 shows a serial interface between the DACx311 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DACx311, while the MOSI output drives the serial data line of the DAC. The SYNC signal is derived from a port line (PC7), similar to what was done for the 8051.

Application Information (continued)



NOTE: (1) Additional pins omitted for clarity.

Figure 86. DACx311 to 68HC11 Interface

The 68HC11 should be configured so that its CPOL bit is a 0 and its CPHA bit is a 1. This configuration causes data appearing on the MOSI output to be valid on the falling edge of SCK. When data are being transmitted to the DAC, the SYNC line is taken low (PC7). Serial data from the 68HC11 are transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data are transmitted MSB first. In order to load data to the DACx311, PC7 is held low after the first eight bits are transferred, and a second serial write operation is performed to the DAC; PC7 is taken high at the end of this procedure.

9.2 Typical Applications

9.2.1 Loop Powered Transmitter

The described loop powered transmitter can accurately source currents from 4 mA to 20 mA.

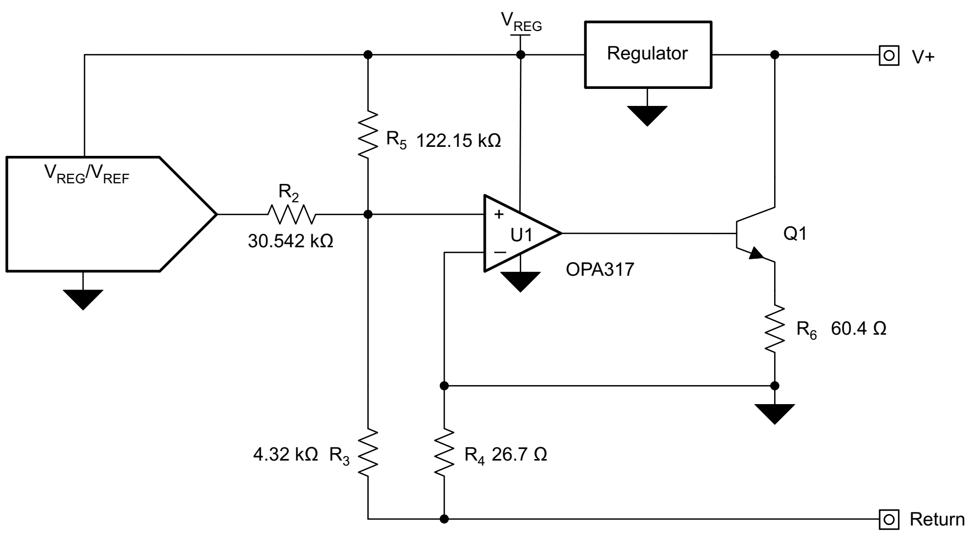


Figure 87. Loop Powered Transmitter Schematic

9.2.1.1 Design Requirements

The transmitter has only two external input terminals; a supply connection and a ground (or return) connection. The transmitter communicates back to the host, typically a PLC analog input module, by precisely controlling the magnitude of the return current. In order to conform to the 4-mA to 20-mA communication standards, the complete transmitter must consume less than 4 mA of current.

The complete design of this circuit is outlined in TIPD158, *Low Cost Loop-Powered 4-20mA Transmitter EMC/EMI Tested Reference Design*. The design is expected to be low-cost and deliver immunity to the IEC61000-4 suite of tests with minimum impact on the accuracy of the system. Reference design TIPD158 includes the design goals, simulated results, and measured performance.

Typical Applications (continued)

9.2.1.2 Detailed Design Procedure

Amplifier U1 uses negative feedback to make sure that the potentials at the inverting (V–) and noninverting (V+) input terminals are equal. In this configuration, V– is directly tied to the local GND; therefore, the potential at the noninverting input terminal is driven to local ground. Thus, the voltage difference across R_2 is the DAC output voltage (VOUT), and the voltage difference across R_5 is the regulator voltage (VREG). These voltage differences cause currents to flow through R_2 and R_5, as illustrated in Figure 88.

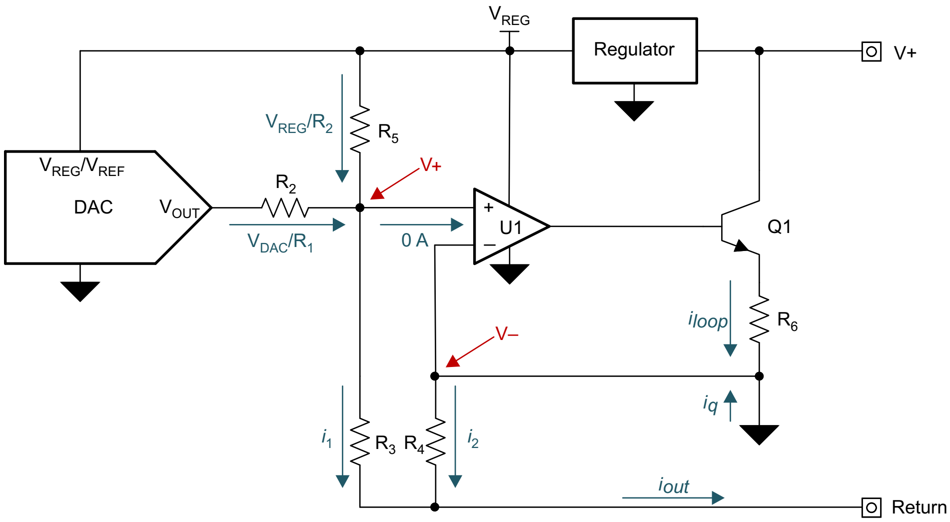


Figure 88. Voltage to Current Conversion

The currents from R_2 and R_5 sum into i_1 (defined in Equation 2), and i_1 flows through R_3.

$$i_1 = \frac{V_{DAC}}{R_2} + \frac{V_{REG}}{R_5} \tag{2}$$

Amplifier U2 drives the base of Q1, the NPN bipolar junction transistor (BJT), to allow current to flow through R_4 so that the voltage drops across R_3 and R_4 remain equal. This design keeps the inverting and noninverting terminals at the same potential. A small part of the current through R_4 is sourced by the quiescent current of all of the components used in the transmitter design (regulator, amplifier, and DAC). The voltage drops across R_3 and R_4 are equal; therefore, different-sized resistors cause different current flow through each resistor. Use these different-sized resistors to apply gain to the current flow through R_4 by controlling the ratio of resistor R_3 to R_4, as shown in Equation 3:

$$\begin{aligned} V+ &= i_1 \cdot R_3 \\ V- &= i_2 \cdot R_4 \Rightarrow i_2 = \frac{i_1 \cdot R_3}{R_4} \\ V+ &= V- \end{aligned} \tag{3}$$

The current gain in the circuit helps allow a majority of the output current to come directly from the loop through Q1 instead of from the voltage-to-current converter. This current gain, in addition to the low-power components, keeps the current consumption of the voltage-to-current converter low. Currents i_1 and i_2 sum to form output current i_{out}, as shown in Equation 4:

$$i_{out} = i_1 + i_2 = \frac{V_{DAC}}{R_2} + \frac{V_{REG}}{R_5} + \frac{R_3}{R_4} \cdot \left(\frac{V_{DAC}}{R_2} + \frac{V_{REG}}{R_5}\right) = \left(\frac{V_{DAC}}{R_2} + \frac{V_{REG}}{R_5}\right) \cdot \left(1 + \frac{R_3}{R_4}\right) \tag{4}$$

The complete transfer function, arranged as a function of input code, is shown in Equation 5. The remaining sections divide this circuit into blocks for simplified discussion.

$$i_{out}(Code) = \left(\frac{V_{REG} \cdot Code}{2^{Resolution} \cdot R_2} + \frac{V_{REG}}{R_5}\right) \cdot \left(1 + \frac{R_3}{R_4}\right) \tag{5}$$

Typical Applications (continued)

Resistor R_6 is included to reduce the gain of transistor Q1, and therefore, reduce the closed-loop gain of the voltage-to-current converter for a stable design. Size resistors R_2, R_3, R_4, and R_5 based on the full-scale range of the DAC, regulator voltage, and the desired current output range of the design.

9.2.1.3 Application Curves

Figure 89 shows the measured transfer function of the circuit. Figure 90 shows the total unadjusted error (TUE) of the circuit, staying below 0.15 %FSR.

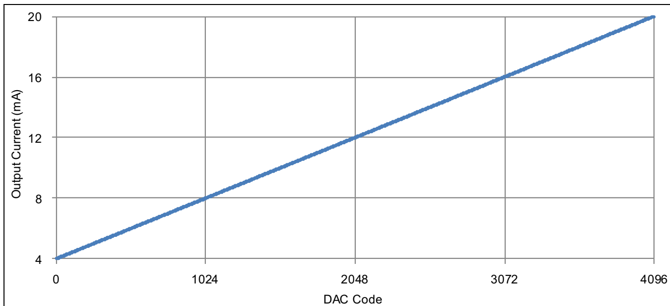


Figure 89. Output Current vs Code

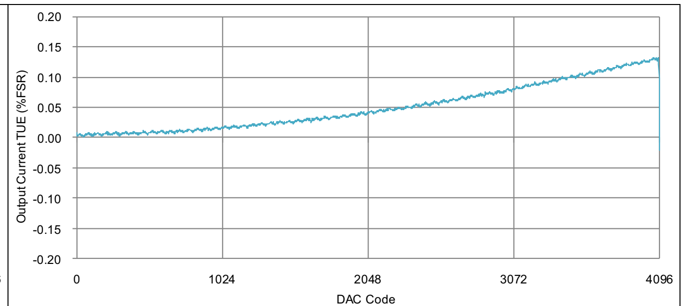


Figure 90. Current Total Unadjusted Error vs Code

9.2.2 Using the REF5050 as a Power Supply for the DACx311

As a result of the extremely low supply current required by the DACx311, an alternative option is to use a REF5050 5-V precision voltage reference to supply the required voltage to the part, as shown in Figure 91. This option is especially useful if the power supply is too noisy or if the system supply voltages are at some value other than 5 V. The REF5050 outputs a steady supply voltage for the DACx311. If the REF5050 is used, the current needed to supply DACx311 is typically 110 µA at 5 V, with no load on the output of the DAC. When the DAC output is loaded, the REF5050 also needs to supply the current to the load. The total current required (with a 5 kΩ load on the DAC output) is:

110 µA + (5 V / 5 kΩ) = 1.11 mA

The load regulation of the REF5050 is typically 0.002%/mA, which results in an error of 90 µV for the 1.1 mA current drawn from it. This value corresponds to a 0.07 LSB error at 12 bits (DAC7311).

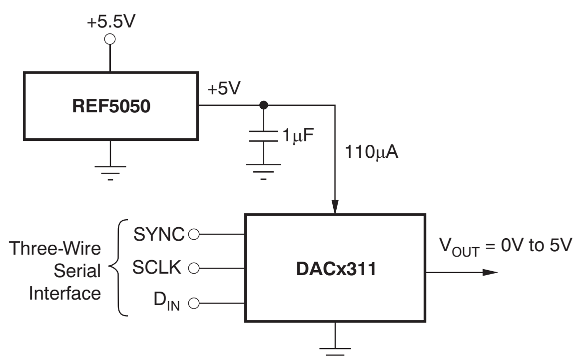


Figure 91. REF5050 as Power Supply to DACx311

For other power-supply voltages, alternative references such as the REF3030 (3 V), REF3033 (3.3 V), or REF3220 (2.048 V) are recommended. For a full list of available voltage references from TI, see the TI web site at www.ti.com.

Typical Applications (continued)

9.2.3 Bipolar Operation Using the DACx311

The DACx311 has been designed for single-supply operation but a bipolar output range is also possible using the circuit in Figure 92. The circuit shown gives an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an OPA211, OPA340, or OPA703 as the output amplifier. For a full list of available operational amplifiers from TI, see the TI web site at www.ti.com

The output voltage for any input code can be calculated as follows:

$$V_O = \left[AV_{DD} \times \left(\frac{D}{2^n}\right) \times \left(\frac{R_1 + R_2}{R_1}\right) - AV_{DD} \times \left(\frac{R_2}{R_1}\right) \right]$$

where

- n = resolution in bits; either 8 (DAC5311), 10 (DAC6311), or 12 (DAC7311).
- D = decimal equivalent of the binary code that is loaded to the DAC register. It ranges from 0 to 255 for 8-bit DAC5311; from 0 to 1023 for the 10-bit DAC6311; and 0 to 4095 for the 12-bit DAC7311. (6)

With AV_{DD} = 5 V, $R_1 = R_2$ = 10 kΩ:

$$V_O = \left(\frac{10 \times D}{2^n}\right) - 5V \tag{7}$$

The resulting output voltage range is ±5 V. Code 000h corresponds to a –5-V output and FFFh (12-bit level) corresponding to a +5-V output.

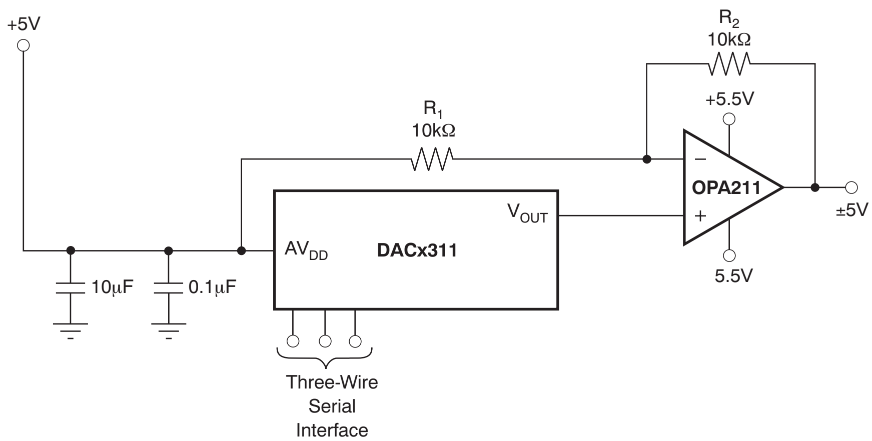


Figure 92. Bipolar Operation With the DACx311

10 Power Supply Recommendations

The DACx311 is designed to operate with a unipolar analog power supply ranging from 2.0 V to 5.5 V on the AV_{DD} pin. The AV_{DD} pin supplies power to the digital and analog circuits (including the resistor string) inside the DAC. The current consumption of this pin is specified in the *Electrical Characteristics* table. Use a 1 µF to 10 µF capacitor in parallel with a 0.1 µF bypass capacitor on this pin to remove high-frequency noise.

11 Layout

11.1 Layout Guidelines

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The DACx311 offers single-supply operation; it is often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to achieve good performance from the converter.

Because of the single ground pin of the DACx311, all return currents, including digital and analog return currents, must flow through the GND pin. Ideally, GND is connected directly to an analog ground plane. This plane should be separate from the ground connection for the digital components until they are connected at the power entry point of the system.

The power applied to AV_{DD} should be well-regulated and low-noise. Switching power supplies and dc/dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as the internal logic switches state. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. This condition is particularly true for the DACx311, as the power supply is also the reference voltage for the DAC.

As with the GND connection, AV_{DD} should be connected to a 5 V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. In addition, 1-μF to 10-μF and 0.1-μF bypass capacitors are strongly recommended. In some situations, additional bypassing may be required, such as a 100 μF electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors—all designed to essentially low-pass filter the 5-V supply, removing high-frequency noise.

11.2 Layout Example

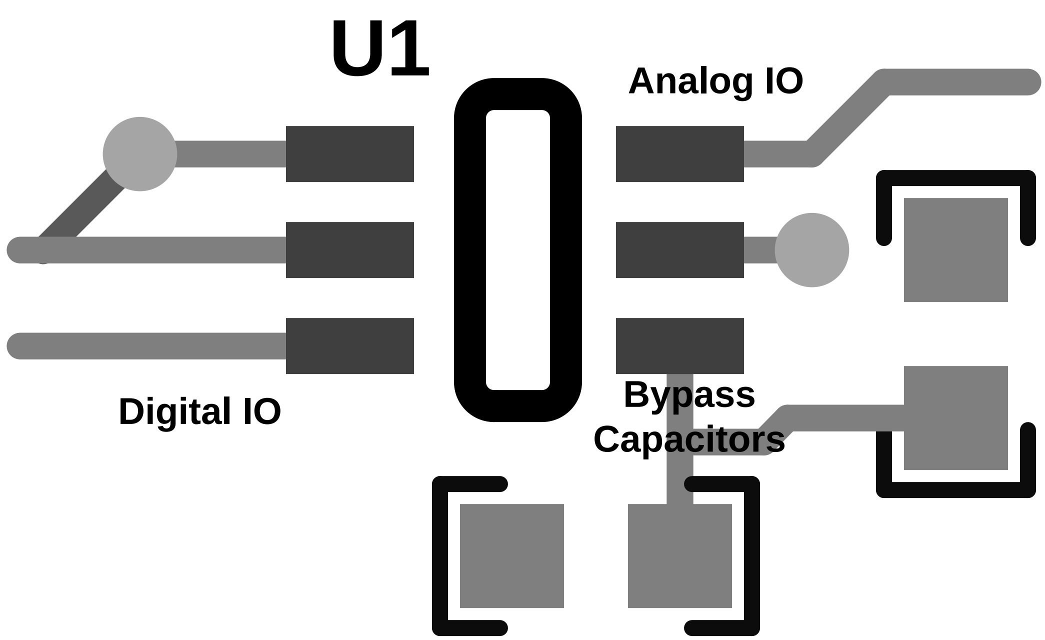


Figure 93. Recommended Layout

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DAC5311	Click here	Click here	Click here	Click here	Click here
DAC6311	Click here	Click here	Click here	Click here	Click here
DAC7311	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
SPI, QSPI are trademarks of Motorola, Inc.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC5311IDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	D53	Samples
DAC5311IDCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	D53	Samples
DAC5311IDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	D53	Samples
DAC6311IDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	D63	Samples
DAC6311IDCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	D63	Samples
DAC6311IDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	D63	Samples
DAC6311IDCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	D63	Samples
DAC7311IDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	D73	Samples
DAC7311IDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	D73	Samples
DAC7311IDCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	D73	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF DAC5311 :

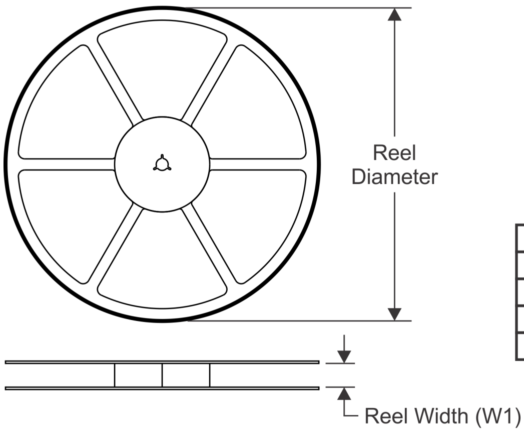
- Automotive: DAC5311-Q1

NOTE: Qualified Version Definitions:

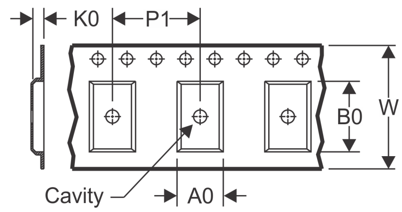
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

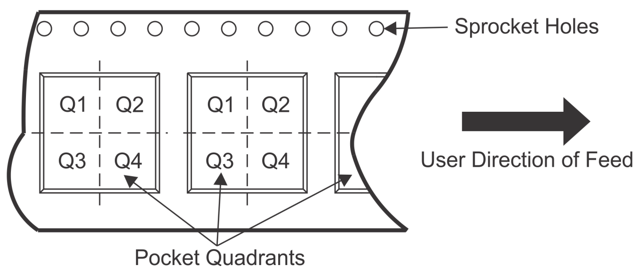


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

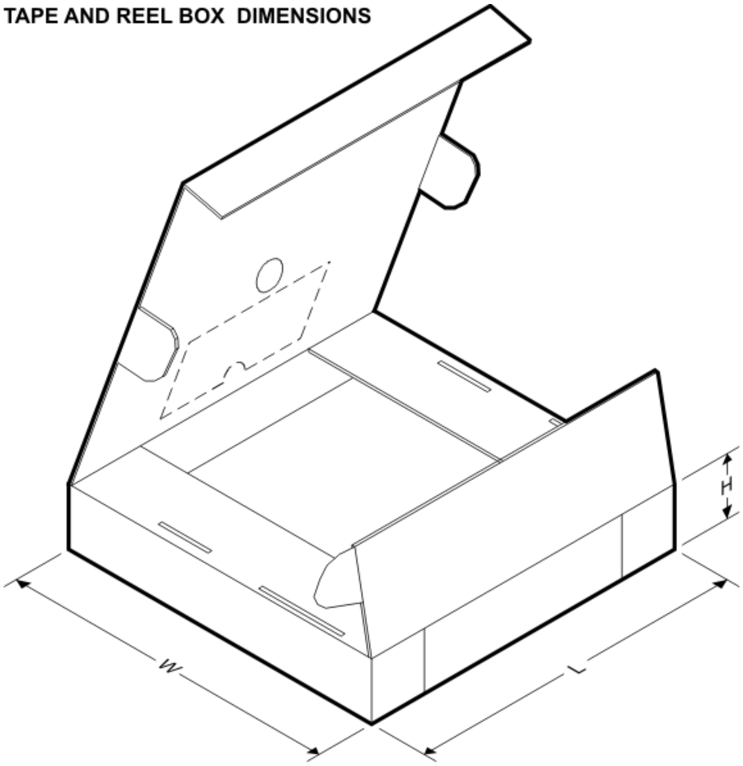
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC5311IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
DAC5311IDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
DAC6311IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
DAC6311IDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
DAC7311IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
DAC7311IDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

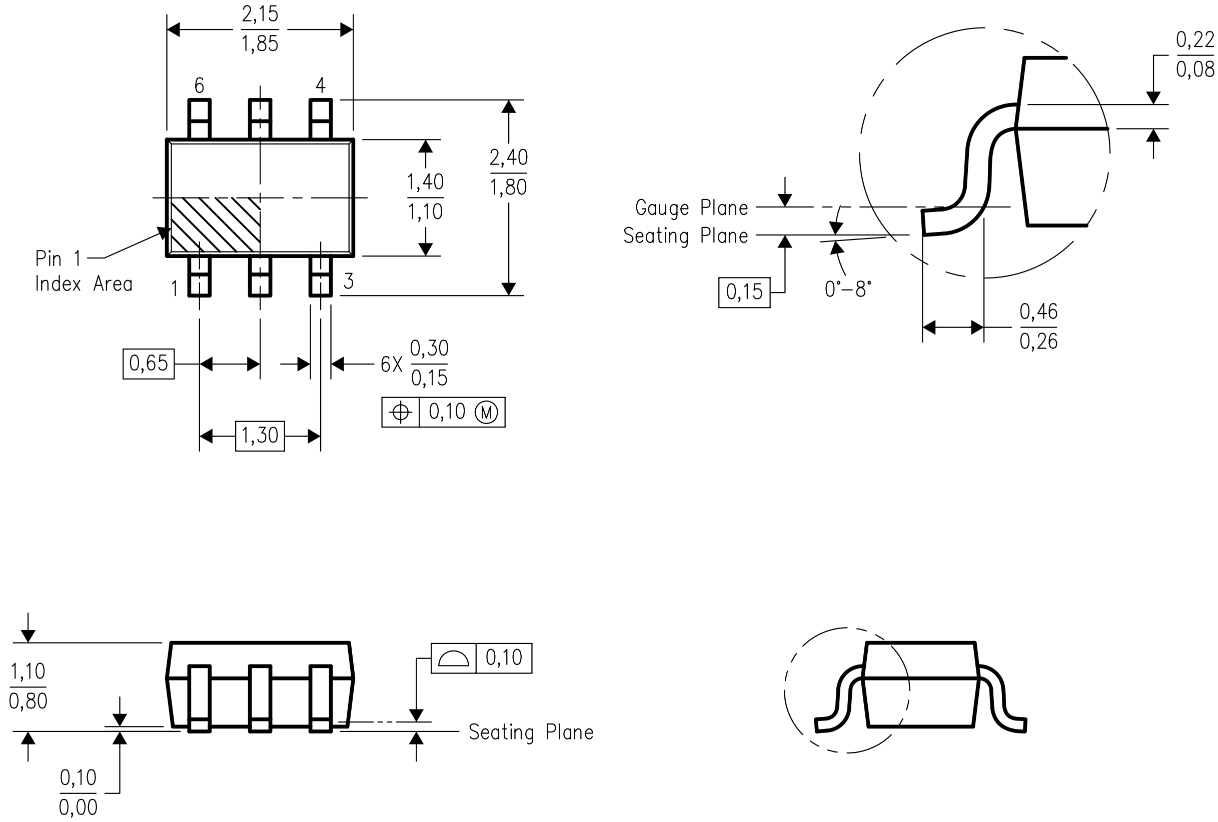
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC5311IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
DAC5311IDCKT	SC70	DCK	6	250	180.0	180.0	18.0
DAC6311IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
DAC6311IDCKT	SC70	DCK	6	250	180.0	180.0	18.0
DAC7311IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
DAC7311IDCKT	SC70	DCK	6	250	180.0	180.0	18.0

DCK (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



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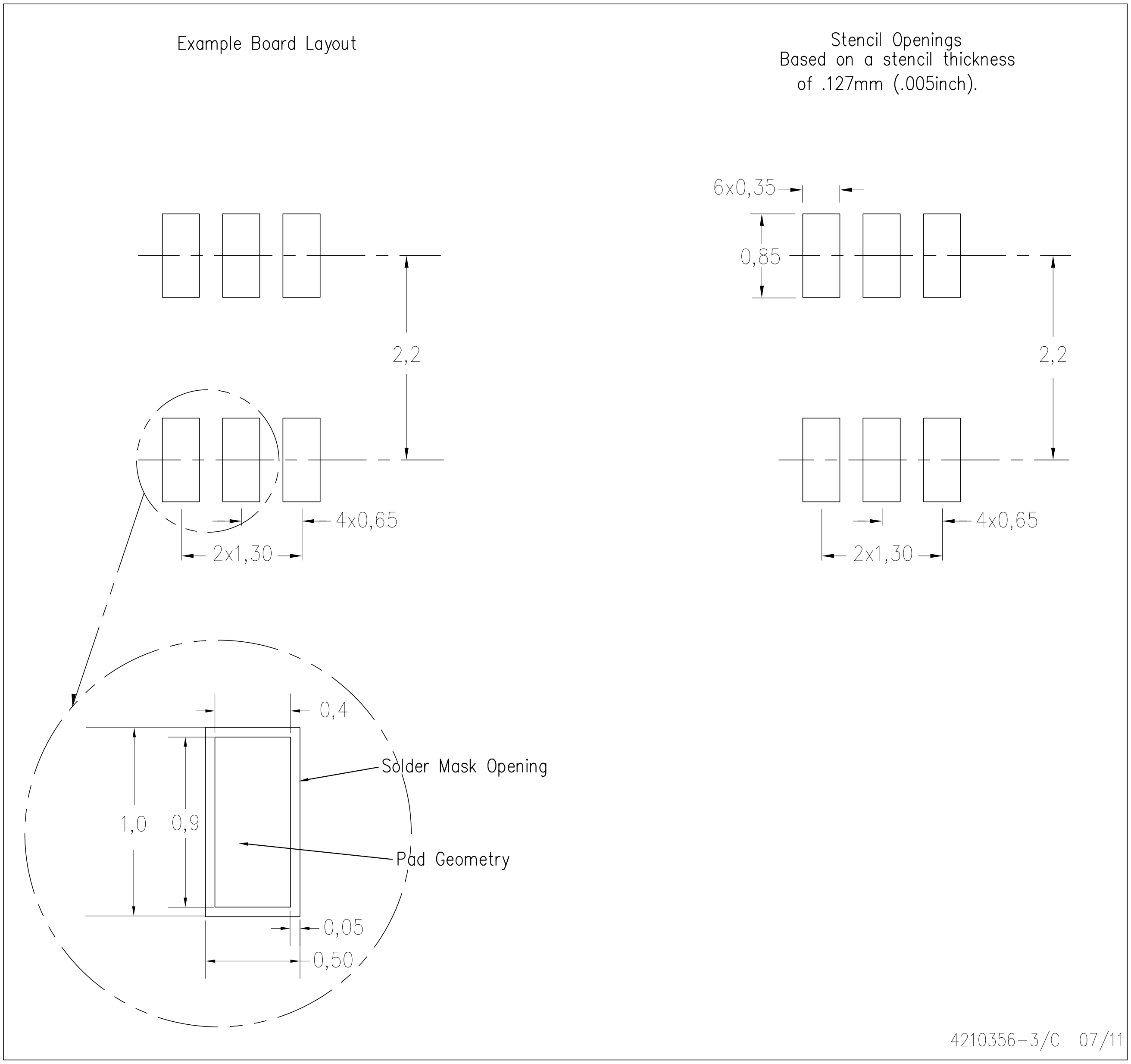
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.