

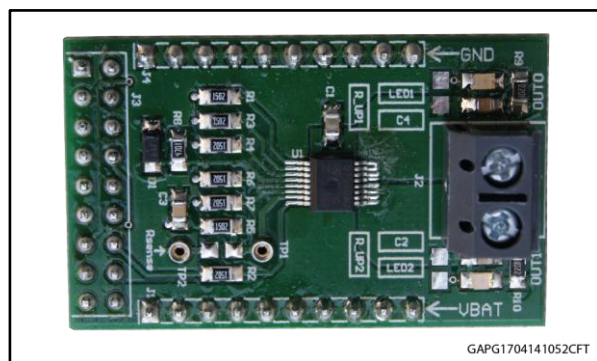


THE DATASHEET OF EV-VND7050AJ



VND7050AJ evaluation board

Data brief



Features

Max transient supply voltage	V_{CC}	40 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per Ch)	R_{ON}	50 m Ω
Current limitation (typ)	I_{LIMH}	30 A
Stand-by current (max)	I_{STBY}	0.5 μ A

- Simple single IC application board dedicated for VND7050AJ
- Provides electrical connectivity and thermal heat-sinking for easy prototyping
- General device features
 - Double channel smart high-side driver with MultiSense analog feedback
 - Very low standby current
 - Compatible with 3 V and 5 V CMOS outputs

- Diagnostic functions
 - Multiplexed analog feedback of: load current with high precision proportional current mirror, V_{CC} supply voltage and T_{CHIP} device temperature
 - Overload and short to ground (power limitation) indication
 - Thermal shutdown indication
 - OFF-state open-load detection
 - Output short to V_{CC} detection
 - Sense enable/disable
- Protections
 - Undervoltage shutdown
 - Overvoltage clamp
 - Load current limitation
 - Self limiting of fast thermal transients
 - Configurable latch-off on overtemperature or power limitation with dedicated fault reset pin
 - Loss of ground and loss of V_{CC}
 - Reverse battery with external components
 - Electrostatic discharge protection

Applications

Typical applications are all types of automotive resistive, inductive and capacitive loads.

Table 1: Device summary

Order code	Reference
EV-VND7050AJ	VND7050AJ evaluation board

2 Board connections

Figure 2: "Evaluation board connections" shows the placement of the connectors to be used for supplying the evaluation board, connecting the load and controlling the functionality and diagnostic of the device.

Figure 2: Evaluation board connections

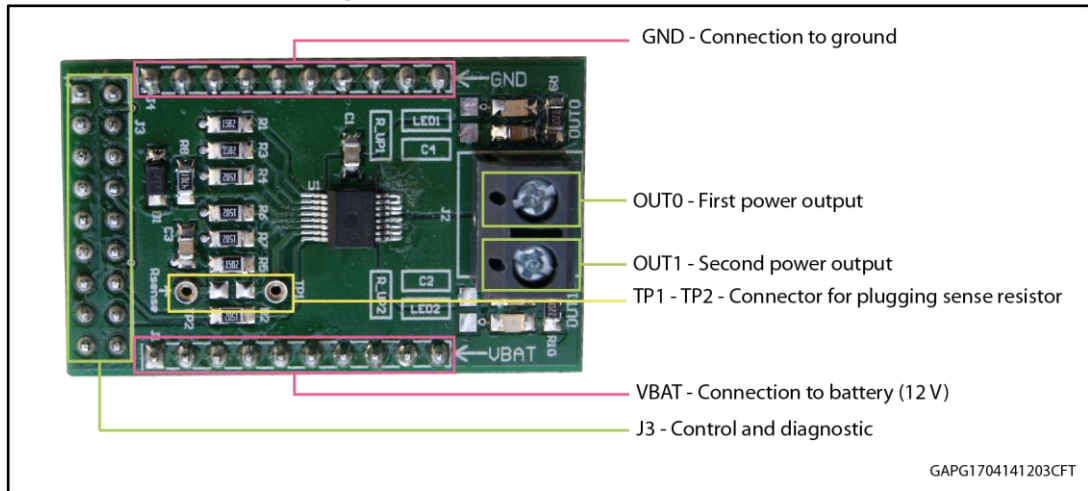


Table 2: J3 connector: pin functions

Connector	Pin number	Pin name	Pin function
J3	1...4	N/A	Not connected
J3	5	IN_PullUP	Connection to optional external pull-up resistor for open load detection in off-state.
J3	6	+5V	5 V Power Supply
J3	7	FaultRST	Active low compatible with 3 V and 5 V CMOS outputs pin; it unlatches the output in case of fault; If kept low, sets the outputs in auto-restart
J3	8	MultiSense	Multiplexed analog sense output pin; it delivers a current proportional to the selected diagnostic: load current, supply voltage or chip temperature
J3	9	S_EN	Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the MultiSense diagnostic pin.
J3	10	SEL0	Active high compatible with 3 V and 5 V CMOS outputs pin; together with SEL1, it addresses the MultiSense multiplexer
J3	11	SEL1	Active high compatible with 3 V and 5 V CMOS outputs pin; together with SEL0, it addresses the MultiSense multiplexer
J3	12	N/A	Not connected
J3	13	IN0	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls OUT0 switch state
J3	14	IN1	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls OUT1 switch state
J3	15...18	N/A	Not connected

In case the user wishes to utilize the Current Sense/MultiSense function of the device, it is necessary to plug a sense resistor in R_{SENSE} .

The package includes a through-hole resistor, to be mounted on TP1-TP2 (see [Figure 4: "Mounting through-hole sense resistor"](#)).

Different R_{SENSE} values can be adopted based on user preference.

Another option is soldering an SMD resistor on the dedicated PCB pad, as shown in [Figure 5: "Pads for soldering SMD resistor"](#).

Figure 3: No sense resistor



Figure 4: Mounting through-hole sense resistor

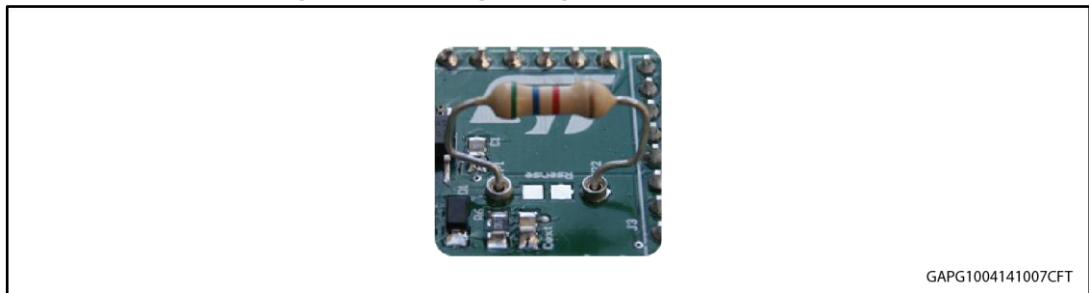
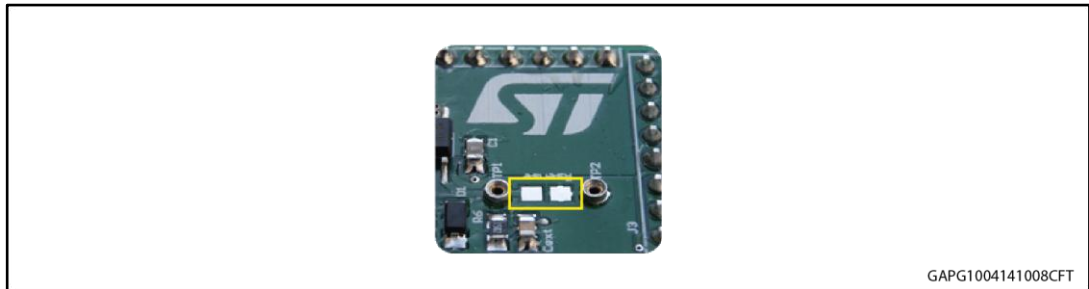


Figure 5: Pads for soldering SMD resistor



3 Thermal data

Table 3: Thermal data

Symbol	Parameter	Max	Unit
$R_{thj-amb}$	Thermal resistance junction-ambient (MAX)	39	°C/W

Table 4: PCB specifications

Parameter	Value
Board dimensions	25 mm x 41.5 mm
Number of Cu layer	2
Layer Cu thickness	35 μ m
Board finish thickness	1.6 mm +/- 10%
Board Material	FR4
Thermal vias separation	1.1 mm
Thermal vias diameter	0.5 mm

4 Revision history

Table 5: Revision history

Date	Revision	Changes
15-May-2014	1	Initial release.
21-Jul-2014	2	Updated <i>Figure 1: "Evaluation board schematic"</i>
02-Sep-2015	3	Updated <i>Section "Features"</i> and <i>Section 1: "Description"</i>

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