



**THE DATASHEET OF
CY8C21345-24PVXAT**

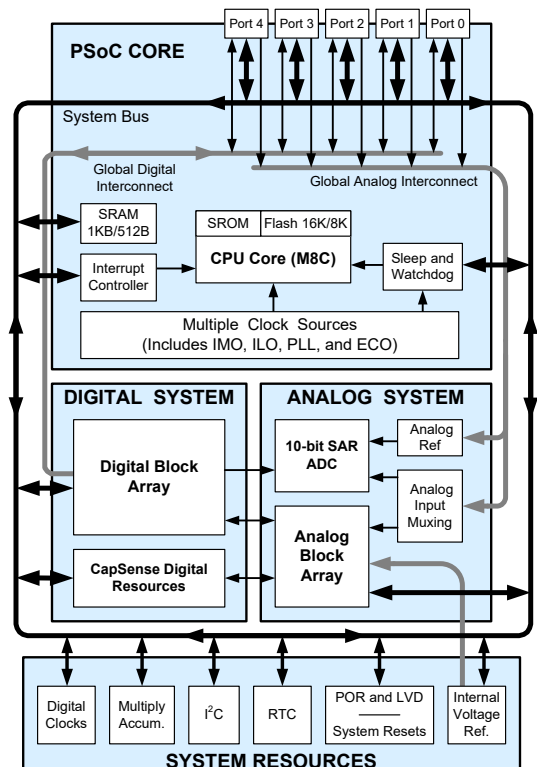


Features

- Automotive Electronics Council (AEC) Q100 qualified
- Powerful Harvard-architecture processor
 - M8C processor speeds up to 24 MHz
 - 8 × 8 multiply, 32-bit accumulate
 - Low power at high speed
 - Automotive A-grade: 3.0 V to 5.25 V operation at -40 °C to +85 °C temperature range
 - Automotive E-grade: 4.75 V to 5.25 V operation at -40 °C to +125 °C temperature range
- Advanced peripherals (PSoC® blocks)
 - Six analog Type 'E' PSoC blocks provide:
 - Up to four comparators with digital-to-analog converters (DAC) references
 - Up to 10-bit single or dual analog-to-digital converters (ADCs)
 - Up to eight digital PSoC blocks provide:
 - 8 to 32-bit timers, counters, and pulse width modulators (PWMs)
 - One-shot, multi-shot mode in timers and PWMs
 - PWM with deadband in one digital block
 - Shift register, cyclical redundancy check (CRC), and pseudo random sequence (PRS) modules
 - Full- or half-duplex UARTs
 - SPI masters or slaves, 8- to 16-bit variable data length
 - Connectable to all general-purpose I/O (GPIO) pins
 - Complex peripherals by combining blocks
 - Powerful synchronization support, analog module operations can be synchronized by digital blocks or external signals.
- High-speed 10-bit successive approximation register (SAR) ADC with sample and hold optimized for embedded control
- CY8C22345H devices Integrate Immersion® TouchSense® Haptics Technology for ERM drive control
- Precision, programmable clocking
 - Internal oscillator up to 24 MHz
 - High accuracy 24 MHz with optional 32-kHz crystal and phase locked loop (PLL)
 - Optional external oscillator, up to 24 MHz
 - Internal low speed, low-power oscillator for watchdog and sleep functionality
- Flexible on-chip memory
 - Up to 16 KB flash program storage, 1000 erase/write cycles
 - Up to 1 KB SRAM data storage
 - In-System Serial Programming (ISSP)
 - Partial flash updates
 - Flexible protection modes
 - EEPROM emulation in flash
- Optimized CapSense® resource
 - Supports two CapSense channels with simultaneous scanning

- Two current DACs provide programmable sensor tuning in firmware
- Two dedicated clock resources for CapSense
- Two dedicated 16-bit timers/counters for CapSense scanning
- Versatile analog mux
 - Common internal analog bus
 - Simultaneous connection of I/O combinations
- Programmable pin configurations
 - 25 mA sink, 10 mA drive on all GPIOs
 - Pull-up, pull-down, high Z, strong, or open-drain drive modes on all GPIOs
 - Analog input on all GPIOs
 - Configurable interrupt on all GPIOs
- Additional system resources:
 - I²C master, slave, or multi-master
 - Operation up to 400 kHz
 - Hardware address detection feature
 - Watchdog and sleep timers
 - User-configurable low voltage detection
 - Integrated supervisory circuit
 - On-chip precision voltage reference
 - Hardware real time clock (RTC) block

Block Diagram



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PSoC Functional Overview

The PSoC programmable system-on-chip series of products consists of many devices. These devices are designed to replace multiple traditional MCU-based system components with one low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, as well as programmable interconnects. This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The PSoC architecture, shown in the [Block Diagram on page 1](#), consists of four main areas: PSoC core, digital system, analog system, and system resources. Configurable global busing allows the combining of all the device resources into a complete custom system. The PSoC family can have up to five I/O ports connecting to the global digital and analog interconnects, providing access to eight digital blocks^[1] and six analog blocks.

PSoC Core

The PSoC core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO.

The M8C CPU core is a powerful processor with speeds up to 24 MHz (up to 12 MHz for E-grade devices), providing four MIPS (two MIPS for E-grade devices) 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller to simplify the programming of real time embedded events.

Program execution is timed and protected using the included Sleep Timer and watchdog timer (WDT).

Memory encompasses 16 KB of flash (8 KB for CY8C21x45 devices) for program storage, 1 KB of SRAM (512 bytes for CY8C21x45 devices) for data storage, and EEPROM emulation using the flash. Program flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

The PSoC device incorporates flexible internal clock generators, including a 24-MHz internal main oscillator (IMO). For A-grade devices the 24-MHz IMO can also be doubled to 48 MHz for use by the digital system. A low-power 32-kHz internal low-speed oscillator (ILO) is provided for the Sleep Timer and WDT. If crystal accuracy is required, the 32.768 kHz external crystal oscillator (ECO) is available for use as a RTC, and can optionally generate a crystal-accurate 24-MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a system resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Each pin can also generate a system interrupt.

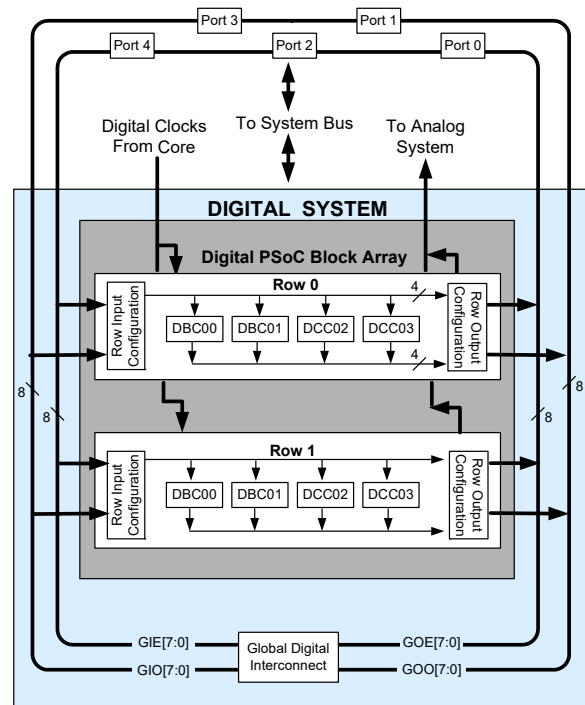
Note

1. CY8C22x45 devices have 2 digital rows with 8 digital blocks. CY8C21x45 devices only have 1 digital row with 4 digital blocks.

Digital System

The digital system is composed of eight digital PSoC blocks. Each block is an 8-bit resource that may be used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user modules.

Figure 1. Digital System Block Diagram^[1]



Digital peripheral configurations are:

- PWMs (8- to 16-bit)
- PWMs with deadband (8- to 32-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- One-shot and multi-shot modules
- Full or half-duplex 8-bit UART with selectable parity (up to two full-duplex or four half-duplex)
- SPI master and slave (up to four total) with programmable data length from 8 to 16 bits.
- Shift register (1- to 32-bit)
- I²C master, slave, or multi-master (one available)
- CRC/generator (16-bit)
- IrDA (up to two)
- PRS generators (8- to 32-bit)

The digital blocks may be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This provides a choice of system resources for your application. Family resources are shown in [Table 1 on page 5](#).

Analog System

The Analog System of CY8C21x45 and CY8C22x45 PSoC devices consists of a 10-bit SAR ADC and six configurable analog blocks.

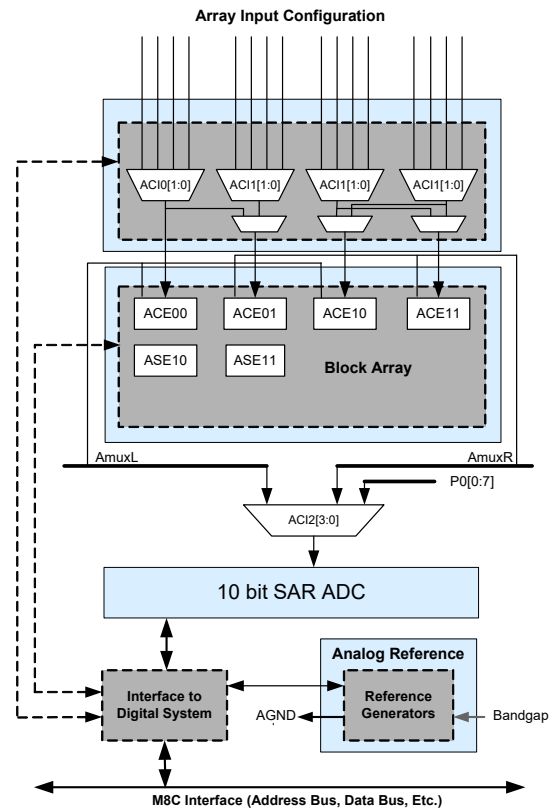
The programmable 10-bit SAR ADC is an optimized ADC with a fast maximum sample rate. External filters are required on ADC input channels for antialiasing. This ensures that any out-of-band content is not folded into the input signal band.

Reconfigurable analog resources allow creating complex analog signal flows. Analog peripherals are very flexible and may be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (single or dual, with up to 10-bit resolution)
- Pin-to-pin comparator
- Single-ended comparators (up to four) with absolute (1.3 V) reference or DAC reference
- Precision voltage reference (1.3 V nominal)

CY8C21x45 and CY8C22x45 devices have six limited-functionality Type 'E' analog blocks. These analog blocks are arranged in four columns. Each column contains one continuous time (CT) Type E block. The first two columns also have a switched capacitor (SC) type E block. Refer to the [PSoC Technical Reference Manual](#) for CY8C21x45 and CY8C22x45 devices for detailed information on the Type E analog blocks.

Figure 2. Analog System Block Diagram



Haptics TS2000 Controller

The CY8C22x45H family of devices features an easy-to-use Haptics controller resource with up to 14 different effects. These effects are available for use with three different, selectable ERM modules.

Additional System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful for complete systems. Additional resources include a MAC, low voltage detection, and power on reset. The merits of each system resource are:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks may be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Additional digital resources and clocks dedicated to and optimized for CapSense.
- RTC hardware block.

- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math and digital filters.
- The I²C module provides 0 to 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power on reset (POR) circuit eliminates the need for a system supervisor.
- An internal voltage reference provides an absolute reference for the analog system, including ADCs and DACs.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have varying numbers of digital and analog blocks. The following table lists the resources available for specific PSoC device groups. The PSoC families covered by this datasheet are highlighted in the table.

Table 1. PSoC Device Characteristics

| PSoC Part Number | Digital I/O | Digital Rows | Digital Blocks | Analog Inputs | Analog Outputs | Analog Columns | Analog Blocks | SRAM Size | Flash Size |
|---------------------------|-------------|--------------|----------------|---------------|----------------|----------------|-----------------------------|-----------|------------|
| CY8C29x66 ^[2] | up to 64 | 4 | 16 | up to 12 | 4 | 4 | 12 | 2 K | 32 K |
| CY8C28xxx | up to 44 | up to 3 | up to 12 | up to 44 | up to 4 | up to 6 | up to 12 + 4 ^[3] | 1 K | 16 K |
| CY8C27x43 | up to 44 | 2 | 8 | up to 12 | 4 | 4 | 12 | 256 | 16 K |
| CY8C24x94 ^[2] | up to 56 | 1 | 4 | up to 48 | 2 | 2 | 6 | 1 K | 16 K |
| CY8C24x23A ^[2] | up to 24 | 1 | 4 | up to 12 | 2 | 2 | 6 | 256 | 4 K |
| CY8C23x33 | up to 26 | 1 | 4 | up to 12 | 2 | 2 | 4 | 256 | 8 K |
| CY8C22x45 ^[2] | up to 38 | 2 | 8 | up to 38 | 0 | 4 | 6 ^[3] | 1 K | 16 K |
| CY8C21x45 ^[2] | up to 24 | 1 | 4 | up to 24 | 0 | 4 | 6 ^[3] | 512 | 8 K |
| CY8C21x34 ^[2] | up to 28 | 1 | 4 | up to 28 | 0 | 2 | 4 ^[3] | 512 | 8 K |
| CY8C21x23 | up to 16 | 1 | 4 | up to 8 | 0 | 2 | 4 ^[3] | 256 | 4 K |
| CY8C20x34 ^[2] | up to 28 | 0 | 0 | up to 28 | 0 | 0 | 3 ^[3, 4] | 512 | 8 K |
| CY8C20xx6 | up to 36 | 0 | 0 | up to 36 | 0 | 0 | 3 ^[3, 4] | up to 2 K | up to 32 K |

Notes

2. Automotive qualified devices available in this group.
3. Limited analog functionality.
4. Two analog blocks and one CapSense[®] block.

Getting Started

For in depth information, along with detailed programming details, see the *PSoC[®] Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest [PSoC device datasheets](#) on the web.

Application Notes

[Cypress application notes](#) are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

[PSoC Development Kits](#) are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

[Free PSoC technical training](#) (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the [CYPros Consultants](#) web site.

Solutions Library

Visit our growing [library of solution focused designs](#). Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

[Technical support](#) – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary Integrated Design Environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
 - Hardware and software I²C slaves and masters
 - Full-speed USB 2.0
 - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for a given application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality In-Circuit Emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24-MHz) operation.

Designing with PSoC Designer

The development process for the PSoC[®] device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select [User Modules](#).
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a pulse width modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Pinouts

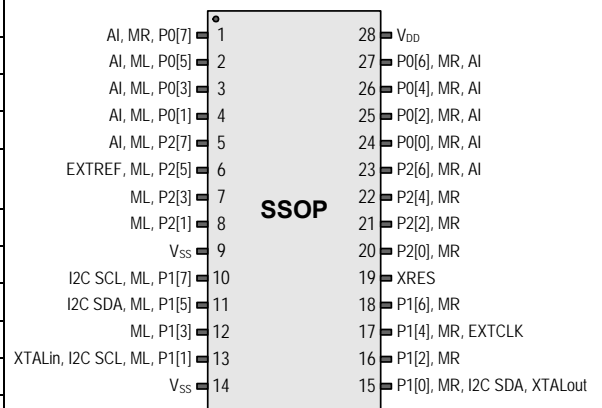
The automotive CY8C21x45 and CY8C22x45 PSoC devices are available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a "P") is capable of digital I/O and connection to the common analog mux bus. However, V_{SS}, V_{DD}, and XRES are not capable of digital I/O.

28-pin Part Pinout

Table 2. 28-pin Part Pinout (SSOP)

| Pin No. | Type | | Pin Name | Description |
|---------|---------|--------|-----------------|---|
| | Digital | Analog | | |
| 1 | I/O | I, MR | P0[7] | Analog column mux input, C _{MOD} capacitor pin |
| 2 | I/O | I, ML | P0[5] | Analog column mux input, C _{MOD} capacitor pin |
| 3 | I/O | I, ML | P0[3] | Analog column mux input |
| 4 | I/O | I, ML | P0[1] | Analog column mux input |
| 5 | I/O | I, ML | P2[7] | Direct input to analog block |
| 6 | I/O | ML | P2[5] | Optional SAR ADC external reference (EXTREF) |
| 7 | I/O | ML | P2[3] | |
| 8 | I/O | ML | P2[1] | |
| 9 | Power | | V _{SS} | Ground connection |
| 10 | I/O | ML | P1[7] | I ² C serial clock (SCL) |
| 11 | I/O | ML | P1[5] | I ² C serial data (SDA) |
| 12 | I/O | ML | P1[3] | |
| 13 | I/O | ML | P1[1] | Crystal input (XTALin), I ² C SCL, ISSP-SCLK ⁵ |
| 14 | Power | | V _{SS} | Ground connection |
| 15 | I/O | MR | P1[0] | Crystal output (XTALout), I ² C SDA, ISSP-SDATA ⁵ |
| 16 | I/O | MR | P1[2] | |
| 17 | I/O | MR | P1[4] | Optional external clock input (EXTCLK) |
| 18 | I/O | MR | P1[6] | |
| 19 | Input | | XRES | Active high external reset with internal pull-down |
| 20 | I/O | MR | P2[0] | |
| 21 | I/O | MR | P2[2] | |
| 22 | I/O | MR | P2[4] | |
| 23 | I/O | I, MR | P2[6] | Direct input to analog block |
| 24 | I/O | I, MR | P0[0] | Analog column mux input |
| 25 | I/O | I, MR | P0[2] | Analog column mux input |
| 26 | I/O | I, MR | P0[4] | Analog column mux input |
| 27 | I/O | I, MR | P0[6] | Analog column mux input |
| 28 | Power | | V _{DD} | Supply voltage |

Figure 3. CY8C21345 and CY8C22345 28-pin PSoC Device



LEGEND: A = Analog, I = Input, O = Output, MR= Right analog mux bus input, ML= Left analog mux bus input.

Note

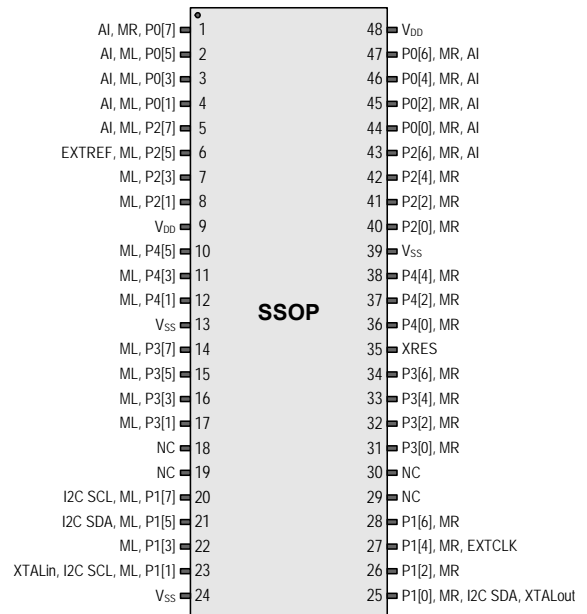
5. These are the ISSP pins, which are not High Z after exiting a reset state. See the [PSoC Technical Reference Manual](#) for CY8C21x45 and CY8C22x45 devices for details.

48-pin Part Pinout

Table 3. 48-pin Part Pinout (SSOP)

| Pin No. | Type | | Pin Name | Description |
|---------|---------|--------|-----------------|---|
| | Digital | Analog | | |
| 1 | I/O | I, MR | P0[7] | Analog column mux input, C _{MOD} capacitor pin |
| 2 | I/O | I, ML | P0[5] | Analog column mux input, C _{MOD} capacitor pin |
| 3 | I/O | I, ML | P0[3] | Analog column mux input |
| 4 | I/O | I, ML | P0[1] | Analog column mux input |
| 5 | I/O | I, ML | P2[7] | Direct input to analog block |
| 6 | I/O | ML | P2[5] | Optional SAR ADC external reference |
| 7 | I/O | ML | P2[3] | |
| 8 | I/O | ML | P2[1] | |
| 9 | Power | | V _{DD} | Supply voltage |
| 10 | I/O | ML | P4[5] | |
| 11 | I/O | ML | P4[3] | |
| 12 | I/O | ML | P4[1] | |
| 13 | Power | | V _{SS} | Ground connection |
| 14 | I/O | ML | P3[7] | |
| 15 | I/O | ML | P3[5] | |
| 16 | I/O | ML | P3[3] | |
| 17 | I/O | ML | P3[1] | |
| 18 | | | NC | Not connected |
| 19 | | | NC | Not connected |
| 20 | I/O | ML | P1[7] | I ² C serial clock |
| 21 | I/O | ML | P1[5] | I ² C serial data |
| 22 | I/O | ML | P1[3] | |
| 23 | I/O | ML | P1[1] | Crystal input (XTALin), I ² C SCL, ISSP-SCLK ^[6] |
| 24 | Power | | V _{SS} | |
| 25 | I/O | MR | P1[0] | Crystal output (XTALout), I ² C SDA, ISSP-SDATA ^[6] |
| 26 | I/O | MR | P1[2] | |
| 27 | I/O | MR | P1[4] | Optional external clock input |
| 28 | I/O | MR | P1[6] | |
| 29 | | | NC | Not connected |
| 30 | | | NC | Not connected |
| 31 | I/O | MR | P3[0] | |
| 32 | I/O | MR | P3[2] | |
| 33 | I/O | MR | P3[4] | |
| 34 | I/O | MR | P3[6] | |
| 35 | Input | | XRES | Active high external reset with internal pull-down |
| 36 | I/O | MR | P4[0] | |
| 37 | I/O | MR | P4[2] | |
| 38 | I/O | MR | P4[4] | |

Figure 4. CY8C21645 and CY8C22645 48-pin PSoc Device



Note

6. These are the ISSP pins, which are not High Z after exiting a reset state. See the [PSoc Technical Reference Manual](#) for CY8C21x45 and CY8C22x45 devices for details.

Table 3. 48-pin Part Pinout (SSOP) (continued)

| Pin No. | Type | | Pin Name | Description |
|---------|---------|--------|-----------------|------------------------------|
| | Digital | Analog | | |
| 39 | Power | | V _{SS} | Ground connection |
| 40 | I/O | MR | P2[0] | |
| 41 | I/O | MR | P2[2] | |
| 42 | I/O | MR | P2[4] | |
| 43 | I/O | I, MR | P2[6] | Direct input to analog block |
| 44 | I/O | I, MR | P0[0] | Analog column mux input |
| 45 | I/O | I, MR | P0[2] | Analog column mux input |
| 46 | I/O | I, MR | P0[4] | Analog column mux input |
| 47 | I/O | I, MR | P0[6] | Analog column mux input |
| 48 | Power | | V _{DD} | Supply voltage |

LEGEND: A = Analog, I = Input, O = Output, MR= Right analog mux bus input, ML= Left analog mux bus input

Registers

This section lists the registers of this PSoC device family by mapping tables. For detailed register information, refer to the [PSoC Technical Reference Manual](#) for CY8C21x45 and CY8C22x45 devices.

Register Conventions

The register conventions specific to this section are listed in the following table.

Table 4. Abbreviations

| Convention | Description |
|------------|-----------------------------------|
| RW | Read and write register or bit(s) |
| R | Read register or bit(s) |
| W | Write register or bit(s) |
| L | Logical register or bit(s) |
| C | Clearable register or bit(s) |
| # | Access is bit specific |

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and must not be accessed.

Table 5. Register Map Bank 0 Table: User Space

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|----------|--------------|--------|------------|--------------|--------|----------|--------------|--------|-----------|--------------|--------|
| PRT0DR | 00 | RW | | 40 | | ASE10CR0 | 80 | RW | | C0 | |
| PRT0IE | 01 | RW | | 41 | | | 81 | | | C1 | |
| PRT0GS | 02 | RW | | 42 | | | 82 | | | C2 | |
| PRT0DM2 | 03 | RW | | 43 | | | 83 | | | C3 | |
| PRT1DR | 04 | RW | | 44 | | ASE11CR0 | 84 | RW | | C4 | |
| PRT1IE | 05 | RW | | 45 | | | 85 | | | C5 | |
| PRT1GS | 06 | RW | | 46 | | | 86 | | | C6 | |
| PRT1DM2 | 07 | RW | | 47 | | | 87 | | | C7 | |
| PRT2DR | 08 | RW | | 48 | | | 88 | | PWMVREF0 | C8 | # |
| PRT2IE | 09 | RW | | 49 | | | 89 | | PWMVREF1 | C9 | # |
| PRT2GS | 0A | RW | | 4A | | | 8A | | IDAC_MODE | CA | RW |
| PRT2DM2 | 0B | RW | | 4B | | | 8B | | PWM_SRC | CB | # |
| PRT3DR | 0C | RW | | 4C | | | 8C | | TS_CR0 | CC | RW |
| PRT3IE | 0D | RW | | 4D | | | 8D | | TS_CMPH | CD | RW |
| PRT3GS | 0E | RW | | 4E | | | 8E | | TS_Cmpl | CE | RW |
| PRT3DM2 | 0F | RW | | 4F | | | 8F | | TS_CR1 | CF | RW |
| PRT4DR | 10 | RW | CSD0_DR0_L | 50 | R | | 90 | | CUR_PP | D0 | RW |
| PRT4IE | 11 | RW | CSD0_DR1_L | 51 | W | | 91 | | STK_PP | D1 | RW |
| PRT4GS | 12 | RW | CSD0_CNT_L | 52 | R | | 92 | | | D2 | |
| PRT4DM2 | 13 | RW | CSD0_CR0 | 53 | # | | 93 | | IDX_PP | D3 | RW |
| | 14 | | CSD0_DR0_H | 54 | R | | 94 | | MVR_PP | D4 | RW |
| | 15 | | CSD0_DR1_H | 55 | W | | 95 | | MVW_PP | D5 | RW |
| | 16 | | CSD0_CNT_H | 56 | R | | 96 | | I2C0_CFG | D6 | RW |
| | 17 | | CSD0_CR1 | 57 | RW | | 97 | | I2C0_SCR | D7 | # |
| | 18 | | CSD1_DR0_L | 58 | R | | 98 | | I2C0_DR | D8 | RW |
| | 19 | | CSD1_DR1_L | 59 | W | | 99 | | I2C0_MSCR | D9 | # |
| | 1A | | CSD1_CNT_L | 5A | R | | 9A | | INT_CLR0 | DA | RW |
| | 1B | | CSD1_CR0 | 5B | # | | 9B | | INT_CLR1 | DB | RW |
| | 1C | | CSD1_DR0_H | 5C | R | | 9C | | INT_CLR2 | DC | RW |
| | 1D | | CSD1_DR1_H | 5D | W | | 9D | | INT_CLR3 | DD | RW |
| | 1E | | CSD1_CNT_H | 5E | R | | 9E | | INT_MSK3 | DE | RW |
| | 1F | | CSD1_CR1 | 5F | RW | | 9F | | INT_MSK2 | DF | RW |
| DBC00DR0 | 20 | # | AMX_IN | 60 | RW | | A0 | | INT_MSK0 | E0 | RW |
| DBC00DR1 | 21 | W | AMUX_CFG | 61 | RW | | A1 | | INT_MSK1 | E1 | RW |
| DBC00DR2 | 22 | RW | PWM_CR | 62 | RW | | A2 | | INT_VC | E2 | RC |
| DBC00CR0 | 23 | # | ARF_CR | 63 | RW | | A3 | | RES_WDT | E3 | W |
| DBC01DR0 | 24 | # | CMP_CR0 | 64 | # | | A4 | | | | |
| DBC01DR1 | 25 | W | ASY_CR | 65 | # | | A5 | | | | |
| DBC01DR2 | 26 | RW | CMP_CR1 | 66 | RW | | A6 | | DEC_CR0 | E6 | RW |
| DBC01CR0 | 27 | # | | 67 | | | A7 | | DEC_CR1 | E7 | RW |
| DCC02DR0 | 28 | # | ADC0_CR | 68 | # | | A8 | | MUL0_X | E8 | W |
| DCC02DR1 | 29 | W | ADC1_CR | 69 | # | | A9 | | MUL0_Y | E9 | W |
| DCC02DR2 | 2A | RW | SADC_DH | 6A | RW | | AA | | MUL0_DH | EA | R |
| DCC02CR0 | 2B | # | SADC_DL | 6B | RW | | AB | | MUL0_DL | EB | R |
| DCC03DR0 | 2C | # | TMP_DR0 | 6C | RW | | AC | | ACC0_DR1 | EC | RW |
| DCC03DR1 | 2D | W | TMP_DR1 | 6D | RW | | AD | | ACC0_DR0 | ED | RW |
| DCC03DR2 | 2E | RW | TMP_DR2 | 6E | RW | | AE | | ACC0_DR3 | EE | RW |
| DCC03CR0 | 2F | # | TMP_DR3 | 6F | RW | | AF | | ACC0_DR2 | EF | RW |
| DBC10DR0 | 30 | # | | 70 | | RDI0RI | B0 | RW | | F0 | |
| DBC10DR1 | 31 | W | | 71 | | RDI0SYN | B1 | RW | | F1 | |
| DBC10DR2 | 32 | RW | ACE00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| DBC10CR0 | 33 | # | ACE00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| DBC11DR0 | 34 | # | | 74 | | RDI0LT1 | B4 | RW | | F4 | |
| DBC11DR1 | 35 | W | | 75 | | RDI0RO0 | B5 | RW | | F5 | |
| DBC11DR2 | 36 | RW | ACE01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| DBC11CR0 | 37 | # | ACE01CR2 | 77 | RW | RDI0DSM | B7 | RW | CPU_F | F7 | RL |
| DCC12DR0 | 38 | # | | 78 | | RDI1RI | B8 | RW | | F8 | |
| DCC12DR1 | 39 | W | | 79 | | RDI1SYN | B9 | RW | | F9 | |
| DCC12DR2 | 3A | RW | | 7A | | RDI1IS | BA | RW | | FA | |
| DCC12CR0 | 3B | # | | 7B | | RDI1LT0 | BB | RW | | FB | |
| DCC13DR0 | 3C | # | | 7C | | RDI1LT1 | BC | RW | IDACR_D | FC | RW |
| DCC13DR1 | 3D | W | | 7D | | RDI1RO0 | BD | RW | IDACL_D | FD | RW |
| DCC13DR2 | 3E | RW | | 7E | | RDI1RO1 | BE | RW | CPU_SCR1 | FE | # |
| DCC13CR0 | 3F | # | | 7F | | RDI1DSM | BF | RW | CPU_SCR0 | FF | # |

Blank fields are Reserved and must not be accessed.

Access is bit specific.

Table 6. Register Map Bank 1 Table: Configuration Space

| Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access |
|----------|--------------|--------|------------|--------------|--------|--------------|--------------|--------|-----------|--------------|--------|
| PRT0DM0 | 00 | RW | | 40 | | ASE10CR0 | 80 | RW | | C0 | |
| PRT0DM1 | 01 | RW | | 41 | | | 81 | | | C1 | |
| PRT0IC0 | 02 | RW | | 42 | | | 82 | | | C2 | |
| PRT0IC1 | 03 | RW | | 43 | | | 83 | | | C3 | |
| PRT1DM0 | 04 | RW | | 44 | | ASE11CR0 | 84 | RW | | C4 | |
| PRT1DM1 | 05 | RW | | 45 | | | 85 | | | C5 | |
| PRT1IC0 | 06 | RW | | 46 | | | 86 | | | C6 | |
| PRT1IC1 | 07 | RW | | 47 | | | 87 | | | C7 | |
| PRT2DM0 | 08 | RW | | 48 | | | 88 | | | C8 | |
| PRT2DM1 | 09 | RW | | 49 | | | 89 | | | C9 | |
| PRT2IC0 | 0A | RW | | 4A | | | 8A | | | CA | |
| PRT2IC1 | 0B | RW | | 4B | | | 8B | | | CB | |
| PRT3DM0 | 0C | RW | | 4C | | | 8C | | | CC | |
| PRT3DM1 | 0D | RW | | 4D | | | 8D | | | CD | |
| PRT3IC0 | 0E | RW | | 4E | | | 8E | | | CE | |
| PRT3IC1 | 0F | RW | | 4F | | | 8F | | | CF | |
| PRT4DM0 | 10 | RW | CMP0CR1 | 50 | RW | | 90 | | GDI_O_IN | D0 | RW |
| PRT4DM1 | 11 | RW | CMP0CR2 | 51 | RW | | 91 | | GDI_E_IN | D1 | RW |
| PRT4IC0 | 12 | RW | | 52 | | | 92 | | GDI_O_OU | D2 | RW |
| PRT4IC1 | 13 | RW | VDAC50CR0 | 53 | RW | | 93 | | GDI_E_OU | D3 | RW |
| | 14 | | CMP1CR1 | 54 | RW | | 94 | | | D4 | |
| | 15 | | CMP1CR2 | 55 | RW | | 95 | | | D5 | |
| | 16 | | | 56 | | | 96 | | | D6 | |
| | 17 | | VDAC51CR0 | 57 | RW | | 97 | | | D7 | |
| | 18 | | CSCMPCR0 | 58 | # | | 98 | | MUX_CR0 | D8 | RW |
| | 19 | | CSCMPGOEN | 59 | RW | | 99 | | MUX_CR1 | D9 | RW |
| | 1A | | CSLUTCRO | 5A | RW | | 9A | | MUX_CR2 | DA | RW |
| | 1B | | CMPCOLMUX | 5B | RW | | 9B | | MUX_CR3 | DB | RW |
| | 1C | | CMPPWMCR | 5C | RW | | 9C | | DAC_CR1# | DC | RW |
| | 1D | | CMPFLTCR | 5D | RW | | 9D | | OSC_GO_EN | DD | RW |
| | 1E | | CMPCLK1 | 5E | RW | | 9E | | OSC_CR4 | DE | RW |
| | 1F | | CMPCLK0 | 5F | RW | | 9F | | OSC_CR3 | DF | RW |
| DBC00FN | 20 | RW | CLK_CR0 | 60 | RW | GDI_O_IN_CR | A0 | RW | OSC_CR0 | E0 | RW |
| DBC00IN | 21 | RW | CLK_CR1 | 61 | RW | GDI_E_IN_CR | A1 | RW | OSC_CR1 | E1 | RW |
| DBC00OU | 22 | RW | ABF_CR0 | 62 | RW | GDI_O_OU_CR | A2 | RW | OSC_CR2 | E2 | RW |
| DBC00CR1 | 23 | RW | AMD_CR0 | 63 | RW | GDI_E_OU_CR | A3 | RW | VLT_CR | E3 | RW |
| DBC01FN | 24 | RW | CMP_GO_EN | 64 | RW | RTC_H | A4 | RW | VLT_CMP | E4 | R |
| DBC01IN | 25 | RW | CMP_GO_EN1 | 65 | RW | RTC_M | A5 | RW | ADC0_TR | E5 | RW |
| DBC01OU | 26 | RW | AMD_CR1 | 66 | RW | RTC_S | A6 | RW | ADC1_TR | E6 | RW |
| DBC01CR1 | 27 | RW | ALT_CR0 | 67 | RW | RTC_CR | A7 | RW | V2BG_TR | E7 | RW |
| DCC02FN | 28 | RW | ALT_CR1 | 68 | RW | SADC_CR0 | A8 | RW | IMO_TR | E8 | W |
| DCC02IN | 29 | RW | CLK_CR2 | 69 | RW | SADC_CR1 | A9 | RW | ILO_TR | E9 | W |
| DCC02OU | 2A | RW | AMUX_CFG1 | 6A | RW | SADC_CR2 | AA | RW | BDG_TR | EA | RW |
| DBC02CR1 | 2B | RW | CLK_CR3 | 6B | RW | SADC_CR3TRIM | AB | RW | ECO_TR | EB | W |
| DCC03FN | 2C | RW | TMP_DR0 | 6C | RW | SADC_CR4 | AC | RW | MUX_CR4 | EC | RW |
| DCC03IN | 2D | RW | TMP_DR1 | 6D | RW | I2C0_AD | AD | RW | | ED | |
| DCC03OU | 2E | RW | TMP_DR2 | 6E | RW | | AE | | | EE | |
| DBC03CR1 | 2F | RW | TMP_DR3 | 6F | RW | | AF | | | EF | |
| DBC10FN | 30 | RW | | 70 | | RDI0RI | B0 | RW | | F0 | |
| DBC10IN | 31 | RW | | 71 | | RDI0SYN | B1 | RW | | F1 | |
| DBC10OU | 32 | RW | ACE00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| DBC10CR1 | 33 | RW | ACE00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| DBC11FN | 34 | RW | | 74 | | RDI0LT1 | B4 | RW | | F4 | |
| DBC11IN | 35 | RW | | 75 | | RDI0RO0 | B5 | RW | | F5 | |
| DBC11OU | 36 | RW | ACE01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| DBC11CR1 | 37 | RW | ACE01CR2 | 77 | RW | RDI0DSM | B7 | RW | CPU_F | F7 | RL |
| DCC12FN | 38 | RW | | 78 | | RDI1RI | B8 | RW | | F8 | |
| DCC12IN | 39 | RW | | 79 | | RDI1SYN | B9 | RW | | F9 | |
| DCC12OU | 3A | RW | | 7A | | RDI1IS | BA | RW | FLS_PR1 | FA | RW |
| DBC12CR1 | 3B | RW | | 7B | | RDI1LT0 | BB | RW | | FB | |
| DCC13FN | 3C | RW | | 7C | | RDI1LT1 | BC | RW | | FC | |
| DCC13IN | 3D | RW | | 7D | | RDI1RO0 | BD | RW | DAC_CR0# | FD | RW |
| DCC13OU | 3E | RW | | 7E | | RDI1RO1 | BE | RW | CPU_SCR1 | FE | # |
| DBC13CR1 | 3F | RW | | 7F | | RDI1DSM | BF | RW | CPU_SCR0 | FF | # |

Blank fields are Reserved and must not be accessed.

Access is bit specific.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 7. Absolute Maximum Ratings

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-----------------------|--|-----------------------|--------|-----------------------|----------|---|
| T _{STG} | Storage temperature | -55 | 25 | +150 | °C | Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ±25 °C. Time spent in storage at a temperature greater than 65 °C counts toward the Flash _{DR} electrical specification in Table 16 on page 20 . |
| T _{BAKETEMP} | Bake temperature | - | 125 | See package label | °C | |
| t _{BAKETIME} | Bake time | See package label | - | 72 | Hours | |
| T _A | Ambient temperature with power applied A-grade devices E-grade devices | -40 -40 | - - | +85 +125 | °C °C | |
| V _{DD} | Supply voltage on V _{DD} relative to V _{SS} | -0.5 | - | +6.0 | V | |
| V _{IO} | DC input voltage | V _{SS} - 0.5 | - | V _{DD} + 0.5 | V | |
| V _{IOz} | DC voltage applied to tristate | V _{SS} - 0.5 | - | V _{DD} + 0.5 | V | |
| I _{MIO} | Maximum current into any port pin | -25 | - | +50 | mA | |
| ESD | Electrostatic discharge voltage | 2000 | - | - | V | Human body model ESD |
| LU | Latch up current | - | - | 200 | mA | |

Operating Temperature

Table 8. Operating Temperature

| Symbol | Description | Min | Typ | Max | Units | Notes |
|----------------|--|------------|--------|--------------|----------|---|
| T _A | Ambient temperature A-grade devices E-grade devices | -40 -40 | - - | +85 +125 | °C °C | |
| T _J | Junction temperature A-grade devices E-grade devices | -40 -40 | - - | +100 +135 | °C °C | The temperature rise from ambient to junction is package specific. See Table 27 on page 34 . The user must limit the power consumption to comply with this requirement. |

Electrical Specifications

This section presents the DC and AC electrical specifications for automotive CY8C21x45 and CY8C22x45 PSoC devices. For the latest electrical specifications, check the most recent data sheet by visiting the web at <http://www.cypress.com>.

Specifications are valid for A-grade devices at $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, $T_J \leq 100\text{ }^{\circ}\text{C}$, and for E-grade devices at $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$, $T_J \leq 135\text{ }^{\circ}\text{C}$, unless noted otherwise.

Figure 5. Voltage vs. CPU Frequency for A-grade Devices

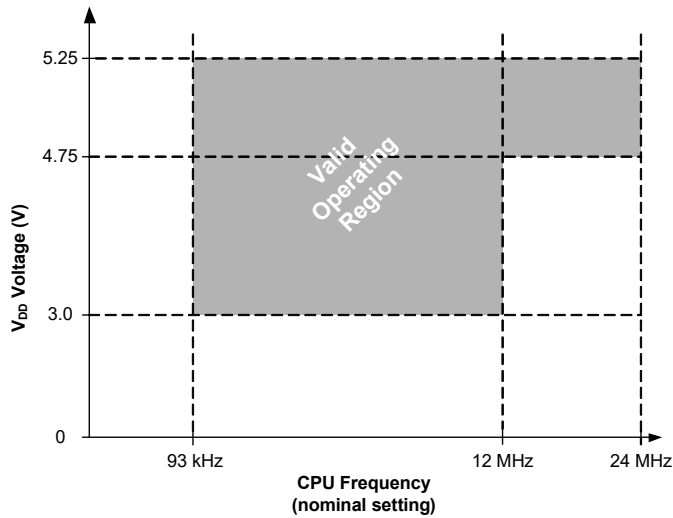


Figure 6. Voltage vs. CPU Frequency for E-grade Devices

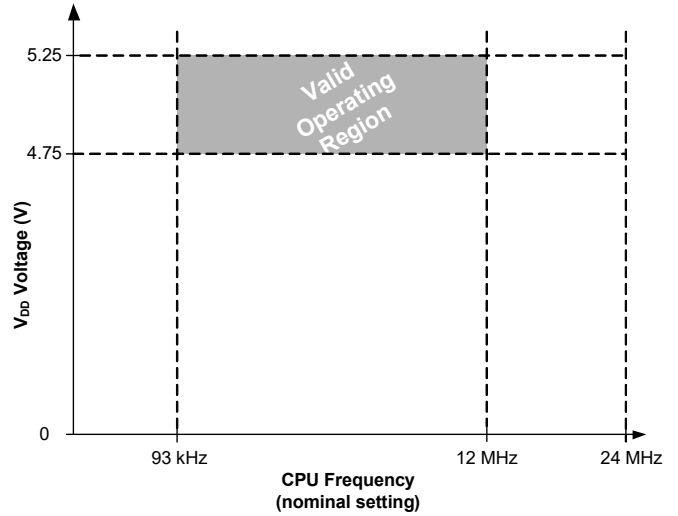
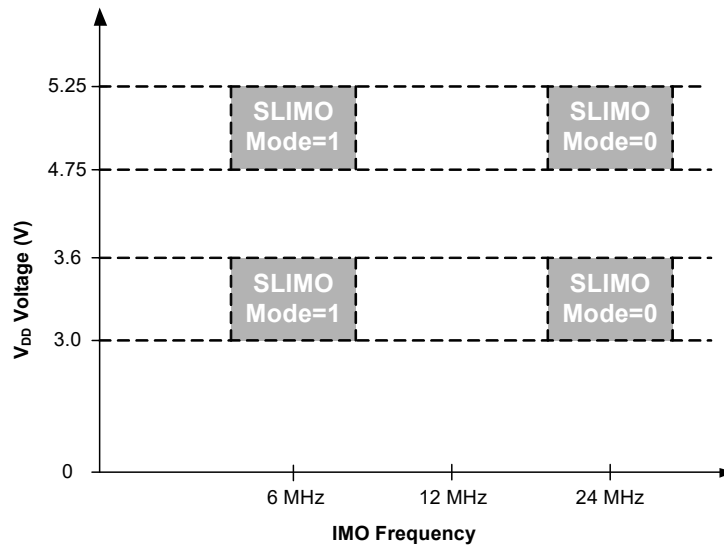


Figure 7. IMO Frequency Trim Options (A-grade Devices Only)



DC Electrical Characteristics

DC Chip Level Specifications

Table 9 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40°C to 85°C , or 3.0 V to 3.6 V and -40°C to 85°C . Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40°C to 125°C . Typical parameters apply to 5 V and 3.3 V at 25°C , unless specified otherwise, and are for design guidance only.

Table 9. DC Chip Level Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------|--|-------------|-------------|----------------|---|--|
| V_{DD} | Supply voltage A-grade devices E-grade devices | 3.0 4.75 | – – | 5.25 5.25 | V V | See Table 15 on page 19 |
| I_{DD} | Supply current A-grade devices, $3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ A-grade devices, $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$ E-grade devices | – – – | 4 7 8 | 7 12 15 | mA mA mA | CPU = 3 MHz, 48 MHz disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, Analog blocks disabled |
| I_{SB} | Sleep (mode) current A-grade devices, $3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ A-grade devices, $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$ E-grade devices | – – – | 3 4 4 | 12 25 25 | μA μA μA | Everything disabled except ILO, POR, LVD, Sleep Timer, and WDT circuits |
| I_{SBXTL} | Sleep (mode) current with ECO A-grade devices, $3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ A-grade devices, $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$ E-grade devices | – – – | 4 5 5 | 13 26 26 | μA μA μA | Everything disabled except ECO, POR, LVD, Sleep Timer, and WDT circuits |
| V_{REF} | Reference voltage (Bandgap) | 1.275 | 1.30 | 1.325 | V | Trimmed for appropriate V_{DD} setting. |

DC GPIO Specifications

Table 10 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 85 °C, or 3.0 V to 3.6 V and -40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 10. DC GPIO Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|------------------|-----------------------------------|-----------------------|-----|------|-------|---|
| R _{PU} | Pull-up resistor | 4 | 5.6 | 8 | kΩ | |
| R _{PD} | Pull-down resistor | 4 | 5.6 | 8 | kΩ | Also applies to the internal pull-down resistor on the XRES pin |
| V _{OH} | High output level | V _{DD} - 1.0 | – | – | V | I _{OH} = 10 mA, V _{DD} = 4.75 to 5.25 V (80 mA maximum combined I _{OH} budget) |
| V _{OL} | Low output level | – | – | 0.75 | V | I _{OL} = 25 mA, V _{DD} = 4.75 to 5.25 V (100 mA maximum combined I _{OL} budget) |
| | | – | – | 0.65 | V | I _{OL} = 5 mA, V _{DD} = 3.0 to 3.6 V |
| I _{OH} | High-level source current | 10 | – | – | mA | V _{OH} ≥ V _{DD} - 1.0 V, see the limitations of the total current in the note for V _{OH} . |
| I _{OL} | Low-level sink current | 25 | – | – | mA | V _{OL} ≤ 0.75 V, see the limitations of the total current in the note for V _{OL} . |
| V _{IL} | Input low level | – | – | 0.8 | V | |
| V _{IH} | Input high level | 2.1 | – | – | V | |
| V _H | Input hysteresis | – | 60 | – | mV | |
| I _{IL} | Input leakage (absolute value) | – | 1 | – | nA | Gross tested to 1 μA |
| C _{IN} | Capacitive load on pins as input | – | 3.5 | 10 | pF | Package and pin dependent. T _A = 25 °C |
| C _{OUT} | Capacitive load on pins as output | – | 3.5 | 10 | pF | Package and pin dependent. T _A = 25 °C |

DC Operational Amplifier Specifications

The following table lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40°C to 85°C , or 3.0 V to 3.6 V and -40°C to 85°C . Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40°C to 125°C . Typical parameters apply to 5 V and 3.3 V at 25°C , unless specified otherwise, and are for design guidance only.

Table 11. DC Operational Amplifier Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|----------------------------|---|--------|--------|---------------------|--------------------------------|--|
| V_{OSOA} | Input offset voltage (absolute value) | – | 2.5 | 15 | mV | |
| I_{SOA} | Supply current (absolute value) A-grade devices E-grade devices | – – | – – | 30 35 | μA μA | |
| TCV_{OSOA} | Average input offset voltage drift | – | 10 | – | $\mu\text{V}/^{\circ}\text{C}$ | |
| $I_{\text{EBOA}}^{[7]}$ | Input leakage current (Port 0 analog pins) | – | 200 | – | pA | Gross tested to $1\ \mu\text{A}$ |
| C_{INOA} | Input capacitance (Port 0 analog pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. $T_A = 25^{\circ}\text{C}$ |
| V_{CMOA} | Common mode voltage range | 0.5 | – | $V_{\text{DD}} - 1$ | V | |

DC IDAC Specifications

The following table lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40°C to 85°C , or 3.0 V to 3.6 V and -40°C to 85°C . Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40°C to 85°C . Typical parameters apply to 5 V and 3.3 V at 25°C , unless specified otherwise, and are for design guidance only.

Table 12. DC IDAC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|----------------------------------|--|-----|------|------|---------------|---|
| $\text{IDAC}_{\text{GAIN}}$ | IDAC gain | – | 75.4 | 218 | nA/bit | IDAC gain at 1x current gain |
| | | – | 335 | 693 | nA/bit | IDAC gain at 4x current gain |
| | | – | 1160 | 2410 | nA/bit | IDAC gain at 16x current gain |
| | | – | 2340 | 5700 | nA/bit | IDAC gain at 32x current gain |
| | Monotonicity | No | – | – | – | IDAC gain is non-monotonous at step intervals of (0x10) |
| $\text{IDAC}_{\text{GAIN_VAR}}$ | IDAC gain variation over temperature -40°C to 85°C | – | 3.22 | – | nA | at 1x current gain |
| | | – | 18.1 | – | nA | at 4x current gain |
| | | – | 59.9 | – | nA | at 16x current gain |
| | | – | 120 | – | nA | at 32x current gain |
| I_{IDAC} | IDAC current at maximum code (0xFF) | – | 19.2 | – | μA | at 1x current gain |
| | | – | 85.4 | – | μA | at 4x current gain |
| | | – | 295 | – | μA | at 16x current gain |
| | | – | 596 | – | μA | at 32x current gain |

Note

7. Atypical behavior: I_{EBOA} of Port 0 Pin 0 is below 1 nA at 25°C ; 50 nA over temperature. Use Port 0 Pins 1 – 7 for the lowest leakage of 200 nA.

DC SAR10 ADC Specifications

Table 13 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 85 °C, or 3.0 V to 3.6 V and -40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 13. DC SAR10 ADC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------|---|--------------|--------|------------|----------------|--|
| V _{ADCREF} | Reference voltage at pin P2[5] when configured as ADC reference voltage | 3.0 | – | 5.25 | V | When V _{REF} is buffered inside ADC, the voltage level at P2[5] (when configured as ADC reference voltage) must be always maintained to be at least 300 mV less than the chip supply voltage level on V _{DD} pin. (V _{ADCREF} < V _{DD}) |
| I _{ADCREF} | Current into P2[5] when configured as ADC V _{REF} | – | – | 100 | µA | Disables the internal voltage reference buffer |
| INL _{ADC} | Integral nonlinearity A-grade devices E-grade devices | -3.0 -5.0 | – – | 3.0 5.0 | LSbit LSbit | 10-bit resolution |
| DNL _{ADC} | Differential nonlinearity A-grade devices E-grade devices | -1.5 -4.0 | – – | 1.5 4.0 | LSbit LSbit | 10-bit resolution |

DC Analog Mux Bus Specifications

Table 14 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 85 °C, or 3.0 V to 3.6 V and -40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 14. DC Analog Mux Bus Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|------------------|--|-----|-----|-----|-------|-------|
| R _{SW} | Switch resistance to common analog bus | – | – | 400 | Ω | |
| R _{GND} | Resistance of initialization switch to GND | – | – | 800 | Ω | |

DC POR and LVD Specifications

Table 15 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 85 °C, or 3.0 V to 3.6 V and -40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 15. DC POR and LVD Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--|---|--|--|--|----------------------------|--|
| V_{PPOR1} V_{PPOR2} | V_{DD} value for PPOR trip PORLEV[1:0] = 01b PORLEV[1:0] = 10b | – – | 2.82 4.55 | 2.95 4.73 | V V | V_{DD} must be greater than or equal to 3.0 V during startup, reset from the XRES pin, or reset from Watchdog. |
| V_{LVD2} V_{LVD3} V_{LVD4} V_{LVD5} V_{LVD6} V_{LVD7} | V_{DD} value for LVD trip VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b | 2.95 3.06 4.37 4.50 4.62 4.71 | 3.02 3.13 4.48 4.64 4.73 4.81 | 3.09 3.20 4.55 4.75 4.83 4.95 | V V V V V V | |

DC Programming Specifications

Table 16 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 16. DC Programming Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes | |
|-----------------------|---|---------------------------|---------|-----------------|-------|--|--|
| V _{DDP} | V _{DD} for programming and erase | 4.5 | 5 | 5.5 | V | This specification applies to the functional requirements of external programmer tools | |
| V _{DDL} | Low V _{DD} for verify | A-grade devices | 3.0 | 3.1 | 3.2 | V | This specification applies to the functional requirements of external programmer tools |
| | | E-grade devices | 4.7 | 4.8 | 4.9 | V | |
| V _{DDHV} | High V _{DD} for verify | 5.1 | 5.2 | 5.3 | V | This specification applies to the functional requirements of external programmer tools | |
| V _{DDIWRITE} | Supply voltage for flash write operation | A-grade devices | 3.0 | – | 5.25 | V | This specification applies to this device when it is executing internal flash writes |
| | | E-grade devices | 4.75 | – | 5.25 | V | |
| I _{DDP} | Supply current during programming or verify | – | 5 | 25 | mA | | |
| V _{ILP} | Input low voltage during programming or verify | – | – | 0.8 | V | | |
| V _{IHP} | Input high voltage during programming or verify | 2.2 | – | – | V | | |
| I _{ILP} | Input current when applying V _{ILP} to P1[0] or P1[1] during programming or verify | – | – | 0.2 | mA | Driving internal pull-down resistor | |
| I _{IHP} | Input current when applying V _{IHP} to P1[0] or P1[1] during programming or verify | – | – | 1.5 | mA | Driving internal pull-down resistor | |
| V _{OLV} | Output low voltage during programming or verify | – | – | 0.75 | V | | |
| V _{OHV} | Output high voltage during programming or verify | V _{DD} – 1.0 | – | V _{DD} | V | | |
| Flash _{ENPB} | Flash endurance (per block) [8, 9] | A-grade devices | 1,000 | – | – | – | Erase/write cycles per block |
| | | E-grade devices | 100 | – | – | – | |
| Flash _{ENT} | Flash endurance (total) [9, 10] | CY8C21x45 A-grade devices | 128,000 | – | – | – | Erase/write cycles |
| | | CY8C22x45 A-grade devices | 256,000 | – | – | – | |
| | | CY8C21x45 E-grade devices | 12,800 | – | – | – | |
| | | CY8C22x45 E-grade devices | 25,600 | – | – | – | |
| | | | | | | | |
| Flash _{DR} | Flash data retention [9] | A-grade devices | 10 | – | – | Years | |
| | | E-grade devices | 10 | – | – | Years | |

Notes

8. The erase/write cycle limit per block (Flash_{ENPB}) is only guaranteed if the device operates within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.
9. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.
10. The maximum total number of allowed erase/write cycles is the minimum Flash_{ENPB} value multiplied by the number of flash blocks in the device.

AC Electrical Characteristics

AC Chip Level Specifications

The following tables list the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 85 °C, or 3.0 V to 3.6 V and -40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 17. AC Chip-Level Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-----------------------|--|-------|------|--------------------------|-------|---|
| F _{IMO24} | Internal main oscillator frequency for 24 MHz A-grade devices, 4.75 V ≤ V _{DD} ≤ 5.25 V | 22.8 | 24 | 25.2 ^[11] | MHz | Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 7 on page 14 . |
| | A-grade devices, 3.0 V ≤ V _{DD} ≤ 3.6 V | 22.5 | 24 | 25.5 ^[11] | MHz | |
| | E-grade devices | 22.3 | 24 | 25.7 ^[11] | MHz | |
| F _{IMO6} | Internal main oscillator frequency for 6 MHz A-grade devices | 5.5 | 6 | 6.5 ^[11] | MHz | Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 7 on page 14 . |
| | E-grade devices | 5.5 | 6 | 6.5 ^[11] | MHz | |
| F _{CPU1} | CPU frequency (5 V V _{DD} operation) A-grade devices E-grade devices | 0.089 | – | 25.2 ^[11] | MHz | SLIMO mode = 0. |
| | | 0.089 | – | 12.6 ^[11] | MHz | |
| F _{CPU2} | CPU frequency (3.3 V V _{DD} operation) | 0.089 | – | 12.6 ^[11] | MHz | A-grade devices only. SLIMO mode = 0. |
| F _{BLK5} | Digital PSoC block frequency (5 V V _{DD} operation) A-grade devices E-grade devices | 0 | 48 | 50.4 ^[11, 12] | MHz | Refer to Table 20 on page 24 . |
| | | 0 | 24 | 25.2 ^[11, 12] | MHz | |
| F _{BLK33} | Digital PSoC block frequency (3.3 V V _{DD} operation) | 0 | 24 | 24.6 ^[11] | MHz | A-grade devices only |
| F _{32K1} | ILO frequency | 15 | 32 | 75 | kHz | This specification applies when the ILO has been trimmed. |
| F _{32KU} | ILO untrimmed frequency | 5 | – | 100 | kHz | After a reset and before the M8C processor starts to execute, the ILO is not trimmed. |
| t _{XRST} | External reset pulse width | 10 | – | – | μs | |
| DC _{24M} | 24 MHz duty cycle | 40 | 50 | 60 | % | |
| DC _{ILO} | ILO duty cycle | 20 | 50 | 80 | % | |
| F _{out48M} | 48 MHz output frequency | 45.6 | 48.0 | 50.4 ^[11] | MHz | |
| F _{MAX} | Maximum frequency of signal on row input or row output | – | – | 12.6 | MHz | |
| SR _{POWERUP} | Power supply slew rate | – | – | 250 | V/ms | V _{DD} slew rate during power-up. |
| t _{POWERUP} | Time between end of POR state and CPU code execution | – | 16 | 100 | ms | Power-up from 0 V. |

Notes

11. Accuracy derived from IMO with appropriate trim for V_{DD} range
12. Refer to the individual user module data sheets for information on maximum frequencies for user modules.

Table 17. AC Chip-Level Specifications (continued)

| Symbol | Description | Min | Typ | Max | Units | Notes |
|------------------------------|--|-----|-----|------|-------|--------|
| $t_{\text{JIT_IMO}}^{[13]}$ | 24 MHz IMO cycle-to-cycle jitter (RMS) | – | 200 | 700 | ps | |
| | 24 MHz IMO long term N cycle-to-cycle jitter (RMS) | – | 300 | 900 | ps | N = 32 |
| | 24 MHz IMO period jitter (RMS) | – | 100 | 400 | ps | |
| $t_{\text{JIT_PLL}}^{[13]}$ | PLL cycle-to-cycle jitter (RMS) | – | 200 | 800 | ps | |
| | PLL long term N cycle-to-cycle jitter (RMS) | – | 300 | 1200 | ps | N = 32 |
| | PLL period jitter (RMS) | – | 100 | 700 | ps | |

Note

 13. Refer to Cypress Jitter Specifications document, [Understanding Datasheet Jitter Specifications for Cypress Timing Products](#) for more information.

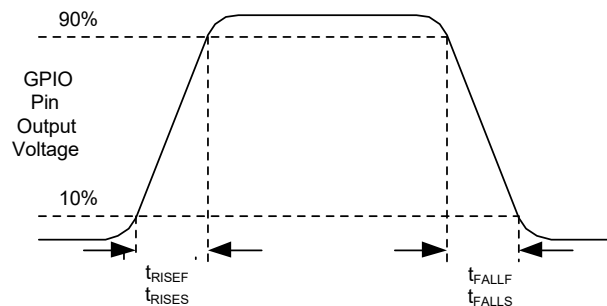
AC GPIO Specifications

Table 18 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 85 °C, or 3.0 V to 3.6 V and -40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 18. AC GPIO Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------|---|--------|----------|----------|----------|--------------------|
| f_{GPIO} | GPIO operating frequency | 0 | – | 12.6 | MHz | Normal strong mode |
| t_{RISEF} | Rise time, normal strong mode, Load = 50 pF A-grade devices E-grade devices | 3 3 | – – | 18 24 | ns ns | Refer to Figure 8 |
| t_{FALLF} | Fall time, normal strong mode, Load = 50 pF A-grade devices E-grade devices | 2 2 | – – | 18 28 | ns ns | Refer to Figure 8 |
| t_{RISES} | Rise time, slow strong mode, Load = 50 pF A-grade devices E-grade devices | 7 7 | 27 32 | – – | ns ns | Refer to Figure 8 |
| t_{FALLS} | Fall time, slow strong mode, Load = 50 pF A-grade devices E-grade devices | 7 7 | 22 28 | – – | ns ns | Refer to Figure 8 |

Figure 8. GPIO Timing Diagram



AC Operational Amplifier Specifications

Table 19 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 85 °C, or 3.0 V to 3.6 V and -40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 19. AC Operational Amplifier Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|------------|--------------------------------------|-----|-----|-----|-------|-------|
| t_{COMP} | Comparator mode response time, 50 mV | – | – | 100 | ns | |

AC Digital Block Specifications

The following tables list the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 85 °C, or 3.0 V to 3.6 V and -40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 20. AC Digital Block Specifications

| Function | Description | Min | Typ | Max | Units | Notes |
|-------------------|--|--------------------|-----|----------------------|-------|---|
| All functions | Block Input Clock Frequency | | | | | |
| | $V_{DD} \geq 4.75\text{ V}$ | – | – | 50.4 ^[15] | MHz | |
| | $V_{DD} < 4.75\text{ V}$ | – | – | 25.2 ^[15] | MHz | |
| Timer | Input Clock Frequency | | | | | |
| | No Capture, $V_{DD} \geq 4.75\text{ V}$ | – | – | 50.4 ^[15] | MHz | |
| | No Capture, $V_{DD} < 4.75\text{ V}$ | – | – | 25.2 ^[15] | MHz | |
| | With Capture | – | – | 25.2 ^[15] | MHz | |
| | Capture Pulse Width | 50 ^[14] | – | – | ns | |
| Counter | Input Clock Frequency | | | | | |
| | No Enable Input, $V_{DD} \geq 4.75\text{ V}$ | – | – | 50.4 ^[15] | MHz | |
| | No Enable Input, $V_{DD} < 4.75\text{ V}$ | – | – | 25.2 ^[15] | MHz | |
| | With Enable Input | – | – | 25.2 ^[15] | MHz | |
| | Enable Input Pulse Width | 50 ^[14] | – | – | ns | |
| Dead Band | Kill Pulse Width | | | | | |
| | Asynchronous Restart Mode | 20 | – | – | ns | |
| | Synchronous Restart Mode | 50 ^[14] | – | – | ns | |
| | Disable Mode | 50 ^[14] | – | – | ns | |
| | Input Clock Frequency | | | | | |
| | $V_{DD} \geq 4.75\text{ V}$ | – | – | 50.4 ^[15] | MHz | |
| | $V_{DD} < 4.75\text{ V}$ | – | – | 25.2 ^[15] | MHz | |
| CRCPRS (PRS Mode) | Input Clock Frequency | | | | | |
| | $V_{DD} \geq 4.75\text{ V}$ | – | – | 50.4 ^[15] | MHz | |
| | $V_{DD} < 4.75\text{ V}$ | – | – | 25.2 ^[15] | MHz | |
| CRCPRS (CRC Mode) | Input Clock Frequency | – | – | 25.2 ^[15] | MHz | |
| SPIM | Input Clock Frequency | – | – | 8.4 ^[15] | MHz | The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2. |
| SPIS | Input Clock (SCLK) Frequency | – | – | 4.2 ^[15] | MHz | The input clock is the SPI SCLK in SPIS mode. |
| | Width of SS_Negated Between Transmissions | 50 ^[14] | – | – | ns | |

Note

14. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

Table 20. AC Digital Block Specifications (continued)

| Function | Description | Min | Typ | Max | Units | Notes |
|-------------|-----------------------------------|-----|-----|----------------------|-------|---|
| Transmitter | Input Clock Frequency | | | | | The baud rate is equal to the input clock frequency divided by 8. |
| | $V_{DD} \geq 4.75$ V, 2 Stop Bits | – | – | 50.4 ^[15] | MHz | |
| | $V_{DD} \geq 4.75$ V, 1 Stop Bit | – | – | 25.2 ^[15] | MHz | |
| | $V_{DD} < 4.75$ V | – | – | 25.2 ^[15] | MHz | |
| Receiver | Input Clock Frequency | | | | | The baud rate is equal to the input clock frequency divided by 8. |
| | $V_{DD} \geq 4.75$ V, 2 Stop Bits | – | – | 50.4 ^[15] | MHz | |
| | $V_{DD} \geq 4.75$ V, 1 Stop Bit | – | – | 25.2 ^[15] | MHz | |
| | $V_{DD} < 4.75$ V | – | – | 25.2 ^[15] | MHz | |

Note

 15. Accuracy derived from IMO with appropriate trim for V_{DD} range.

AC External Clock Specifications

The following tables list the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 21. AC External Clock Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------|------------------------|-------|-----|------|-------|-------|
| F _{OSCEXT} | Frequency | 0.093 | – | 24.6 | MHz | |
| – | High period | 20.0 | – | 5300 | ns | |
| – | Low period | 20.0 | – | – | ns | |
| – | Power-up IMO to switch | 150 | – | – | μs | |

AC SAR10 ADC Specifications

Table 22 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 22. AC SAR10 ADC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------------|-------------------------------|-----|-----|-----|-------|--|
| F _{INADC} | SAR ADC input clock frequency | – | – | 2 | MHz | The sample rate of the SAR10 ADC is equal to F _{INADC} divided by 13. |

AC Programming Specifications

Table 23 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 85 °C, or 3.0 V to 3.6 V and -40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 23. AC Programming Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------|---|-----|-----|---------------------|-------|--|
| t_{RSCLK} | Rise time of SCLK | 1 | – | 20 | ns | |
| t_{FSCLK} | Fall time of SCLK | 1 | – | 20 | ns | |
| t_{SSCLK} | Data setup time to falling edge of SCLK | 40 | – | – | ns | |
| t_{HSCLK} | Data hold time from falling edge of SCLK | 40 | – | – | ns | |
| F_{SCLK} | Frequency of SCLK | 0 | – | 8 | MHz | |
| F_{SCLK3} | Frequency of SCLK | 0 | – | 6 | MHz | $V_{DD} \leq 3.6$ V |
| t_{ERASEB} | Flash erase time (block) | – | 10 | 40 ^[16] | ms | |
| t_{WRITE} | Flash block write time | – | 40 | 160 ^[16] | ms | |
| t_{DSCLK} | Data out delay from falling edge of SCLK | – | – | 55 | ns | $V_{DD} > 3.6$ V, 30 pF load |
| t_{DSCLK3} | Data out delay from falling edge of SCLK | – | – | 65 | ns | 3.0 V $\leq V_{DD} \leq 3.6$ V, 30 pF load |
| t_{PRGH} | Total flash block program time ($t_{ERASEB} + t_{WRITE}$), hot | – | – | 100 ^[16] | ms | $T_J \geq 0$ °C |
| t_{PRGC} | Total flash block program time ($t_{ERASEB} + t_{WRITE}$), cold | – | – | 200 ^[16] | ms | $T_J < 0$ °C |

Note

16. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note [AN2015](#) for more information.

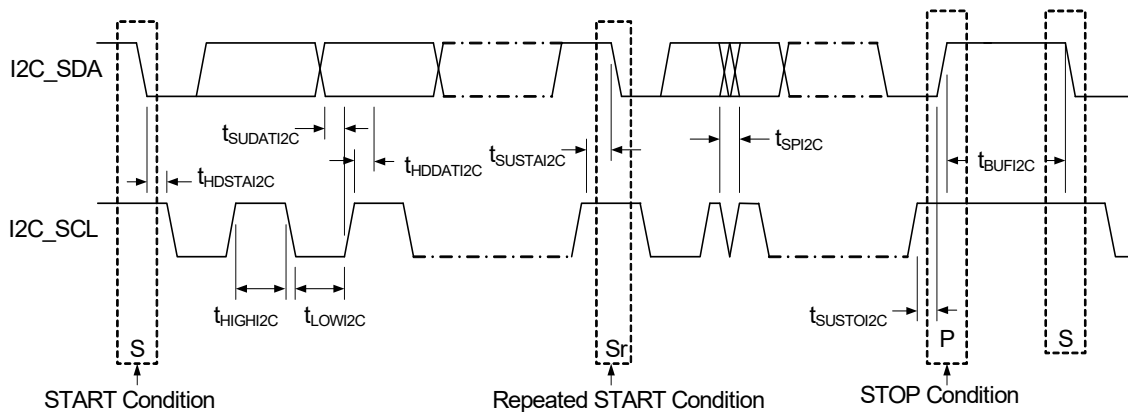
AC I²C Specifications

Table 24 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 85 °C, or 3.0 V to 3.6 V and -40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 24. AC Characteristics of the I²C SDA and SCL Pins

| Symbol | Description | Standard Mode | | Fast Mode | | Units |
|-----------------------|--|---------------|----------|-----------|----------|-------|
| | | Min | Max | Min | Max | |
| F _{SCL I2C} | SCL clock frequency | 0 | 100 [17] | 0 | 400 [17] | kHz |
| t _{HDSTAI2C} | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 4.0 | – | 0.6 | – | μs |
| t _{LOWI2C} | LOW period of the SCL clock | 4.7 | – | 1.3 | – | μs |
| t _{HIGHI2C} | HIGH period of the SCL clock | 4.0 | – | 0.6 | – | μs |
| t _{SUSTAI2C} | Setup time for a repeated START condition | 4.7 | – | 0.6 | – | μs |
| t _{HDDATI2C} | Data hold time | 0 | – | 0 | – | μs |
| t _{SUDATI2C} | Data setup time | 250 | – | 100 [18] | – | ns |
| t _{SUSTOI2C} | Setup time for STOP condition | 4.0 | – | 0.6 | – | μs |
| t _{BUFI2C} | Bus-free time between a STOP and START condition | 4.7 | – | 1.3 | – | μs |
| t _{SPI2C} | Pulse width of spikes are suppressed by the input filter | – | – | 0 | 50 | ns |

Figure 9. Definition for Timing for Fast/Standard Mode on the I²C Bus



Notes

- F_{SCL I2C} is derived from SysClk of the PSoC. This specification assumes that SysClk is operating at 24 MHz, nominal. If SysClk is at a lower frequency, then the F_{SCL I2C} specification adjusts accordingly.
- A Fast-Mode I²C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement t_{SUDATI2C} ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + t_{SUDATI2C} = 1000 + 250 = 1250 ns (according to the standard-mode I²C-bus specification) before the SCL line is released.

Development Tool Selection

This section presents the development tools available for the automotive CY8C21x45 and CY8C22x45 families.

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for years. PSoC Designer is available free of charge at <http://www.cypress.com>. PSoC Designer comes with a free C compiler.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at <http://www.cypress.com>.

Development Kits

All development kits can be purchased from the Cypress Online Store. The online store also has the most up to date information on kit contents, descriptions, and availability.

CY3215-DK Basic Development Kit

The **CY3215-DK** is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface allows users to run, halt, and single step the processor and view the contents of specific memory locations. Advanced emulation features are also supported through PSoC Designer. The kit includes:

- ICE-Cube unit
- 28-pin PDIP emulation pod for CY8C29466-24PXI
- 28-pin CY8C29466-24PXI PDIP PSoC device samples (two)
- PSoC Designer software CD
- ISSP cable
- MiniEval socket programming and evaluation board
- Backward compatibility cable (for connecting to legacy pods)
- Universal 110/220 power supply (12 V)
- European plug adapter
- USB 2.0 cable
- Getting Started guide
- Development kit registration form

CY3280-22X45 Universal CapSense Controller Board

The **CY3280-22X45** controller board is an additional controller board for the **CY3280-BK1 Universal CapSense Controller Kit**. The Universal CapSense Controller kit is designed for easy prototyping and debug of CapSense designs with pre-defined control circuitry and plug-in hardware. The CY3280-22X45 kit contains no plug-in hardware. Therefore, it is only usable if plug-in hardware is purchased as part of the CY3280-BK1 kit or other separate kits. The kit includes:

- CY3280-22X45 universal CapSense controller board
- CY3280-22X45 universal CapSense controller board CD
- DC power supply
- Printed documentation

CY3280-CPM1 CapSensePlus Module

The **CY3280-CPM1 CapSensePlus Module** is a plug-in module board for the CY3280-22X45 CapSense controller board kit. This plug-in module has no capacitive sensors on it. Instead, it has other general circuitry (such as a seven-segment display, potentiometer, LEDs, buttons, thermistor) that can be used to develop applications that require capacitive sensing along with other additional functionality. To use this kit, a CY3280-22X45 kit is required.

Evaluation Tools

All evaluation tools can be purchased from the Cypress online store. The online store also has the most up-to-date information on kit contents, descriptions, and availability.

CY3210-PSoCEval1

The **CY3210-PSoCEval1 kit** features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, an RS-232 port, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- 28-pin CY8C29466-24PXI PDIP PSoC device sample (two)
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3210-MiniProg1

The **CY3210-MiniProg1** kit allows the user to program PSoC devices through the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC through a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-pin CY8C29466-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

Accessories (Emulation and Programming)

Table 25. Emulation and Programming Accessories

| Part Number | Pin Package | Pod Kit ^[19] | Foot Kit ^[20] | Prototyping Module | Adapter ^[21] |
|---|-------------|-------------------------|--------------------------|--------------------|-------------------------|
| CY8C21345-24PVXA CY8C21345-12PVXE CY8C22345-24PVXA CY8C22345H-24PVXA CY8C22345-12PVXE | 28-pin SSOP | CY3250-22345 | CY3250-28SSOP-FK | – | AS-28-28-02SS-6ENP-GANG |
| CY8C21645-24PVXA CY8C21645-12PVXE CY8C22645-24PVXA CY8C22645-12PVXE | 48-pin SSOP | – | – | – | AS-48-48-01SS-6-GANG |

CY3207ISSP In-System Serial Programmer

The **CY3207ISSP** is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note CY3207ISSP needs special software and is not compatible with PSoC Programmer. This software is free and can be downloaded from <http://www.cypress.com>. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240-V power supply, Euro-Plug adapter
- USB 2.0 cable

Notes

19. Pod kit contains an emulation pod, a flex-cable (connects the pod to the ICE), two feet, and device samples.

20. Foot kit includes surface mount feet that can be soldered to the target PCB.

21. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at <http://www.emulation.com>.

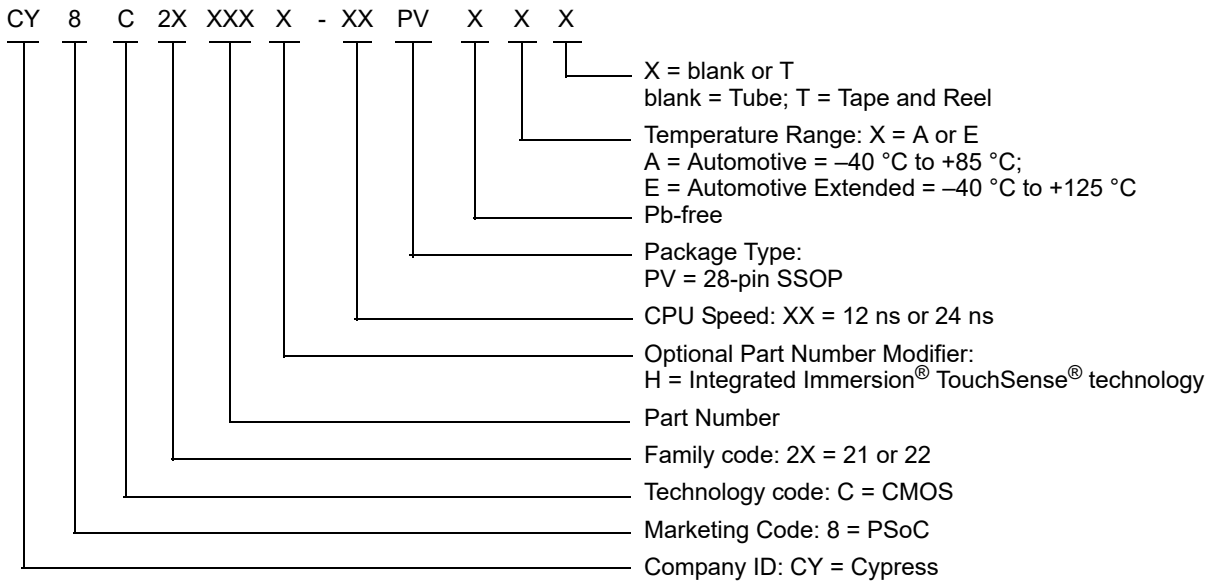
Ordering Information

The following table lists the key package features and ordering codes of the automotive CY8C21x45 and CY8C22x45 device families.

Table 26. PSoC Device Family Key Features and Ordering Information

| Package | Ordering Code | Flash (Bytes) | SRAM (Bytes) | Temperature Range | Digital Blocks | Analog Blocks | Digital I/O Pins | Analog Inputs | Analog Outputs | XRES Pin |
|---------------------------------------|--------------------|---------------|--------------|-------------------|----------------|---------------|------------------|---------------|----------------|----------|
| 28-pin (210-Mil) SSOP | CY8C21345-24PVXA | 8 K | 512 | -40 °C to +85 °C | 4 | 6 | 24 | 24 | 0 | Yes |
| 28-pin (210-Mil) SSOP (Tape and Reel) | CY8C21345-24PVXAT | 8 K | 512 | -40 °C to +85 °C | 4 | 6 | 24 | 24 | 0 | Yes |
| 28-pin (210-Mil) SSOP | CY8C21345-12PVXE | 8 K | 512 | -40 °C to +125 °C | 4 | 6 | 24 | 24 | 0 | Yes |
| 28-pin (210-Mil) SSOP (Tape and Reel) | CY8C21345-12PVXET | 8 K | 512 | -40 °C to +125 °C | 4 | 6 | 24 | 24 | 0 | Yes |
| 28-pin (210-Mil) SSOP | CY8C22345-24PVXA | 16 K | 1 K | -40 °C to +85 °C | 8 | 6 | 24 | 24 | 0 | Yes |
| 28-pin (210-Mil) SSOP (Tape and Reel) | CY8C22345-24PVXAT | 16 K | 1 K | -40 °C to +85 °C | 8 | 6 | 24 | 24 | 0 | Yes |
| 28-pin (210-Mil) SSOP | CY8C22345H-24PVXA | 16 K | 1 K | -40 °C to +85 °C | 8 | 6 | 24 | 24 | 0 | Yes |
| 28-pin (210-Mil) SSOP (Tape and Reel) | CY8C22345H-24PVXAT | 16 K | 1 K | -40 °C to +85 °C | 8 | 6 | 24 | 24 | 0 | Yes |
| 28-pin (210-Mil) SSOP | CY8C22345-12PVXE | 16 K | 1 K | -40 °C to +125 °C | 8 | 6 | 24 | 24 | 0 | Yes |
| 28-pin (210-Mil) SSOP (Tape and Reel) | CY8C22345-12PVXET | 16 K | 1 K | -40 °C to +125 °C | 8 | 6 | 24 | 24 | 0 | Yes |
| 48-pin (300-Mil) SSOP | CY8C21645-24PVXA | 8 K | 512 | -40 °C to +85 °C | 4 | 6 | 38 | 38 | 0 | Yes |
| 48-pin (300-Mil) SSOP (Tape and Reel) | CY8C21645-24PVXAT | 8 K | 512 | -40 °C to +85 °C | 4 | 6 | 38 | 38 | 0 | Yes |
| 48-pin (300-Mil) SSOP | CY8C21645-12PVXE | 8 K | 512 | -40 °C to +125 °C | 4 | 6 | 38 | 38 | 0 | Yes |
| 48-pin (300-Mil) SSOP (Tape and Reel) | CY8C21645-12PVXET | 8 K | 512 | -40 °C to +125 °C | 4 | 6 | 38 | 38 | 0 | Yes |
| 48-pin (300-Mil) SSOP | CY8C22645-24PVXA | 16 K | 1 K | -40 °C to +85 °C | 8 | 6 | 38 | 38 | 0 | Yes |
| 48-pin (300-Mil) SSOP (Tape and Reel) | CY8C22645-24PVXAT | 16 K | 1 K | -40 °C to +85 °C | 8 | 6 | 38 | 38 | 0 | Yes |
| 48-pin (300-Mil) SSOP | CY8C22645-12PVXE | 16 K | 1 K | -40 °C to +125 °C | 8 | 6 | 38 | 38 | 0 | Yes |
| 48-pin (300-Mil) SSOP (Tape and Reel) | CY8C22645-12PVXET | 16 K | 1 K | -40 °C to +125 °C | 8 | 6 | 38 | 38 | 0 | Yes |

Ordering Code Definitions



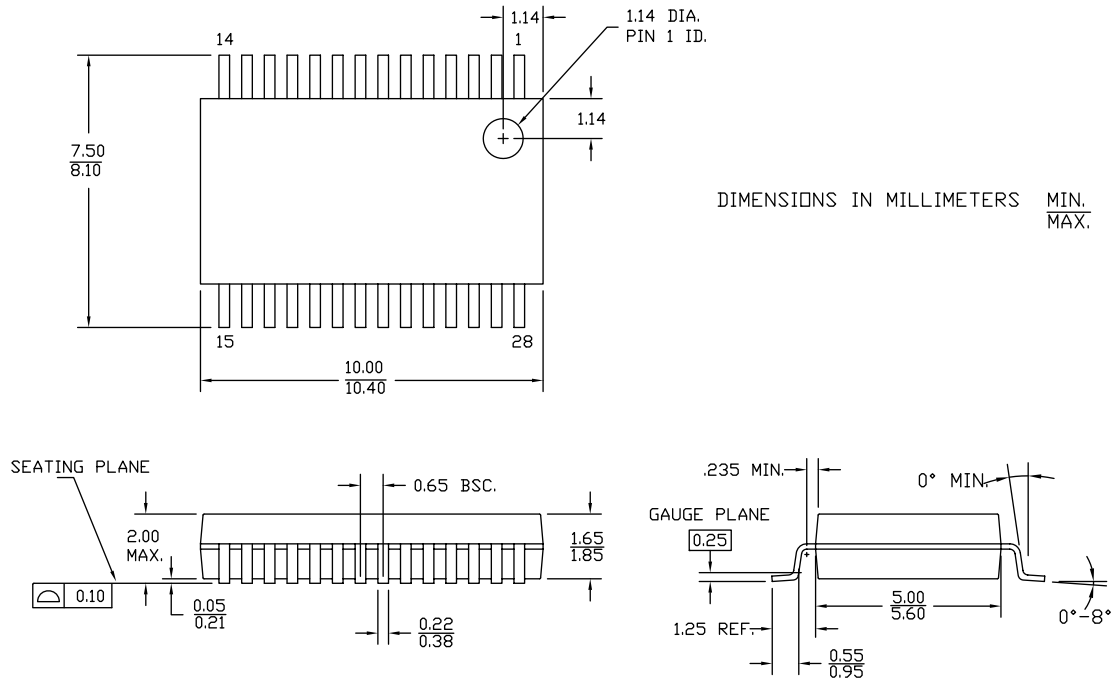
Packaging Information

Package Dimensions

This section provides the packaging specifications for the automotive CY8C21x45 and CY8C22x45 PSoC devices. The thermal impedances for each package and the typical package capacitance on crystal pins are given.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at <http://www.cypress.com>.

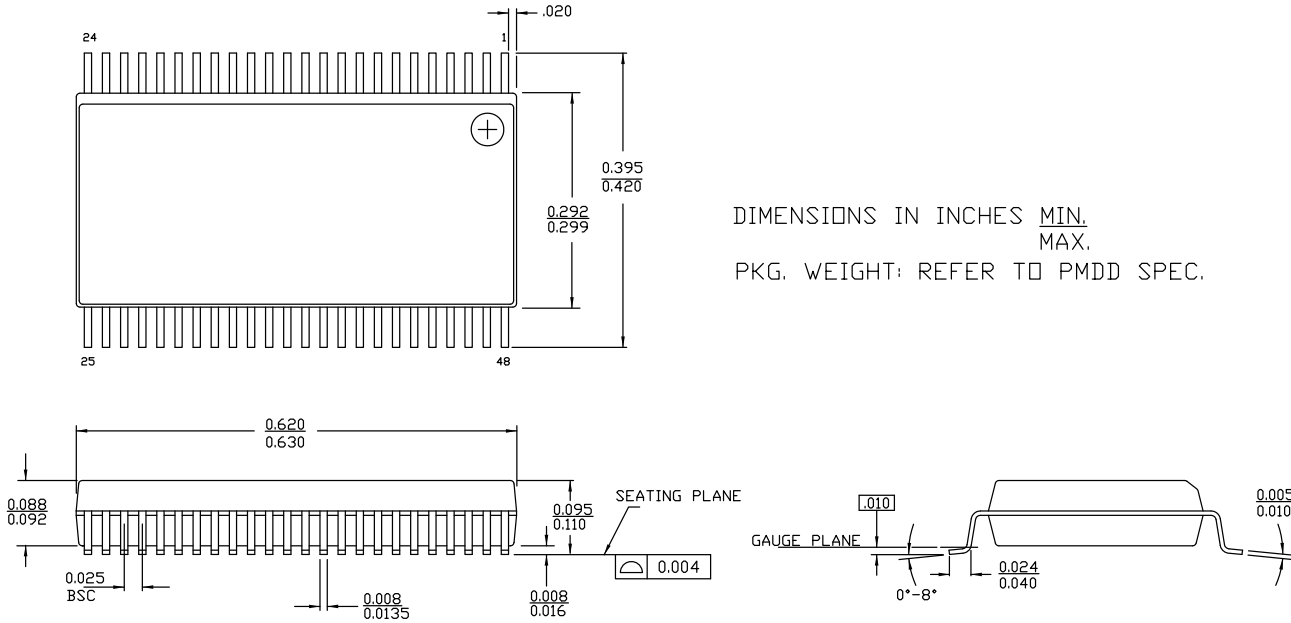
Figure 10. 28-pin SSOP (210 Mils) Package Outline, 51-85079



51-85079 *F

Package Dimensions (continued)

Figure 11. 48-pin SSOP (300 Mils) Package Outline, 51-85061



51-85061 *F

Thermal Impedances

Table 27. Thermal Impedances per Package

| Package | Typical θ_{JA} [22] |
|-------------|----------------------------|
| 28-pin SSOP | 97.6 °C/W |
| 48-pin SSOP | 69 °C/W |

Capacitance on Crystal Pins

Table 28. Typical Package Capacitance on Crystal Pins

| Package | Package Capacitance |
|-------------|---------------------|
| 28-pin SSOP | 2.8 pF |
| 48-pin SSOP | 3.3 pF |

Solder Reflow Specifications

Table 29 shows the solder reflow temperature limits that must not be exceeded.

Table 29. Solder Reflow Specifications

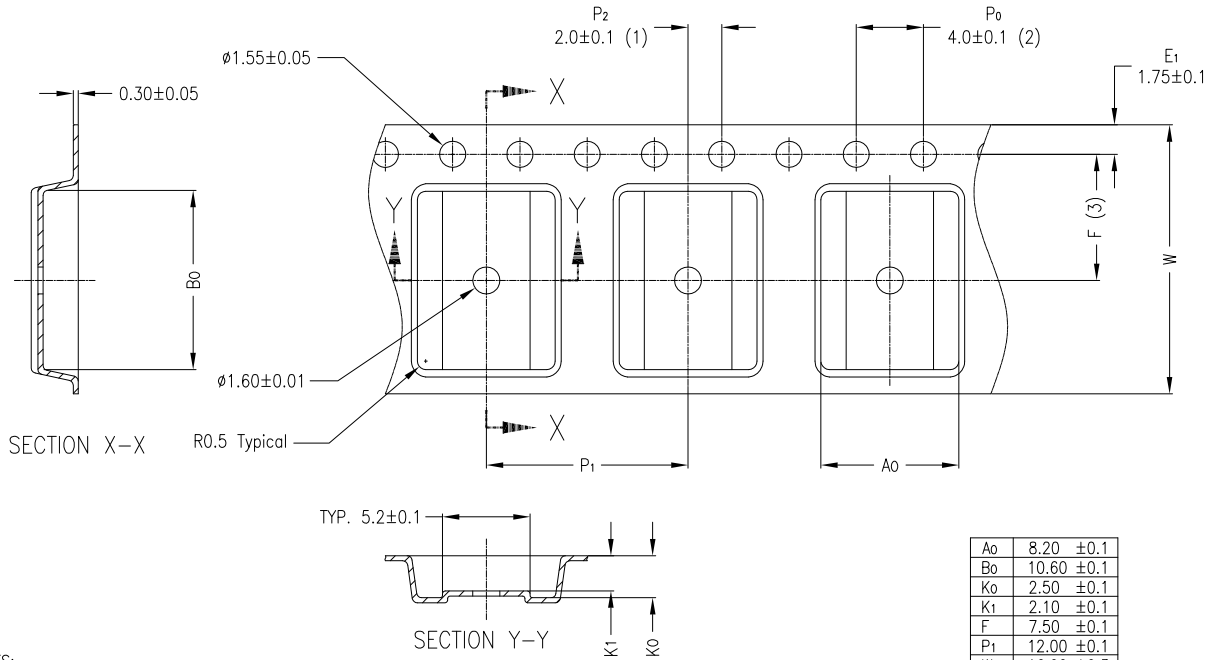
| Package | Maximum Peak Temperature (T_C) | Maximum Time above $T_C - 5\text{ °C}$ |
|-------------|------------------------------------|--|
| 28-pin SSOP | 260 °C | 30 seconds |
| 48-pin SSOP | 260 °C | 30 seconds |

Note

22. $T_J = T_A + \text{POWER} \times \theta_{JA}$

Tape and Reel Information

Figure 12. 28-pin SSOP (209 Mils) Carrier Tape, 51-51100



NOTES:

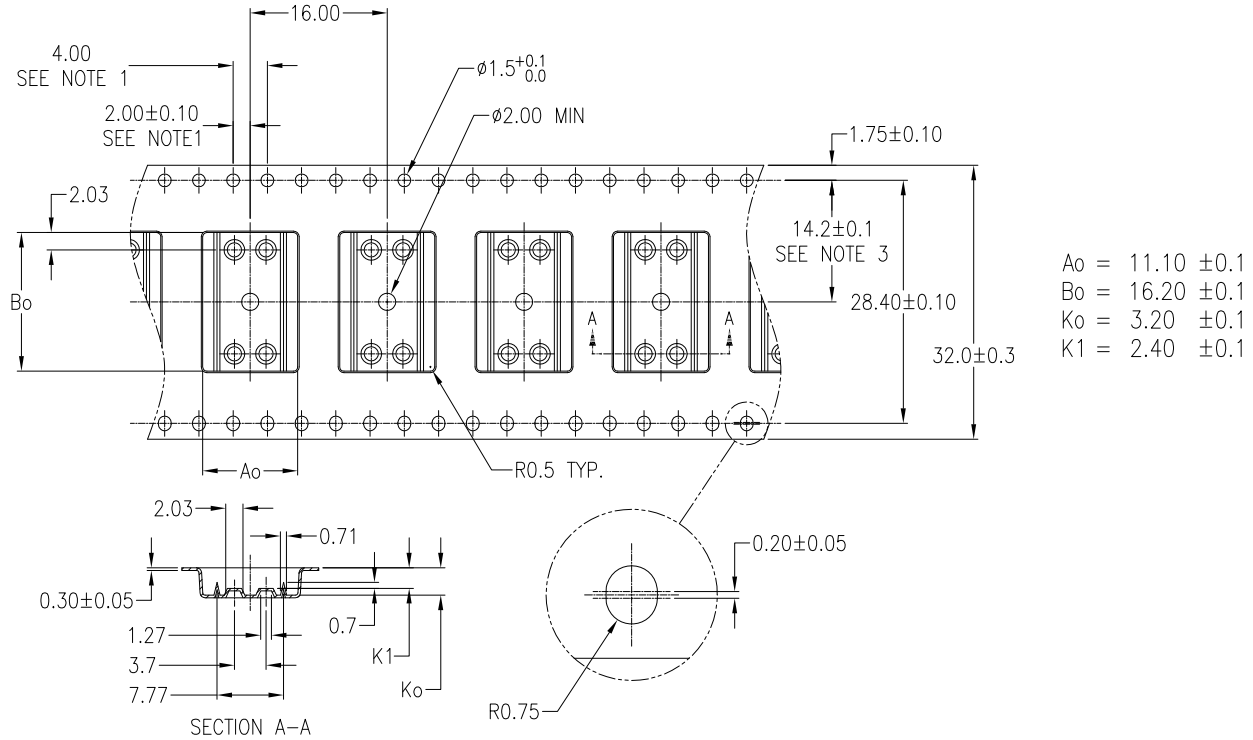
- (1) Measured from centerline of sprocket hole to centerline of pocket.
- (2) Cumulative tolerance of 10 sprocket holes is ± 0.10.
- (3) Measured from centerline of sprocket hole to centerline of pocket
- 4 Material: Conductive Polystyrene
- 5 Camber not to exceed 1mm in 100mm
- 6 Supplier P/N: SSOP28-3 CL3 22B3 Lxx W16

51-51100 *D

Figure 13. 48-pin SSOP (300 Mils) Carrier Tape, 51-51104

NOTES:

1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE



51-51104 *E

Table 30. Tape and Reel Specifications

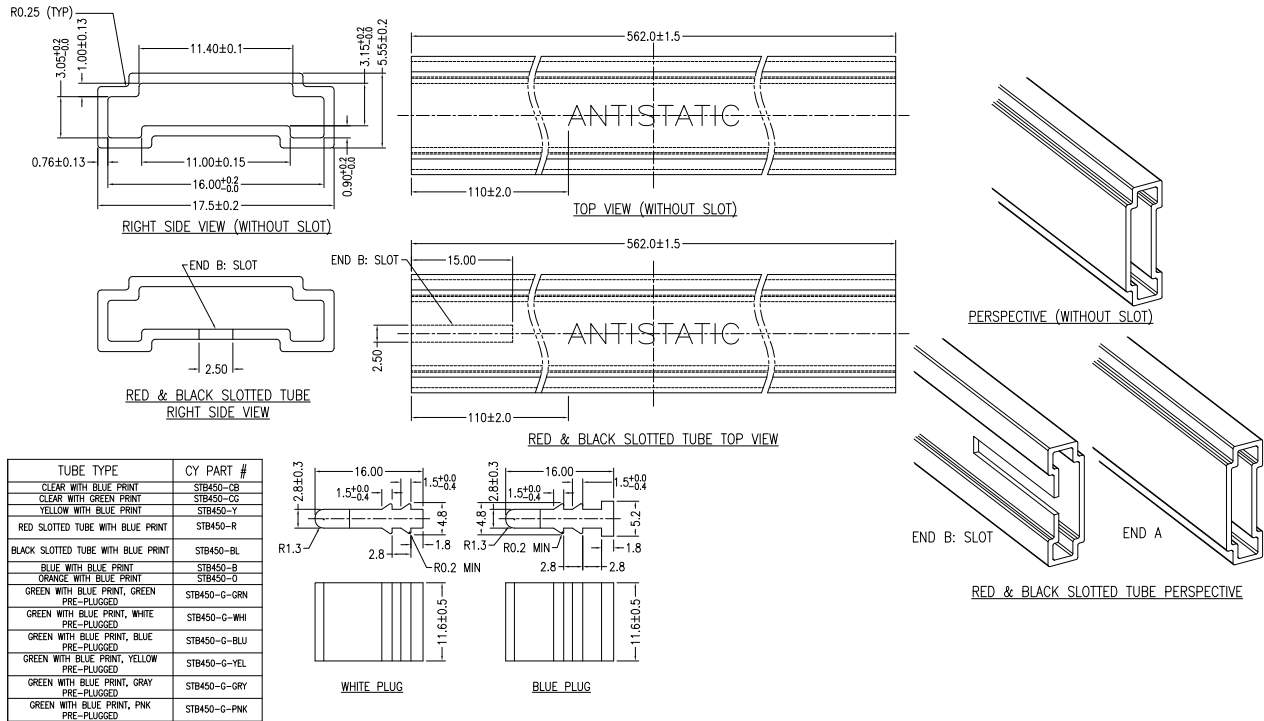
| Package | Cover Tape Width (mm) | Hub Size (inches) | Minimum Leading Empty Pockets | Minimum Trailing Empty Pockets | Standard Full Reel Quantity |
|-------------|-----------------------|-------------------|-------------------------------|--------------------------------|-----------------------------|
| 28-pin SSOP | 13.3 | 7 | 42 | 25 | 1000 |
| 48-pin SSOP | 25.5 | 4 | 32 | 19 | 1000 |

Tube Information

Figure 14. 28-pin SSOP, 32-pin SOIC (450 Mils Body) Shipping Tube, 51-51029

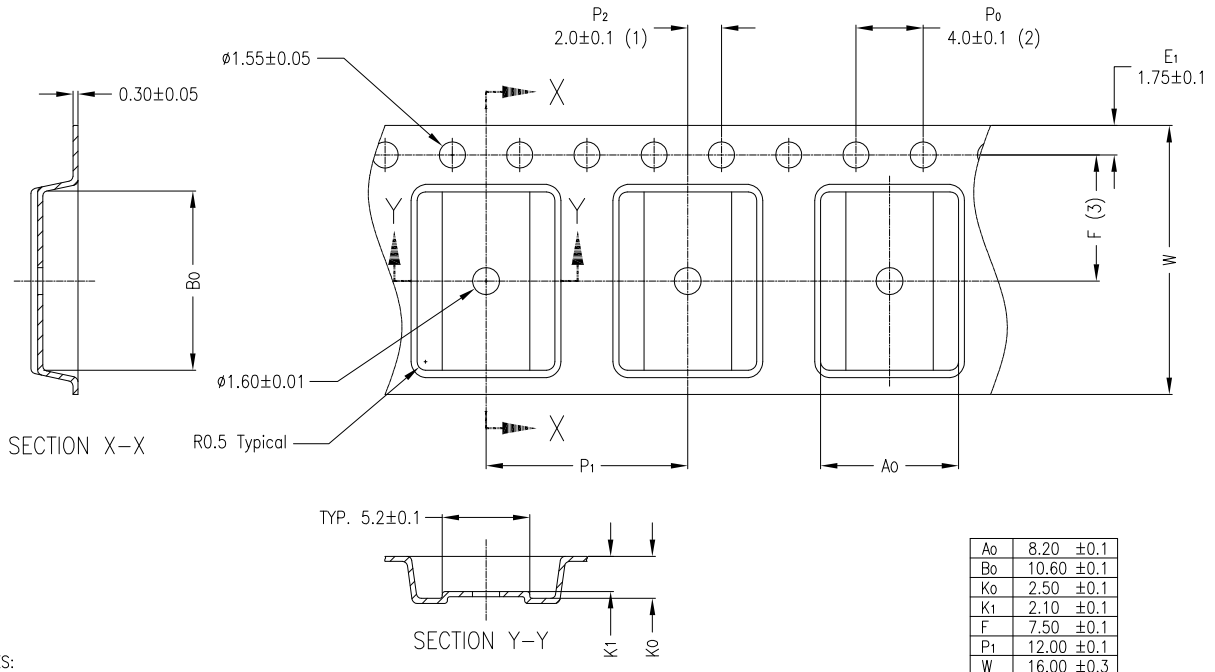
NOTE:

1. MARK "ANTISTATIC" WITH 3.0mm HIGH AND 25.4±0.5mm LENGTH IN BLUE COLOR
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. TUBE MATERIAL : HARD PVC CLEAR.
4. PLUG MATERIAL : PPR 48
5. WHITE PLUG NEED COMPLETELY INSERT TO TUBE BEFORE SHIPPING AND THE TIP ALIGN WITH TUBE EDGE.
6. THE BLUE PLUG ENCLOSE TOGETHER WITH THE SHIPMENT.
7. 25 UNITS PER TUBE.
8. TUBE PART NUMBER WITH SLOT : STB450-R , STB450-BL



51-51029 *G

Figure 15. 48-pin SSOP (300 Mils) Tube, 51-51000



NOTES:

- (1) Measured from centerline of sprocket hole to centerline of pocket.
- (2) Cumulative tolerance of 10 sprocket holes is ± 0.10 .
- (3) Measured from centerline of sprocket hole to centerline of pocket
- 4 Material: Conductive Polystyrene
- 5 Camber not to exceed 1mm in 100mm
- 6 Supplier P/N: SSOP28-3 CL3 22B3 Lxx W16

51-51000 *M

Acronyms

Table 31 lists the acronyms that are used in this document.

Table 31. Acronyms Used in this Datasheet

| Acronym | Description | Acronym | Description |
|------------------|---|-------------------|---|
| AC | alternating current | LVD | low voltage detect |
| ADC | analog-to-digital converter | MAC | multiply-accumulate |
| AEC | Automotive Electronics Council | MCU | microcontroller unit |
| API | application programming interface | MIPS | million instructions per second |
| CMOS | complementary metal oxide semiconductor | PCB | printed circuit board |
| CPU | central processing unit | PDIP | plastic dual inline package |
| CRC | cyclic redundancy check | PGA | programmable gain amplifier |
| CSD | capsense sigma delta | POR | power-on reset |
| CT | continuous time | PPOR | precision POR |
| DAC | digital-to-analog converter | PRS | pseudo-random sequence |
| DC | direct current | PSoC [®] | Programmable System-on-Chip |
| DNL | differential nonlinearity | PWM | pulse-width modulator |
| ECO | external crystal oscillator | RMS | root mean square |
| EEPROM | electrically erasable programmable read-only memory | RTC | real time clock |
| GPIO | general-purpose I/O | SAR | successive approximation register |
| I ² C | inter-integrated circuit | SC | switched capacitor |
| I/O | input/output | SLIMO | slow IMO |
| ICE | in-circuit emulator | SPI | serial peripheral interface |
| IDE | integrated development environment | SRAM | static random-access memory |
| ILO | internal low speed oscillator | SROM | supervisory read-only memory |
| IMO | internal main oscillator | SSOP | shrunk small outline package |
| INL | integral nonlinearity | UART | universal asynchronous receiver transmitter |
| IrDA | infrared data association | USB | universal serial bus |
| ISSP | in-system serial programming | WDT | watchdog timer |
| LCD | liquid crystal display | XRES | external reset |
| LED | light-emitting diode | | |

Reference Documents

CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC[®] Programmable System-on-Chip Technical Reference Manual (TRM) (001-14463)

Design Aids – Reading and Writing PSoC[®] Flash – AN2015 (001-40459)

Understanding Data Sheet Jitter Specifications for Cypress Timing Products (001-71968)

Document Conventions

Units of Measure

Table 32 lists the units of measure that are used in this document.

Table 32. Units of Measure

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|--------|-----------------------|--------|-----------------|
| kB | 1024 bytes | ms | millisecond |
| °C | degree Celsius | mV | millivolt |
| kHz | kilohertz | nA | nanoampere |
| kΩ | kilohm | ns | nanosecond |
| LSbit | least-significant bit | W | ohm |
| MHz | megahertz | % | percent |
| μA | microampere | pF | picofarad |
| μs | microsecond | ps | picosecond |
| μV | microvolt | pA | picoampere |
| mA | milliampere | V | volt |
| mm | millimeter | W | watt |

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimals.

Glossary

| | |
|---|--|
| active high | <ol style="list-style-type: none"> 1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states. |
| analog blocks | The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more. |
| analog-to-digital (ADC) | A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation. |
| API (Application Programming Interface) | A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications. |
| asynchronous | A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal. |
| bandgap reference | A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference. |
| bandwidth | <ol style="list-style-type: none"> 1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum. |
| bias | <ol style="list-style-type: none"> 1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device. |

Glossary (continued)

| | |
|-------------------------------|--|
| block | <ol style="list-style-type: none">1. A functional unit that performs a single function, such as an oscillator.2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block. |
| buffer | <ol style="list-style-type: none">1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written.2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device.3. An amplifier used to lower the output impedance of a system. |
| bus | <ol style="list-style-type: none">1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns.2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0].3. One or more conductors that serve as a common connection for a group of related devices. |
| clock | The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks. |
| comparator | An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements. |
| compiler | A program that translates a high level language, such as C, into machine language. |
| configuration space | In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to '1'. |
| crystal oscillator | An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components. |
| cyclic redundancy check (CRC) | A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression. |
| data bus | A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions. |
| debugger | A hardware and software system that allows the user to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory. |
| dead band | A period of time when neither of two or more signals are in their active state or in transition. |
| digital blocks | The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI. |
| digital-to-analog (DAC) | A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation. |
| duty cycle | The relationship of a clock period high time to its low time, expressed as a percent. |
| emulator | Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system. |

Glossary (continued)

| | |
|---------------------------------|--|
| external reset (XRES) | An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state. |
| flash | An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off. |
| Flash block | The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes. |
| frequency | The number of cycles or events per unit of time, for a periodic function. |
| gain | The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB. |
| I ² C | A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I ² C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I ² C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode. |
| ICE | The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer). |
| input/output (I/O) | A device that introduces data into or extracts data from a system. |
| interrupt | A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed. |
| interrupt service routine (ISR) | A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution. |
| jitter | <ol style="list-style-type: none">1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams.2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles. |
| low-voltage detect (LVD) | A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls below a selected threshold. |
| M8C | An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space. |
| master device | A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the slave device . |
| microcontroller | An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor. |
| mixed-signal | The reference to a circuit containing both analog and digital techniques and components. |

Glossary (continued)

| | |
|-----------------------------|---|
| modulator | A device that imposes a signal on a carrier. |
| noise | <ol style="list-style-type: none">1. A disturbance that affects a signal and that may distort the information carried by the signal.2. The random variations of one or more characteristics of any entity such as voltage, current, or data. |
| oscillator | A circuit that may be crystal controlled and is used to generate a clock frequency. |
| parity | A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity). |
| phase-locked loop (PLL) | An electronic circuit that controls an oscillator so that it maintains a constant phase angle relative to a reference signal. |
| pinouts | The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names. |
| port | A group of pins, usually eight. |
| power on reset (POR) | A circuit that forces the PSoC device to reset when the voltage is below a pre-set level. This is one type of hardware reset. |
| PSoC [®] | Cypress Semiconductor's PSoC [®] is a registered trademark and Programmable System-on-Chip [™] is a trademark of Cypress. |
| PSoC Designer [™] | The software for Cypress' Programmable System-on-Chip technology. |
| pulse width modulator (PWM) | An output in the form of duty cycle which varies as a function of the applied measurand |
| RAM | An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in. |
| register | A storage device with a specific capacity, such as a bit or byte. |
| reset | A means of bringing a system back to a know state. See hardware reset and software reset. |
| ROM | An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in. |
| serial | <ol style="list-style-type: none">1. Pertaining to a process in which all events occur one after the other.2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel. |
| settling time | The time it takes for an output signal or value to stabilize after the input has changed from one value to another. |
| shift register | A memory storage device that sequentially shifts a word either left or right to output a stream of serial data. |
| slave device | A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device. |

Glossary (continued)

| | |
|----------------|---|
| SRAM | An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device. |
| SROM | An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash. |
| stop bit | A signal following a character or block that prepares the receiving device to receive the next character or block. |
| synchronous | <ol style="list-style-type: none">1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal.2. A system whose operation is synchronized by a clock signal. |
| tri-state | A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net. |
| UART | A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits. |
| user modules | Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level Application Programming Interface (API) for the peripheral function. |
| user space | The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program. |
| V_{DD} | A name for a power net meaning “voltage drain.” The most positive power supply signal. Usually 5 V or 3.3 V. |
| V_{SS} | A name for a power net meaning “voltage source.” The most negative power supply signal. |
| watchdog timer | A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time. |

Errata

This section describes the errata for the CY8C21x45, CY8C22x45 family of PSoC devices. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

| Part Number | Device Characteristics |
|-------------|------------------------|
| CY8C21345 | All Variants |
| CY8C21645 | All Variants |
| CY8C22345 | All Variants |
| CY8C22645 | All Variants |

CY8C21x45, CY8C22x45 Qualification Status

Product Status: In Production

Errata Summary

The following table defines the errata applicable for this PSoC family device.

| Items | Part Number | Silicon Revision | Fix Status |
|---|---|------------------|--|
| 1. Free Running Nonstop Reading cause 7 LSB Pseudo Code Variation in SAR10ADC | All CY8C21x45, CY8C22x45 devices affected | All | Silicon fix not planned. Use workaround. |
| 2. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes | All CY8C21x45, CY8C22x45 devices affected | All | Silicon fix not planned. Use workaround. |

1. Free Running Nonstop Reading cause 7 LSB Pseudo Code Variation in SAR10ADC

■ Problem Definition

In free running mode, there can be a variation of up to 7 LSB in the digital output of SAR10 ADC.

■ Parameters Affected

Code Variation. This is not a specified parameter.

It is defined as the number of unique output codes generated by the ADC for a given constant input voltage, in addition to the correct code. For example, for an input voltage of 2.000 V, the expected code is 190hex and the ADC generates three codes: 191hex, 190hex, and 192hex. The code variation is 2 LSB.

■ Trigger Condition(S)

SAR10 ADC is configured in the free running mode. When ADC is operated in free running mode, for a constant input voltage output of ADC can have a variation of up to 7LSB. This can be resolved by using the averaging technique or by disabling the free running mode before reading the data and enabling again after reading the data.

■ Scope of Impact

Inaccurate output is possible.

■ Workaround

This issue can be averted by using one or both of the following workarounds. Consult a Cypress representative for additional assistance.

- Use the averaging technique. That is, take multiple samples of the input, and use a digital averaging filter.
- Disable the free running mode before reading data out, and enable the free running mode after completing the read operation.

■ Fix Status

No silicon fix is planned.

2. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes

■ Problem Definition

Asynchronous Digital Communications Interfaces may fail framing beyond 0 to 70 °C. This problem does not affect end-product usage between 0 and 70 °C.

■ Parameters Affected

The IMO frequency tolerance. The worst case deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is $\pm 5\%$.

■ Trigger Condiiton(S)

The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the datasheet limit of $\pm 2.5\%$ when operated beyond the temperature range of 0 to +70 °C.

■ Scope of Impact

This problem may affect UART, IrDA, and FSK implementations.

■ Workaround

Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.

■ Fix Status

The cause of this problem and its solution has been identified. No silicon fix is planned to correct the deficiency in silicon.

Document History Page

| Document Title: CY8C21345/CY8C21645/CY8C22345/CY8C22345H/CY8C22645, Automotive PSoC [®] Programmable System-on-Chip [™] Document Number: 001-55397 | | | | |
|---|---------|-----------------|-----------------|---|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 2759868 | VIVG | 09/04/2009 | New data sheet. |
| *A | 2788690 | VIVG | 10/20/2009 | Added 48 SSOP to the marketing part numbers. Corrected the I _{SOA} spec in table 13/14. Changed the ThetaJA values based on PE inputs. |
| *B | 2792800 | VIVG | 10/26/2009 | Corrected typo in ordering information table (Digital I/O for 48-SSOP devices) |
| *C | 2822630 | BTK | 12/07/2009 | Added CY8C22345H devices and updated Features section and PSoC Functional Overview section to include haptics device information. Updated Features section. Added Contents section. Updated PSoC Functional Overview section. Updated Block Diagram of device. Updated PSoC Device Characteristics table. Updated Pinouts section. Fixed issues with the Register Map tables. Added a figure for SLIMO configuration. Updated footnotes for the DC Programming Specifications table. Corrected V _{DDIWRITE} and Flash _{ENT} electrical specifications. Updated Ordering Information section. Added Development Tool Selection section. Combined 5 V DC Operational Amplifier Specifications table with 3.3 V DC Operational Amplifier Specifications table. Updated all AC specifications to conform to 5% IMO accuracy and 8.33% SLIMO accuracy. Split up electrical specifications for A-grade and E-grade devices in the Absolute Maximum Ratings, Operating Temperature, DC Chip Level Specifications, DC Programming Specifications, and AC Chip-Level Specifications tables. Added Solder Reflow Peak Temperature table. Added T _{PRGH} , T _{PRGC} , I _{OL} , I _{OH} , F _{32KU} , DC _{ILO} , and T _{POWERUP} electrical specifications. Added maximum values and updated typical values for T _{ERASEB} and T _{WRITE} electrical specifications. Replaced T _{RAMP} electrical specification with SR _{POWERUP} electrical specification. |
| *D | 2905459 | NJF | 04/06/2010 | Updated Cypress website links Added T _{BAKETEMP} , T _{BAKETIME} , and Fout48M electrical specifications Removed sections 'Third Party Tools' 'Build a PSoC Emulator into your Board' Updated package diagrams Updated Ordering Information table Updated Solder Reflow Peak Temperature specifications. Updated the Getting Started and Designing with PSoC Designer sections. Converted data sheet from Preliminary to Final Deleted 5% oscillator accuracy reference in the Features section. Deleted reference to a specific SAR10 ADC sample rate in the Analog System section. Updated the following Electrical Specifications: I _{DD} , I _{SB} , I _{SBXTL} , V _{REF} , V _{CMOA} , I _{ADCREF} , INL _{ADC} , DNL _{ADC} , V _{PPOR2} , Flash _{DR} , F _{IMO24} , T _{RiseF} , T _{FallF} , T _{RiseS} , T _{FallS} . Deleted the SPS _{ADC} electrical specification, the DC Low Power Comparator Specifications, the AC Low Power Comparator Specifications, and the AC Analog Mux Bus Specifications. |
| *E | 2915673 | VIVG | 04/16/2010 | Post to external web |
| *F | 2991841 | BTK | 07/23/2010 | Added a clarifying note to the V _{PPOR1} electrical specification. Added CY8C22345-12PVXE(T) devices. Moved Document Conventions to the end of the document. |
| *G | 3037161 | BTK | 09/23/2010 | Added CY8C21345-12PVXE(T) devices to the Ordering Information section. |
| *H | 3085024 | BTK | 11/12/2010 | Added CY8C21645-12PVXE(T), CY8C21645-24PVXA(T), CY8C22645-12PVXE(T), and CY8C22645-24PVXA(T) devices to the Ordering Information section. |
| *I | 3200275 | BTK | 03/18/2011 | Added tape and reel packaging information. |

Document History Page (continued)

| Document Title: CY8C21345/CY8C21645/CY8C22345/CY8C22345H/CY8C22645, Automotive PSoC [®] Programmable System-on-Chip [™] Document Number: 001-55397 | | | | |
|---|---------|-----------------|-----------------|---|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| *J | 3341627 | BTK/NJF | 08/11/2011 | Updated I ² C timing diagram to improve clarity. Updated wording, formatting, and notes of the AC Digital Block Specifications table to improve clarity. Added V _{DDP} , V _{DDL} , and V _{DDHV} electrical specifications to give more information for programming the device. Updated solder reflow temperature specifications to give more clarity. Updated the jitter specifications. Updated PSoC Device Characteristics table. Updated the F _{32KHz} electrical specification. Updated note for R _{PD} electrical specification. Updated note for the T _{STG} electrical specification to add more clarity. Removed CY8C22345H-24PVXA(T) devices from datasheet. |
| *K | 3732256 | MASJ | 10/04/2012 | Updated Features (Included CY8C22345H device related information). Updated PSoC Functional Overview (Updated Digital System (Changed PWM description string from "8- to 32-bit" to "8- and 16-bit"), added Haptics TS2000 Controller). Updated Development Tool Selection (Updated Accessories (Emulation and Programming) (Updated Table 25)). Updated Electrical Specifications (Updated DC Electrical Characteristics (Updated DC GPIO Specifications (Updated Table 10 (To include the V _{OL} specification for V _{DD} = 3.0 to 3.6 V condition)))). Updated Ordering Information (Updated part numbers). Updated Packaging Information (Updated Package Dimensions (spec 51-85061 (Changed revision from *D to *F), spec 51-51100 (Changed revision from *B to *C)), updated Tape and Reel Information (spec 51-51100 (Changed revision from *B to *C)), added Tube Information (spec 51-51029, spec 51-51000)). |
| *L | 4479445 | ASRI | 08/20/2014 | Updated Electrical Specifications : Updated DC Electrical Characteristics : Added DC IDAC Specifications . Updated Packaging Information : Updated Tape and Reel Information : spec 51-51100 – Changed revision from *C to *D. spec 51-51104 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review. |
| *M | 4513128 | ASRI | 09/25/2014 | Updated Packaging Information : Updated Tube Information : spec 51-51000 – Changed revision from *K to *L. Added Errata . |
| *N | 5958799 | MVRE | 11/06/2017 | Updated Packaging Information : Updated Package Dimensions : spec 51-85079 – Changed revision from *E to *F. Updated Tube Information : spec 51-51029 – Changed revision from *E to *G. spec 51-51000 – Changed revision from *L to *M. Updated to new template. Completing Sunset Review. |
| *O | 6015432 | MVRE | 01/05/2018 | Updated to new template. |

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