



**THE DATASHEET OF  
CY7C60445-32LQXC**

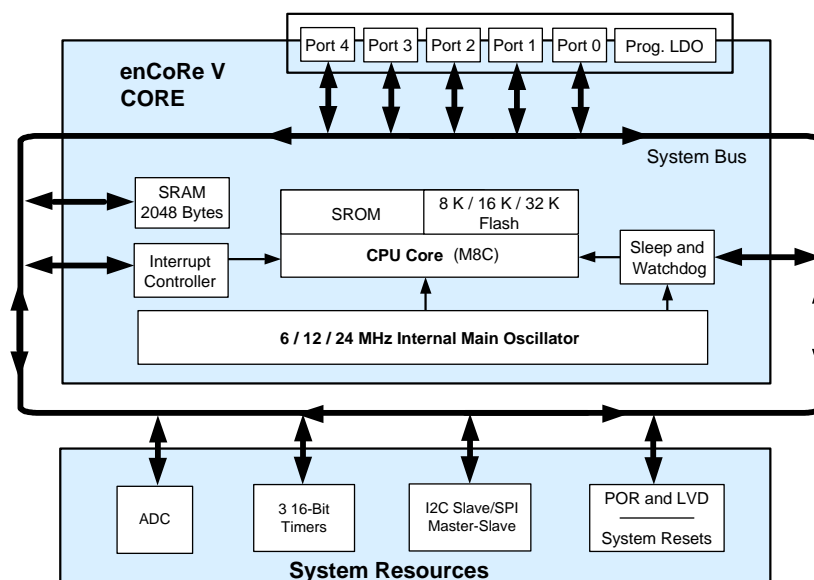


# enCoRe™ V Low Voltage Microcontroller

## Features

- Powerful Harvard Architecture processor
  - M8C processor speeds running up to 24 MHz
  - Low power at high processing speeds
  - Interrupt controller
  - 1.71 V to 3.6 V operating voltage
  - Commercial temperature range: 0 °C to +70 °C
- Flexible on-chip memory
  - Up to 32 K flash program storage
    - 50,000 erase and write cycles
    - Flexible protection modes
  - Up to 2048 bytes SRAM data storage
  - In-system serial programming (ISSP)
- Complete development tools
  - Free development tool (PSoC® Designer™)
  - Full-featured, in-circuit emulator and programmer
  - Full-speed emulation
  - Complex breakpoint structure
  - 128 K trace memory
- Precision, programmable clocking
  - Crystal-less oscillator with support for an external crystal or resonator
  - Internal ±5.0% 6, 12, or 24 MHz main oscillator
- Internal low-speed oscillator at 32 kHz for watchdog and sleep. The frequency range is 19 to 50 kHz with a 32 kHz typical value
- Programmable pin configurations
  - Up to 36 GPIO (depending on package)
  - 25 mA sink current on all GPIO
  - Pull-up, High Z, open drain, CMOS drive modes on all GPIO
  - CMOS drive mode (5 mA source current) on Ports 0 and 1:
    - 20 mA (at 3.0 V) total source current
  - Low dropout voltage regulator for Port 1 pins:
    - Programmable to output 3.0, 2.5, or 1.8V
  - Selectable, regulated digital I/O on Port 1
  - Configurable input threshold for Port 1
  - Hot-swappable capability on Port 1
- Additional system resources
  - Configurable communication speeds
  - I<sup>2</sup>C Slave
    - Selectable to 50 kHz, 100 kHz, or 400 kHz
    - Implementation requires no clock stretching
    - Implementation during sleep modes with less than 100 mA
    - Hardware address detection
  - SPI master and SPI slave
    - Configurable between 46.9 kHz and 12 MHz
  - Three 16-bit timers
  - 10-bit ADC used to monitor battery voltage or other signals with external components
  - Watchdog and sleep timers
  - Integrated supervisory circuit

## enCoRe V LV Block Diagram



**Errata:** For information on silicon errata, see "Errata" on page 35. Details include trigger conditions, devices affected, and proposed workaround.

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## Functional Overview

The enCoRe V LV family of devices are designed to replace multiple traditional low voltage microcontroller system components with one, low cost single chip programmable component. Communication peripherals (I<sup>2</sup>C/SPI), a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as illustrated in [enCoRe V LV Block Diagram](#), is comprised of two main areas: the CPU core and the system resources. Depending on the enCoRe V LV package, up to 36 GPIO are also included.

Enhancements over the Cypress's legacy low-voltage microcontrollers include faster CPU at lower voltage operation, lower current consumption, twice the RAM and flash, hot-swappable I/Os, I<sup>2</sup>C hardware address recognition, new very low-current sleep mode, and new package options.

### The enCoRe V LV Core

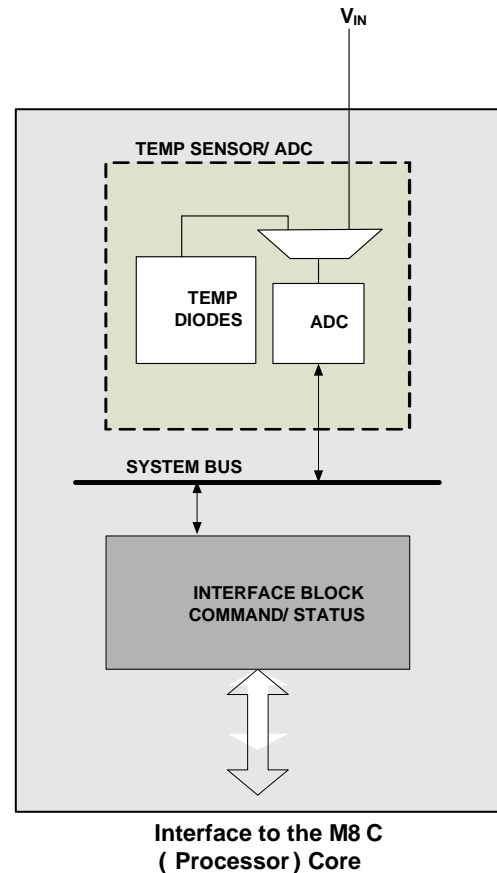
The enCoRe V LV Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO (internal main oscillator) and ILO (internal low-speed oscillator). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four-MIPS, 8-bit Harvard architecture microprocessor.

System Resources provide additional capability, such as a configurable I<sup>2</sup>C slave and SPI master-slave communication interface and various system resets supported by the M8C.

### 10-bit ADC

The ADC on enCoRe V LV device is an independent block with a state machine interface to control accesses to the block. The ADC is housed together with the temperature sensor core and can be connected to this or the Analog Mux Bus. As a default operation, the ADC is connected to the temperature sensor diodes to give digital values of the temperature.

Figure 1. ADC System Performance Block Diagram



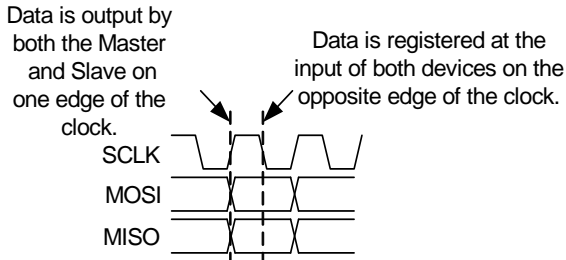
The ADC User Module contains an integrator block and one comparator with positive and negative input set by the MUXes. The input to the integrator stage comes from the Analog Global Input Mux or the temperature sensor with an input voltage range of 0 V to 1.3 V, where 1.3 V is 72% of full scale.

In the ADC only configuration (the ADC MUX selects the Analog Mux Bus, not the default temperature sensor connection), an external voltage can be connected to the input of the modulator for voltage conversion. The ADC is run for a number of cycles set by the timer, depending upon the resolution of the ADC desired by the user. A counter counts the number of trips by the comparator, which is proportional to the input voltage. The Temp Sensor block clock speed is 36 MHz and is divided down to 1 to 12 MHz for ADC operation.

### SPI

The serial peripheral interconnect (SPI) 3-wire protocol uses both edges of the clock to enable synchronous communication without the need for stringent setup and hold requirements.

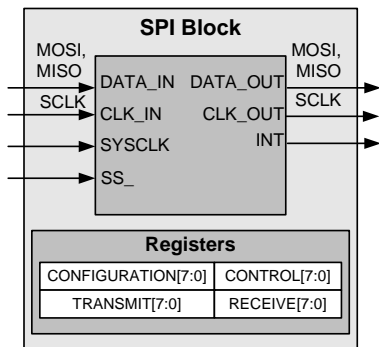
**Figure 2. Basic SPI Configuration**



A device can be a master or slave. A master outputs clock and data to the slave device and inputs slave data. A slave device inputs clock and data from the master device and outputs data for input to the master. Together, the master and slave are essentially a circular Shift register, where the master generates the clocking and initiates data transfers.

A basic data transfer occurs when the master sends eight bits of data, along with eight clocks. In any transfer, both master and slave transmit and receive simultaneously. If the master only sends data, the received data from the slave is ignored. If the master wishes to receive data from the slave, the master must send dummy bytes to generate the clocking for the slave to send data back.

**Figure 3. SPI Block Diagram**



SPI configuration register (SPI\_CFG) sets master/slave functionality, clock speed and interrupt select. SPI control register (SPI\_CR) provides four control bits and four status bits for device interfacing and synchronization.

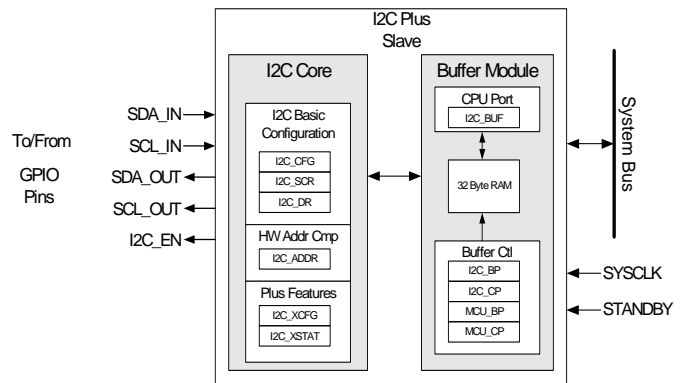
The SPIM hardware has no support for driving the Slave Select (SS\_) signal. The behavior and use of this signal is application and enCoRe V device dependent and, if required, must be implemented in firmware.

There is an additional data input in the SPIS, Slave Select (SS\_), which is an active low signal. SS\_ must be asserted to enable the SPIS to receive and transmit. SS\_ has two high level functions: 1) To allow for the selection of a given slave in a multi-slave environment, and 2) To provide additional clocking for TX data queuing in SPI modes 0 and 1.

### I<sup>2</sup>C Slave

The I<sup>2</sup>C slave enhanced communications block is a serial-to-parallel processor, designed to interface the enCoRe V LV device to a two-wire I<sup>2</sup>C serial communications bus. To eliminate the need for excessive CPU intervention and overhead, the block provides I<sup>2</sup>C-specific support for status detection and generation of framing bits. By default, the I<sup>2</sup>C Slave Enhanced module is firmware compatible with the previous generation of I<sup>2</sup>C slave functionality. However, this module provides new features that are configurable to implement significant flexibility for both internal and external interfacing.

**Figure 4. I<sup>2</sup>C Block Diagram**



The basic I<sup>2</sup>C features include:

- \*Slave, transmitter, and receiver operation
- \*Byte processing for low CPU overhead
- \*Interrupt or polling CPU interface
- \*Support for clock rates of up to 400 kHz
- \*7- or 10-bit addressing (through firmware support)
- \*SMBus operation (through firmware support)

Enhanced features of the I<sup>2</sup>C Slave Enhanced Module include:

- \*Support for 7-bit hardware address compare
- \*Flexible data buffering schemes
- \*A 'no bus stalling' operating mode
- \*A low power bus monitoring mode

The I<sup>2</sup>C block controls the data (SDA) and the clock (SCL) to the external I<sup>2</sup>C interface through direct connections to two dedicated GPIO pins. When I<sup>2</sup>C is enabled, these GPIO pins are not available for general purpose use. The enCoRe V LV CPU firmware interacts with the block through I/O register reads and writes, and firmware synchronization is implemented through polling and/or interrupts.

In the default operating mode, which is firmware compatible with previous versions of I<sup>2</sup>C slave modules, the I<sup>2</sup>C bus is stalled upon every received address or byte, and the CPU is required to read the data or supply data as required before the I<sup>2</sup>C bus continues. However, this I<sup>2</sup>C Slave Enhanced module provides new data buffering capability as an enhanced feature. In the EZI<sup>2</sup>C buffering mode, the I<sup>2</sup>C slave interface appears as a 32-byte RAM buffer to the external I<sup>2</sup>C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave never stalls the bus. In this protocol, the data available in the RAM (this is managed by the CPU) is valid.

### Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The following statements describe the merits of each system resource:

- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- The 3.6 V maximum input, 1.8, 2.5, or 3 V selectable output, low dropout regulator (LDO) provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.
- Standard Cypress PSoC IDE tools are available for debugging the enCoRe V LV family of parts.

## Getting Started

The quickest way to understanding the enCoRe V silicon is by reading this datasheet and using the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the enCoRe V integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, refer to the *PSoC Programmable System-on-Chip Technical Reference Manual*, for CY8C28xxx PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, reference the latest enCoRe V device datasheets on the web at <http://www.cypress.com>.

## Application Notes

[Cypress application notes](#) are an excellent introduction to the wide variety of possible PSoC designs.

## Development Kits

[PSoC Development Kits](#) are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

## Training

[Free PSoC technical training](#) (on demand, webinars, and workshops), which is available online via [www.cypress.com](http://www.cypress.com), covers a wide variety of topics and skill levels to assist you in your designs.

## CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the [CYPros Consultants](#) web site.

## Solutions Library

Visit our growing [library of solution focused designs](#). Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

## Technical Support

[Technical support](#) – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

## Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I<sup>2</sup>C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

## PSoC Designer Software Subsystems

### *Design Entry*

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

### *Code Generation Tools*

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

**Assemblers.** The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

**C Language Compilers.** C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

### *Debugger*

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

### *Online Help System*

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

### *In-Circuit Emulator*

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

## Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select [user modules](#).
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

### Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

### Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module

parameter, and other information that you may need to successfully implement your design.

### Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

### Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.



32-Pin Part Pinout

Figure 6. CY7C60445 32-Pin enCoRe V LV Device

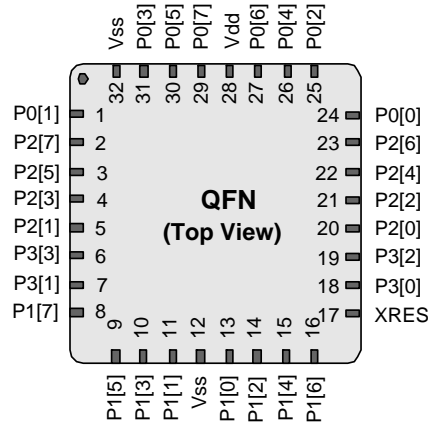


Table 2. 32-Pin Part Pinout (QFN)

| Pin No. | Type        | Name                   | Description   |
|---------|-------------|------------------------|---|
| 1       | IOH         | P0[1]                  | Digital I/O   |
| 2       | I/O         | P2[7]                  | Digital I/O   |
| 3       | I/O         | P2[5]                  | Digital I/O, crystal out (Xout)                       |
| 4       | I/O         | P2[3]                  | Digital I/O, crystal in (Xin)                         |
| 5       | I/O         | P2[1]                  | Digital I/O   |
| 6       | I/O         | P3[3]                  | Digital I/O   |
| 7       | I/O         | P3[1]                  | Digital I/O   |
| 8       | IOHR        | P1[7]                  | Digital I/O, I <sup>2</sup> C SCL, SPI SS             |
| 9       | IOHR        | P1[5]                  | Digital I/O, I <sup>2</sup> C SDA, SPI MISO           |
| 10      | IOHR        | P1[3]                  | Digital I/O, SPI CLK                                  |
| 11      | IOHR        | P1[1] <sup>(1,2)</sup> | Digital I/O, ISSP CLK, I <sup>2</sup> C SCL, SPI MOSI |
| 12      | Power       | Vss                    | Ground connection                                     |
| 13      | IOHR        | P1[0] <sup>(1,2)</sup> | Digital I/O, ISSP DATA, I <sup>2</sup> C SDA, SPI CLK |
| 14      | IOHR        | P1[2]                  | Digital I/O   |
| 15      | IOHR        | P1[4]                  | Digital I/O, optional external clock input (EXTCLK)   |
| 16      | IOHR        | P1[6]                  | Digital I/O   |
| 17      | Reset Input | XRES                   | Active high external reset with internal pull-down    |
| 18      | I/O         | P3[0]                  | Digital I/O   |
| 19      | I/O         | P3[2]                  | Digital I/O   |
| 20      | I/O         | P2[0]                  | Digital I/O   |
| 21      | I/O         | P2[2]                  | Digital I/O   |
| 22      | I/O         | P2[4]                  | Digital I/O   |
| 23      | I/O         | P2[6]                  | Digital I/O   |
| 24      | IOH         | P0[0]                  | Digital I/O   |

**Table 2. 32-Pin Part Pinout (QFN) (continued)**

| Pin No. | Type  | Name  | Description                            |
|---------|-------|-------|--|
| 25      | IOH   | P0[2] | Digital I/O                            |
| 26      | IOH   | P0[4] | Digital I/O                            |
| 27      | IOH   | P0[6] | Digital I/O                            |
| 28      | Power | Vdd   | Supply voltage                         |
| 29      | IOH   | P0[7] | Digital I/O                            |
| 30      | IOH   | P0[5] | Digital I/O                            |
| 31      | IOH   | P0[3] | Digital I/O                            |
| 32      | Power | Vss   | Ground connection                      |
| CP      | Power | Vss   | Center pad must be connected to ground |

**LEGEND** I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

48-Pin Part Pinout

Figure 7. CY7C60455/CY7C60456 48-Pin enCoRe V LV Device

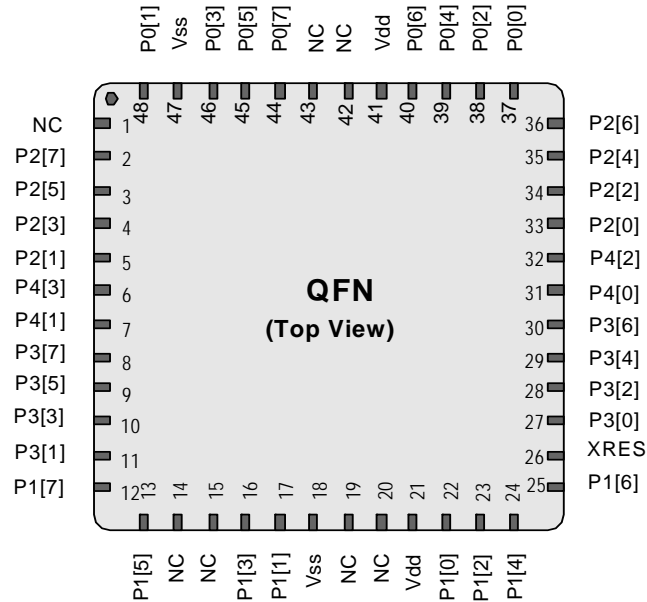


Table 3. 48-Pin Part Pinout (QFN)

| Pin No. | Type  | Name                    | Description   |
|---------|-------|-------------------------|---|
| 1       | NC    | NC                      | No connection   |
| 2       | I/O   | P2[7]                   | Digital I/O   |
| 3       | I/O   | P2[5]                   | Digital I/O, crystal out (Xout)                       |
| 4       | I/O   | P2[3]                   | Digital I/O, crystal in (Xin)                         |
| 5       | I/O   | P2[1]                   | Digital I/O   |
| 6       | I/O   | P4[3]                   | Digital I/O   |
| 7       | I/O   | P4[1]                   | Digital I/O   |
| 8       | I/O   | P3[7]                   | Digital I/O   |
| 9       | I/O   | P3[5]                   | Digital I/O   |
| 10      | I/O   | P3[3]                   | Digital I/O   |
| 11      | I/O   | P3[1]                   | Digital I/O   |
| 12      | IOHR  | P1[7]                   | Digital I/O, I <sup>2</sup> C SCL, SPI SS             |
| 13      | IOHR  | P1[5]                   | Digital I/O, I <sup>2</sup> C SDA, SPI MISO           |
| 14      | NC    | NC                      | No connection   |
| 15      | NC    | NC                      | No connection   |
| 16      | IOHR  | P1[3]                   | Digital I/O, SPI CLK                                  |
| 17      | IOHR  | P1[1] <sup>[1, 2]</sup> | Digital I/O, ISSP CLK, I <sup>2</sup> C SCL, SPI MOSI |
| 18      | Power | Vss                     | Supply ground   |
| 19      | NC    | NC                      | No connection   |
| 20      | NC    | NC                      | No connection   |

**Table 3. 48-Pin Part Pinout (QFN) (continued)**

| Pin No. | Type  | Name                    | Description   |
|---------|-------|-------------------------|---|
| 21      | Power | Vdd                     | Supply voltage                                      |
| 22      | IOHR  | P1[0] <sup>[1, 2]</sup> | Digital I/O, ISSP DATA, I2C SDA, SPI CLK            |
| 23      | IOHR  | P1[2]                   | Digital I/O   |
| 24      | IOHR  | P1[4]                   | Digital I/O, optional external clock input (EXTCLK) |
| 25      | IOHR  | P1[6]                   | Digital I/O   |
| 26      | XRES  | Ext Reset               | Active high external reset with internal pull-down  |
| 27      | I/O   | P3[0]                   | Digital I/O   |
| 28      | I/O   | P3[2]                   | Digital I/O   |
| 29      | I/O   | P3[4]                   | Digital I/O   |
| 30      | I/O   | P3[6]                   | Digital I/O   |
| 31      | I/O   | P4[0]                   | Digital I/O   |
| 32      | I/O   | P4[2]                   | Digital I/O   |
| 33      | I/O   | P2[0]                   | Digital I/O   |
| 34      | I/O   | P2[2]                   | Digital I/O   |
| 35      | I/O   | P2[4]                   | Digital I/O   |
| 36      | I/O   | P2[6]                   | Digital I/O   |
| 37      | IOH   | P0[0]                   | Digital I/O   |
| 38      | IOH   | P0[2]                   | Digital I/O   |
| 39      | IOH   | P0[4]                   | Digital I/O   |
| 40      | IOH   | P0[6]                   | Digital I/O   |
| 41      | Power | Vdd                     | Supply voltage                                      |
| 42      | NC    | NC                      | No connection                                       |
| 43      | NC    | NC                      | No connection                                       |
| 44      | IOH   | P0[7]                   | Digital I/O   |
| 45      | IOH   | P0[5]                   | Digital I/O   |
| 46      | IOH   | P0[3]                   | Digital I/O   |
| 47      | Power | Vss                     | Supply ground                                       |
| 48      | IOH   | P0[1]                   | Digital I/O   |
| CP      | Power | Vss                     | Center pad must be connected to ground              |

**LEGEND** I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

## Register Reference

The section discusses the registers of the enCoRe V LV device. It lists all the registers in mapping tables, in address order.

### Register Conventions

The register conventions specific to this section are listed in the following table.

**Table 4. Register Conventions**

| Convention | Description                |
|------------|----------------------------|
| R          | Read register or bits      |
| W          | Write register or bits     |
| L          | Logical register or bits   |
| C          | Clearable register or bits |
| #          | Access is bit specific     |

### Register Mapping Tables

The enCoRe V LV device has a total register address space of 512 bytes. The register space is also referred to as I/O space and is broken into two parts: Bank 0 (user space) and Bank 1 (configuration space). The XIO bit in the Flag register (CPU\_F) determines which bank the user is currently in. When the XIO bit is set, the user is said to be in the 'extended' address space or the 'configuration' registers.

Table 5. Register Map Bank 0 Table: User Space

| Name    | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name      | Addr (0,Hex) | Access | Name      | Addr (0,Hex) | Access |
|---------|--------------|--------|------|--------------|--------|-----------|--------------|--------|-----------|--------------|--------|
| PRT0DR  | 00           | RW     |      | 40           |        |           | 80           |        |           | C0           |        |
| PRT0IE  | 01           | RW     |      | 41           |        |           | 81           |        |           | C1           |        |
|         | 02           |        |      | 42           |        |           | 82           |        |           | C2           |        |
|         | 03           |        |      | 43           |        |           | 83           |        |           | C3           |        |
| PRT1DR  | 04           | RW     |      | 44           |        |           | 84           |        |           | C4           |        |
| PRT1IE  | 05           | RW     |      | 45           |        |           | 85           |        |           | C5           |        |
|         | 06           |        |      | 46           |        |           | 86           |        |           | C6           |        |
|         | 07           |        |      | 47           |        |           | 87           |        |           | C7           |        |
| PRT2DR  | 08           | RW     |      | 48           |        |           | 88           |        | I2C_XCFG  | C8           | RW     |
| PRT2IE  | 09           | RW     |      | 49           |        |           | 89           |        | I2C_XSTAT | C9           | R      |
|         | 0A           |        |      | 4A           |        |           | 8A           |        | I2C_ADDR  | CA           | RW     |
|         | 0B           |        |      | 4B           |        |           | 8B           |        | I2C_BP    | CB           | R      |
| PRT3DR  | 0C           | RW     |      | 4C           |        |           | 8C           |        | I2C_CP    | CC           | R      |
| PRT3IE  | 0D           | RW     |      | 4D           |        |           | 8D           |        | CPU_BP    | CD           | RW     |
|         | 0E           |        |      | 4E           |        |           | 8E           |        | CPU_CP    | CE           | R      |
|         | 0F           |        |      | 4F           |        |           | 8F           |        | I2C_BUF   | CF           | RW     |
| PRT4DR  | 10           | RW     |      | 50           |        |           | 90           |        | CUR_PP    | D0           | RW     |
| PRT4IE  | 11           | RW     |      | 51           |        |           | 91           |        | STK_PP    | D1           | RW     |
|         | 12           |        |      | 52           |        |           | 92           |        |           | D2           |        |
|         | 13           |        |      | 53           |        |           | 93           |        | IDX_PP    | D3           | RW     |
|         | 14           |        |      | 54           |        |           | 94           |        | MVR_PP    | D4           | RW     |
|         | 15           |        |      | 55           |        |           | 95           |        | MVW_PP    | D5           | RW     |
|         | 16           |        |      | 56           |        |           | 96           |        | I2C_CFG   | D6           | RW     |
|         | 17           |        |      | 57           |        |           | 97           |        | I2C_SCR   | D7           | #      |
|         | 18           |        |      | 58           |        |           | 98           |        | I2C_DR    | D8           | RW     |
|         | 19           |        |      | 59           |        |           | 99           |        |           | D9           |        |
|         | 1A           |        |      | 5A           |        |           | 9A           |        | INT_CLR0  | DA           | RW     |
|         | 1B           |        |      | 5B           |        |           | 9B           |        | INT_CLR1  | DB           | RW     |
|         | 1C           |        |      | 5C           |        |           | 9C           |        | INT_CLR2  | DC           | RW     |
|         | 1D           |        |      | 5D           |        |           | 9D           |        | INT_CLR3  | DD           | RW     |
|         | 1E           |        |      | 5E           |        |           | 9E           |        | INT_MSK2  | DE           | RW     |
|         | 1F           |        |      | 5F           |        |           | 9F           |        | INT_MSK1  | DF           | RW     |
|         | 20           |        |      | 60           |        |           | A0           |        | INT_MSK0  | E0           | RW     |
|         | 21           |        |      | 61           |        |           | A1           |        | INT_SW_EN | E1           | RW     |
|         | 22           |        |      | 62           |        |           | A2           |        | INT_VC    | E2           | RC     |
|         | 23           |        |      | 63           |        |           | A3           |        | RES_WDT   | E3           | W      |
|         | 24           |        |      | 64           |        |           | A4           |        | INT_MSK3  | E4           | RW     |
|         | 25           |        |      | 65           |        |           | A5           |        |           | E5           |        |
|         | 26           |        |      | 66           |        |           | A6           |        |           | E6           |        |
|         | 27           |        |      | 67           |        |           | A7           |        |           | E7           |        |
|         | 28           |        |      | 68           |        |           | A8           |        |           | E8           |        |
| SPI_TXR | 29           | W      |      | 69           |        |           | A9           |        |           | E9           |        |
| SPI_RXR | 2A           | R      |      | 6A           |        |           | AA           |        |           | EA           |        |
| SPI_CR  | 2B           | #      |      | 6B           |        |           | AB           |        |           | EB           |        |
|         | 2C           |        |      | 6C           |        |           | AC           |        |           | EC           |        |
|         | 2D           |        |      | 6D           |        |           | AD           |        |           | ED           |        |
|         | 2E           |        |      | 6E           |        |           | AE           |        |           | EE           |        |
|         | 2F           |        |      | 6F           |        |           | AF           |        |           | EF           |        |
|         | 30           |        |      | 70           |        | PT0_CFG   | B0           | RW     |           | F0           |        |
|         | 31           |        |      | 71           |        | PT0_DATA1 | B1           | RW     |           | F1           |        |
|         | 32           |        |      | 72           |        | PT0_DATA0 | B2           | RW     |           | F2           |        |
|         | 33           |        |      | 73           |        | PT1_CFG   | B3           | RW     |           | F3           |        |
|         | 34           |        |      | 74           |        | PT1_DATA1 | B4           | RW     |           | F4           |        |
|         | 35           |        |      | 75           |        | PT1_DATA0 | B5           | RW     |           | F5           |        |
|         | 36           |        |      | 76           |        | PT2_CFG   | B6           | RW     |           | F6           |        |
|         | 37           |        |      | 77           |        | PT2_DATA1 | B7           | RW     | CPU_F     | F7           | RL     |
|         | 38           |        |      | 78           |        | PT2_DATA0 | B8           | RW     |           | F8           |        |
|         | 39           |        |      | 79           |        |           | B9           |        |           | F9           |        |
|         | 3A           |        |      | 7A           |        |           | BA           |        |           | FA           |        |
|         | 3B           |        |      | 7B           |        |           | BB           |        |           | FB           |        |
|         | 3C           |        |      | 7C           |        |           | BC           |        |           | FC           |        |
|         | 3D           |        |      | 7D           |        |           | BD           |        |           | FD           |        |
|         | 3E           |        |      | 7E           |        |           | BE           |        | CPU_SCR1  | FE           | #      |
|         | 3F           |        |      | 7F           |        |           | BF           |        | CPU_SCR0  | FF           | #      |

Gray fields are reserved and should not be accessed. # Access is bit specific.

**Table 6. Register Map Bank 1 Table: Configuration Space**

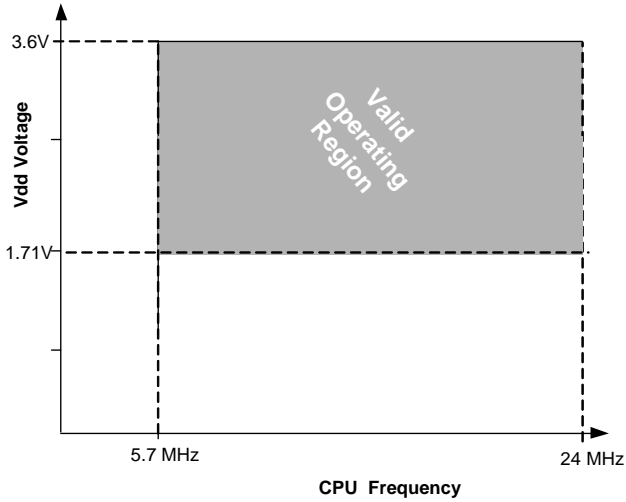
| Name    | Addr (1,Hex) | Access | Name    | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name     | Addr (1,Hex) | Access |
|---------|--------------|--------|---------|--------------|--------|------|--------------|--------|----------|--------------|--------|
| PRT0DM0 | 00           | RW     |         | 40           |        |      | 80           |        |          | C0           |        |
| PRT0DM1 | 01           | RW     |         | 41           |        |      | 81           |        |          | C1           |        |
|         | 02           |        |         | 42           |        |      | 82           |        |          | C2           |        |
|         | 03           |        |         | 43           |        |      | 83           |        |          | C3           |        |
| PRT1DM0 | 04           | RW     |         | 44           |        |      | 84           |        |          | C4           |        |
| PRT1DM1 | 05           | RW     |         | 45           |        |      | 85           |        |          | C5           |        |
|         | 06           |        |         | 46           |        |      | 86           |        |          | C6           |        |
|         | 07           |        |         | 47           |        |      | 87           |        |          | C7           |        |
| PRT2DM0 | 08           | RW     |         | 48           |        |      | 88           |        |          | C8           |        |
| PRT2DM1 | 09           | RW     |         | 49           |        |      | 89           |        |          | C9           |        |
|         | 0A           |        |         | 4A           |        |      | 8A           |        |          | CA           |        |
|         | 0B           |        |         | 4B           |        |      | 8B           |        |          | CB           |        |
| PRT3DM0 | 0C           | RW     |         | 4C           |        |      | 8C           |        |          | CC           |        |
| PRT3DM1 | 0D           | RW     |         | 4D           |        |      | 8D           |        |          | CD           |        |
|         | 0E           |        |         | 4E           |        |      | 8E           |        |          | CE           |        |
|         | 0F           |        |         | 4F           |        |      | 8F           |        |          | CF           |        |
| PRT4DM0 | 10           | RW     |         | 50           |        |      | 90           |        |          | D0           |        |
| PRT4DM1 | 11           | RW     |         | 51           |        |      | 91           |        |          | D1           |        |
|         | 12           |        |         | 52           |        |      | 92           |        |          | D2           |        |
|         | 13           |        |         | 53           |        |      | 93           |        |          | D3           |        |
|         | 14           |        |         | 54           |        |      | 94           |        |          | D4           |        |
|         | 15           |        |         | 55           |        |      | 95           |        |          | D5           |        |
|         | 16           |        |         | 56           |        |      | 96           |        |          | D6           |        |
|         | 17           |        |         | 57           |        |      | 97           |        |          | D7           |        |
|         | 18           |        |         | 58           |        |      | 98           |        |          | D8           |        |
|         | 19           |        |         | 59           |        |      | 99           |        |          | D9           |        |
|         | 1A           |        |         | 5A           |        |      | 9A           |        |          | DA           |        |
|         | 1B           |        |         | 5B           |        |      | 9B           |        |          | DB           |        |
|         | 1C           |        |         | 5C           |        |      | 9C           |        | IO_CFG   | DC           | RW     |
|         | 1D           |        |         | 5D           |        |      | 9D           |        | OUT_P1   | DD           | RW     |
|         | 1E           |        |         | 5E           |        |      | 9E           |        |          | DE           |        |
|         | 1F           |        |         | 5F           |        |      | 9F           |        |          | DF           |        |
|         | 20           |        |         | 60           |        |      | A0           |        | OSC_CR0  | E0           | RW     |
|         | 21           |        |         | 61           |        |      | A1           |        | ECO_CFG  | E1           | #      |
|         | 22           |        |         | 62           |        |      | A2           |        | OSC_CR2  | E2           | RW     |
|         | 23           |        |         | 63           |        |      | A3           |        | VLT_CR   | E3           | RW     |
|         | 24           |        |         | 64           |        |      | A4           |        | VLT_CMP  | E4           | R      |
|         | 25           |        |         | 65           |        |      | A5           |        |          | E5           |        |
|         | 26           |        |         | 66           |        |      | A6           |        |          | E6           |        |
|         | 27           |        |         | 67           |        |      | A7           |        |          | E7           |        |
|         | 28           |        |         | 68           |        |      | A8           |        | IMO_TR   | E8           | W      |
| SPI_CFG | 29           | RW     |         | 69           |        |      | A9           |        | ILO_TR   | E9           | W      |
|         | 2A           |        |         | 6A           |        |      | AA           |        |          | EA           |        |
|         | 2B           |        |         | 6B           |        |      | AB           |        | SLP_CFG  | EB           | RW     |
|         | 2C           |        | TMP_DR0 | 6C           | RW     |      | AC           |        | SLP_CFG2 | EC           | RW     |
|         | 2D           |        | TMP_DR1 | 6D           | RW     |      | AD           |        | SLP_CFG3 | ED           | RW     |
|         | 2E           |        | TMP_DR2 | 6E           | RW     |      | AE           |        |          | EE           |        |
|         | 2F           |        | TMP_DR3 | 6F           | RW     |      | AF           |        |          | EF           |        |
|         | 30           |        |         | 70           |        |      | B0           |        |          | F0           |        |
|         | 31           |        |         | 71           |        |      | B1           |        |          | F1           |        |
|         | 32           |        |         | 72           |        |      | B2           |        |          | F2           |        |
|         | 33           |        |         | 73           |        |      | B3           |        |          | F3           |        |
|         | 34           |        |         | 74           |        |      | B4           |        |          | F4           |        |
|         | 35           |        |         | 75           |        |      | B5           |        |          | F5           |        |
|         | 36           |        |         | 76           |        |      | B6           |        |          | F6           |        |
|         | 37           |        |         | 77           |        |      | B7           |        | CPU_F    | F7           | RL     |
|         | 38           |        |         | 78           |        |      | B8           |        |          | F8           |        |
|         | 39           |        |         | 79           |        |      | B9           |        |          | F9           |        |
|         | 3A           |        |         | 7A           |        |      | BA           |        |          | FA           |        |
|         | 3B           |        |         | 7B           |        |      | BB           |        |          | FB           |        |
|         | 3C           |        |         | 7C           |        |      | BC           |        |          | FC           |        |
|         | 3D           |        |         | 7D           |        |      | BD           |        |          | FD           |        |
|         | 3E           |        |         | 7E           |        |      | BE           |        |          | FE           |        |
|         | 3F           |        |         | 7F           |        |      | BF           |        |          | FF           |        |

Gray fields are reserved and should not be accessed. # Access is bit specific.

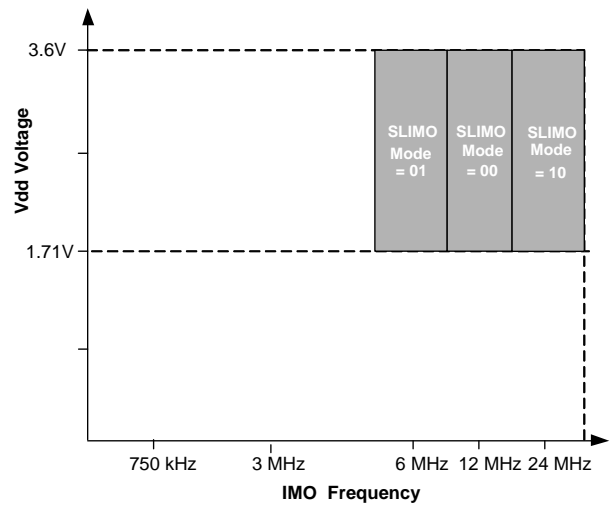
## Electrical Specifications

This section presents the DC and AC electrical specifications of the enCoRe V LV devices. For the most up to date electrical specifications, verify that you have the most recent datasheet available by visiting the company web site at <http://www.cypress.com>.

**Figure 8. Voltage versus CPU Frequency**



**Figure 9. IMO Frequency Trim Options**



### Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

**Table 7. Absolute Maximum Ratings**

| Symbol           | Description                                | Conditions   | Min                   | Typ | Max                   | Units |
|------------------|--|--|-----------------------|-----|-----------------------|-------|
| T <sub>STG</sub> | Storage temperature <sup>[3]</sup>         | Higher storage temperatures reduces data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability. | -55                   | +25 | +125                  | °C    |
| V <sub>dd</sub>  | Supply voltage relative to V <sub>ss</sub> |  | -0.5                  | -   | +6.0                  | V     |
| V <sub>IO</sub>  | DC input voltage                           |  | V <sub>ss</sub> - 0.5 | -   | V <sub>dd</sub> + 0.5 | V     |
| V <sub>IOZ</sub> | DC voltage applied to tristate             |  | V <sub>ss</sub> - 0.5 | -   | V <sub>dd</sub> + 0.5 | V     |
| I <sub>MIO</sub> | Maximum current into any Port pin          |  | -25                   | -   | +50                   | mA    |
| ESD              | Electro static discharge voltage           | Human body model ESD   | 2000                  | -   | -                     | V     |
| LU               | Latch up current                           | In accordance with JESD78 standard   | -                     | -   | 200                   | mA    |

### Operating Temperature

**Table 8. Operating Temperature**

| Symbol          | Description   | Conditions   | Min | Typ | Max | Units |
|-----------------|---|--|-----|-----|-----|-------|
| T <sub>AC</sub> | Ambient commercial temperature                        |  | 0   |     | +70 | °C    |
| T <sub>JC</sub> | Operational commercial die temperature <sup>[4]</sup> | The temperature rise from ambient to junction is package specific. Refer the table " <a href="#">Thermal Impedances</a> " on page 32. The user must limit the power consumption to comply with this requirement. | 0   |     | +85 | °C    |

#### Notes

3. Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrade reliability.
4. The temperature rise from ambient to junction is package specific. See [Thermal Impedances on page 32](#). The user must limit the power consumption to comply with this requirement.

## DC Electrical Characteristics

### DC Chip Level Specifications

Table 9 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 9. DC Chip Level Specifications**

| Symbol                | Description                                    | Conditions   | Min  | Typ | Max | Units |
|-----------------------|--|--|------|-----|-----|-------|
| Vdd <sup>[5, 6]</sup> | Supply voltage                                 | See table titled <a href="#">DC POR and LVD Specifications on page 23</a> .    | 1.71 | –   | 3.6 | V     |
| I <sub>DD24</sub>     | Supply current, IMO = 24 MHz                   | Conditions are Vdd ≤ 3.0 V, T <sub>A</sub> = 25 °C, CPU = 24 MHz<br>No I2C/SPI | –    | 2.9 | 4.0 | mA    |
| I <sub>DD12</sub>     | Supply current, IMO = 12 MHz                   | Conditions are Vdd ≤ 3.0 V, T <sub>A</sub> = 25 °C, CPU = 12 MHz<br>No I2C/SPI | –    | 1.7 | 2.6 | mA    |
| I <sub>DD6</sub>      | Supply current, IMO = 6 MHz                    | Conditions are Vdd ≤ 3.0 V, T <sub>A</sub> = 25 °C, CPU = 6 MHz<br>No I2C/SPI  | –    | 1.2 | 1.8 | mA    |
| I <sub>SB1</sub>      | Standby current with POR, LVD, and Sleep timer | Vdd ≤ 3.0V, T <sub>A</sub> = 25 °C, I/O regulator turned off                   | –    | 1.1 | 1.5 | μA    |
| I <sub>SB0</sub>      | Deep sleep current                             | Vdd ≤ 3.0 V, T <sub>A</sub> = 25 °C, I/O regulator turned off                  | –    | 0.1 | –   | μA    |

### Notes

- When Vdd remains in the range from 1.71 V to 1.9 V for more than 50 μsec, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 μsec to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SR<sub>POWER\_UP</sub> parameter.
- If powering down in standby sleep mode, to properly detect and recover from a VDD brown out condition any of the following actions must be taken:
  - Bring the device out of sleep before powering down.
  - Assure that VDD falls below 100 mV before powering backup.
  - Set the No Buzz bit in the OSC\_CR0 register to keep the voltage monitoring circuit powered during sleep.
  - Increase the buzz rate to assure that the falling edge of VDD is captured. The rate is configured through the PSSDC bits in the SLP\_CFG register.
 For the referenced registers, refer to the enCoRe V Technical Reference Manual. In deep sleep mode, additional low power voltage monitoring circuitry allows VDD brown out conditions to be detected for edge rates slower than 1 V/ms.

**DC General Purpose I/O Specifications [7]**

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 1.71 V to 3.6 V and  $0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$ . Typical parameters apply to 3.3 V at 25 °C. These are for design guidance only.

**Table 10. 3.0 V to 3.6 V DC GPIO Specifications**

| Symbol            | Description  | Conditions  | Min                   | Typ   | Max  | Units |
|-------------------|--|---|-----------------------|-------|------|-------|
| R <sub>PU</sub>   | Pull-up resistor   | –   | 4                     | 5.6   | 8    | kΩ    |
| V <sub>OH1</sub>  | High output voltage<br>Port 2 or 3 pins  | IOH ≤ 10 μA, maximum of 10 mA source current in all I/Os  | V <sub>DD</sub> – 0.2 | –     | –    | V     |
| V <sub>OH2</sub>  | High output voltage<br>Port 2 or 3 pins  | IOH = 1 mA, maximum of 20 mA source current in all I/Os   | V <sub>DD</sub> – 0.9 | –     | –    | V     |
| V <sub>OH3</sub>  | High output voltage<br>Port 0 or 1 pins with LDO regulator disabled for Port 1 | IOH < 10 μA, maximum of 10 mA source current in all I/Os  | V <sub>DD</sub> – 0.2 | –     | –    | V     |
| V <sub>OH4</sub>  | High output voltage<br>Port 0 or 1 pins with LDO regulator disabled for Port 1 | IOH = 5 mA, maximum of 20 mA source current in all I/Os   | V <sub>DD</sub> – 0.9 | –     | –    | V     |
| V <sub>OH5</sub>  | High output voltage<br>Port 1 pins with LDO regulator enabled for 3 V out      | IOH < 10 μA, V <sub>DD</sub> > 3.1 V, maximum of 4 I/Os all sourcing 5 mA   | 2.85                  | 3.00  | 3.3  | V     |
| V <sub>OH6</sub>  | High output voltage<br>Port 1 pins with LDO regulator enabled for 3 V out      | IOH = 5 mA, V <sub>DD</sub> > 3.1 V, maximum of 20 mA source current in all I/Os  | 2.20                  | –     | –    | V     |
| V <sub>OH7</sub>  | High output voltage<br>Port 1 pins with LDO enabled for 2.5 V out              | IOH < 10 μA, V <sub>DD</sub> > 2.7 V, maximum of 20 mA source current in all I/Os   | 2.35                  | 2.50  | 2.75 | V     |
| V <sub>OH8</sub>  | High output voltage<br>Port 1 pins with LDO enabled for 2.5 V out              | IOH = 2 mA, V <sub>DD</sub> > 2.7 V, maximum of 20 mA source current in all I/Os  | 1.90                  | –     | –    | V     |
| V <sub>OH9</sub>  | High output voltage<br>Port 1 pins with LDO enabled for 1.8 V out              | IOH < 10 μA, V <sub>DD</sub> > 2.7 V, maximum of 20 mA source current in all I/Os   | 1.60                  | 1.80  | 2.1  | V     |
| V <sub>OH10</sub> | High output voltage<br>Port 1 pins with LDO enabled for 1.8 V out              | IOH = 1 mA, V <sub>DD</sub> > 2.7 V, maximum of 20 mA source current in all I/Os  | 1.20                  | –     | –    | V     |
| V <sub>OL</sub>   | Low output voltage   | IOL = 25 mA, V <sub>DD</sub> > 3.3 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]) | –                     | –     | 0.75 | V     |
| V <sub>IL</sub>   | Input low voltage  | –   | –                     | –     | 0.80 | V     |
| V <sub>IH</sub>   | Input high voltage   | –   | 2.00                  | –     | –    | V     |
| V <sub>H</sub>    | Input hysteresis voltage   | –   | –                     | 80    | –    | mV    |
| I <sub>IL</sub>   | Input leakage (absolute value)   | –   | –                     | 0.001 | 1    | μA    |
| C <sub>PIN</sub>  | Pin capacitance  | Package and pin dependent<br>Temp = 25 °C   | 0.5                   | 1.7   | 5    | pF    |

**Note**

7. **Errata:** P1[3], P1[6], and P1[7] pins are susceptible to latch up when the I/O sink current exceeds 25 mA per pin on these pins. Add a series resistor > 300 Ω to P1[3], P1[6], and P1[7] pins to restrict current to within latch up limits. For more information please refer to "Errata" on page 35.

**Table 11. 2.4 V to 3.0 V DC GPIO Specifications**

| Symbol            | Description  | Conditions   | Min                   | Typ   | Max  | Units |
|-------------------|--|--|-----------------------|-------|------|-------|
| R <sub>PU</sub>   | Pull-up resistor   | –  | 4                     | 5.6   | 8    | kΩ    |
| V <sub>OH1</sub>  | High output voltage<br>Port 2 or 3 pins  | I <sub>OH</sub> < 10 μA, maximum of 10 mA source current in all I/Os   | V <sub>dd</sub> – 0.2 | –     | –    | V     |
| V <sub>OH2</sub>  | High output voltage<br>Port 2 or 3 pins  | I <sub>OH</sub> = 0.2 mA, maximum of 10 mA source current in all I/Os  | V <sub>dd</sub> – 0.4 | –     | –    | V     |
| V <sub>OH3</sub>  | High output voltage<br>Port 0 or 1 pins with LDO regulator disabled for Port 1 | I <sub>OH</sub> < 10 μA, maximum of 10 mA source current in all I/Os   | V <sub>dd</sub> – 0.2 | –     | –    | V     |
| V <sub>OH4</sub>  | High output voltage<br>Port 0 or 1 pins with LDO regulator disabled for Port 1 | I <sub>OH</sub> = 2 mA, maximum of 10 mA source current in all I/Os  | V <sub>dd</sub> – 0.5 | –     | –    | V     |
| V <sub>OH5A</sub> | High output voltage<br>Port 1 pins with LDO enabled for 1.8 V out              | I <sub>OH</sub> < 10 μA, V <sub>dd</sub> > 2.4V, maximum of 20 mA source current in all I/Os.  | 1.50                  | 1.80  | 2.10 | V     |
| V <sub>OH6A</sub> | High output voltage<br>Port 1 pins with LDO enabled for 1.8 V out              | I <sub>OH</sub> = 1 mA, V <sub>dd</sub> > 2.4V, maximum of 20 mA source current in all I/Os  | 1.20                  | –     | –    | V     |
| V <sub>OL</sub>   | Low output voltage   | I <sub>OL</sub> = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]) | –                     | –     | 0.75 | V     |
| V <sub>IL</sub>   | Input low voltage  | –  | –                     | –     | 0.72 | V     |
| V <sub>IH</sub>   | Input high voltage   | –  | 1.4                   | –     | –    | V     |
| V <sub>H</sub>    | Input hysteresis voltage   | –  | –                     | 80    | –    | mV    |
| I <sub>IL</sub>   | Input leakage (absolute value)   | –  | –                     | 0.001 | 1    | μA    |
| C <sub>PIN</sub>  | Capacitive load on pins  | Package and pin dependent<br>Temp = 25 °C  | 0.5                   | 1.7   | 5    | pF    |

**Table 12. 1.71 V to 2.4 V DC GPIO Specifications**

| Symbol           | Description  | Conditions  | Min                    | Typ   | Max                   | Units |
|------------------|--|---|------------------------|-------|-----------------------|-------|
| R <sub>PU</sub>  | Pull-up resistor   | –   | 4                      | 5.6   | 8                     | kΩ    |
| V <sub>OH1</sub> | High output voltage<br>Port 2 or 3 pins  | I <sub>OH</sub> = 10 μA, maximum of 10 mA source current in all I/Os  | V <sub>dd</sub> – 0.2  | –     | –                     | V     |
| V <sub>OH2</sub> | High output voltage<br>Port 2 or 3 pins  | I <sub>OH</sub> = 0.5 mA, maximum of 10 mA source current in all I/Os   | V <sub>dd</sub> – 0.5  | –     | –                     | V     |
| V <sub>OH3</sub> | High output voltage<br>Port 0 or 1 pins with LDO regulator disabled for Port 1 | I <sub>OH</sub> = 100 μA, maximum of 10 mA source current in all I/Os   | V <sub>dd</sub> – 0.2  | –     | –                     | V     |
| V <sub>OH4</sub> | High output voltage<br>Port 0 or 1 pins with LDO regulator disabled for Port 1 | I <sub>OH</sub> = 2 mA, maximum of 10 mA source current in all I/Os   | V <sub>dd</sub> – 0.5  | –     | –                     | V     |
| V <sub>OL</sub>  | Low output voltage   | I <sub>OL</sub> = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]) | –                      | –     | 0.4                   | V     |
| V <sub>IL</sub>  | Input low voltage  | –   | –                      | –     | 0.3 x V <sub>dd</sub> | V     |
| V <sub>IH</sub>  | Input high voltage   | –   | 0.65 x V <sub>dd</sub> | –     | –                     | V     |
| V <sub>H</sub>   | Input hysteresis voltage   | –   | –                      | 80    | –                     | mV    |
| I <sub>IL</sub>  | Input leakage (absolute value)   | –   | –                      | 0.001 | 1                     | μA    |
| C <sub>PIN</sub> | Capacitive load on pins  | Package and pin dependent.<br>Temp = 25 °C  | 0.5                    | 1.7   | 5                     | pF    |

## ADC Electrical Specifications

**Table 13. ADC User Module Electrical Specifications**

| Symbol                 | Description                  | Conditions  | Min                    | Typ                    | Max                    | Units |
|------------------------|------------------------------|---|------------------------|------------------------|------------------------|-------|
| <b>Input</b>           |                              |   |                        |                        |                        |       |
| V <sub>IN</sub>        | Input voltage range          | –   | 0                      | –                      | VREFADC                | V     |
| C <sub>IIN</sub>       | Input capacitance            | –   |                        | –                      | 5                      | pF    |
| R <sub>IN</sub>        | Input resistance             | Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution                 | 1/(500fF × data clock) | 1/(400fF × data clock) | 1/(300fF × data clock) | Ω     |
| <b>Reference</b>       |                              |   |                        |                        |                        |       |
| V <sub>REFADC</sub>    | ADC reference voltage        | –   | 1.14                   | –                      | 1.26                   | V     |
| <b>Conversion Rate</b> |                              |   |                        |                        |                        |       |
| F <sub>CLK</sub>       | Data clock                   | Source is chip's internal main oscillator. See AC Chip-Level Specifications for accuracy  | 2.25                   | –                      | 6                      | MHz   |
| S8                     | 8-bit sample rate            | Data Clock set to 6 MHz.<br>Sample Rate = 0.001/<br>(2 <sup>Resolution</sup> /Data Clock) | –                      | –                      | –                      | ksps  |
| S10                    | 10-bit sample rate           | Data Clock set to 6 MHz.<br>Sample Rate = 0.001/<br>(2 <sup>Resolution</sup> /Data Clock) | –                      | 5.859                  | –                      | ksps  |
| <b>DC Accuracy</b>     |                              |   |                        |                        |                        |       |
| RES                    | Resolution                   | Can be set to 8-, 9-, or 10-bit   | 8                      | –                      | 10                     | bits  |
| DNL                    | Differential nonlinearity    | –   | –1                     | –                      | +2                     | LSB   |
| INL                    | Integral nonlinearity        | –   | –2                     | –                      | +2                     | LSB   |
| E <sub>Offset</sub>    | Offset error                 | 8-bit resolution  | 0                      | 3.2                    | 19.2                   | LSB   |
|                        |                              | 10-bit resolution   | 0                      | 12.8                   | 76.8                   | LSB   |
| E <sub>gain</sub>      | Gain error                   | For any resolution  | –5                     | –                      | +5                     | %FSR  |
| <b>Power</b>           |                              |   |                        |                        |                        |       |
| I <sub>ADC</sub>       | Operating current            | –   | –                      | 2.1                    | 2.6                    | mA    |
| PSRR                   | Power supply rejection ratio | PSRR (V <sub>dd</sub> > 3.0 V)  | –                      | 24                     | –                      | dB    |
|                        |                              | PSRR (V <sub>dd</sub> < 3.0 V)  | –                      | 30                     | –                      | dB    |

### DC POR and LVD Specifications

Table 14 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 14. DC POR and LVD Specifications**

| Symbol      | Description   | Min  | Typ  | Max  | Units |
|-------------|---|------|------|------|-------|
| $V_{PPOR0}$ | Vdd Value for PPOR Trip <sup>(8)</sup><br>PORLEV[1:0] = 00b, HPOR = 0 | 1.61 | 1.66 | 1.71 | V     |
| $V_{PPOR1}$ | PORLEV[1:0] = 00b, HPOR = 1   |      | 2.36 | 2.41 | V     |
| $V_{PPOR2}$ | PORLEV[1:0] = 01b, HPOR = 1   |      | 2.60 | 2.66 | V     |
| $V_{PPOR3}$ | PORLEV[1:0] = 10b, HPOR = 1   |      | 2.82 | 2.95 | V     |
| $V_{LVD0}$  | Vdd Value for LVD Trip<br>VM[2:0] = 000b <sup>(9)</sup>               | 2.40 | 2.45 | 2.51 | V     |
| $V_{LVD1}$  | VM[2:0] = 001b <sup>(10)</sup>  | 2.64 | 2.71 | 2.78 | V     |
| $V_{LVD2}$  | VM[2:0] = 010b <sup>(11)</sup>  | 2.85 | 2.92 | 2.99 | V     |
| $V_{LVD3}$  | VM[2:0] = 011b  | 2.95 | 3.02 | 3.09 | V     |
| $V_{LVD4}$  | VM[2:0] = 100b  | 3.06 | 3.13 | 3.20 | V     |
| $V_{LVD5}$  | VM[2:0] = 101b  | 1.84 | 1.9  | 2.32 | V     |
| $V_{LVD6}$  | VM[2:0] = 110b <sup>(12)</sup>  | 1.75 | 1.8  | 1.84 | V     |

### DC Programming Specifications

Table 15 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 15. DC Programming Specifications**

| Symbol                | Description  | Min                    | Typ | Max                  | Units  |
|-----------------------|--|------------------------|-----|----------------------|--------|
| $V_{ddIWRITE}$        | Supply voltage for flash write operations  | 1.71                   | –   | 5.25                 | V      |
| $I_{DDP}$             | Supply current during programming or verify  | –                      | 5   | 25                   | mA     |
| $V_{ILP}$             | Input low voltage during programming or verify   | –                      | –   | $V_{IL}^{[11]}$      | V      |
| $V_{IHP}$             | Input high voltage during programming or verify  | 1.71                   | –   | $V_{ddIWRITE} + 0.3$ | V      |
| $I_{ILP}$             | Input current when applying $V_{ilp}$ to P1[0] or P1[1] during programming or verify <sup>(13)</sup> | –                      | –   | 0.2                  | mA     |
| $I_{IHP}$             | Input current when applying $V_{ihp}$ to P1[0] or P1[1] during programming or verify <sup>(13)</sup> | –                      | –   | 1.5                  | mA     |
| $V_{OLP}$             | Output low voltage during programming or verify  | –                      | –   | $V_{ss} + 0.75$      | V      |
| $V_{OHP}$             | Output high voltage during programming or verify   | $V_{ddIWRITE} - 0.9$ V | –   | $V_{ddIWRITE}$       | V      |
| Flash <sub>ENPB</sub> | Flash write endurance <sup>(15)</sup>  | 50,000                 | –   | –                    | Cycles |
| Flash <sub>DR</sub>   | Flash data retention <sup>(16)</sup>   | 10                     | 20  | –                    | Years  |

### Notes

8. Vdd must be greater than or equal to 1.71 V during startup, reset from the XRES pin, or reset from watchdog.
9. Always greater than 50 mV above  $V_{PPOR1}$  for falling supply.
10. Always greater than 50 mV above  $V_{PPOR2}$  for falling supply.
11. Always greater than 50 mV above  $V_{PPOR3}$  for falling supply.
12. Always greater than 50 mV above  $V_{PPOR0}$  voltage for falling supply.
13. Driving internal pull-down resistor.
14. See appropriate DC General Purpose I/O Specifications [7] table.
15. Erase/write cycles per block.
16. Following maximum Flash write cycles at  $T_{amb} = 55C$  and  $T_j = 70C$ .

**AC Electrical Characteristics**
*AC Chip Level Specifications*

Table 16 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 16. AC Chip Level Specifications**

| Symbol                 | Description   | Conditions  | Min  | Typ | Max  | Units |
|------------------------|---|---|------|-----|------|-------|
| F <sub>CPU</sub>       | Processing frequency                                      |   | 5.7  | –   | 25.2 | MHz   |
| F <sub>32K1</sub>      | Internal low speed oscillator frequency                   | Trimmed for 3.3 V operation using factory trim values | 19   | 32  | 50   | kHz   |
| F <sub>32K_U</sub>     | Internal low speed oscillator (ILO) untrimmed frequency)  | –   | 13   | 32  | 82   | kHz   |
| F <sub>32K2</sub>      | Internal low speed oscillator frequency                   | Untrimmed   | 13   | 32  | 82   | kHz   |
| F <sub>IMO24</sub>     | Internal main oscillator stability for 24 MHz ± 5%        | –   | 22.8 | 24  | 25.2 | MHz   |
| F <sub>IMO12</sub>     | Internal main oscillator stability for 12 MHz             | –   | 11.4 | 12  | 12.6 | MHz   |
| F <sub>IMO6</sub>      | Internal main oscillator stability for 6 MHz              | –   | 5.7  | 6.0 | 6.3  | MHz   |
| DC <sub>IMO</sub>      | Duty Cycle of IMO   | –   | 40   | 50  | 60   | %     |
| DC <sub>ILO</sub>      | Internal low speed oscillator duty cycle                  | –   | 40   | 50  | 60   | %     |
| SR <sub>POWER_UP</sub> | Power supply slew rate                                    | –   | –    | –   | 250  | V/ms  |
| T <sub>XRST</sub>      | External reset pulse width at power up                    | After supply voltage is valid                         | 1    | –   | –    | ms    |
| T <sub>XRST2</sub>     | External reset pulse width after power up <sup>[17]</sup> | Applies after part has booted                         | 10   | –   | –    | μs    |

**Note**

17. The minimum required XRES pulse length is longer when programming the device (see Table 19 on page 26).

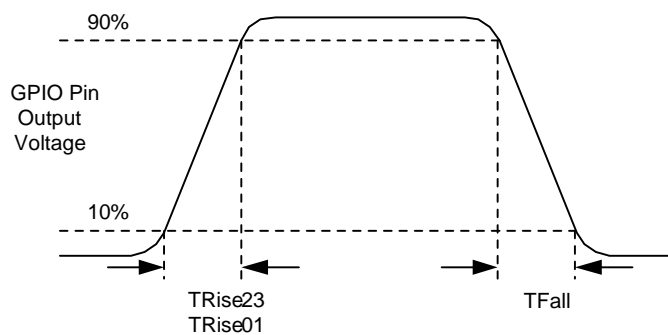
AC General Purpose IO Specifications

Table 17 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 17. AC GPIO Specifications

| Symbol            | Description   | Conditions  | Min | Typ | Max   | Units |
|-------------------|---|---|-----|-----|---|-------|
| F <sub>GPIO</sub> | GPIO operating frequency  | Normal strong mode, port 0, 1   | 0   | –   | 6 MHz for<br>1.71 V < V <sub>dd</sub> < 2.4 V | MHz   |
|                   |   |   | 0   | –   | 12 MHz for<br>2.4 V < V <sub>dd</sub> < 3.6 V |       |
|                   |   | Normal strong mode, Port 2, 3   | 0   | –   | 3 MHz for<br>1.71 V < V <sub>dd</sub> < 2.4 V | MHz   |
|                   |   |   |     |     | 6 MHz for<br>3.0 V < V <sub>dd</sub> < 3.6 V  |       |
| TRise23           | Rise time, strong mode, load = 50 pF<br>Ports 2 or 3            | V <sub>dd</sub> = 3.0 to 3.6 V, 10% – 90%                             | 15  | –   | 80  | ns    |
| TRise23L          | Rise time, strong mode low supply, load = 50 pF<br>Ports 2 or 3 | V <sub>dd</sub> = 1.71 to 3.0 V, 10% – 90%                            | 15  | –   | 80  | ns    |
| TRise01           | Rise time, strong mode, load = 50 pF<br>Ports 0 or 1            | V <sub>dd</sub> = 3.0 to 3.6 V, 10% – 90%<br>LDO enabled or disabled  | 10  | –   | 50  | ns    |
| TRise01L          | Rise time, strong mode low supply, load = 50 pF<br>Ports 0 or 1 | V <sub>dd</sub> = 1.71 to 3.0 V, 10% – 90%<br>LDO enabled or disabled | 15  | –   | 80  | ns    |
| TFall             | Fall time, strong mode, load = 50 pF, All Ports                 | V <sub>dd</sub> = 3.0 to 3.6 V, 10% – 90%                             | 10  | –   | 50  | ns    |
| TFallL            | Fall time, strong mode low supply, load = 50 pF, all ports      | V <sub>dd</sub> = 1.71 to 3.0 V, 10% - 90%                            | 10  | –   | 70  | ns    |

Figure 10. GPIO Timing Diagram



AC External Clock Specifications

Table 18 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. AC External Clock Specifications

| Symbol              | Description            | Conditions | Min   | Typ | Max  | Units |
|---------------------|------------------------|------------|-------|-----|------|-------|
| F <sub>OSCEXT</sub> | Frequency              | –          | 0.750 | –   | 25.2 | MHz   |
| –                   | High period            | –          | 20.6  | –   | 5300 | ns    |
| –                   | Low period             | –          | 20.6  | –   | –    | ns    |
| –                   | Power up IMO to switch | –          | 150   | –   | –    | μs    |

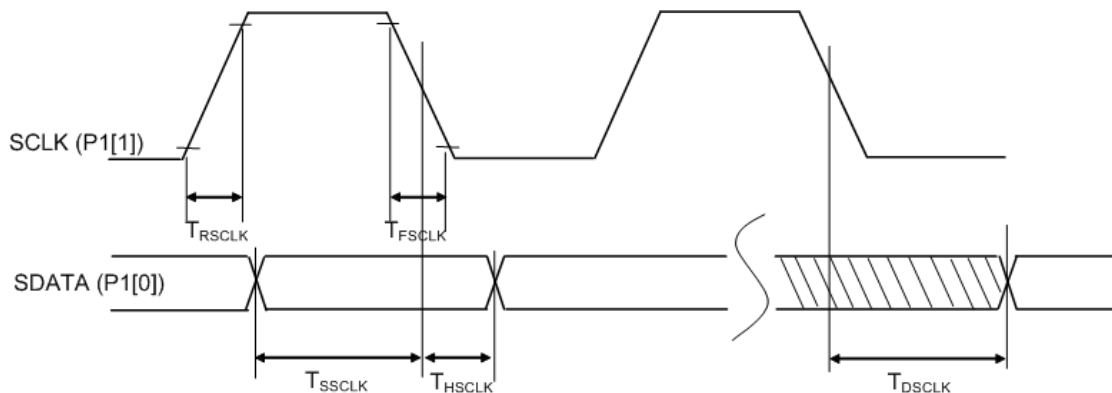
AC Programming Specifications

Table 19 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. AC Programming Specifications

| Symbol              | Description                               | Conditions  | Min | Typ | Max | Units |
|---------------------|---|---|-----|-----|-----|-------|
| T <sub>RSCLK</sub>  | Rise time of SCLK                         | –   | 1   | –   | 20  | ns    |
| T <sub>FSCLK</sub>  | Fall time of SCLK                         | –   | 1   | –   | 20  | ns    |
| T <sub>SSCLK</sub>  | Data set up time to falling edge of SCLK  | –   | 40  | –   | –   | ns    |
| T <sub>HSCLK</sub>  | Data hold time from falling edge of SCLK  | –   | 40  | –   | –   | ns    |
| F <sub>SCLK</sub>   | Frequency of SCLK                         | –   | 0   | –   | 8   | MHz   |
| T <sub>ERASEB</sub> | Flash erase time (block)                  | –   | –   | –   | 18  | ms    |
| T <sub>WRITE</sub>  | Flash block write time                    | –   | –   | –   | 25  | ms    |
| T <sub>DSCLK1</sub> | Data out delay from falling edge of SCLK  | 3.0 V < V <sub>dd</sub> < 3.6 V                             | –   | –   | 85  | ns    |
| T <sub>DSCLK2</sub> | Data out delay from falling edge of SCLK  | 1.71 V < V <sub>dd</sub> < 3.0 V                            | –   | –   | 130 | ns    |
| T <sub>XRST3</sub>  | External reset pulse width after power up | Required to enter programming mode when coming out of sleep | 263 | –   | –   | μs    |

Figure 11. Timing Diagram - AC Programming Cycle



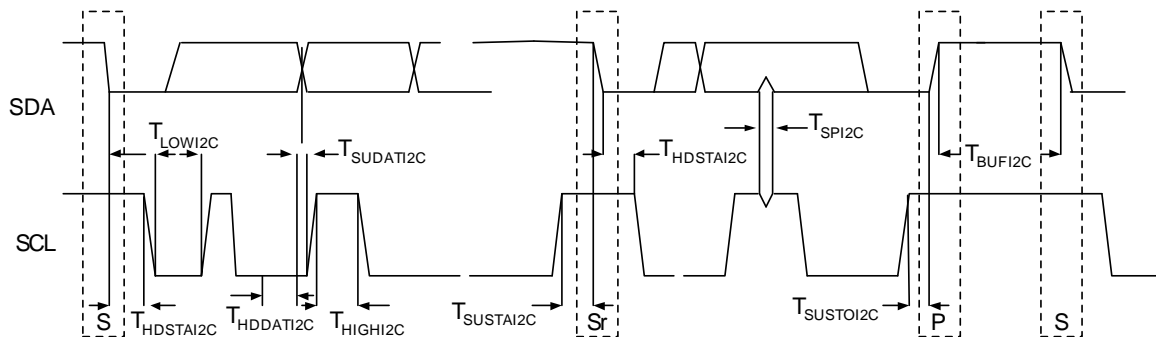
AC I<sup>2</sup>C Specifications

Table 20 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 20. AC Characteristics of the I<sup>2</sup>C SDA and SCL Pins

| Symbol                 | Description  | Standard Mode |     | Fast Mode           |     | Units |
|------------------------|--|---------------|-----|---------------------|-----|-------|
|                        |  | Min           | Max | Min                 | Max |       |
| F <sub>SCL I2C</sub>   | SCL clock frequency  | 0             | 100 | 0                   | 400 | kHz   |
| T <sub>HDSTAI2C</sub>  | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 4.0           | –   | 0.6                 | –   | μs    |
| T <sub>LOWI2C</sub>    | LOW period of the SCL clock  | 4.7           | –   | 1.3                 | –   | μs    |
| T <sub>HIGHI2C</sub>   | HIGH period of the SCL clock   | 4.0           | –   | 0.6                 | –   | μs    |
| T <sub>SUSTA I2C</sub> | Setup Time for a Repeated START condition  | 4.7           | –   | 0.6                 | –   | μs    |
| T <sub>HDDATI2C</sub>  | Data hold time   | 0             | –   | 0                   | –   | μs    |
| T <sub>SUDATI2C</sub>  | Data setup time  | 250           | –   | 100 <sup>(18)</sup> | –   | ns    |
| T <sub>SUSTOI2C</sub>  | Setup time for STOP condition  | 4.0           | –   | 0.6                 | –   | μs    |
| T <sub>BUFI2C</sub>    | Bus free time between a STOP and START condition   | 4.7           | –   | 1.3                 | –   | μs    |
| T <sub>SPI2C</sub>     | Pulse width of spikes are suppressed by the input filter                                     | –             | –   | 0                   | 50  | ns    |

Figure 12. Definition of Timing for Fast/Standard Mode on the I<sup>2</sup>C Bus



Note

18. A fast mode I2C bus device can be used in a standard mode I2C bus system, but the requirement  $t_{SU, DAT} \leq 250$  ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  $t_{rmax} + t_{SU, DAT} = 1000 + 250 = 1250$  ns (according to the standard mode I2C bus specification) before the SCL line is released.

**Table 21. SPI Master AC Specifications**

| Symbol                | Description             | Conditions   | Min       | Typ | Max    | Units |
|-----------------------|-------------------------|--|-----------|-----|--------|-------|
| F <sub>SCLK</sub>     | SCLK clock frequency    | V <sub>DD</sub> ≥ 2.4 V<br>V <sub>DD</sub> < 2.4 V | –         | –   | 6<br>3 | MHz   |
| DC                    | SCLK duty cycle         | –  | –         | 50  | –      | %     |
| T <sub>SETUP</sub>    | MISO to SCLK setup time | V <sub>DD</sub> ≥ 2.4 V<br>V <sub>DD</sub> < 2.4 V | 60<br>100 | –   | –      | ns    |
| T <sub>HOLD</sub>     | SCLK to MISO hold time  | –  | 40        | –   | –      | ns    |
| T <sub>OUT_VAL</sub>  | SCLK to MOSI valid time | –  | –         | –   | 40     | ns    |
| T <sub>OUT_HIGH</sub> | MOSI high time          | –  | 40        | –   | –      | ns    |

**Table 22. SPI Slave AC Specifications**

| Symbol                 | Description                    | Conditions   | Min    | Typ | Max     | Units |
|------------------------|--------------------------------|--|--------|-----|---------|-------|
| F <sub>SCLK</sub>      | SCLK clock frequency           | V <sub>DD</sub> ≥ 2.4 V<br>V <sub>DD</sub> < 2.4 V | –      | –   | 12<br>6 | MHz   |
| T <sub>LOW</sub>       | SCLK low time                  | –  | 41.67  | –   | –       | ns    |
| T <sub>HIGH</sub>      | SCLK high time                 | –  | 41.67  | –   | –       | ns    |
| T <sub>SETUP</sub>     | MOSI to SCLK setup time        | –  | 30     | –   | –       | ns    |
| T <sub>HOLD</sub>      | SCLK to MOSI hold time         | –  | 50     | –   | –       | ns    |
| T <sub>SS_MISO</sub>   | SS high to MISO valid          | –  | –      | –   | 153     | ns    |
| T <sub>SCLK_MISO</sub> | SCLK to MISO valid             | –  | –      | –   | 125     | ns    |
| T <sub>SS_HIGH</sub>   | SS high time                   | –  | –      | –   | 50      | ns    |
| T <sub>SS_CLK</sub>    | Time from SS low to first SCLK | –  | 2/SCLK | –   | –       | ns    |
| T <sub>CLK_SS</sub>    | Time from last SCLK to SS high | –  | 2/SCLK | –   | –       | ns    |

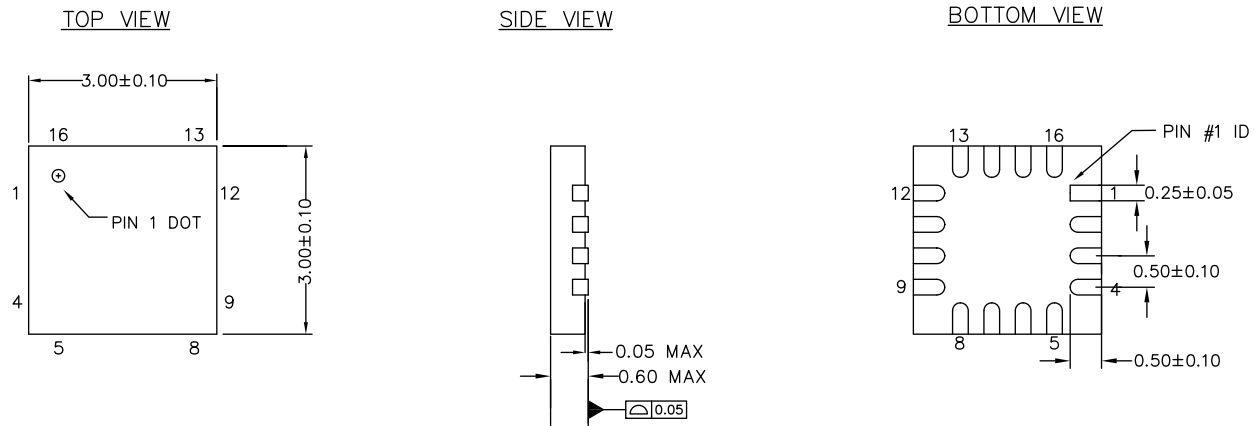
## Package Diagrams

This section illustrates the packaging specifications for the enCoRe V LV device, along with the thermal impedances for each package.

**Important Note** Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the enCoRe V LV emulation tools and their dimensions, refer to the development kit.

### Packaging Dimensions

**Figure 13. 16-pin Chip-On-Lead (3 x 3 x 0.6 mm) LG16A/LD16A (Sawn) Package Outline, 001-09116**

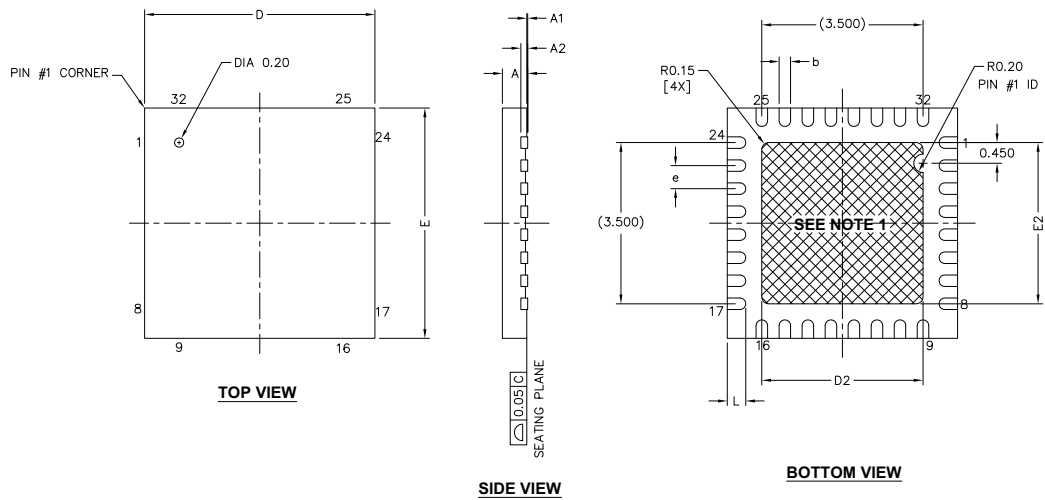


#### NOTES

1. REFERENCE JEDEC # MO-220
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-09116 \*J

Figure 14. 32-pin QFN (5 × 5 × 0.55 mm) LQ32 3.5 × 3.5 E-Pad (Sawn) Package Outline, 001-42168



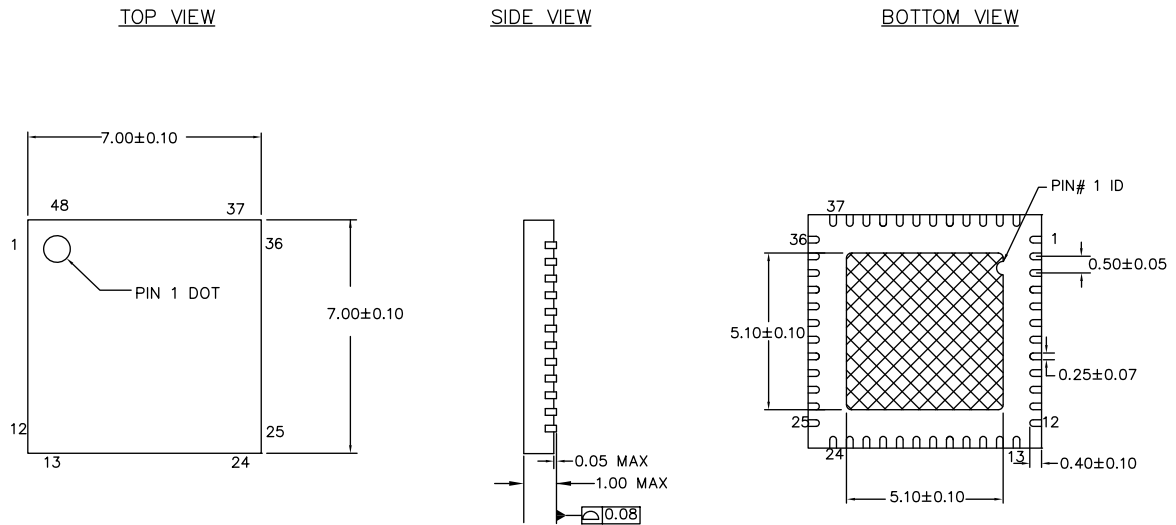
| SYMBOL | DIMENSIONS |       |       |
|--------|------------|-------|-------|
|        | MIN.       | NOM.  | MAX.  |
| A      | 0.50       | 0.55  | 0.60  |
| A1     | -          | 0.020 | 0.045 |
| A2     | 0.15 BSC   |       |       |
| D      | 4.90       | 5.00  | 5.10  |
| D2     | 3.40       | 3.50  | 3.60  |
| E      | 4.90       | 5.00  | 5.10  |
| E2     | 3.40       | 3.50  | 3.60  |
| L      | 0.30       | 0.40  | 0.50  |
| b      | 0.18       | 0.25  | 0.30  |
| e      | 0.50 TYP   |       |       |

NOTES:


1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 \*F

Figure 15. 48-pin QFN (7 x 7 x 1 mm) LT48A 5.1 x 5.1 E-Pad (Sawn) Package Outline, 001-13191



NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT:  $13 \pm 1$  mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 \*H

## Thermal Impedances

Table 23. Thermal Impedances

| Package                | Typical $\theta_{JA}$ <sup>(19)</sup> |
|------------------------|---------------------------------------|
| 16 QFN                 | 32.69 °C/W                            |
| 32 QFN <sup>(20)</sup> | 19.51 °C/W                            |
| 48 QFN <sup>(20)</sup> | 17.68 °C/W                            |

## Capacitance on Crystal Pins

Table 24. Typical Package Capacitance on Crystal Pins

| Package | Package Capacitance |
|---------|---------------------|
| 32 QFN  | 3.2 pF              |
| 48 QFN  | 3.3 pF              |

## Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 25. Solder Reflow Peak Temperature

| Package    | Minimum Peak Temperature <sup>(21)</sup> | Maximum Peak Temperature |
|------------|--|--------------------------|
| 16-pin QFN | 240 °C                                   | 260 °C                   |
| 32-pin QFN | 240 °C                                   | 260 °C                   |
| 48-pin QFN | 240 °C                                   | 260 °C                   |

### Notes

19.  $T_J = T_A + \text{Power} \times \theta_{JA}$ .

20. To achieve the thermal impedance specified for the package, solder the center thermal pad to the PCB ground plane.

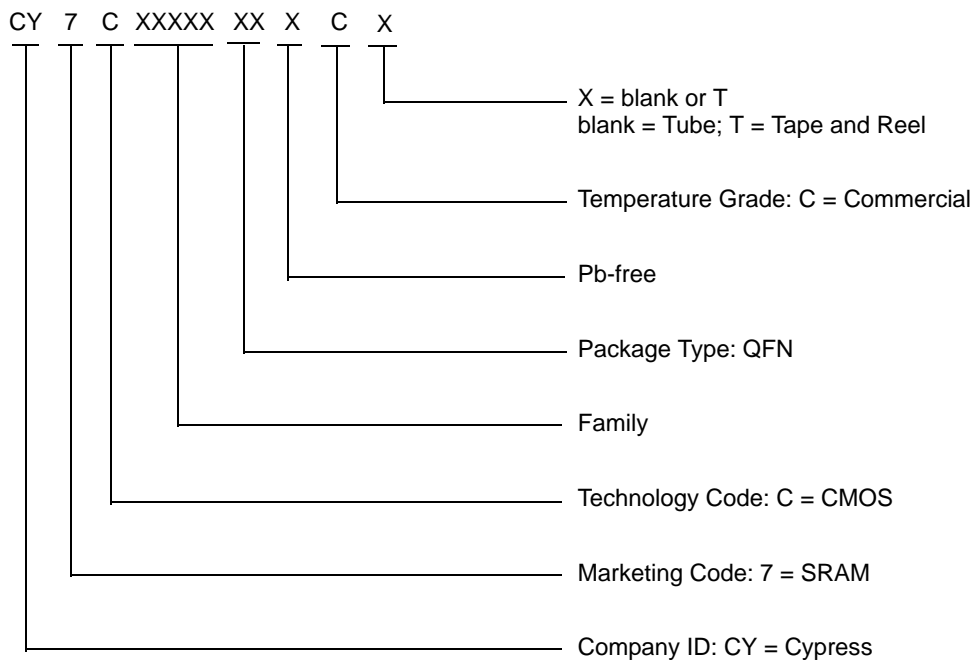
21. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are  $220 \pm 5$  °C with Sn-Pb or  $245 \pm 5$  °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

## Ordering Information

Table 26. Ordering Information

| Ordering Code     | Package Information                           | Flash | SRAM | No. of GPIOs | Target Applications            |
|-------------------|---|-------|------|--------------|--------------------------------|
| CY7C60413-16LKXC  | 16-Pin QFN<br>(3x3 mm)                        | 8 K   | 1 K  | 13           | Feature-rich wireless mouse    |
| CY7C60413-16LKXCT | 16-Pin QFN - (Tape and Reel)<br>(3X3 mm)      | 8 K   | 1 K  | 13           | Feature-rich wireless mouse    |
| CY7C60445-32LQXC  | 32-Pin QFN<br>(5x5x0.55 mm)                   | 16 K  | 1 K  | 28           | Feature-rich wireless mouse    |
| CY7C60445-32LQXCT | 32-Pin QFN - (Tape and Reel)<br>(5x5x0.55 mm) | 16 K  | 1 K  | 28           | Feature-rich wireless mouse    |
| CY7C60455-48LTXC  | 48-Pin QFN<br>(7x7x0.9 mm)                    | 16 K  | 1 K  | 36           | Mid-tier wireless keyboard     |
| CY7C60455-48LTXCT | 48-Pin QFN - (Tape and Reel)<br>(7x7x0.9 mm)  | 16 K  | 1 K  | 36           | Mid-tier wireless keyboard     |
| CY7C60456-48LTXC  | 48-Pin QFN<br>(7x7x0.9 mm)                    | 32 K  | 2 K  | 36           | Feature-rich wireless keyboard |
| CY7C60456-48LTXCT | 48-Pin QFN - (Tape and Reel)<br>(7x7x0.9 mm)  | 32 K  | 2 K  | 36           | Feature-rich wireless keyboard |

### Ordering Code Definitions



## Acronyms

The following table lists the acronyms that are used in this document.

| Acronym | Description                       |
|---------|-----------------------------------|
| API     | application programming interface |
| CPU     | central processing unit           |
| GPIO    | general purpose IO                |
| ICE     | in-circuit emulator               |
| ILO     | internal low speed oscillator     |
| IMO     | internal main oscillator          |
| I/O     | input/output                      |
| LSb     | least significant bit             |
| LVD     | low voltage detect                |
| MSb     | most significant bit              |
| POR     | power on reset                    |
| PPOR    | precision power on reset          |
| PSoC    | Programmable System-on-Chip       |
| SLIMO   | slow IMO                          |
| SRAM    | static random access memory       |

## Document Conventions

### Units of Measure

The following table lists the units of measure that are used in this document.

| Symbol | Unit of Measure               |
|--------|-------------------------------|
| °C     | degree Celsius                |
| dB     | decibels                      |
| fF     | femto farad                   |
| Hz     | hertz                         |
| KB     | 1024 bytes                    |
| Kbit   | 1024 bits                     |
| kHz    | kilohertz                     |
| kΩ     | kilohm                        |
| MHz    | megahertz                     |
| MΩ     | megaohm                       |
| μA     | microampere                   |
| μF     | microfarad                    |
| μH     | microhenry                    |
| μs     | microsecond                   |
| μV     | microvolts                    |
| μVrms  | microvolts root-mean-square   |
| μW     | microwatts                    |
| mA     | milli-ampere                  |
| ms     | milli-second                  |
| mV     | milli-volts                   |
| nA     | nanoampere                    |
| ns     | nanosecond                    |
| nV     | nanovolts                     |
| W      | ohm                           |
| pA     | picoampere                    |
| pF     | picofarad                     |
| pp     | peak-to-peak                  |
| ppm    | parts per million             |
| ps     | picosecond                    |
| sps    | samples per second            |
| σ      | sigma: one standard deviation |
| V      | volts                         |

## Errata

This section describes the errata for the enCoRe V – CY7C643xx and enCoRe V LV – CY7C604xx. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

### CY7C604xx Errata Summary

The following Errata item applies to the **CY7C643xx** and **CY7C604xx** data sheets.

#### 1. Latch up susceptibility when maximum I/O sink current exceeded

##### ■ PROBLEM DEFINITION

P1[3], P1[6], and P1[7] pins are susceptible to latch up when the I/O sink current exceeds 25 mA per pin on these pins.

##### ■ PARAMETERS AFFECTED

LU – Latch up current. Per JESD78A, the maximum allowable latch up current per pin is 100 mA. Cypress internal specification is 200 mA latch up current limit.

##### ■ TRIGGER CONDITIONS

Latch up occurs when both the following conditions are met:

- A. The offending I/O is externally connected to a voltage higher than the I/O high state, causing a current to flow into the pin that exceeds 25 mA.
- B. A Port1 I/O (P1[1], P1[4], and P1[5] respectively) adjacent to the offending I/O is connected to a voltage lower than the I/O low state. This causes a signal that drops below  $V_{SS}$  (signal undershoot) and a current greater than 200 mA to flow out of the pin.

##### ■ SCOPE OF IMPACT

The trigger conditions outlined in this item exceed the maximum ratings specified in the CY7C643xx and CY7C604xx data sheets.

##### ■ WORKAROUND

Add a series resistor  $> 300 \Omega$  to P1[3], P1[6], and P1[7] pins to restrict current to within latch up limits.

##### ■ FIX STATUS

This issue will be corrected in the next new silicon revision.

## Document History Page

| Document Title: CY7C604XX, enCoRe™ V Low Voltage Microcontroller<br>Document Number: 001-12395 |         |                 |                 |  |
|--|---------|-----------------|-----------------|--|
| Rev.   | ECN No. | Orig. of Change | Submission Date | Description of Change  |
| **   | 626516  | TYJ             | See ECN         | New data sheet   |
| *A   | 735721  | TYJ / ARI       | See ECN         | Added new block diagram, replaced TBDs, corrected values, updated pinout information, changed part number to reflect new specifications.   |
| *B   | 1120504 | ARI             | See ECN         | Corrected the description to pin 29 on Table 1, the Typ/Max values for $I_{SB0}$ on the DC chip-level specifications, and the Min voltage value for $V_{ddIWRITE}$ in the DC Programming Specifications table.<br>Corrected Flash Write Endurance minimum value in the DC Programming Specifications table.<br>Corrected the Flash Erase Time max value and the Flash Block Write Time max value in the AC Programming Specifications table.<br>Implemented new latest template.                     |
| *C   | 1225864 | AESA / ARI      | See ECN         | Corrected the description to pin 13, 29 on Table 1 and 22,44 on Table 2. Added sections Register Reference, Register Conventions and Register Mapping Tables. Corrected Max values on the DC Chip-Level Specifications table.  |
| *D   | 1446763 | AESA            | See ECN         | Changed $T_{ERASEB}$ parameter, max value to 18ms in Table 13, AC Programming Specification.   |
| *E   | 1639963 | AESA            | See ECN         | Post to <a href="http://www.cypress.com">www.cypress.com</a>   |
| *F   | 2138889 | TYJ / PYRS      | See ECN         | Updated Ordering Code table:<br>- Ordering code changed for 32-QFN package: From -32LKXC to -32LTXC<br>- Added a new package type – “LTXC” for 48-QFN<br>- Included Tape and Reel ordering code for 32-QFN and 48-QFN packages<br>Changed active current values at 24, 12 and 6MHz in table “DC Chip-Level Specifications”<br>- IDD24: 2.15 to 3.1mA<br>- IDD12: 1.45 to 2.0mA<br>- IDD6: 1.1 to 1.5mA<br>Added information on using P1[0] and P1[1] as the I2C interface during POR or reset events |

**Document History Page** (continued)

| Document Title: CY7C604XX, enCoRe™ V Low Voltage Microcontroller<br>Document Number: 001-12395 |         |                  |                 |   |
|--|---------|------------------|-----------------|---|
| Rev.   | ECN No. | Orig. of Change  | Submission Date | Description of Change   |
| *G   | 2583853 | TYJ / PYRS / HMT | 10/10/08        | <p>Converted from Preliminary to Final<br/>           ADC resolution changed from 10-bit to 8-bit<br/>           On Page1, SPI Master and Slave – speeds changed<br/>           Rephrased battery monitoring clause in page 1 to include “with external components”<br/>           Included ADC specifications table<br/>           Voh5, Voh7, Voh9 specs changed<br/>           Flash data retention – condition added to Note [15]<br/>           Input leakage spec changed to 25 nA max<br/>           Under AC Char, Frequency accuracy of ILO corrected<br/>           GPIO rise time for ports 0,1 and ports 2,3 made common<br/>           AC Programming specifications updated<br/>           Included AC Programming cycle timing diagram<br/>           AC SPI specification updated<br/>           Spec change for 32-QFN package<br/>           Input Leakage Current maximum value changed to 1 uA<br/>           Maximum specification for <math>V_{OH5A}</math> parameter changed from 2.0 to 2.1V<br/>           Minimum voltages for <math>F_{SPIM}</math> and <math>F_{SPIS}</math> specifications changed from 1.8V to 1.71V (Table 18)<br/>           Updated <math>V_{OHV}</math> parameter in Table 13<br/>           Updated Thermal impedance values for the packages - Table 20.<br/>           Update Development Tools, add Designing with PSoC Designer. Edit, fix links and table format. Update TMs. Update maximum data in Table 12. DC POR and LVD Specifications.</p> |
| *H   | 2653717 | DVJA / PYRS      | 02/04/09        | <p>Changed master page from CY7C60445, CY7C6045X to CY7C604XX.<br/>           Updated Features, Functional Overview, Development Tools, and Designing with PSoC Designer sections.<br/>           Removed ‘GUI - graphical user interface’ from Document Conventions acronym table.<br/>           Added Figure 1 and Table 1 (16-pin part information) to Pin Configurations section.<br/>           Removed ‘O - Only a read/write register or bits’ in Table 4<br/>           Edited Table 8: removed 10-bit resolution information and corrected units column.<br/>           Added Figure 9 (16-pin part information) to Package Dimensions section.<br/>           Added ‘Package Handling’ section.<br/>           Added 8K part ‘CY7C60413-16LKXC’ to Ordering Information.</p>   |
| *I   | 2714694 | DVJA / AESA      | 06/04/2009      | <p>Updated Block Diagram.<br/>           Added 10-bit ADC, SPI, and I2C Slave sections.<br/>           ADC Resolution changed from 8-bit to 10-bit<br/>           Updated Figure 9: 5.7 MHz minimum CPU frequency<br/>           Updated Table 15 AC Chip Level Specs<br/>           Figure 8: Changed minimum CPU Frequency from 750 kHz to 5.7 MHz</p>  |
| *J   | 2764460 | DVJA / AESA      | 09/15/2009      | <p>Added footnote #5 to Table 10: DC Chip Level Specs<br/>           Added <math>F_{32K2}</math> (Untrimmed) spec to Table 17: AC Chip level Specs<br/>           Changed <math>T_{RAMP}</math> spec to <math>SR_{POWER\_UP}</math> in Table 17: AC Chip Level Specs<br/>           Changed Table 14: ADC Specs<br/>           Added Table 25: Typical Package Capacitance on Crystal Pins</p>  |
| *K   | 2811903 | DVJA             | 11/23/2009      | <p>Added Note 6 on page 18. Changed <math>V_{IHP}</math> in <a href="#">Table 15 on page 23</a></p>   |
| *L   | 3075921 | NXZ              | 11/01/2010      | <p>Added Ordering Code Definition.</p>  |
| *M   | 3283876 | DIVA             | 06/15/2011      | <p>Updated <a href="#">Getting Started</a>, <a href="#">Development Tools</a>, and <a href="#">Designing with PSoC Designer</a>.</p>  |

Document History Page (continued)

| Document Title: CY7C604XX, enCoRe™ V Low Voltage Microcontroller<br>Document Number: 001-12395 |         |                 |                 |   |
|--|---------|-----------------|-----------------|---|
| Rev.   | ECN No. | Orig. of Change | Submission Date | Description of Change   |
| *N   | 3980412 | CSAI            | 04/24/2013      | Updated <a href="#">Package Diagrams</a> :<br>Updated <a href="#">Packaging Dimensions</a> :<br>spec 001-09116 – Changed revision from *E to *H.<br>spec 001-42168 – Changed revision from *D to *E.<br>spec 001-13191 – Changed revision from *E to *G.<br>Added <a href="#">Errata</a> .  |
| *O   | 4074141 | CSAI            | 07/23/2013      | Added Errata footnote (Note 7).<br>Updated <a href="#">Electrical Specifications</a> :<br>Updated <a href="#">DC Electrical Characteristics</a> :<br>Updated <a href="#">DC General Purpose I/O Specifications [7]</a> :<br>Added Note 7 and referred the same note in the heading.<br>Updated <a href="#">Errata</a> .<br>Updated to new template. |
| *P   | 4189348 | CSAI            | 11/12/2013      | Updated <a href="#">Package Diagrams</a> :<br>Updated <a href="#">Packaging Dimensions</a> :<br>spec 001-09116 – Changed revision from *H to *I.<br>Completing Sunset Review.   |
| *Q   | 5836430 | RAJV            | 08/10/2017      | Updated <a href="#">Package Diagrams</a> :<br>Updated <a href="#">Packaging Dimensions</a> :<br>spec 001-09116 – Changed revision from *I to *J.<br>spec 001-42168 – Changed revision from *E to *F.<br>spec 001-13191 – Changed revision from *G to *H.<br>Removed “Package Handling”.<br>Updated to new template.<br>Completing Sunset Review.    |

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