



**THE DATASHEET OF  
CY7C1049BNL-17VC**



**512K x 8 Static RAM**

**Features**

- **High speed**
  - $t_{AA} = 12 \text{ ns}$
- **Low active power**
  - 1320 mW (max.)
- **Low CMOS standby power (Commercial L version)**
  - 2.75 mW (max.)
- **2.0V Data Retention (400  $\mu\text{W}$  at 2.0V retention)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  features**

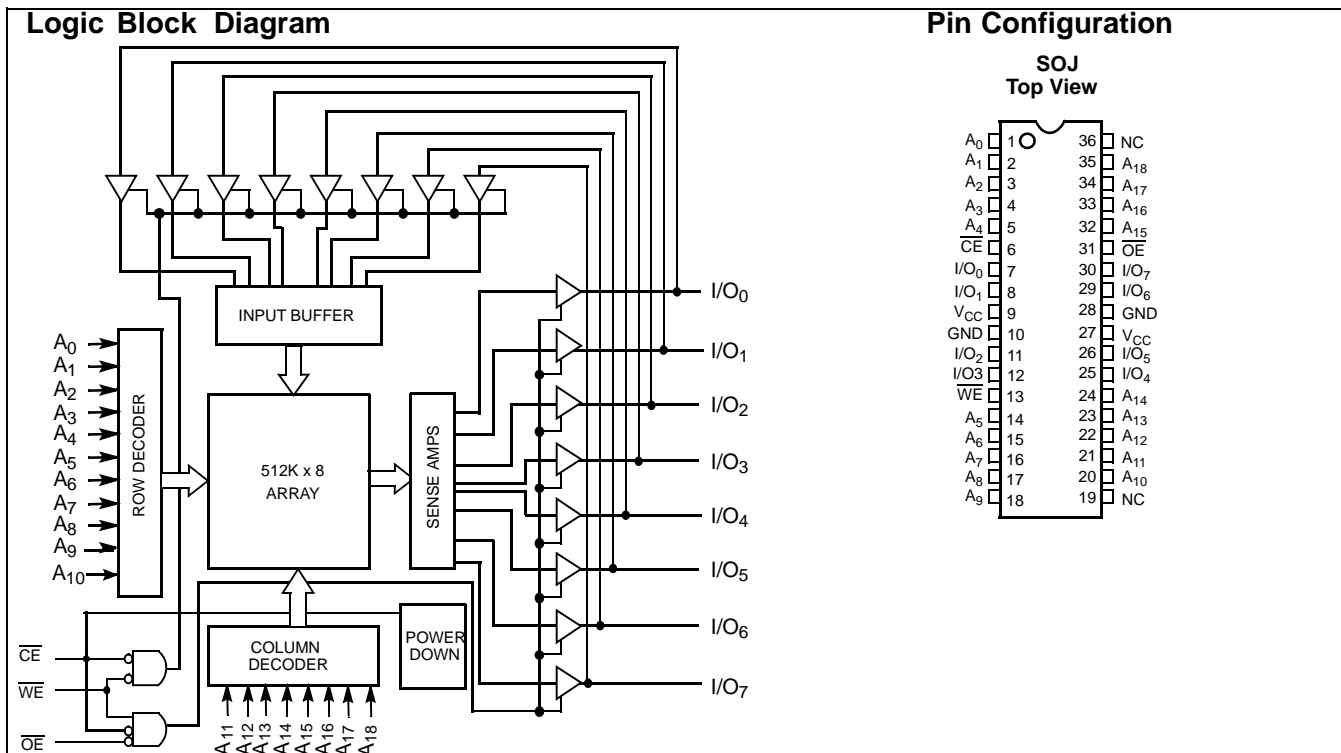
**Functional Description<sup>[1]</sup>**

The CY7C1049BN is a high-performance CMOS static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{\text{CE}}$ ), an active LOW Output Enable ( $\overline{\text{OE}}$ ), and three-state drivers. Writing to the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Write Enable ( $\overline{\text{WE}}$ ) inputs LOW. Data on the eight I/O pins ( $\text{I/O}_0$  through  $\text{I/O}_7$ ) is then written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{18}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing Write Enable ( $\overline{\text{WE}}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ( $\text{I/O}_0$  through  $\text{I/O}_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{\text{CE}}$  HIGH), the outputs are disabled ( $\overline{\text{OE}}$  HIGH), or during a write operation ( $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW).

The CY7C1049BN is available in a standard 400-mil-wide 36-pin SOJ package with center power and ground (revolutionary) pinout.



**Selection Guide**

		7C1049BN-12	7C1049BN-15	7C1049BN-17	7C1049BN-20	7C1049BN-25
Maximum Access Time (ns)		12	15	17	20	25
Maximum Operating Current (mA)		240	220	195	185	180
Maximum CMOS Standby Current (mA)	Com'l	8	8	8	8	8
	Com'l/Ind'l	L	-	0.5	0.5	0.5
	Ind'l	-	-	-	9	9

**Note:**

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied ..... -55°C to +125°C  
 Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[2]</sup> .... -0.5V to +7.0V  
 DC Voltage Applied to Outputs in High Z State<sup>[2]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V  
 DC Input Voltage<sup>[2]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)  
 Latch-Up Current ..... >200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	4.5V–5.5V
Industrial	-40°C to +85°C	

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	7C1049B-12		7C1049B-15		7C1049B-17		Unit		
			Min.	Max.	Min.	Max.	Min.	Max.			
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		V		
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4	V		
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> +0.3	2.2	V <sub>CC</sub> +0.3	2.2	V <sub>CC</sub> +0.3	V		
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		-0.3	0.8	-0.3	0.8	-0.3	0.3	V		
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	-1	+1	-1	+1	μA		
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	+1	-1	+1	-1	+1	μA		
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		240		220		195	mA		
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		40		40		40	mA		
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0	Com'l		8		8		8	mA	
			Com'l	L		-		-		0.5	mA
			Ind'l			-		-		8	mA
			Ind'l	L		-		-		0.5	mA

**Note:**

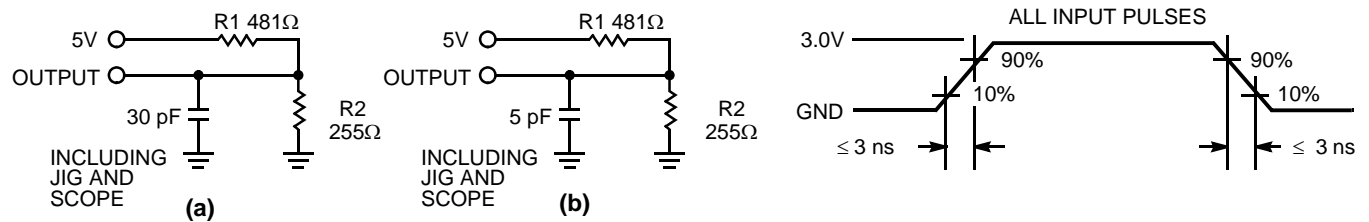
2. Minimum voltage is -2.0V for pulse durations of less than 20 ns.

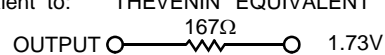
**Electrical Characteristics** Over the Operating Range (continued)

Parameter	Description	Test Conditions	7C1049B-20		7C1049B-25		Unit		
			Min.	Max.	Min.	Max.			
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		V		
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V		
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	V		
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		-0.3	0.8	-0.3	0.8	V		
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	-1	+1	μA		
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	+1	-1	+1	μA		
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		185		180	mA		
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		40		40	mA		
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0	Com'l		8		8	mA	
			Com'l	L		0.5		0.5	mA
			Ind'l			8		8	mA
			Ind'l	L		0.5		0.5	mA

**Capacitance<sup>[3]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	8	pF
C <sub>OUT</sub>	I/O Capacitance		8	pF

**AC Test Loads and Waveforms**


Equivalent to: THÉVENIN EQUIVALENT  

 167Ω in series with 1.73V

**Note:**

3. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics<sup>[4]</sup> Over the Operating Range

Parameter	Description	7C1049B-12		7C1049B-15		7C1049B-17		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>								
t <sub>power</sub>	V <sub>CC</sub> (typical) to the First Access <sup>[5]</sup>	1		1		1		ms
t <sub>RC</sub>	Read Cycle Time	12		15		17		ns
t <sub>AA</sub>	Address to Data Valid		12		15		17	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		12		15		17	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		6		7		8	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[7]</sup>	0		0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		6		7		7	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[7]</sup>	3		3		3		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>		6		7		7	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		12		15		17	ns
<b>Write Cycle<sup>[8, 9]</sup></b>								
t <sub>WC</sub>	Write Cycle Time	12		15		17		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	10		12		12		ns
t <sub>AW</sub>	Address Set-Up to Write End	10		12		12		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	10		12		12		ns
t <sub>SD</sub>	Data Set-Up to Write End	7		8		8		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	3		3		3		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		6		7		8	ns

Notes:

4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
5. This part has a voltage regulator which steps down the voltage from 5V to 3.3V internally. t<sub>power</sub> time has to be provided initially before a read/write operation is started.
6. t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
7. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
8. The internal write time of the memory is defined by the overlap of CE LOW, and WE LOW. CE and WE must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
9. The minimum write cycle time for Write Cycle no. 3 (WE controlled, OE LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.

**Switching Characteristics<sup>[4]</sup> Over the Operating Range (continued)**

Parameter	Description	7C1049B-20		7C1049B-25		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
$t_{power}$	$V_{CC}(\text{typical})$ to the First Access <sup>[5]</sup>	1		1		1
$t_{RC}$	Read Cycle Time	20		25		ns
$t_{AA}$	Address to Data Valid		20		25	ns
$t_{OHA}$	Data Hold from Address Change	3		5		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		20		25	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		8		10	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[7]</sup>	0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		8		10	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[7]</sup>	3		5		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>		8		10	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		20		25	ns
<b>Write Cycle<sup>[8]</sup></b>						
$t_{WC}$	Write Cycle Time	20		25		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	13		15		ns
$t_{AW}$	Address Set-Up to Write End	13		15		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	13		15		ns
$t_{SD}$	Data Set-Up to Write End	9		10		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	3		5		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		8		10	ns

**Data Retention Characteristics Over the Operating Range**

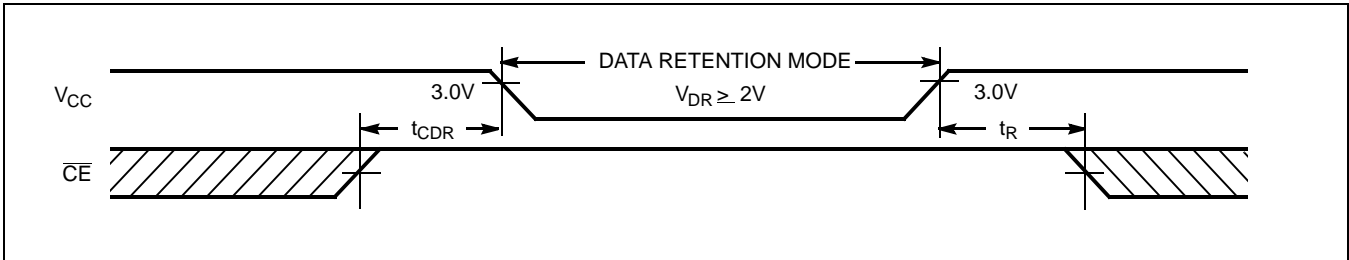
Parameter	Description		Conditions <sup>[11]</sup>		Min.	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention				2.0		V
$I_{CCDR}$	Data Retention Current	Com'l	L	$V_{CC} = V_{DR} = 3.0V,$ $CE \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		200	$\mu A$
		Ind'l				1	mA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time				0		ns
$t_R^{[10]}$	Operation Recovery Time				$t_{RC}$		ns

**Notes:**

 10.  $t_r \leq 3$  ns for the -12 and -15 speeds.  $t_r \leq 5$  ns for the -20 and slower speeds.

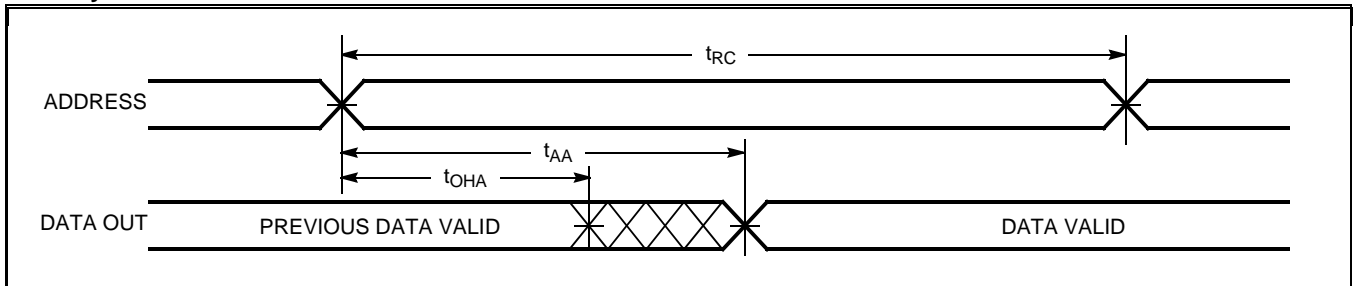
 11. No input may exceed  $V_{CC} + 0.5V$ .

**Data Retention Waveform**

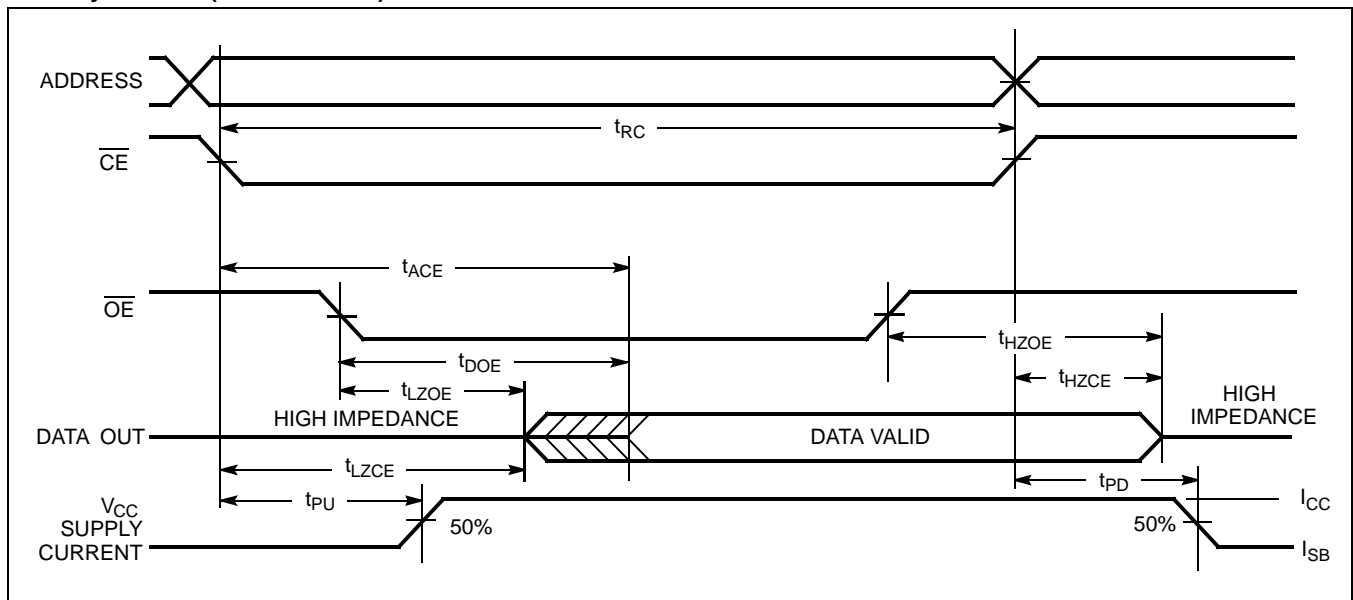


**Switching Waveforms**

**Read Cycle No. 1**<sup>[12, 13]</sup>



**Read Cycle No. 2 (OE Controlled)**<sup>[13, 14]</sup>

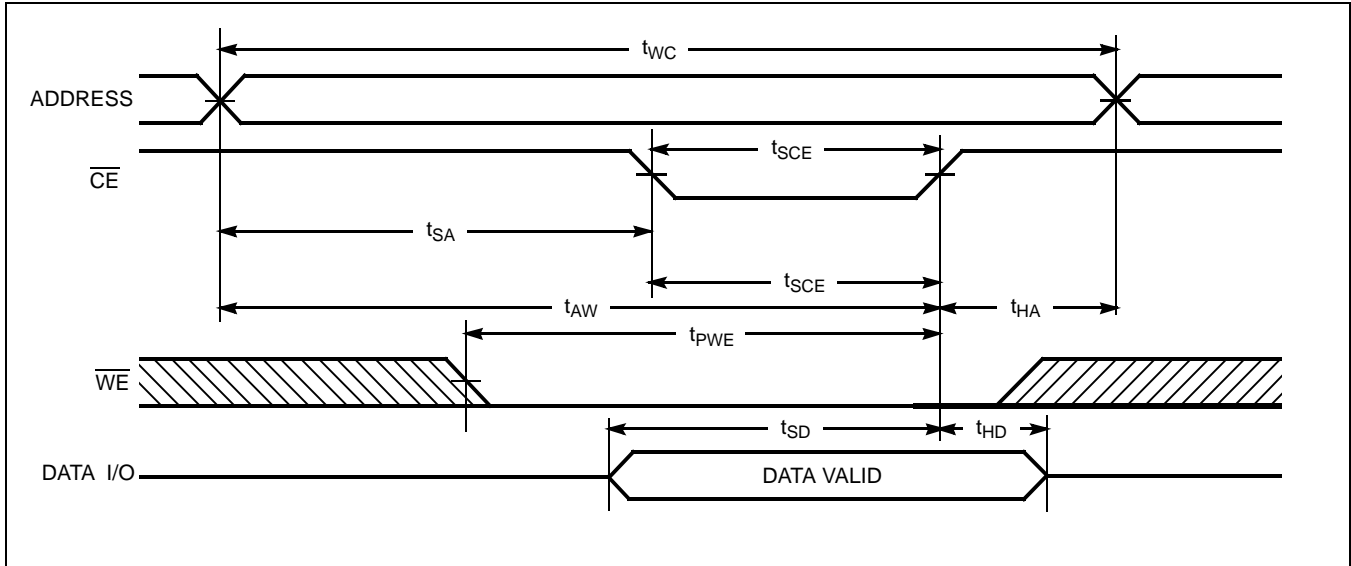


**Notes:**

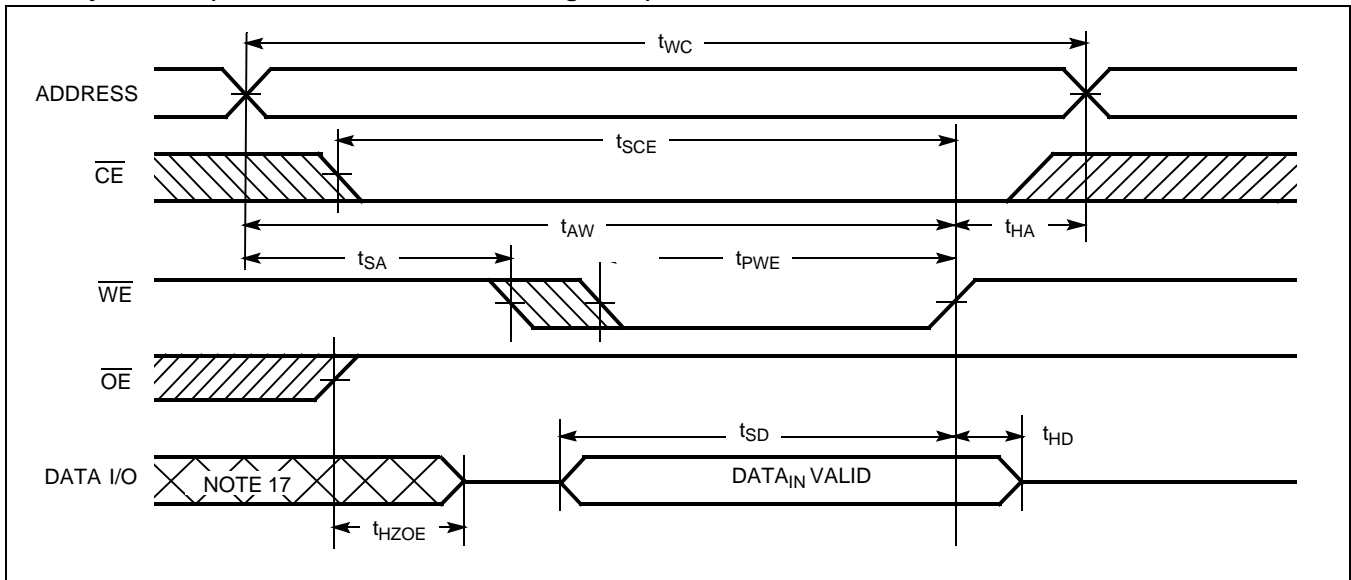
- 12. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
- 13. WE is HIGH for read cycle.
- 14. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ( $\overline{CE}$  Controlled)<sup>[15, 16]</sup>



Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[15, 16]</sup>

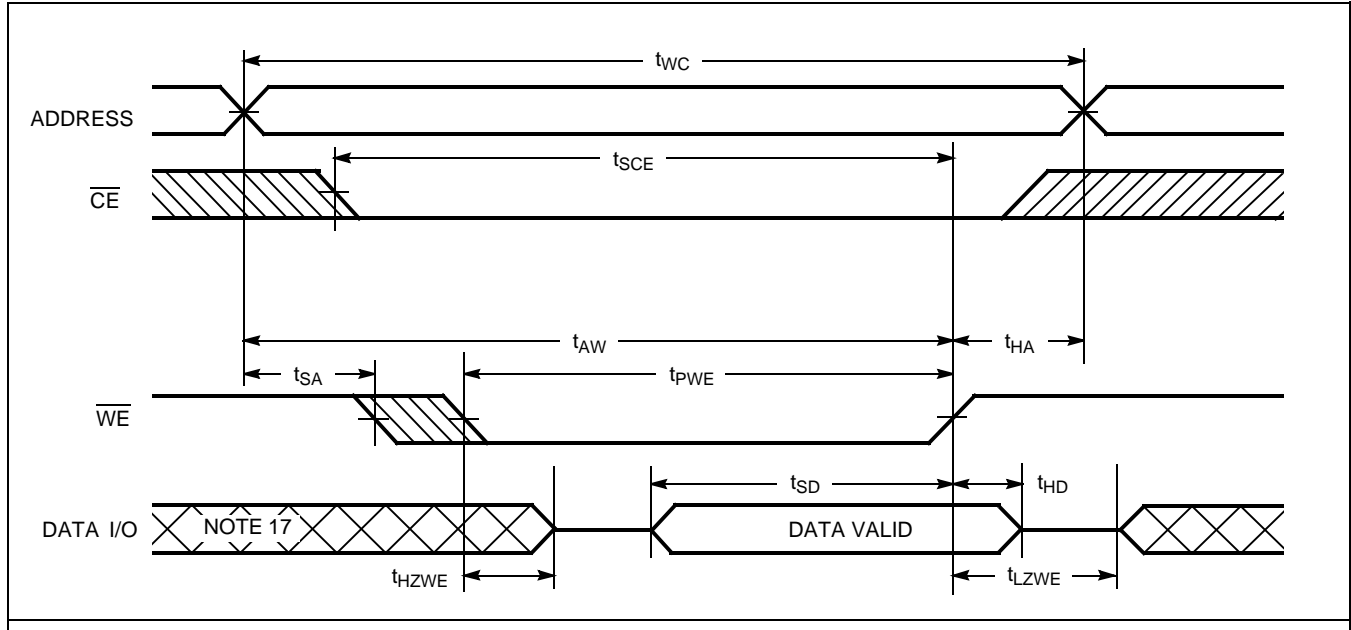


Notes:

- 15. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 16. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.
- 17. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[16]</sup>



Truth Table

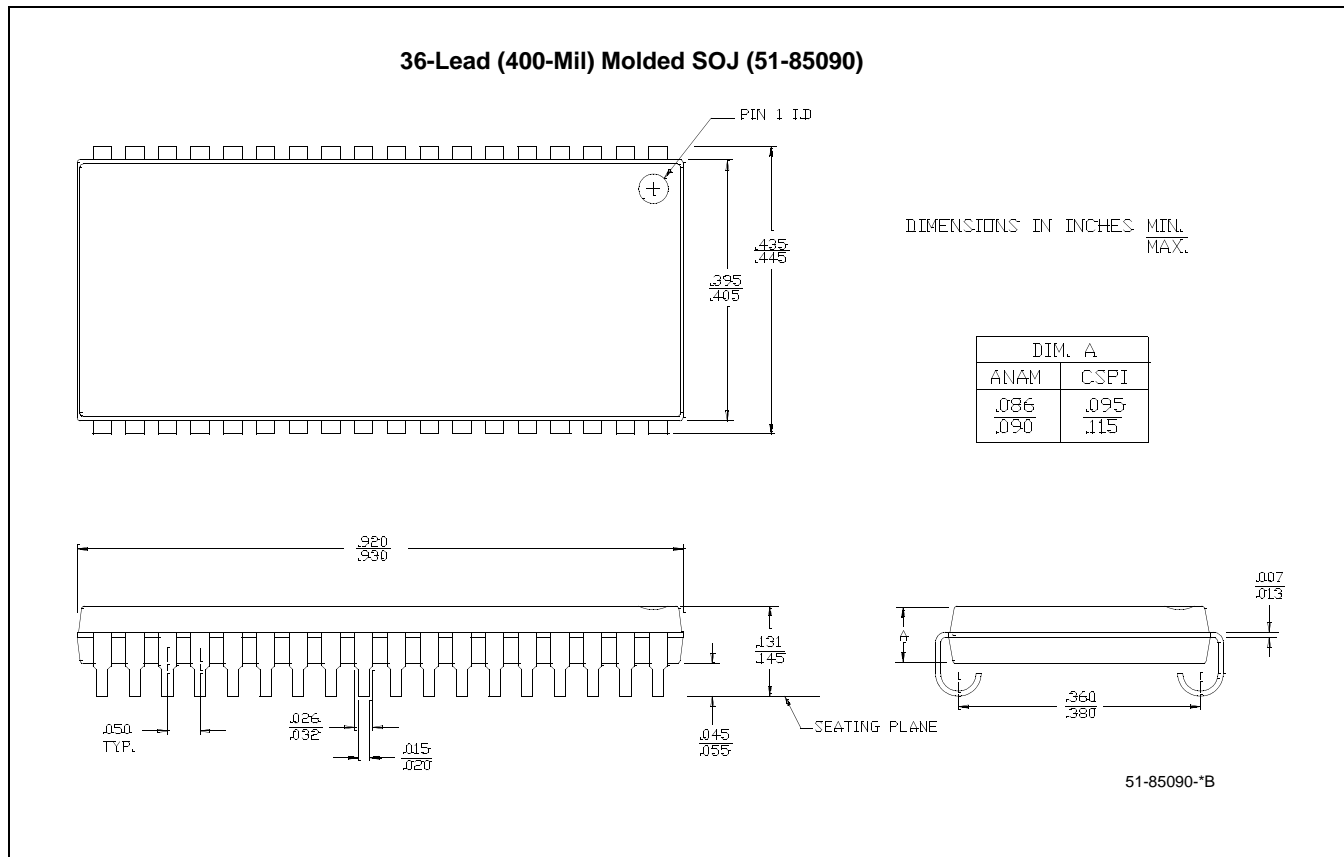
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Power-down	Standby ( $I_{SB}$ )
L	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	L	X	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Selected, Output disabled	Active ( $I_{CC}$ )

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C1049BN-12VC	51-85090	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049BN-12VXC	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-free)	
15	CY7C1049BN-15VC	51-85090	36-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1049BN-15VXC	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-free)	
	CY7C1049BN-15VI	51-85090	36-Lead (400-Mil) Molded SOJ	
17	CY7C1049BN-17VC	51-85090	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049BNL-17VC	51-85090	36-Lead (400-Mil) Molded SOJ	
	CY7C1049BN-17VXC	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-free)	
20	CY7C1049BN-20VC	51-85090	36-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1049BNL-20VC	51-85090	36-Lead (400-Mil) Molded SOJ	
	CY7C1049BN-20VXC	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-free)	
	CY7C1049BN-20VI	51-85090	36-Lead (400-Mil) Molded SOJ	
25	CY7C1049BNL-25VC	51-85090	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049BN-25VI	51-85090	36-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1049BN-25VXI	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-free)	

Please contact local sales representative regarding availability of these parts.

Package Diagram



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**Document History Page**

<b>Document Title: CY7C1049BN 512K x 8 Static RAM</b> <b>Document Number: 001-06501</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	424111	See ECN	NXR	New Data Sheet

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