



THE DATASHEET OF CY74FCT2543CTSOC

CY74FCT2543T

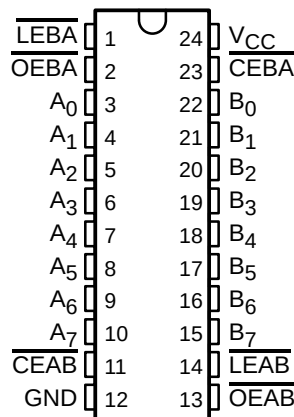
8-BIT LATCHED TRANSCEIVER

WITH 3-STATE OUTPUTS

SCCS042C – SEPTEMBER 1994 – REVISED NOVEMBER 2001

- Function and Pinout Compatible With FCT and F Logic
- 25-Ω Output Series Resistors to Reduce Transmission-Line Reflection Noise
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- 12-mA Output Sink Current
15-mA Output Source Current
- Separation Controls for Data Flow in Each Direction
- Back-to-Back Latches for Storage
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- 3-State Outputs

Q OR SO PACKAGE
(TOP VIEW)



description

The CY74FCT2543T octal latched transceiver contains two sets of eight D-type latches. Separate latch enable ($\overline{LEAB}$, $\overline{LEBA}$) and output enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs permit each latch set to have independent control of inputting and outputting in either direction of data flow. For example, for data flow from A to B, the A-to-B enable ($\overline{CEAB}$) input must be low to enter data from A or to take data from B, as indicated in the function table. With $\overline{CEAB}$ low, a low signal on the A-to-B latch enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B output buffers are active and reflect data present at the output of the A latches. Control of data from B to A is similar, but uses $\overline{CEAB}$, $\overline{LEAB}$, and $\overline{OEAB}$ inputs. On-chip termination resistors at the outputs reduce system noise caused by reflections. The CY74FCT2543T can replace the CY74FCT543T to reduce noise in an existing design.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2001, Texas Instruments Incorporated

CY74FCT2543T

8-BIT LATCHED TRANSCEIVER

WITH 3-STATE OUTPUTS

SCCS042C – SEPTEMBER 1994 – REVISED NOVEMBER 2001

PIN DESCRIPTION

NAME	DESCRIPTION
$\overline{\text{OEAB}}$	A-to-B output-enable input (active low)
$\overline{\text{OEBA}}$	B-to-A output-enable input (active low)
$\overline{\text{CEAB}}$	A-to-B enable input (active low)
$\overline{\text{CEBA}}$	B-to-A enable input (active low)
$\overline{\text{LEAB}}$	A-to-B latch-enable input (active low)
$\overline{\text{LEBA}}$	B-to-A latch-enable input (active low)
A	A-to-B data inputs or B-to-A 3-state outputs
B	B-to-A data inputs or A-to-B 3-state outputs

ORDERING INFORMATION

T _A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	5.3	CY74FCT2543CTQCT	FCT2543C
	SOIC – SO	Tube	5.3	CY74FCT2543CTSOC	FCT2543C
		Tape and reel	5.3	CY74FCT2543CTSOCT	
	QSOP – Q	Tape and reel	6.5	CY74FCT2543ATQCT	FCT2543A
	SOIC – SO	Tube	6.5	CY74FCT2543ATSOC	FCT2543A
		Tape and reel	6.5	CY74FCT2543ATSOCT	
	QSOP – Q	Tape and reel	8.5	CY74FCT2543TQCT	FCT2543

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			LATCH A-TO-B‡	OUTPUT B
CEAB	LEAB	OEAB		
H	X	X	Storing	Z
X	H	X	Storing	X
X	X	H	X	Z
L	L	L	Transparent	Current A inputs
L	H	L	Storing	Previous A inputs

‡ Before $\overline{\text{LEAB}}$ low-to-high transition

H = High logic level, L = Low logic level, X = Don't care,

Z = High-impedance state

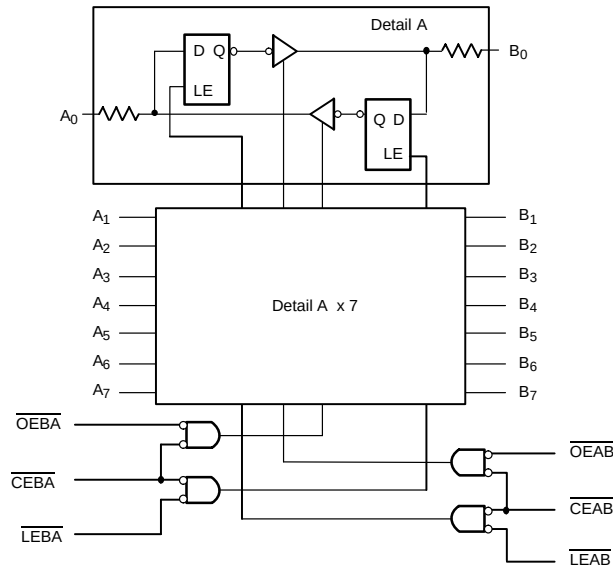
A-to-B data flow shown; B-to-A is the same, except using $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$.

CY74FCT2543T

8-BIT LATCHED TRANSCEIVER WITH 3-STATE OUTPUTS

SCCS042C – SEPTEMBER 1994 – REVISED NOVEMBER 2001

functional block diagram



absolute maximum rating over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range to ground potential	–0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ_{JA} (see Note 1): Q package	61°C/W
SO package	46°C/W
Ambient temperature range with power applied, T_A	–65°C to 135°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.75	5	5.25	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
I_{OH} High-level output current			–15	mA
I_{OL} Low-level output current			12	mA
T_A Operating free-air temperature	–40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

CY74FCT2543T

8-BIT LATCHED TRANSCEIVER

WITH 3-STATE OUTPUTS

SCCS042C – SEPTEMBER 1994 – REVISED NOVEMBER 2001

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V _{IK}	V _{CC} = 4.75 V, I _{IN} = −18 mA			−0.7	−1.2		V
V _{OH}	V _{CC} = 4.75 V, I _{OH} = −15 mA			2.4	3.3		V
V _{OL}	V _{CC} = 4.75 V, I _{OL} = 12 mA				0.3	0.55	V
R _{out}	V _{CC} = 4.75 V, I _{OL} = 12 mA			20	25	40	Ω
V _{hys}	All inputs				0.2		V
I _{IH}	V _{CC} = 5.25 V	V _{IN} = V _{CC}				5	μA
		V _{IN} = 2.7 V				±1	
I _{IL}	V _{CC} = 5.25 V, V _{IN} = 0.5 V					±1	μA
I _{OZH}	V _{CC} = 5.25 V, V _{OUT} = 2.7 V					15	μA
I _{OZL}	V _{CC} = 5.25 V, V _{OUT} = 0.5 V					−15	μA
I _{OS} ‡	V _{CC} = 5.25 V, V _{OUT} = 0 V			−60	−120	−225	mA
I _{off}	V _{CC} = 0 V, V _{OUT} = 4.5 V					±1	μA
I _{CC}	V _{CC} = 5.25 V, V _{IN} ≤ 0.2V, V _{IN} ≥ V _{CC} − 0.2 V				0.1	0.2	mA
ΔI _{CC}	V _{CC} = 5.25 V, V _{IN} = 3.4 V§, f ₁ = 0, Outputs open				0.5	2	mA
I _{CCD} ¶	V _{CC} = 5.25 V, One input switching at 50% duty cycle, Outputs open, CEAB and OEAB = LOW, CEBA = HIGH, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} − 0.2 V				0.06	1.2	mA/MHz
I _C [#]	V _{CC} = 5.25 V, f ₀ = 10 MHz, Outputs open, CEAB and OEAB = LOW, CEBA = HIGH, f ₀ = LEAB = 10 MHz	One bit switching at f ₁ = 5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} − 0.2 V		0.7	1.4	mA
			V _{IN} = 3.4 V or GND		1.2	3.4	
		Eight bits switching at f ₁ = 5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} − 0.2 V		2.8	5.6	
			V _{IN} = 3.4 V or GND		5.1	14.6	
C _i					5	10	pF
C ₀					9	12	pF

† Typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input ($V_{IN} = 3.4\text{ V}$); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.

$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input ($V_{IN} = 3.4\text{ V}$)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.



CY74FCT2543T
8-BIT LATCHED TRANSCEIVER
WITH 3-STATE OUTPUTS

SCCS042C – SEPTEMBER 1994 – REVISED NOVEMBER 2001

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER			CY74FCT2543T		CY74FCT2543AT		CY74FCT2543CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration, $\overline{LEBA}$ or $\overline{LEAB}$ low		5		5		5		ns
t_{su}	Setup time, high or low	A or B before $\overline{LEBA}\downarrow$ or $\overline{LEAB}\downarrow$	2		2		2		ns
t_h	Hold time, high or low	A or B after $\overline{LEBA}\downarrow$ or $\overline{LEAB}\downarrow$	2		2		2		ns

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT2543T		CY74FCT2543AT		CY74FCT2543CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2.5	8.5	2.5	6.5	2.5	5.5	ns
t_{PHL}									
t_{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	2.5	12.5	2.5	8	2.5	7	ns
t_{PHL}									
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	2	12	2	9	2	8	ns
t_{PZL}			2	12	2	9	2	8	
t_{PZH}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	2	12	2	9	2	8	ns
t_{PZL}			2	12	2	9	2	8	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	2	9	2	7.5	2	6.5	ns
t_{PLZ}			2	9	2	7.5	2	6.5	
t_{PHZ}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	2	9	2	7.5	2	6.5	ns
t_{PLZ}			2	9	2	7.5	2	6.5	

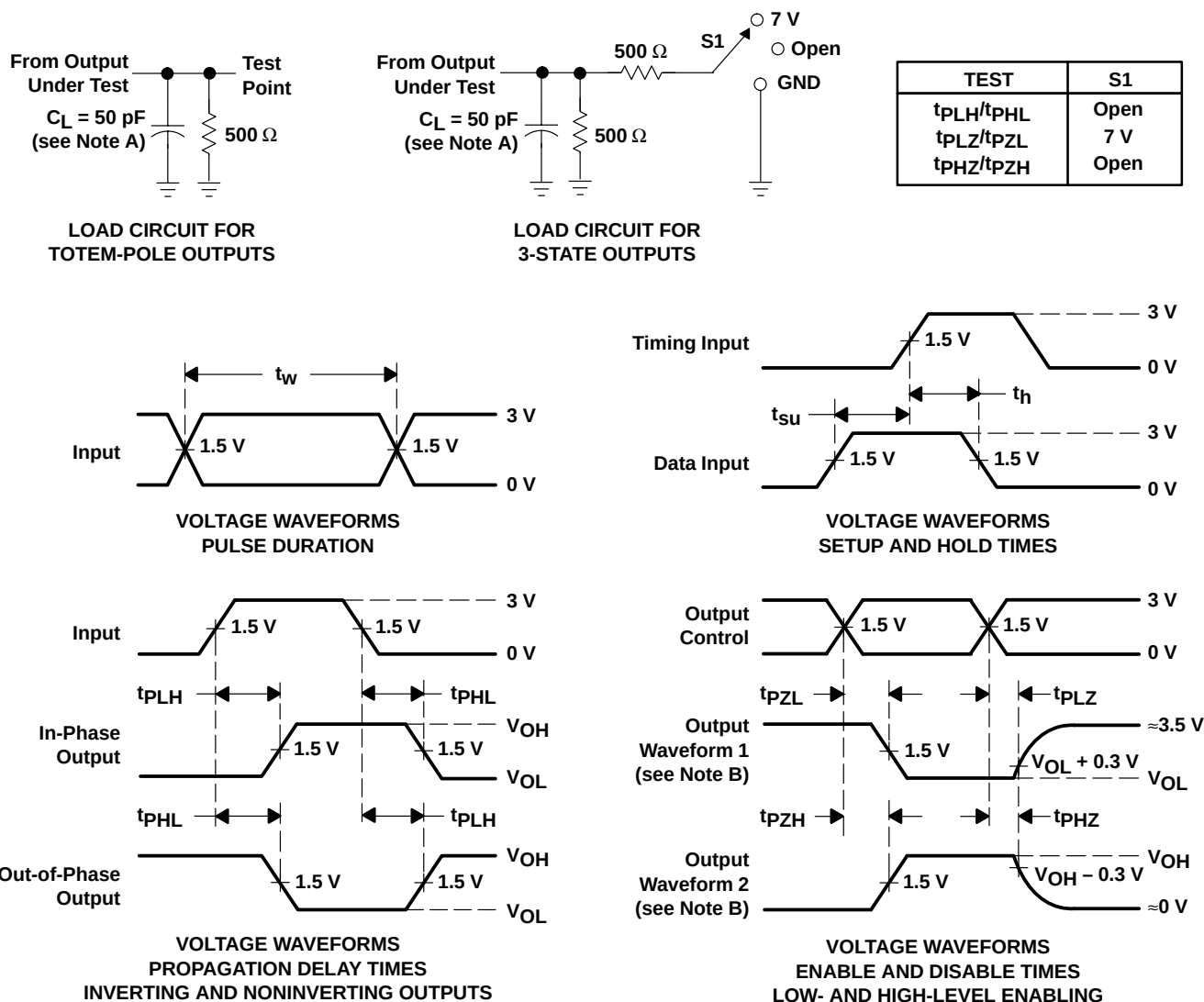
CY74FCT2543T

8-BIT LATCHED TRANSCEIVER

WITH 3-STATE OUTPUTS

SCCS042C – SEPTEMBER 1994 – REVISED NOVEMBER 2001

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CY74FCT2543ATQCT	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT2543A	Samples
CY74FCT2543ATSOC	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT2543A	Samples
CY74FCT2543CTQCT	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT2543C	Samples
CY74FCT2543CTSOC	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT2543C	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

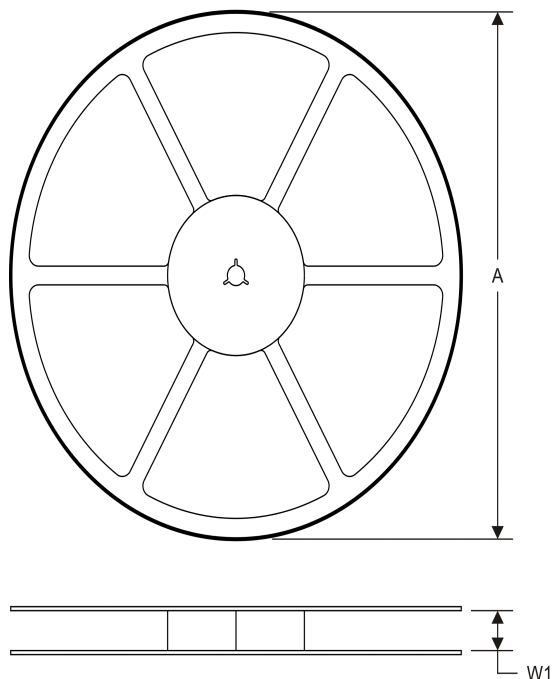
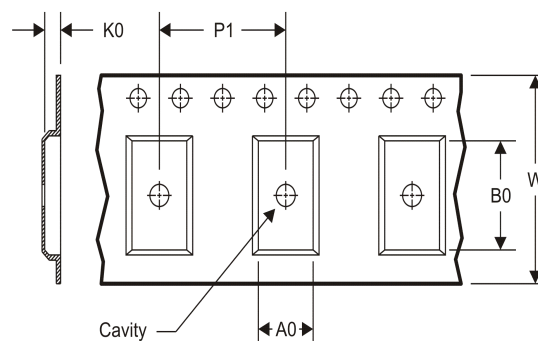
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


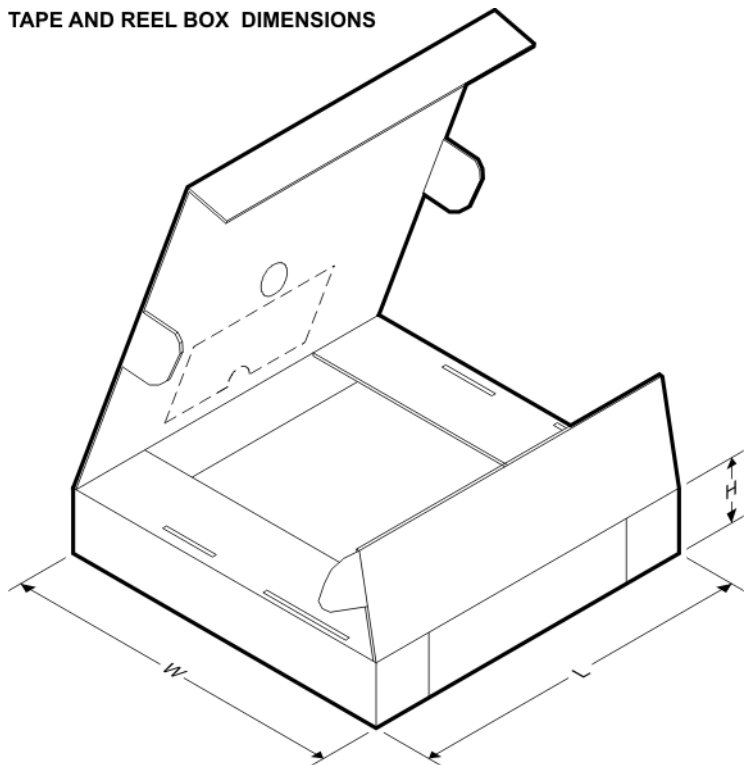
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT2543ATQCT	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT2543CTQCT	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

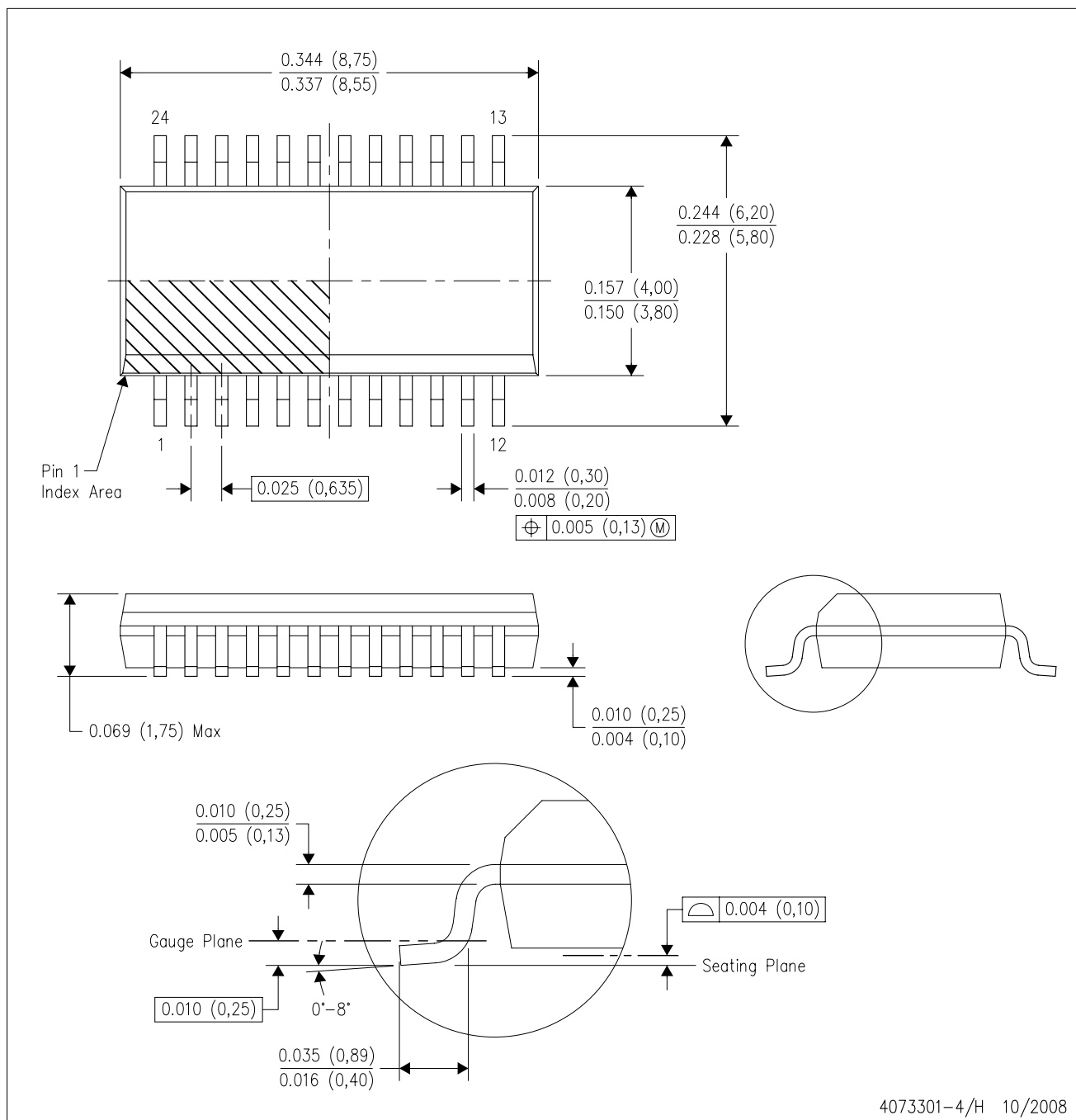


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT2543ATQCT	SSOP	DBQ	24	2500	367.0	367.0	38.0
CY74FCT2543CTQCT	SSOP	DBQ	24	2500	367.0	367.0	38.0

DBQ (R-PDSO-G24)

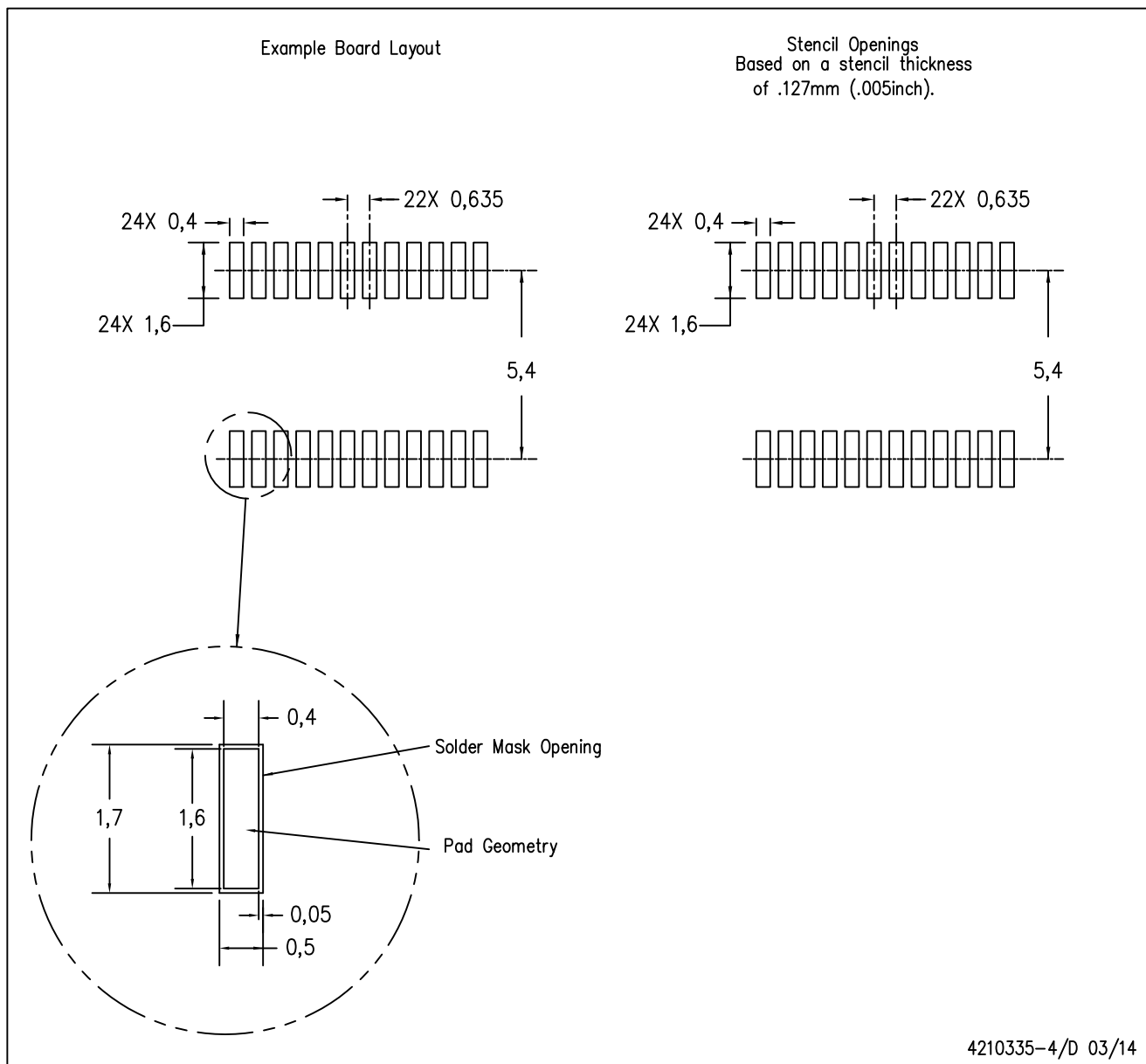
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AE.

DBQ (R-PDSO-G24)

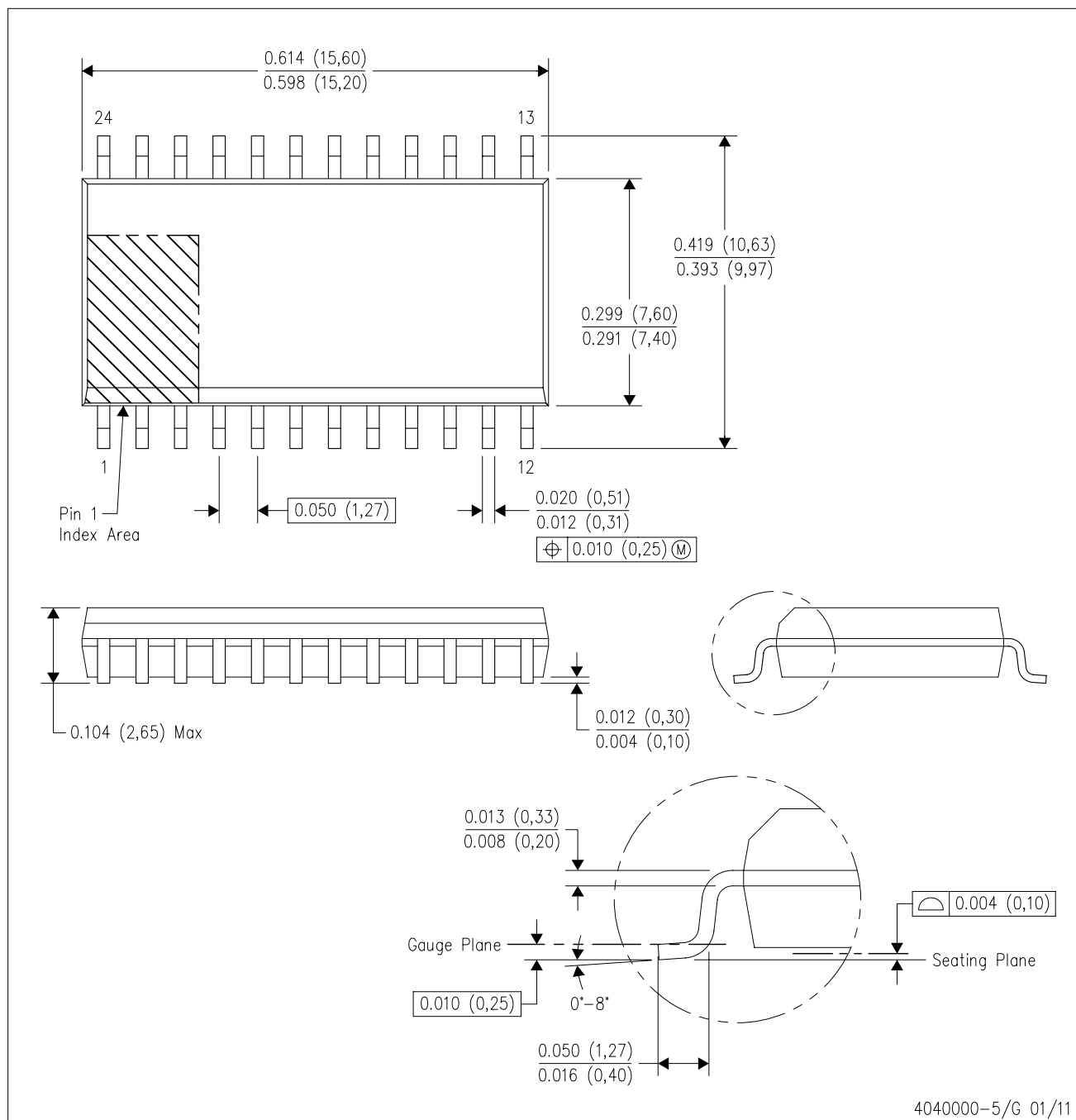
PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

⊖ [View CY74FCT2543CTSOC](#) on WIN SOURCE

⊖ [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management