



**THE DATASHEET OF
CY62157EV30LL-55ZSXET**



Features

- Thin small outline package (TSOP) I package configurable as 512K × 16 or 1M × 8 static RAM (SRAM)
- High speed: 45 ns
- Temperature ranges
 - Industrial: -40 °C to +85 °C
 - Automotive-A: -40 °C to +85 °C
 - Automotive-E: -40 °C to +125 °C
- Wide voltage range: 2.20 V to 3.60 V
- Pin compatible with CY62157DV30
- Ultra low standby power
 - Typical standby current: 2 μA
 - Maximum standby current: 8 μA (Industrial)
- Ultra low active power
 - Typical active current: 1.8 mA at f = 1 MHz
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} features
- Automatic power down when deselected
- Complementary Metal Oxide Semiconductor (CMOS) for optimum speed and power
- Available in Pb-free and non Pb-free 48-ball very fine-pitch ball grid array (VFBGA), Pb-free 44-pin thin small outline package (TSOP) II and 48-pin TSOP I packages

Functional Description

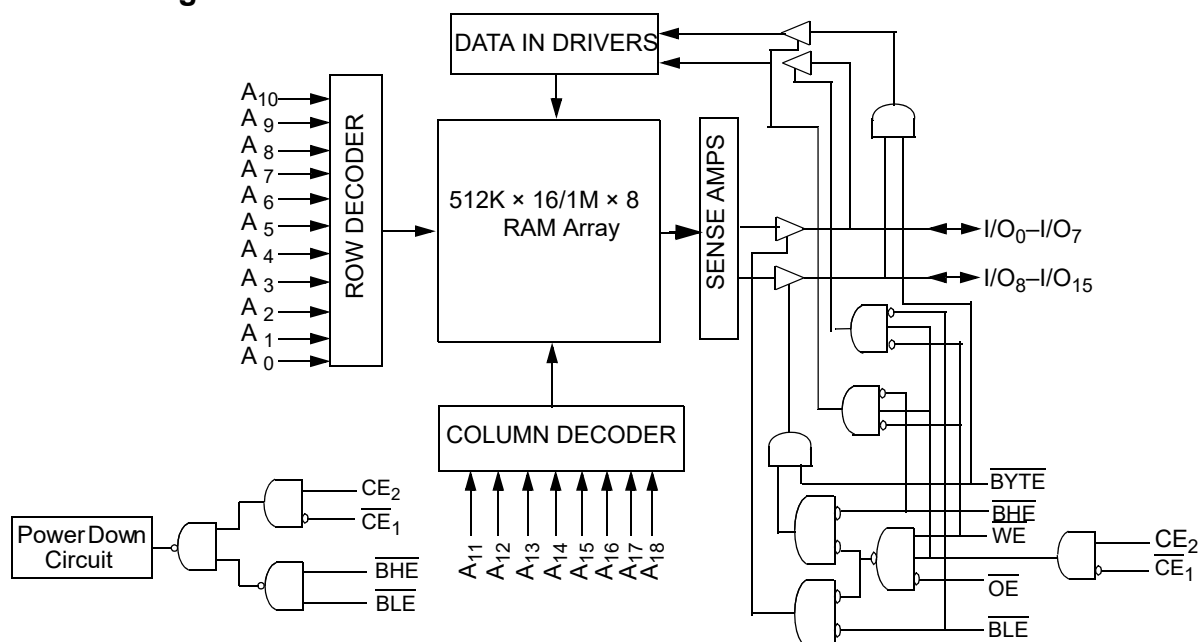
The CY62157EV30 is a high performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Place the device into standby mode when deselected (\overline{CE}_1 HIGH or CE_2 LOW or both \overline{BHE} and \overline{BLE} are HIGH). The input or output pins (I/O₀ through I/O₁₅) are placed in a high impedance state when the device is deselected (\overline{CE}_1 HIGH or CE_2 LOW), the outputs are disabled (\overline{OE} HIGH), Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , \overline{BLE} HIGH), or a write operation is active (CE_1 LOW, CE_2 HIGH and \overline{WE} LOW).

To write to the device, take Chip Enable (\overline{CE}_1 LOW and CE_2 HIGH) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O₀ through I/O₇) is written into the location specified on the address pins (A₀ through A₁₈). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₈).

To read from the device, take Chip Enable (\overline{CE}_1 LOW and CE_2 HIGH) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appear on I/O₀ to I/O₇. If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See Truth Table on page 13 for a complete description of read and write modes.

For a complete list of related documentation, [click here](#).

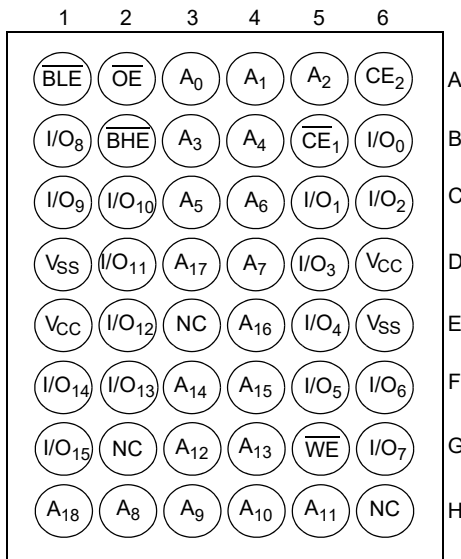
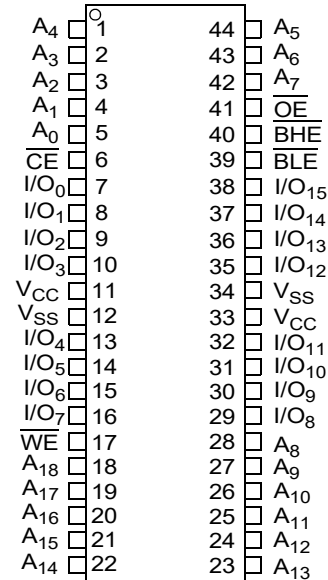
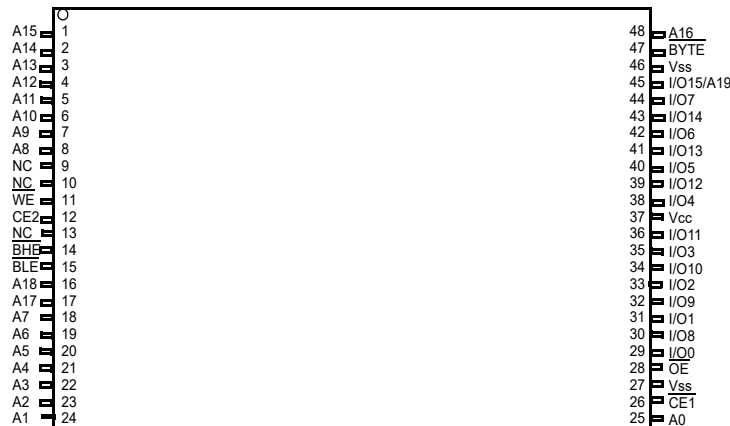
Logic Block Diagram



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Pin Configurations

Figure 1. 48-ball VFBGA pinout (Top View) [1]

Figure 2. 44-pin TSOP II pinout (Top View) [2]

Figure 3. 48-pin TSOP I pinout (Top View) [1, 3]


Product Portfolio

| Product | Range | V _{CC} Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|---------------|-------------------------|---------------------------|---------|----------------------|------------|----------------------------------|-----|---------|-----|--------------------------------|-----|
| | | | | | | Operating I _{CC} , (mA) | | | | Standby, I _{SB2} (μA) | |
| | | f = 1 MHz | | f = f _{max} | | | | | | | |
| | | Min | Typ [4] | Max | | Typ [4] | Max | Typ [4] | Max | Typ [4] | Max |
| CY62157EV30LL | Industrial/Automotive-A | 2.2 | 3.0 | 3.6 | 45 | 1.8 | 3 | 18 | 25 | 2 | 8 |
| | Automotive-E | 2.2 | 3.0 | 3.6 | 55 | 1.8 | 4 | 18 | 35 | 2 | 30 |

Notes

- NC pins are not connected on the die.
- The 44-pin TSOP II package has only one chip enable ($\overline{\text{CE}}$) pin.
- The BYTE pin in the 48-pin TSOP I package must be tied HIGH to use the device as a 512 K × 16 SRAM. The 48-pin TSOP I package can also be used as a 1 M × 8 SRAM by tying the BYTE signal LOW. In the 1 M × 8 configuration, Pin 45 is A19, while BHE, BLE and I/O₈ to I/O₁₄ pins are not used.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage Temperature -65 °C to + 150 °C

Ambient Temperature
with Power Applied -55 °C to + 125 °C

Supply Voltage
to Ground Potential -0.3 V to 3.9 V ($V_{CCmax} + 0.3$ V)

DC Voltage Applied to Outputs
in High Z State ^[5, 6] -0.3 V to 3.9 V ($V_{CCmax} + 0.3$ V)

DC Input Voltage ^[5, 6] -0.3 V to 3.9 V ($V_{CCmax} + 0.3$ V)

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage
(MIL-STD-883, Method 3015) > 2001 V

Latch-Up Current > 200 mA

Operating Range

| Device | Range | Ambient Temperature | V _{CC} ^[7] |
|---------------|---------------------------|---------------------|--------------------------------|
| CY62157EV30LL | Industrial / Automotive-A | -40 °C to +85 °C | 2.2 V to 3.6 V |
| | Automotive-E | -40 °C to +125 °C | |

Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | 45 ns (Industrial/Automotive-A) | | | 55 ns (Automotive-E) | | | Unit |
|---------------------------------|---|--|---------------------------------|--------------------|-----------------------|----------------------|--------------------|-----------------------|------|
| | | | Min | Typ ^[8] | Max | Min | Typ ^[8] | Max | |
| V _{OH} | Output HIGH voltage | I _{OH} = -0.1 mA | 2.0 | - | - | 2.0 | - | - | V |
| | | I _{OH} = -1.0 mA, V _{CC} ≥ 2.70 V | 2.4 | - | - | 2.4 | - | - | V |
| V _{OL} | Output LOW voltage | I _{OL} = 0.1 mA | - | - | 0.4 | - | - | 0.4 | V |
| | | I _{OL} = 2.1 mA, V _{CC} ≥ 2.70 V | - | - | 0.4 | - | - | 0.4 | V |
| V _{IH} | Input HIGH voltage | V _{CC} = 2.2 V to 2.7 V | 1.8 | - | V _{CC} + 0.3 | 1.8 | - | V _{CC} + 0.3 | V |
| | | V _{CC} = 2.7 V to 3.6 V | 2.2 | - | V _{CC} + 0.3 | 2.2 | - | V _{CC} + 0.3 | V |
| V _{IL} | Input LOW voltage | V _{CC} = 2.2 V to 2.7 V | -0.3 | - | 0.6 | -0.3 | - | 0.6 | V |
| | | V _{CC} = 2.7 V to 3.6 V | -0.3 | - | 0.8 | -0.3 | - | 0.8 | V |
| I _{IX} | Input leakage current | GND ≤ V _I ≤ V _{CC} | -1 | - | +1 | -4 | - | +4 | μA |
| I _{OZ} | Output leakage current | GND ≤ V _O ≤ V _{CC} , Output Disabled | -1 | - | +1 | -4 | - | +4 | μA |
| I _{CC} | V _{CC} operating supply current | f = f _{max} = 1/t _{RC} V _{CC} = V _{CCmax} | - | 18 | 25 | - | 18 | 35 | mA |
| | | f = 1 MHz I _{OUT} = 0 mA CMOS levels | - | 1.8 | 3 | - | 1.8 | 4 | |
| I _{SB1} ^[9] | Automatic CE power down current – CMOS inputs | $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V f = f _{max} (Address and Data Only), f = 0 (\overline{OE} and \overline{WE}), V _{CC} = 3.60 V | - | 2 | 8 | - | 2 | 30 | μA |
| I _{SB2} ^[9] | Automatic CE power down current – CMOS inputs | $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0, V _{CC} = 3.60 V | - | 2 | 8 | - | 2 | 30 | μA |

Notes

- V_{IL(min)} = -2.0 V for pulse durations less than 20 ns.
- V_{IH(max)} = V_{CC} + 0.75 V for pulse durations less than 20 ns.
- Full device AC operation assumes a 100 μs ramp time from 0 to V_{CC(min)} and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
- Chip enables (CE₁ and CE₂), byte enables (BHE and BLE) and BYTE (48-pin TSOP I only) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

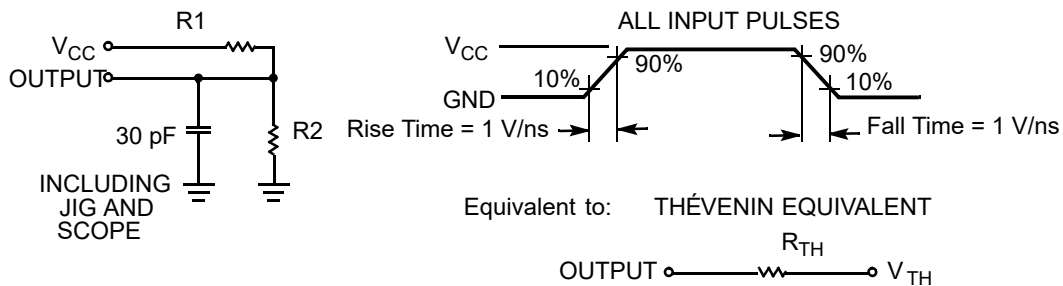
| Parameter ^[10] | Description | Test Conditions | Max | Unit |
|---------------------------|--------------------|---|-----|------|
| C _{IN} | Input capacitance | T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(typ)} | 10 | pF |
| C _{OUT} | Output capacitance | | 10 | pF |

Thermal Resistance

| Parameter ^[10] | Description | Test Conditions | 48-ball BGA | 48-pin TSOP I | 44-pin TSOP II | Unit |
|---------------------------|--|---|-------------|---------------|----------------|------|
| Θ _{JA} | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 48.34 | 55.47 | 55.84 | °C/W |
| Θ _{JC} | Thermal resistance (junction to case) | | 8.78 | 4.08 | 15.79 | °C/W |

AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms



| Parameters | 2.5 V | 3.0 V | Unit |
|-----------------|-------|-------|------|
| R1 | 16667 | 1103 | Ω |
| R2 | 15385 | 1554 | Ω |
| R _{TH} | 8000 | 645 | Ω |
| V _{TH} | 1.20 | 1.75 | V |

Note

10. Tested initially and after any design or process changes that may affect these parameters.

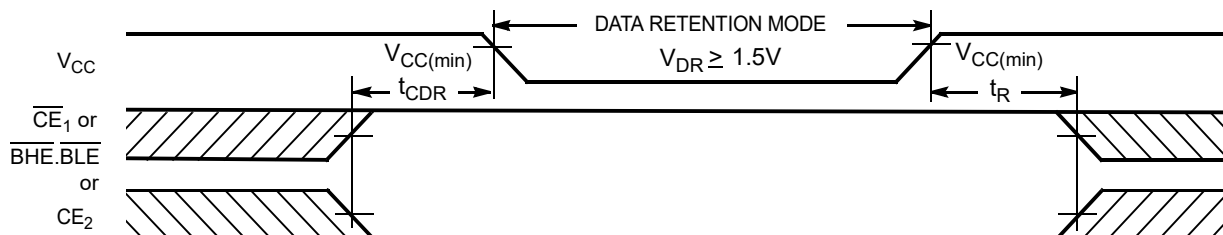
Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Typ ^[11] | Max | Unit |
|----------------------------|--------------------------------------|---|-----|---------------------|-----|---------------|
| V_{DR} | V_{CC} for data retention | | 1.5 | – | – | V |
| I_{CCDR} ^[12] | Data retention current | $V_{CC} = 1.5\text{ V}$, $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$, $CE_2 \leq 0.2\text{ V}$, $(\overline{BHE}\text{ and } \overline{BLE}) \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ | – | 2 | 5 | μA |
| | | | – | – | 30 | |
| t_{CDR} ^[13] | Chip deselect to data retention time | | 0 | – | – | ns |
| t_R ^[14] | Operation recovery time | CY62157EV30LL-45 | 45 | – | – | ns |
| | | CY62157EV30LL-55 | 55 | – | – | |

Data Retention Waveform

Figure 5. Data Retention Waveform^[15]



Notes

11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(\text{typ})}$, $T_A = 25\text{ }^\circ\text{C}$.
12. Chip enables (\overline{CE}_1 and CE_2), byte enables (BHE and BLE) and BYTE (48-pin TSOP I only) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
13. Tested initially and after any design or process changes that may affect these parameters.
14. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$.
15. BHE.BLE is the AND of both BHE and BLE. Deselect the chip by either disabling chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .

Switching Characteristics

Over the Operating Range

| Parameter ^[16, 17] | Description | 45 ns (Industrial/ Automotive-A) | | 55 ns (Automotive-E) | | Unit |
|--|---|-------------------------------------|-----|----------------------|-----|------|
| | | Min | Max | Min | Max | |
| Read Cycle | | | | | | |
| t_{RC} | Read cycle time | 45 | – | 55 | – | ns |
| t_{AA} | Address to data valid | – | 45 | – | 55 | ns |
| t_{OHA} | Data hold from address change | 10 | – | 10 | – | ns |
| t_{ACE} | \overline{CE}_1 LOW and CE_2 HIGH to data valid | – | 45 | – | 55 | ns |
| t_{DOE} | \overline{OE} LOW to data valid | – | 22 | – | 25 | ns |
| t_{LZOE} | \overline{OE} LOW to Low Z ^[18] | 5 | – | 5 | – | ns |
| t_{HZOE} | \overline{OE} HIGH to High Z ^[18, 19] | – | 18 | – | 20 | ns |
| t_{LZCE} | \overline{CE}_1 LOW and CE_2 HIGH to Low Z ^[18] | 10 | – | 10 | – | ns |
| t_{HZCE} | \overline{CE}_1 HIGH and CE_2 LOW to High Z ^[18, 19] | – | 18 | – | 20 | ns |
| t_{PU} | \overline{CE}_1 LOW and CE_2 HIGH to power up | 0 | – | 0 | – | ns |
| t_{PD} | \overline{CE}_1 HIGH and CE_2 LOW to power down | – | 45 | – | 55 | ns |
| t_{DBE} | $\overline{BLE}/\overline{BHE}$ LOW to data valid | – | 45 | – | 55 | ns |
| t_{LZBE} | $\overline{BLE}/\overline{BHE}$ LOW to Low Z ^[18, 20] | 5 | – | 10 | – | ns |
| t_{HZBE} | $\overline{BLE}/\overline{BHE}$ HIGH to High Z ^[18, 19] | – | 18 | – | 20 | ns |
| Write Cycle ^[21, 22] | | | | | | |
| t_{WC} | Write cycle time | 45 | – | 55 | – | ns |
| t_{SCE} | \overline{CE}_1 LOW and CE_2 HIGH to write end | 35 | – | 40 | – | ns |
| t_{AW} | Address setup to write end | 35 | – | 40 | – | ns |
| t_{HA} | Address hold from write end | 0 | – | 0 | – | ns |
| t_{SA} | Address setup to write start | 0 | – | 0 | – | ns |
| t_{PWE} | \overline{WE} pulse width | 35 | – | 40 | – | ns |
| t_{BW} | $\overline{BLE}/\overline{BHE}$ LOW to write end | 35 | – | 40 | – | ns |
| t_{SD} | Data setup to write end | 25 | – | 25 | – | ns |
| t_{HD} | Data hold from write end | 0 | – | 0 | – | ns |
| t_{HZWE} | \overline{WE} LOW to High Z ^[18, 19] | – | 18 | – | 20 | ns |
| t_{LZWE} | \overline{WE} HIGH to Low Z ^[18] | 10 | – | 10 | – | ns |

Notes

16. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the [Figure 4 on page 5](#).
17. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes [AN13842](#) and [AN66311](#). However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
18. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
19. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
20. If both byte enables are toggled together, this value is 10 ns.
21. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
22. The minimum write cycle time for Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) should be equal to the sum of t_{SD} and t_{HZWE} .

Switching Waveforms

Figure 6. Read Cycle No. 1 (Address Transition Controlled) [23, 24]

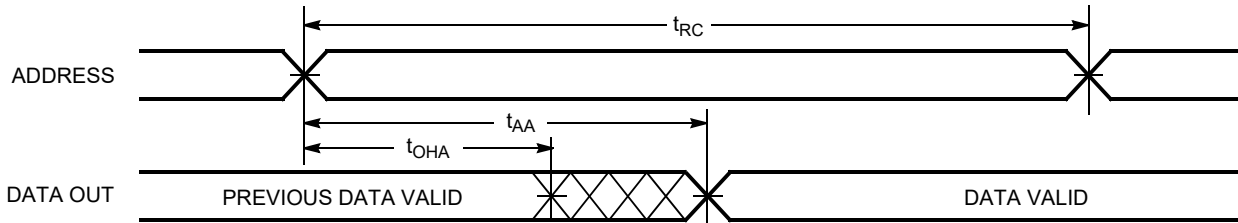
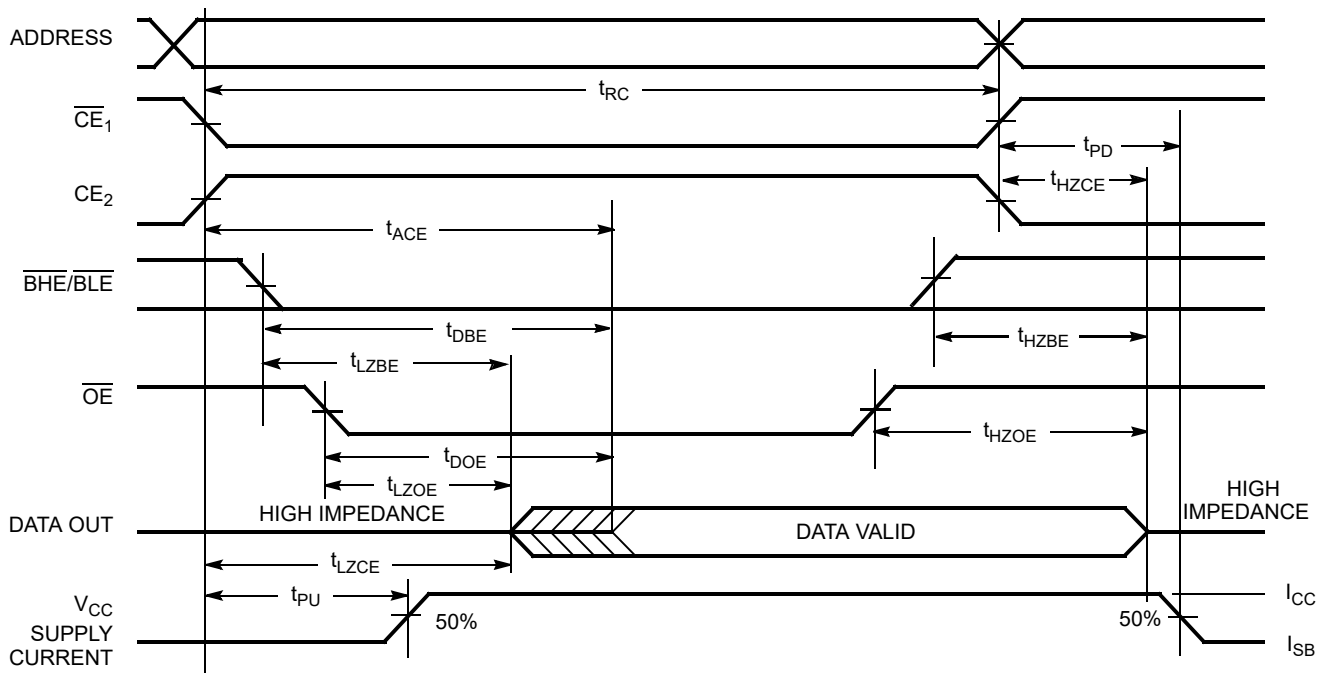


Figure 7. Read Cycle No. 2 (\overline{OE} Controlled) [24, 25]

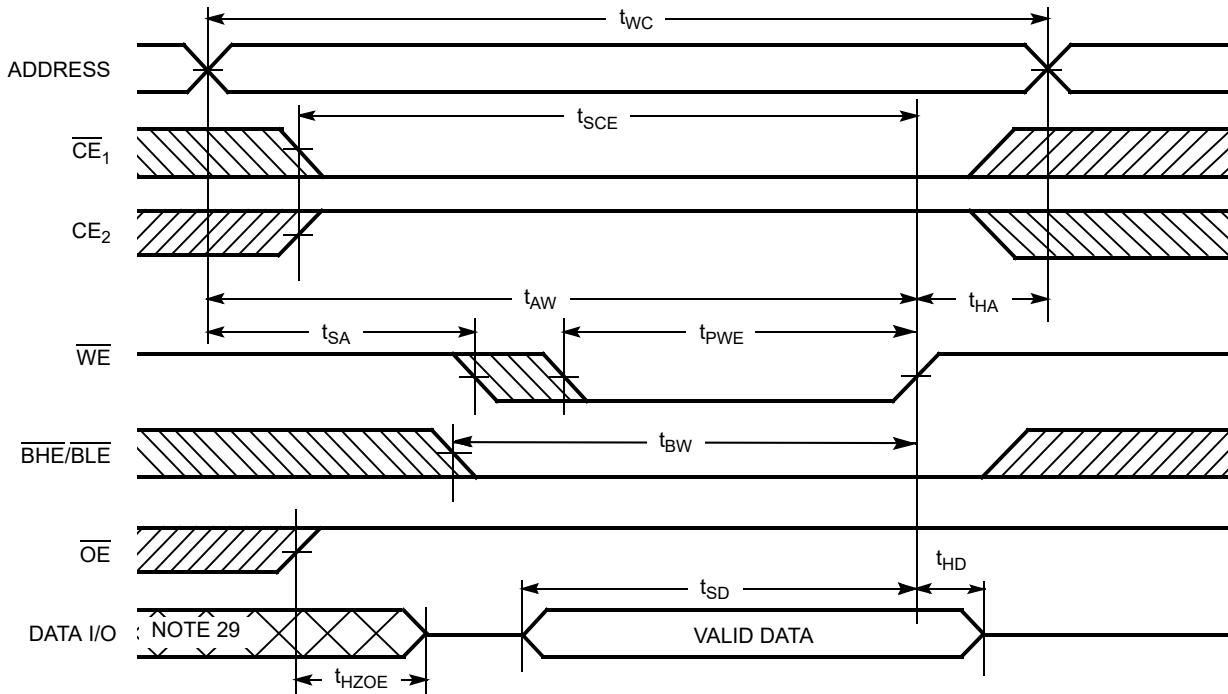


Notes

- 23. The device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} , \overline{BLE} , or both = V_{IL} , and $CE_2 = V_{IH}$.
- 24. WE is HIGH for read cycle.
- 25. Address valid before or similar to \overline{CE}_1 , \overline{BHE} , \overline{BLE} transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 (\overline{WE} Controlled) [26, 27, 28]



Notes

26. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} or both = V_{IL} , and $\overline{CE}_2 = V_{IH}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

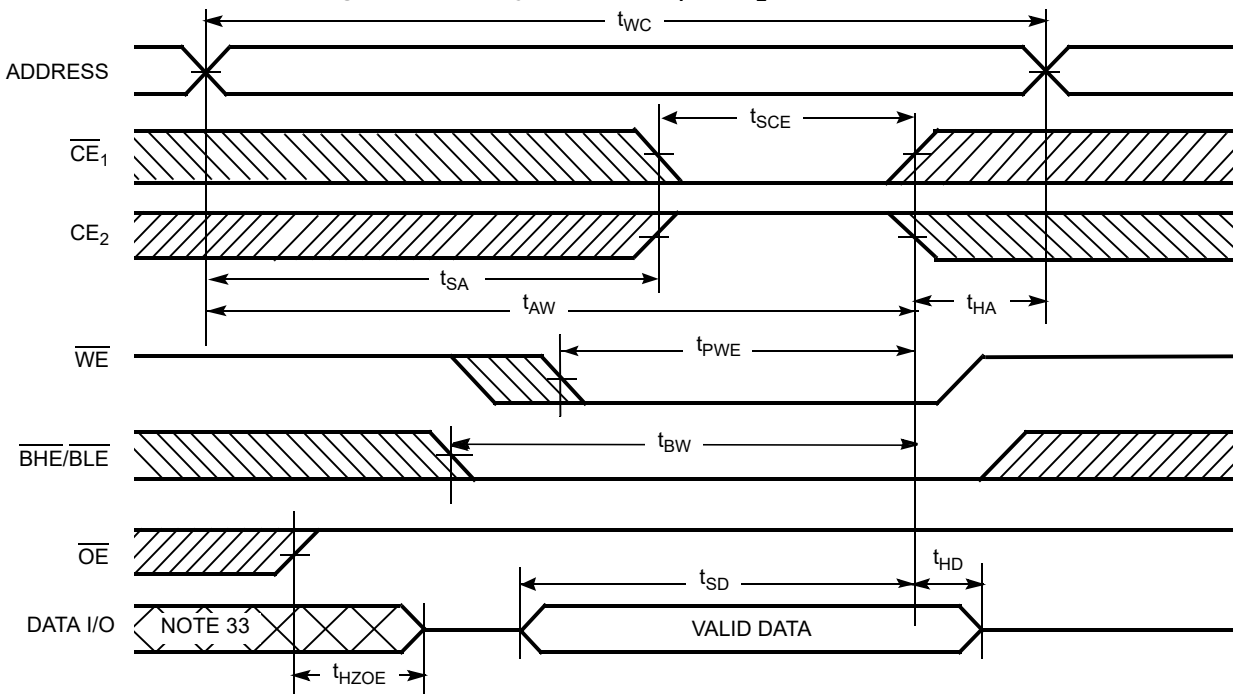
27. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

28. If \overline{CE}_1 goes HIGH and \overline{CE}_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.

29. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 2 (\overline{CE}_1 or CE_2 Controlled) [30, 31, 32]

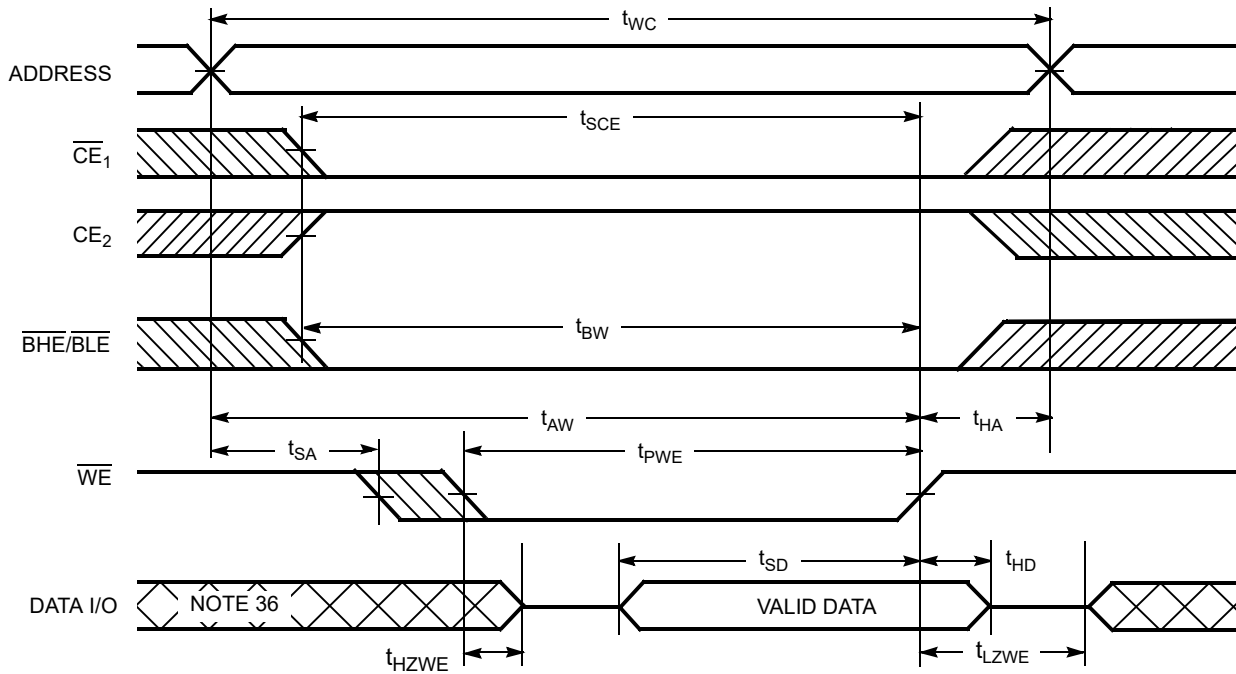


Notes

- 30. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
- 31. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 32. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 33. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 10. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [34, 35]

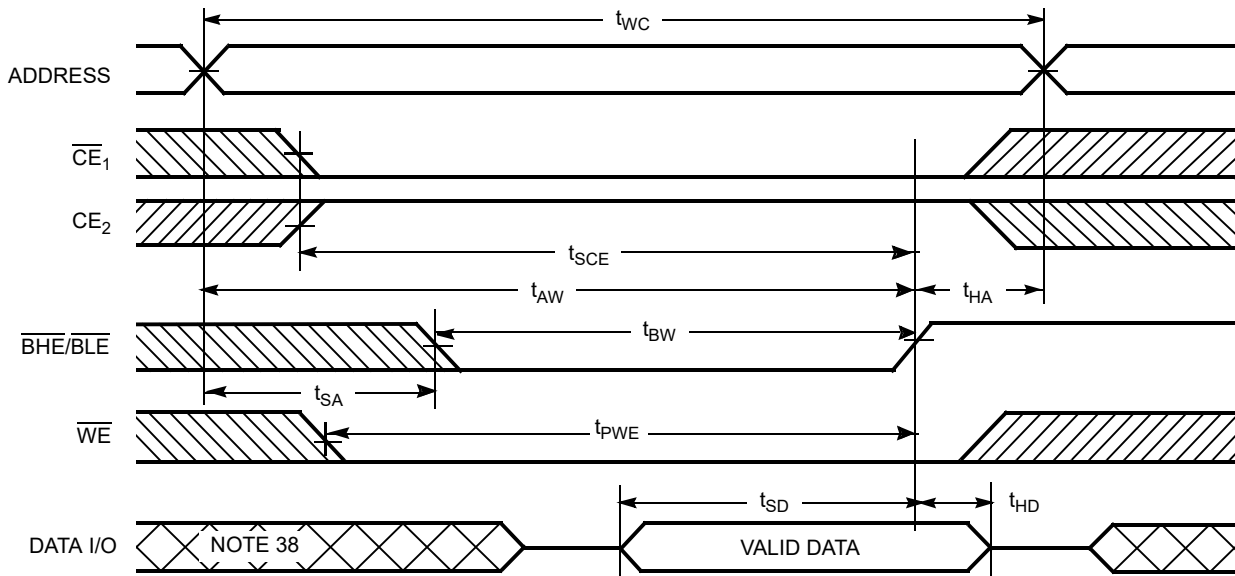


Notes

- 34. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 35. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE} .
- 36. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 11. Write Cycle No. 4 ($\overline{\text{BHE}}/\overline{\text{BLE}}$ Controlled, $\overline{\text{OE}}$ LOW) [37]



Notes

- 37. If $\overline{\text{CE}}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{\text{WE}} = V_{IH}$, the output remains in a high impedance state.
- 38. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

| \overline{CE}_1 | \overline{CE}_2 | \overline{WE} | \overline{OE} | \overline{BHE} | \overline{BLE} | Inputs/Outputs | Mode | Power |
|-------------------|-------------------|-----------------|-----------------|------------------|------------------|--|---------------------|----------------------|
| H | X ^[39] | X | X | X | X | High Z | Deselect/power down | Standby (I_{SB}) |
| X ^[39] | L | X | X | X | X | High Z | Deselect/power down | Standby (I_{SB}) |
| X ^[39] | X ^[39] | X | X | H | H | High Z | Deselect/power down | Standby (I_{SB}) |
| L | H | H | L | L | L | Data Out (I/O_0 – I/O_{15}) | Read | Active (I_{CC}) |
| L | H | H | L | H | L | Data Out (I/O_0 – I/O_7); High Z (I/O_8 – I/O_{15}) | Read | Active (I_{CC}) |
| L | H | H | L | L | H | High Z (I/O_0 – I/O_7); Data Out (I/O_8 – I/O_{15}) | Read | Active (I_{CC}) |
| L | H | H | H | L | H | High Z | Output disabled | Active (I_{CC}) |
| L | H | H | H | H | L | High Z | Output disabled | Active (I_{CC}) |
| L | H | H | H | L | L | High Z | Output disabled | Active (I_{CC}) |
| L | H | L | X | L | L | Data In (I/O_0 – I/O_{15}) | Write | Active (I_{CC}) |
| L | H | L | X | H | L | Data In (I/O_0 – I/O_7); High Z (I/O_8 – I/O_{15}) | Write | Active (I_{CC}) |
| L | H | L | X | L | H | High Z (I/O_0 – I/O_7); Data In (I/O_8 – I/O_{15}) | Write | Active (I_{CC}) |

Note

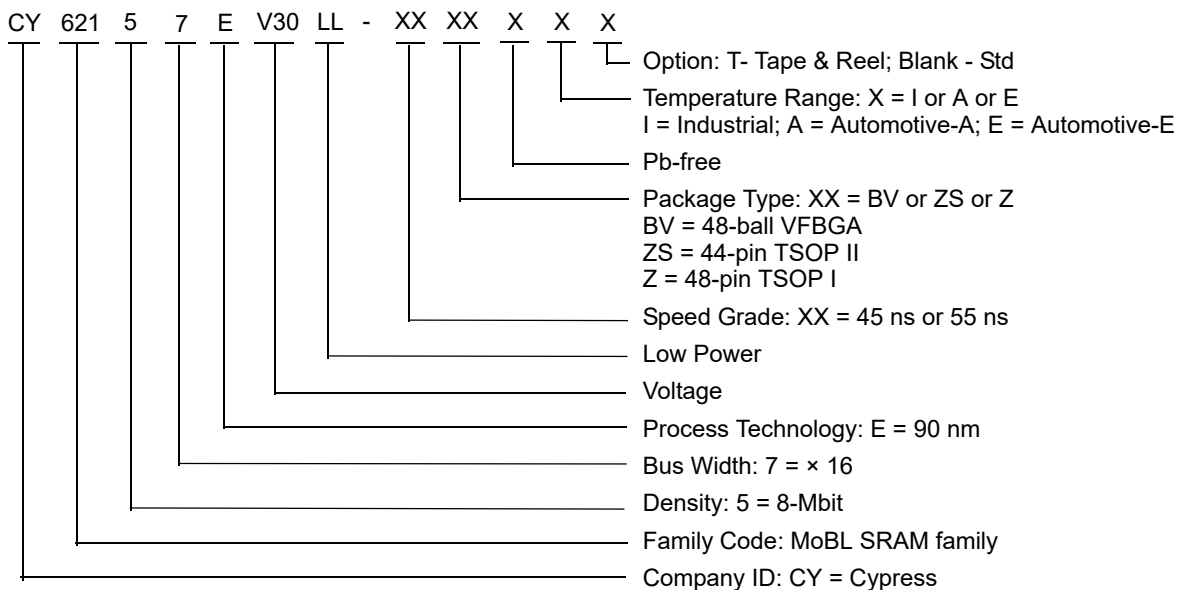
39. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|-----------------------|-----------------------|-------------------------------|-------------------------------|
| 45 | CY62157EV30LL-45BVI | 51-85150 | 48-ball VFBGA | Industrial |
| | CY62157EV30LL-45BVIT | 51-85150 | 48-ball VFBGA | |
| | CY62157EV30LL-45BVXI | 51-85150 | 48-ball VFBGA (Pb-free) | |
| | CY62157EV30LL-45BVXIT | 51-85150 | 48-ball VFBGA (Pb-free) | |
| | CY62157EV30LL-45ZSXI | 51-85087 | 44-pin TSOP Type II (Pb-free) | |
| | CY62157EV30LL-45ZSXIT | 51-85087 | 44-pin TSOP Type II (Pb-free) | |
| | CY62157EV30LL-45ZXI | 51-85183 | 48-pin TSOP Type I (Pb-free) | |
| | CY62157EV30LL-45ZXIT | 51-85183 | 48-pin TSOP Type I (Pb-free) | |
| | Automotive-A | CY62157EV30LL-45BVXA | 51-85150 | 48-ball VFBGA (Pb-free) |
| | | CY62157EV30LL-45BVXAT | 51-85150 | 48-ball VFBGA (Pb-free) |
| | | CY62157EV30LL-45ZSXA | 51-85087 | 44-pin TSOP Type II (Pb-free) |
| | | CY62157EV30LL-45ZSXAT | 51-85087 | 44-pin TSOP Type II (Pb-free) |
| | | CY62157EV30LL-45ZXA | 51-85183 | 48-pin TSOP Type I (Pb-free) |
| | | CY62157EV30LL-45ZXAT | 51-85183 | 48-pin TSOP Type I (Pb-free) |
| 55 | CY62157EV30LL-55ZSXE | 51-85087 | 44-pin TSOP Type II (Pb-free) | Automotive-E |
| | CY62157EV30LL-55ZSXET | 51-85087 | 44-pin TSOP Type II (Pb-free) | |
| | CY62157EV30LL-55ZXE | 51-85183 | 48-pin TSOP Type I (Pb-free) | |
| | CY62157EV30LL-55ZXET | 51-85183 | 48-pin TSOP Type I (Pb-free) | |

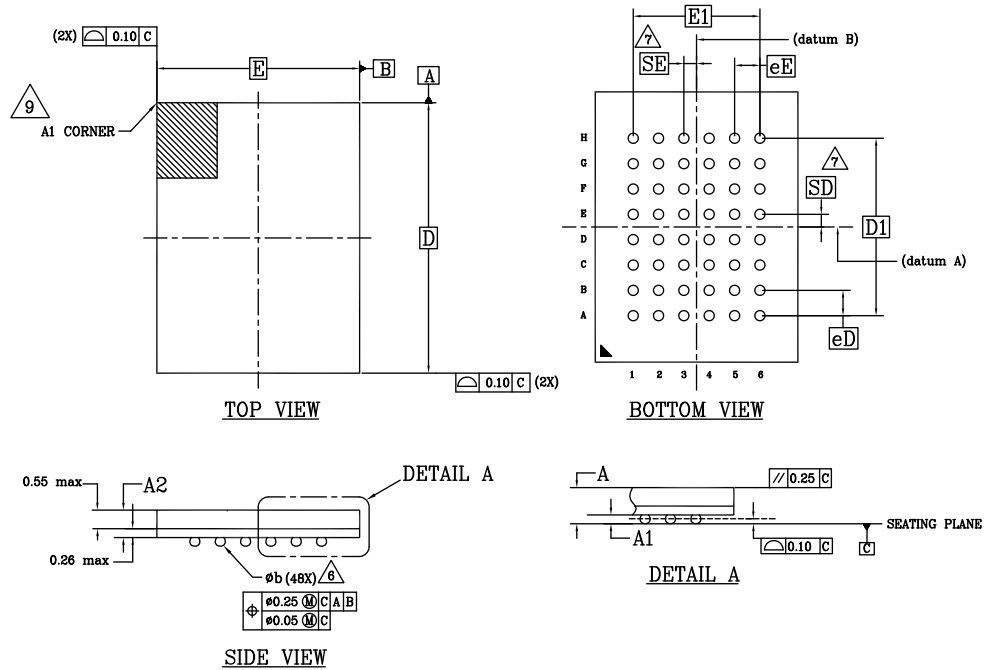
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

Figure 12. 48-pin VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150



| SYMBOL | DIMENSIONS | | |
|--------|------------|------|------|
| | MIN. | NOM. | MAX. |
| A | - | - | 1.00 |
| A1 | 0.16 | - | - |
| A2 | - | - | 0.81 |
| D | 8.00 BSC | | |
| E | 6.00 BSC | | |
| D1 | 5.25 BSC | | |
| E1 | 3.75 BSC | | |
| MD | 8 | | |
| ME | 6 | | |
| n | 48 | | |
| ∅ b | 0.25 | 0.30 | 0.35 |
| eE | 0.75 BSC | | |
| eD | 0.75 BSC | | |
| SD | 0.375 BSC | | |
| SE | 0.375 BSC | | |

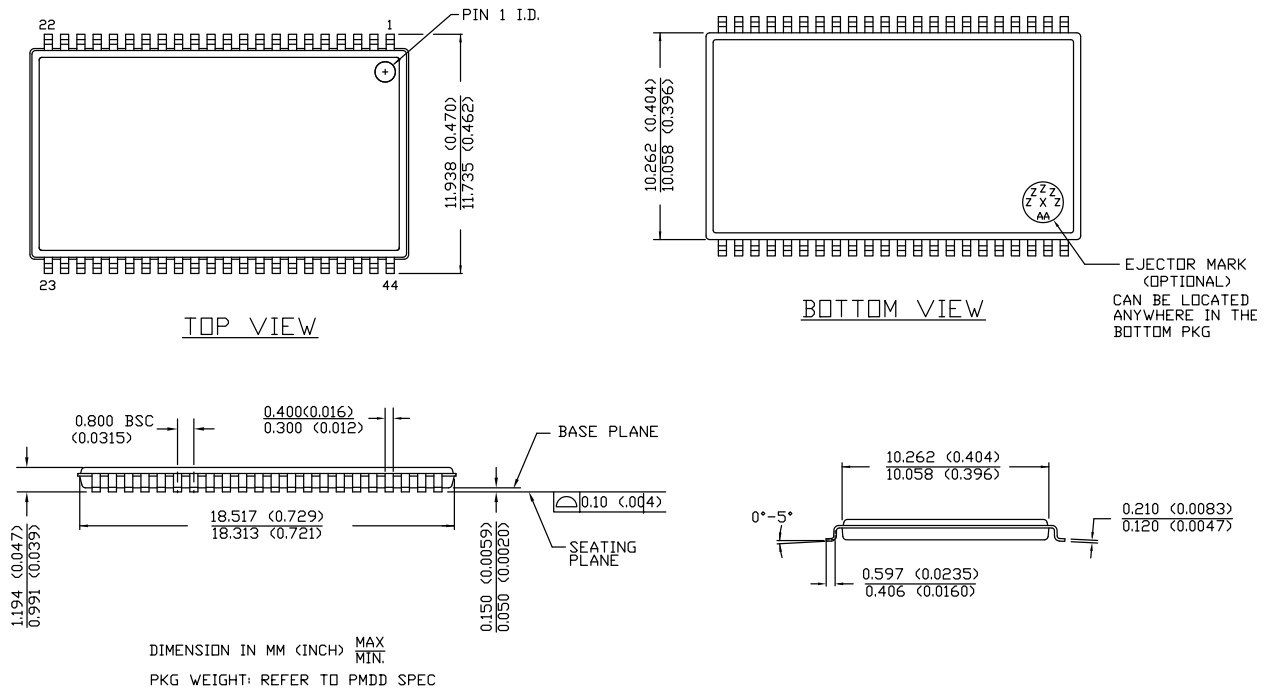
NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-2009.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
- \square REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION, SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION, n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- \triangle DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- \triangle "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- *-* INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- \triangle A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.

51-85150 *1

Package Diagrams (continued)

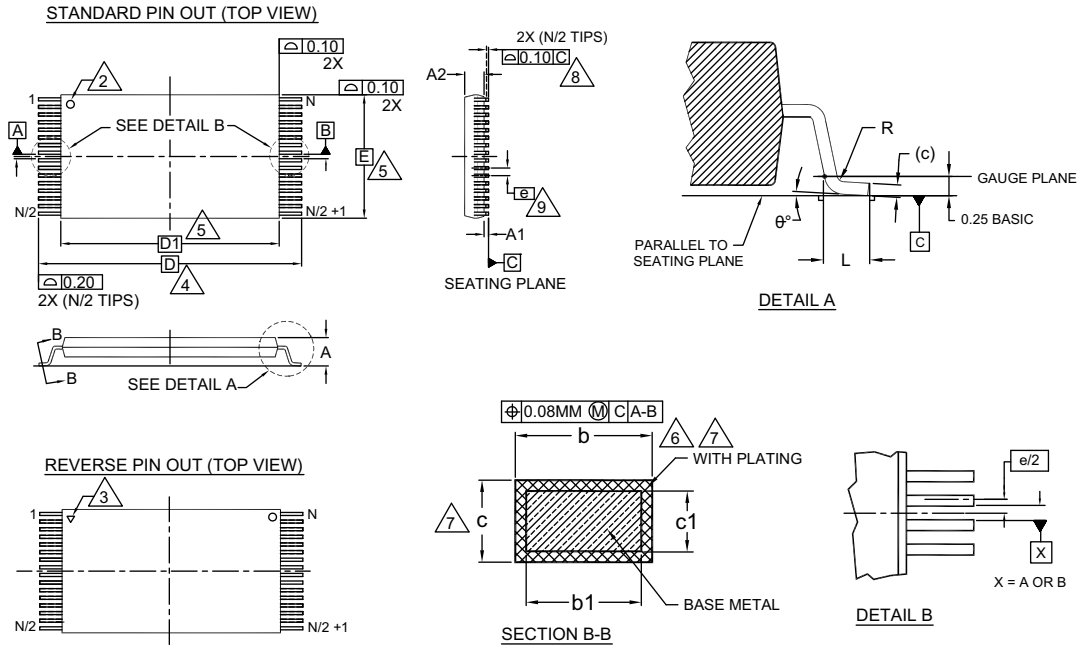
Figure 13. 44-pin TSOP II Package Outline, 51-85087



51-85087 *E

Package Diagrams (continued)

Figure 14. 48-pin TSOP I (18.4 × 12 × 1.2 mm) Package Outline, 51-85183



| SYMBOL | DIMENSIONS | | |
|--------|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b1 | 0.17 | 0.20 | 0.23 |
| b | 0.17 | 0.22 | 0.27 |
| c1 | 0.10 | — | 0.16 |
| c | 0.10 | — | 0.21 |
| D | 20.00 BASIC | | |
| D1 | 18.40 BASIC | | |
| E | 12.00 BASIC | | |
| e | 0.50 BASIC | | |
| L | 0.50 | 0.60 | 0.70 |
| θ | 0° | — | 8 |
| R | 0.08 | — | 0.20 |
| N | 48 | | |

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE [C-]. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm.
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 *F

Acronyms

| Acronym | Description |
|-----------------|---|
| \overline{CE} | Chip Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| \overline{OE} | Output Enable |
| RAM | Random Access Memory |
| SRAM | Static Random Access Memory |
| TSOP | Thin Small Outline Package |
| VFBGA | Very Fine-Pitch Ball Grid Array |
| \overline{WE} | Write Enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| MHz | megahertz |
| μA | microampere |
| μs | microsecond |
| mA | milliampere |
| mm | millimeter |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

Document History Page

| Document Title: CY62157EV30 MoBL [®] , 8-Mbit (512K × 16) Static RAM | | | | |
|---|--------|-----------------|-----------------|--|
| Document Number: 38-05445 | | | | |
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 202940 | AJU | 01/29/2004 | New data sheet. |
| *A | 291272 | SYT | 11/19/2004 | <p>Changed status from Advance Information to Preliminary.</p> <p>Removed 48-pin TSOP I Package related information in all instances across the document.</p> <p>Updated Pin Configurations:</p> <p>Added Note 2 and referred the same note in Figure 2.</p> <p>Updated Operating Range:</p> <p>Updated Note 7 (Replaced 100 μs with 200 μs).</p> <p>Updated Data Retention Characteristics:</p> <p>Changed maximum value of I_{CCDR} parameter from 4 μA to 4.5 μA.</p> <p>Updated Switching Characteristics:</p> <p>Changed minimum value of t_{OHA} parameter from 6 ns to 10 ns corresponding to both 35 and 45 ns speed bins.</p> <p>Changed maximum value of t_{DOE} parameter from 15 ns to 18 ns corresponding to 35 ns speed bin.</p> <p>Changed maximum value of t_{HZOE} parameter from 12 ns to 15 ns corresponding to 35 ns speed bin.</p> <p>Changed maximum value of t_{HZOE} parameter from 15 ns to 18 ns corresponding to 45 ns speed bin.</p> <p>Changed maximum value of t_{HZCE} parameter from 12 ns to 18 ns corresponding to 35 ns speed bin.</p> <p>Changed maximum value of t_{HZCE} parameter from 15 ns to 22 ns corresponding to 45 ns speed bin.</p> <p>Changed maximum value of t_{HZBE} parameter from 12 ns to 15 ns corresponding to 35 ns speed bin.</p> <p>Changed maximum value of t_{HZBE} parameter from 15 ns to 18 ns corresponding to 45 ns speed bin.</p> <p>Changed minimum value of t_{SCE} parameter from 25 ns to 30 ns corresponding to 35 ns speed bin.</p> <p>Changed minimum value of t_{SCE} parameter from 40 ns to 35 ns corresponding to 45 ns speed bin.</p> <p>Changed minimum value of t_{AW} parameter from 25 ns to 30 ns corresponding to 35 ns speed bin.</p> <p>Changed minimum value of t_{AW} parameter from 40 ns to 35 ns corresponding to 45 ns speed bin.</p> <p>Changed minimum value of t_{BW} parameter from 25 ns to 30 ns corresponding to 35 ns speed bin.</p> <p>Changed minimum value of t_{BW} parameter from 40 ns to 35 ns corresponding to 45 ns speed bin.</p> <p>Changed minimum value of t_{SD} parameter from 15 ns to 18 ns corresponding to 35 ns speed bin.</p> <p>Changed minimum value of t_{SD} parameter from 20 ns to 22 ns corresponding to 45 ns speed bin.</p> <p>Changed maximum value of t_{HZWE} parameter from 12 ns to 15 ns corresponding to 35 ns speed bin.</p> <p>Changed maximum value of t_{HZWE} parameter from 15 ns to 18 ns corresponding to 45 ns speed bin.</p> <p>Updated Ordering Information:</p> <p>Updated part numbers.</p> |

Document History Page (continued)

| Document Title: CY62157EV30 MoBL [®] , 8-Mbit (512K × 16) Static RAM Document Number: 38-05445 | | | | |
|--|--------|-----------------|-----------------|---|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| *B | 444306 | NXR | 04/13/2006 | <p>Changed status from Preliminary to Final.</p> <p>Removed 35 ns speed bin related information in all instances across the document.</p> <p>Added 55 ns speed bin related information in all instances across the document.</p> <p>Added 48-pin TSOP I Package related information in all instances across the document.</p> <p>Added Automotive Temperature Range related information in all instances across the document.</p> <p>Updated Pin Configurations:</p> <p>Updated Figure 1 (Replaced DNU with NC in ball E3).</p> <p>Removed Note "DNU pins have to be left floating or tied to V_{SS} to ensure proper application." and its reference.</p> <p>Updated Product Portfolio:</p> <p>Removed "L" and "LL" from the part numbers.</p> <p>Updated Electrical Characteristics:</p> <p>Changed typical value of I_{CC} parameter from 16 mA to 18 mA corresponding to 45 ns speed bin and Test Condition "f = fax = 1/t_{RC}".</p> <p>Changed maximum value of I_{CC} parameter from 28 mA to 25 mA corresponding to 45 ns speed bin and Test Condition "f = fax = 1/t_{RC}".</p> <p>Changed maximum value of I_{CC} parameter from 2.3 mA to 3 mA corresponding to 45 ns speed bin and Test Condition "f = 1 MHz".</p> <p>Updated details in "Test Condition" column corresponding to I_{SB1} parameter.</p> <p>Changed typical value of I_{SB1} parameter from 0.9 μA to 2 μA corresponding to 45 ns speed bin.</p> <p>Changed maximum value of I_{SB1} parameter from 4.5 μA to 8 μA corresponding to 45 ns speed bin.</p> <p>Changed typical value of I_{SB2} parameter from 0.9 μA to 2 μA corresponding to 45 ns speed bin.</p> <p>Changed maximum value of I_{SB2} parameter from 4.5 μA to 8 μA corresponding to 45 ns speed bin.</p> <p>Updated Thermal Resistance:</p> <p>Replaced TBD with values in TSOP II column and updated all remaining values.</p> <p>Updated AC Test Loads and Waveforms:</p> <p>Updated Figure 4 (Replaced 50 pF with 30 pF).</p> <p>Updated Data Retention Characteristics:</p> <p>Added value in "Typ" column for I_{CCDR} parameter.</p> <p>Changed maximum value of I_{CCDR} parameter from 4.5 μA to 5 μA corresponding to Test Condition "Industrial".</p> <p>Changed minimum value of t_R parameter from 100 μs to t_{RC} ns.</p> |

Document History Page (continued)

| Document Title: CY62157EV30 MoBL [®] , 8-Mbit (512K × 16) Static RAM Document Number: 38-05445 | | | | |
|--|---------|-----------------|-----------------|--|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| *B (cont.) | 444306 | NXR | 04/13/2006 | Updated Switching Characteristics : Changed minimum value of t_{LZOE} parameter from 3 ns to 5 ns corresponding to 45 ns speed bin. Changed minimum value of t_{LZCE} parameter from 6 ns to 10 ns corresponding to 45 ns speed bin. Changed maximum value of t_{HZCE} parameter from 22 ns to 18 ns corresponding to 45 ns speed bin. Changed minimum value of t_{LZBE} parameter from 6 ns to 5 ns corresponding to 45 ns speed bin. Changed minimum value of t_{PWE} parameter from 30 ns to 35 ns corresponding to 45 ns speed bin. Changed minimum value of t_{SD} parameter from 22 ns to 25 ns corresponding to 45 ns speed bin. Changed minimum value of t_{LZWE} parameter from 6 ns to 10 ns corresponding to 45 ns speed bin. Added Note 20 and referred the same note in t_{LZBE} parameter. Updated Ordering Information : Updated part numbers. Removed "Package Name" column. Added "Package Diagram" column. |
| *C | 467052 | NXR | 06/06/2006 | Added 1M × 8 configuration related information in all instances across the document. Updated Ordering Information : Updated part numbers. |
| *D | 925501 | VKN | 04/09/2007 | Removed Automotive-E temperature range related information in all instances across the document. Added Preliminary Automotive-A related information in all instances across the document. Updated Electrical Characteristics : Added Note 9 and referred the same note in I_{SB2} parameter. Updated Switching Characteristics : Added Note 17 and referred the same note in "Parameter" column. |
| *E | 1045801 | VKN | 05/08/2007 | Changed Automotive-A temperature range related information from Preliminary to Final. Updated Electrical Characteristics : Updated Note 9. |
| *F | 2724889 | NXR / AESA | 06/26/2009 | Added Automotive-E temperature range related information in all instances across the document. Updated Ordering Information : Updated part numbers. Updated to new template. |
| *G | 2927528 | VKN | 05/04/2010 | Updated Pin Configurations : Updated Figure 3 (Renamed "DNU" pins as "NC"). Updated Truth Table : Added Note 39 and referred the same note in "X" in " \overline{CE}_1 " and " \overline{CE}_2 " columns. Updated Package Diagrams : spec 51-85150 – Changed revision from *D to *E. spec 51-85087 – Changed revision from *A to *C. spec 51-85183 – Changed revision from *A to *B. Updated to new template. |
| *H | 3110053 | PRAS | 12/14/2010 | Changed Table Footnotes to Notes. Updated Ordering Information : No change in part numbers. Added Ordering Code Definitions . |

Document History Page (continued)

| Document Title: CY62157EV30 MoBL [®] , 8-Mbit (512K × 16) Static RAM Document Number: 38-05445 | | | | |
|--|---------|-----------------|-----------------|---|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| *I | 3269771 | RAME | 05/30/2011 | Updated Functional Description : Updated description. Updated Electrical Characteristics : Updated details in “Conditions” column corresponding to I _{SB1} and I _{SB2} parameters. Updated Data Retention Characteristics : Updated details in “Conditions” and “Min” columns corresponding to I _{CCDR} and t _R parameters. Updated Package Diagrams : spec 51-85150 – Changed revision from *E to *F. Added Acronyms and Units of Measure . Updated to new template. Completing Sunset Review. |
| *J | 3578601 | TAVA | 04/11/2012 | Updated Package Diagrams : spec 51-85150 – Changed revision from *F to *G. spec 51-85087 – Changed revision from *C to *D. spec 51-85183 – Changed revision from *B to *C. Completing Sunset Review. |
| *K | 4102449 | VINI | 08/22/2013 | Updated Switching Characteristics : Updated Note 17. Updated Package Diagrams : spec 51-85150 – Changed revision from *G to *H. spec 51-85087 – Changed revision from *D to *E. Updated to new template. |
| *L | 4126231 | VINI | 09/18/2013 | Updated Switching Characteristics : Updated Note 17 (Removed last sentence from Note 17 and added the same sentence as a new note namely Note 18). |
| *M | 4214977 | MEMJ | 12/09/2013 | Updated Pin Configurations : Updated Note 3 (Removed ‘NC’ mentioned at the end of the note). |
| *N | 4578508 | MEMJ | 11/24/2014 | Updated Functional Description : Added “For a complete list of related documentation, click here .” at the end. Updated Switching Characteristics : Added Note 22 and referred the same note in “Write Cycle”. Updated Switching Waveforms : Added Note 35 and referred the same note in Figure 10 . |
| *O | 4748627 | NILE | 04/30/2015 | Updated Package Diagrams : spec 51-85183 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review. |
| *P | 5320972 | NILE | 06/23/2016 | Updated Thermal Resistance : Replaced “two-layer” with “four-layer” in “Test Conditions” column. Updated values of Θ_{JA} , Θ_{JC} parameters corresponding to all packages. Updated Ordering Information : Updated part numbers. Updated to new template. |
| *Q | 5731504 | NILE | 05/10/2017 | Updated Package Diagrams : spec 51-85183 – Changed revision from *D to *F. Updated to new template. Completing Sunset Review. |
| *R | 6517814 | NILE | 03/21/2019 | Updated Package Diagrams : spec 51-85150 – Changed revision from *H to *I. Updated to new template. |

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