THE DATASHEET OF

CY62148EV30LL-45ZSXA

CY62148EV30 MoBL®

4-Mbit (512K × 8) Static RAM

Features

- Very high speed: 45 ns
  - Wide voltage range: 2.20 V to 3.60 V
- Temperature range:
  - Industrial: –40 °C to +85 °C
  - Automotive-A: –40 °C to +85 °C
- Pin compatible with CY62148DV30
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 7 µA (Industrial)
- Ultra low active power
  - Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 36-ball very fine-pitch ball grid array (VFBGA), 32-pin thin small outline package (TSOP) II, and 32-pin small outline integrated circuit (SOIC)[1] packages

Functional Description

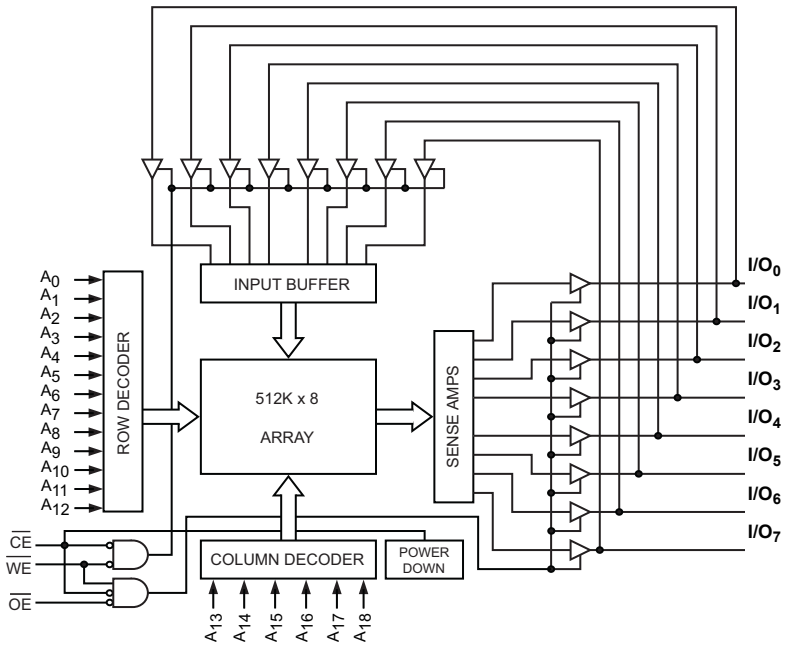
The CY62148EV30 is a high performance CMOS static RAM organized as 512K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected ($\overline{CE}$ HIGH). The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

For a complete list of related 1documentation, click here.

Logic Block Diagram



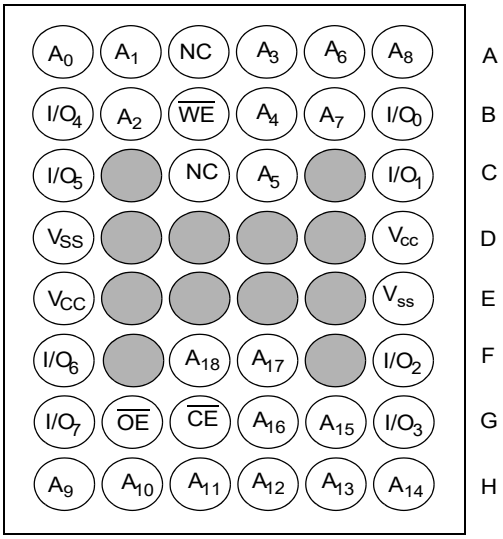
Note
1. SOIC package is available only in 55 ns speed bin.

Contents

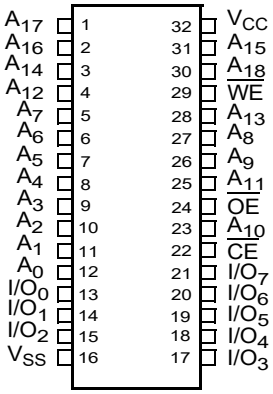
Pin Configurations

VFBGA, SOIC and TSOP II pinouts are as follows. [2, 3]

36-ball VFBGA pinout
Top View



32-pin SOIC/TSOP II pinout
Top View



Product Portfolio

Product		Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
							Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
							f = 1 MHz		f = f_{max}			
			Min	Typ [4]	Max		Typ [4]	Max	Typ [4]	Max	Typ [4]	Max
CY62148EV30LL	VFBGA	Industrial	2.2	3.0	3.6	45	2	2.5	15	20	1	7
	TSOP II	Industrial / Automotive-A										
	SOIC	Industrial	2.2	3.0	3.6	55	2	2.5	15	20	1	7

Notes
2. SOIC package is available only in 55 ns speed bin.
3. NC pins are not connected on the die.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... 55 °C to +125 °C

Supply voltage to ground potential .....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC voltage applied to outputs in High Z State [5, 6] .....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC input voltage [5, 6] .....–0.3 V to $V_{CC(max)}$ + 0.3 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch up current .....> 200 mA

Operating Range

Product	Range	Ambient Temperature	V_{CC} [7]
CY62148EV30	Industrial / Automotive-A	–40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-45 (Industrial / Automotive-A)			-55 [8]			Unit
				Min	Typ [9]	Max	Min	Typ [9]	Max	
V_{OH}	Output high voltage	I_{OH} = –0.1 mA		2.0	–	–	2.0	–	–	V
		I_{OH} = –1.0 mA, $V_{CC} \geq$ 2.70 V		2.4	–	–	2.4	–	–	V
V_{OL}	Output low voltage	I_{OL} = 0.1 mA		–	–	0.4	–	–	0.2	V
		I_{OL} = 2.1 mA, $V_{CC} \geq$ 2.70 V		–	–	0.4	–	–	0.4	V
V_{IH}	Input high voltage	V_{CC} = 2.2 V to 2.7 V		1.8	–	V_{CC} + 0.3	1.8	–	V_{CC} + 0.3	V
		V_{CC} = 2.7 V to 3.6 V		2.2	–	V_{CC} + 0.3	2.2	–	V_{CC} + 0.3	V
V_{IL}	Input low voltage	V_{CC} = 2.2 V to 2.7 V	For VFBGA and TSOP II packages	–0.3	–	0.6	–	–	–	V
			For SOIC package	–	–	–	–0.3	–	0.4 [10]	V
		V_{CC} = 2.7 V to 3.6 V	For VFBGA and TSOP II packages	–0.3	–	0.8	–	–	–	V
			For SOIC package	–	–	–	–0.3	–	0.6 [10]	
I_{IX}	Input leakage current	GND $\leq V_I \leq V_C$		–1	–	+1	–1	–	+1	µA
I_{OZ}	Output leakage current	GND $\leq V_O \leq V_{CC}$, Output disabled		–1	–	+1	–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = $1/t_{RC}$	$V_{CC} = V_{CC(max)}$, I_{OUT} = 0 mA, CMOS levels	–	15	20	–	15	20	mA
		f = 1 MHz		–	2	2.5	–	2	2.5	
I_{SB1} [11]	Automatic CE power down current – CMOS inputs	$\overline{CE} \geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V, $V_{IN} \leq$ 0.2 V, f = f_{max} (Address and Data Only), f = 0 ($\overline{OE}$ and $\overline{WE}$), V_{CC} = 3.60 V		–	1	7	–	1	7	µA
I_{SB2} [11]	Automatic CE power down current – CMOS inputs	$\overline{CE} \geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, V_{CC} = 3.60 V		–	1	7	–	1	7	µA

Notes

5. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
6. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
7. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
8. SOIC package is available only in 55 ns speed bin.
9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
10. Under DC conditions the device meets a V_{IL} of 0.8V (for V_{CC} range of 2.7 V to 3.6 V) and 0.6 V (for V_{CC} range of 2.2 V to 2.7 V). However, in dynamic conditions Input LOW voltage applied to the device must not be higher than 0.6V and 0.4V for the above ranges. This is applicable to SOIC package only.
11. Chip Enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

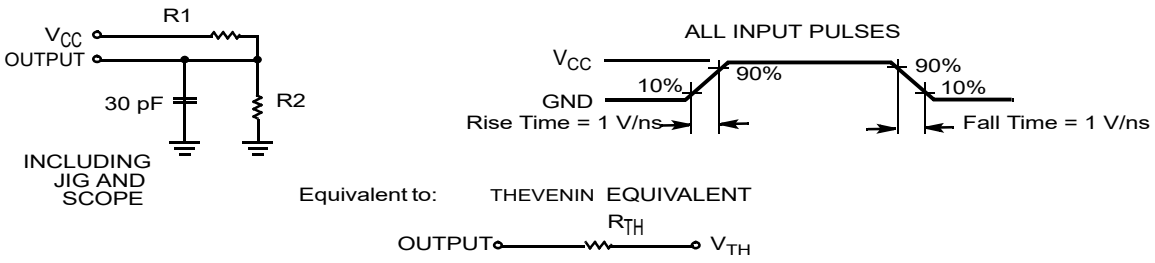
Parameter [12]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [12]	Description	Test Conditions	36-ball VFBGA Package	32-pin TSOP II Package	32-pin SOIC Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	44.79	59.10	51.57	°C/W
Θ_{JC}	Thermal resistance (junction to case)		23.17	12.19	25.01	°C/W

AC Test Loads and Waveforms

Figure 1. AC Test Loads and Waveforms



Parameters	2.50 V	3.0 V	Unit
R_1	16667	1103	Ω
R_2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note
12. Tested initially and after any design or process changes that may affect these parameters.

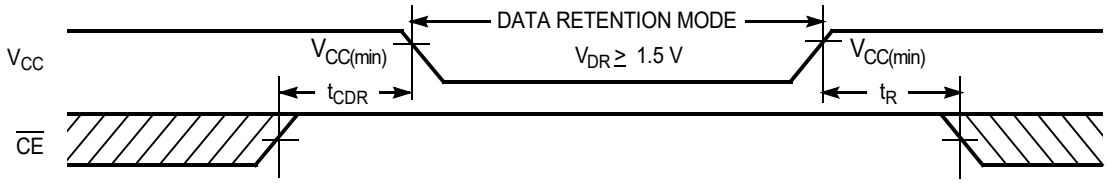
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ [13]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5	–	–	V
I_{CCDR} [14]	Data retention current	V_{CC} = 1.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Industrial / Automotive-A	–	0.8	7	µA
t_{CDR}[15]	Chip deselect to data retention time			0	–	–	ns
t_R[16]	Operation recovery time		CY62148EV30LL-45	45	–	–	ns
			CY62148EV30LL-55	55	–	–	ns

Data Retention Waveform

Figure 2. Data Retention Waveform



Notes

13. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
14. Chip Enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
15. Tested initially and after any design or process changes that may affect these parameters.
16. Full device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

Switching Characteristics

Over the Operating Range

Parameter [17, 18]	Description	-45 (Industrial / Automotive-A)		-55 [19]		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45	–	55	–	ns
t_{AA}	Address to data valid	–	45	–	55	ns
t_{OHA}	Data hold from address change	10	–	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [20]	5	–	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [20, 21]	–	18	–	20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [20]	10	–	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [20, 21]	–	18	–	20	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down	–	45	–	55	ns
Write Cycle [22, 23]						
t_{WC}	Write cycle time	45	–	55	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	40	–	ns
t_{AW}	Address setup to write end	35	–	40	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	40	–	ns
t_{SD}	Data setup to write end	25	–	25	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [20, 21]	–	18	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [20]	10	–	10	–	ns

Notes

17. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the chip enable signal as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Note is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
18. Test Conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 1 on page 5.
19. SOIC package is available only in 55 ns speed bin.
20. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
21. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the output enter a high impedance state.
22. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
23. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 3. Read Cycle No. 1 (Address Transition Controlled) [24, 25]

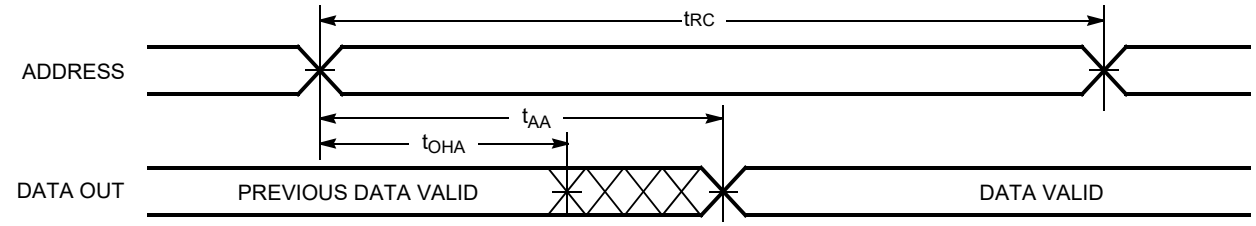


Figure 4. Read Cycle No. 2 ($\overline{OE}$ Controlled) [25, 26]

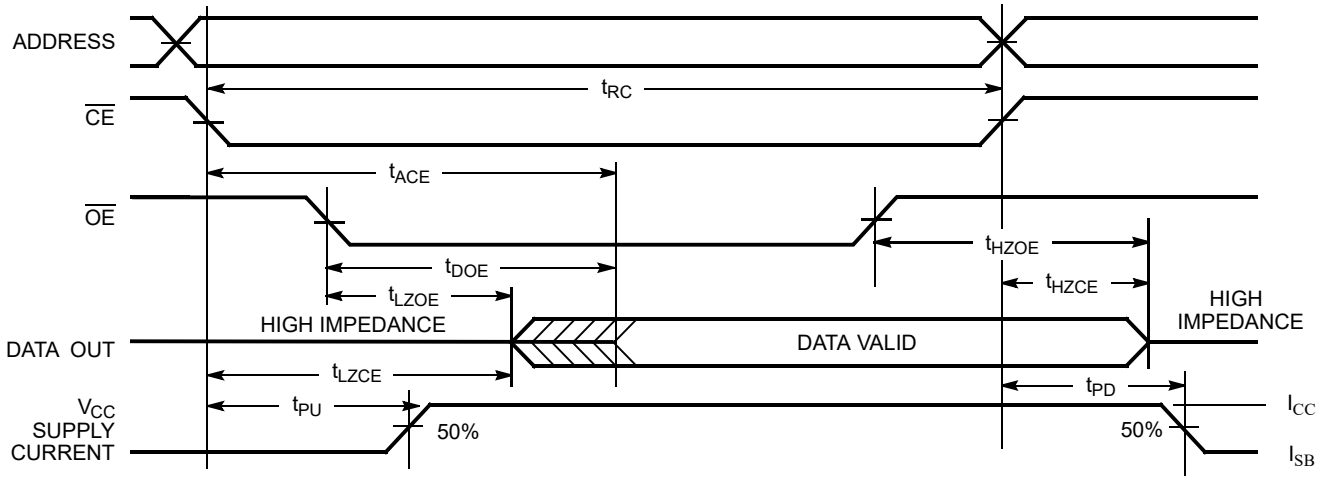
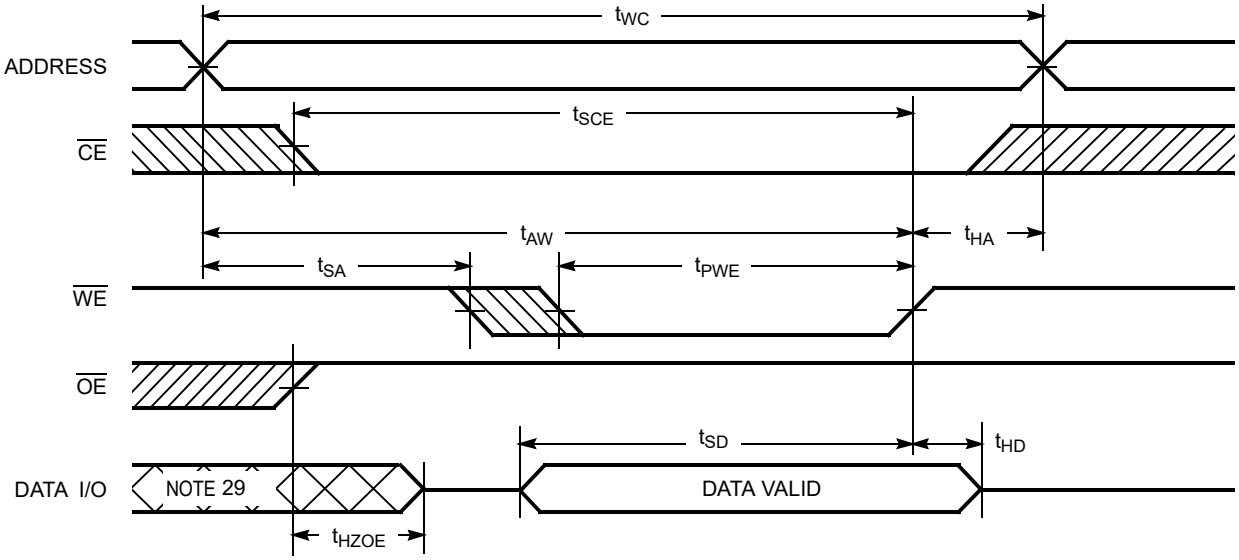


Figure 5. Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) [27, 28]



Notes
24. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
25. $\overline{WE}$ is HIGH for read cycles.
26. Address valid before or similar to $\overline{CE}$ transition LOW.
27. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
28. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
29. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 2 ($\overline{CE}$ Controlled) [30, 31]

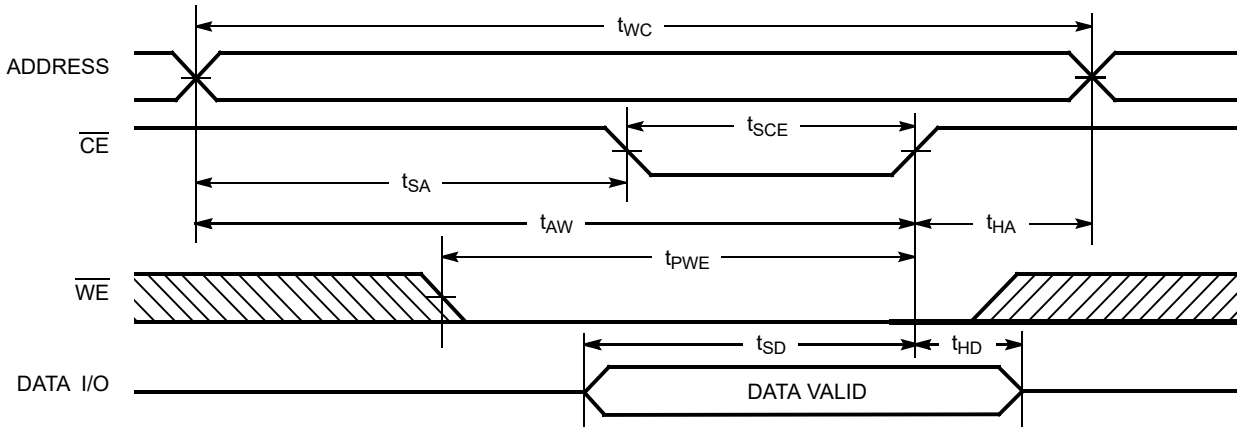
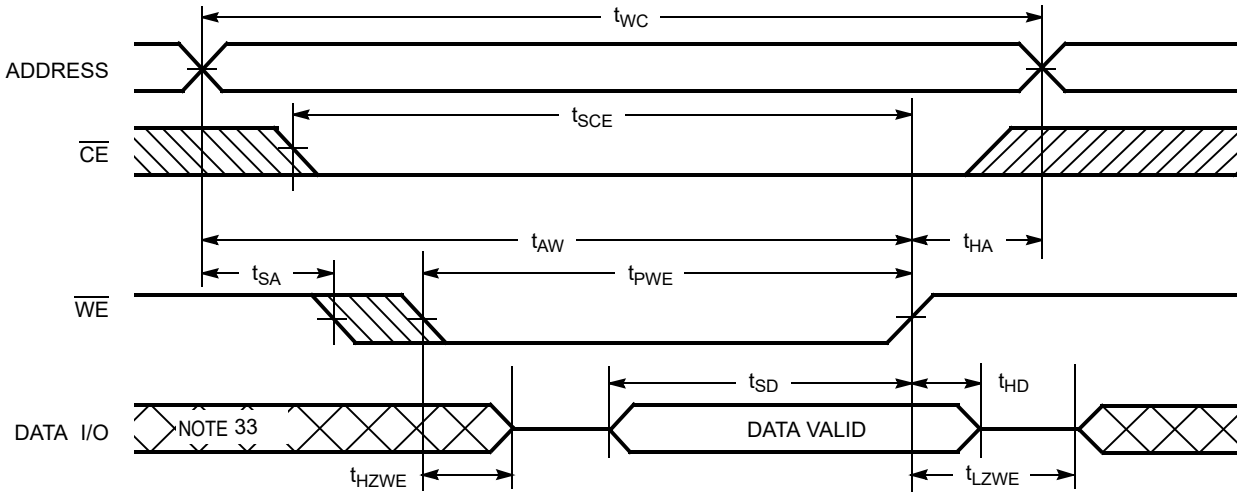


Figure 7. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [31, 32]



Notes
30. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
31. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
32. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.
33. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$ [34]	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power down	Standby (I_{SB})
L	H	L	Data out	Read	Active (I_{CC})
L	H	H	High Z	Output disabled	Active (I_{CC})
L	L	X	Data in	Write	Active (I_{CC})

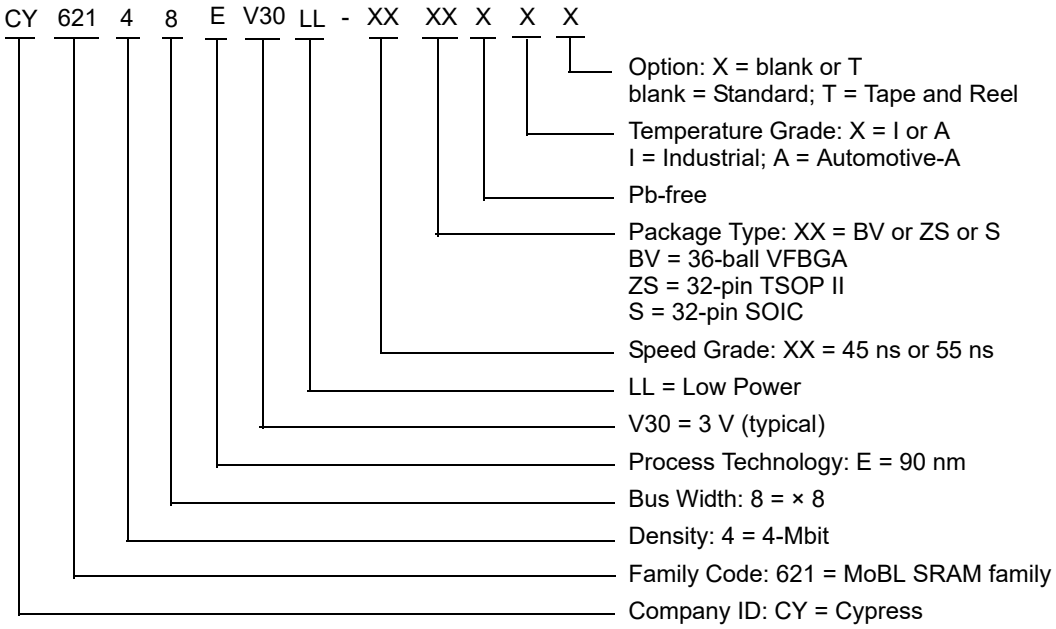
Note
34. Chip enable must be at CMOS levels (not floating). Intermediate voltage levels on this pin is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62148EV30LL-45BVI	51-85149	36-ball VFBGA	Industrial
	CY62148EV30LL-45BVXI	51-85149	36-ball VFBGA (Pb-free)	
	CY62148EV30LL-45BVXIT	51-85149	36-ball VFBGA (Pb-free)	
	CY62148EV30LL-45ZSXI	51-85095	32-pin TSOP II (Pb-free)	
55	CY62148EV30LL-55SXI	51-85081	32-pin SOIC (Pb-free)	Industrial

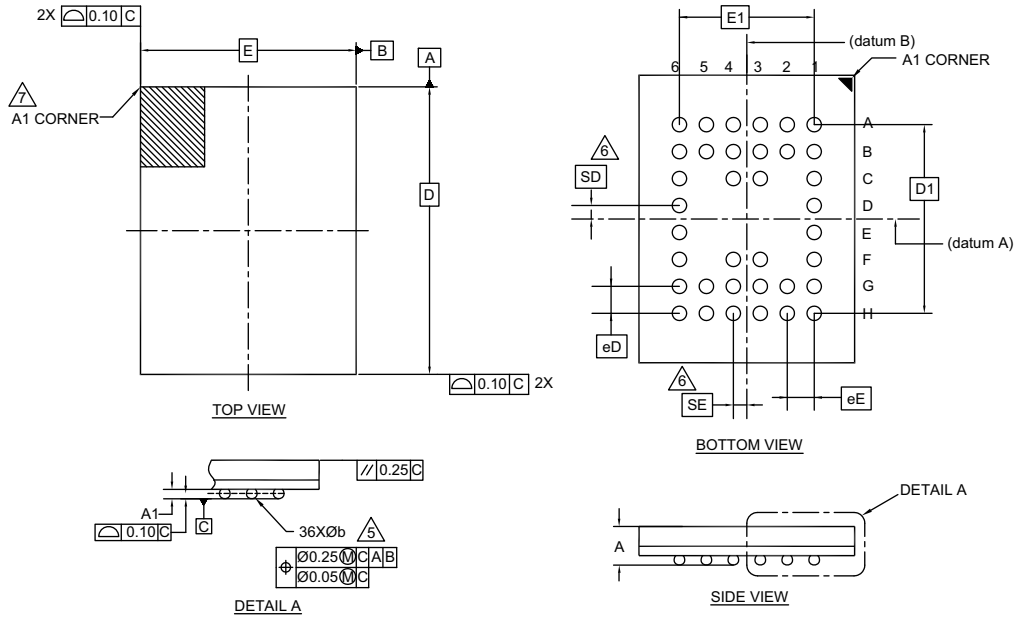
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

Figure 8. 36-ball VFBGA (8.0 × 6.0 × 1.0 mm) Package Outline, 51-85149



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
D	8.00 BSC		
E	6.00 BSC		
D1	5.25 BSC		
E1	3.75 BSC		
MD	8		
ME	6		
N	36		
Ø b	0.25	0.30	0.35
eD	0.75 BSC		
eE	0.75 BSC		
SD	0.375 BSC		
SE	0.375 BSC		

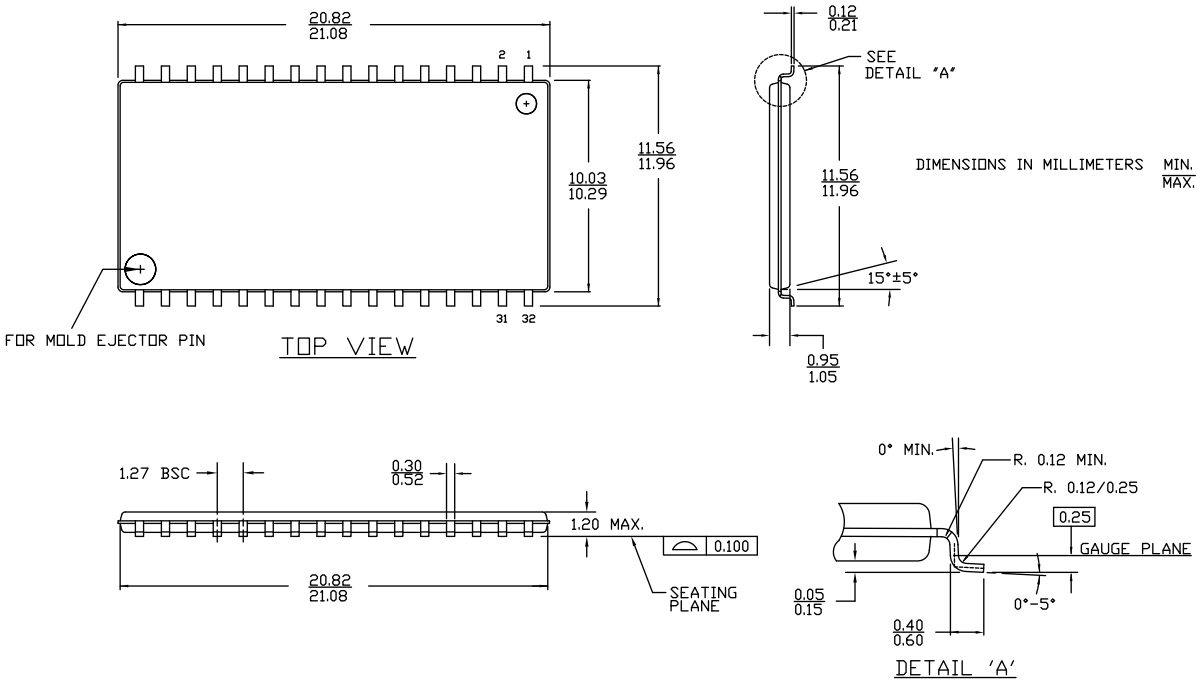
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

51-85149 *G

Package Diagrams (continued)

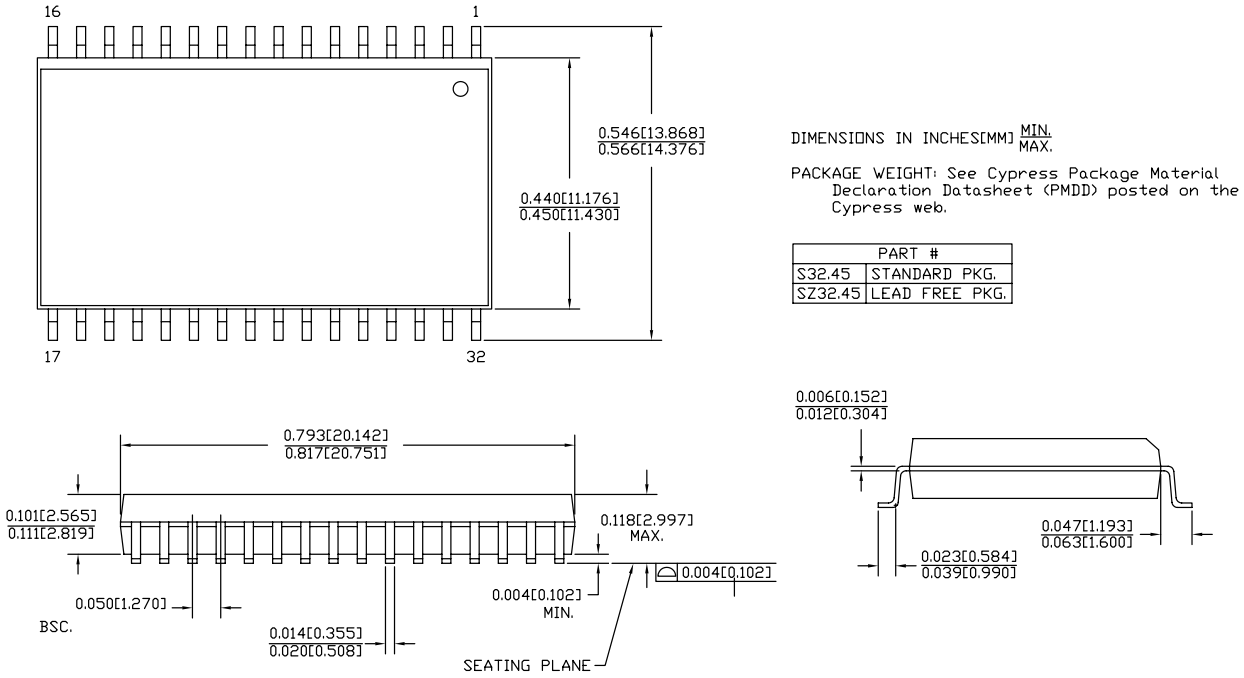
Figure 9. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) Package Outline, 51-85095



51-85095 *D

Package Diagrams (continued)

Figure 10. 32-pin SOIC (450 Mils) Package Outline, 51-85081



51-85081 *E

Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
CMOS	Complementary Metal Oxide Semiconductor
$\overline{CE}$	Chip Enable
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	microampere
mA	milliampere
ns	nanosecond
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62148EV30 MoBL®, 4-Mbit (512K × 8) Static RAM Document Number: 38-05576				
Region	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	223225	AJU	05/05/2004	New data sheet.
*A	247373	SYT	07/28/2004	Changed status from Advance Information to Preliminary. Updated Operating Range (Updated Note 7 (Changed V_{CC} stabilization time from 100 µs to 200 µs)). Updated Data Retention Characteristics (Changed maximum value of I_{CCDR} parameter from 2.0 µA to 2.5 µA; changed minimum value of t_R parameter from 100 µs to t_{RC} ns). Updated Switching Characteristics (Changed minimum value of t_{OHA} parameter from 6 ns to 10 ns for both 35 ns and 45 ns speed bin; changed maximum value of t_{DOE} parameter from 15 ns to 18 ns for 35 ns speed bin; changed maximum value of t_{HZOE}, t_{HZWE} parameters from 12 ns to 15 ns for 35 ns speed bin and 15 ns to 18 ns for 45 ns speed bin; changed minimum value of t_{SCE} from 25 ns to 30 ns for 35 ns speed bin and 40 ns to 35 ns for 45 ns speed bin; changed maximum value of t_{HZCE} parameter from 12 ns to 18 ns for 35 ns speed bin and 15 ns to 22 ns for 45 ns speed bin; changed minimum value of t_{SD} parameter from 15 ns to 18 ns for 35 ns speed bin and 20 ns to 22 ns for 45 ns speed bin). Updated Ordering Information (Updated part numbers (Changed to include Pb-free Packages)).
*B	414807	ZSD	12/16/2005	Changed status from Preliminary to Final. Changed the address of Cypress Semiconductor Corporation on page 1 from “3901 North First Street” to “198 Champion Court”. Updated Features (Removed 35 ns speed bin). Updated Pin Configurations (Changed ball C3 from DNU to NC; removed the Note “DNU pins have to be left floating or tied to V_{SS} to ensure proper application.” and its reference; added 32-pin SOIC pinout). Updated Electrical Characteristics (Removed “L” version of CY62148EV30; changed maximum value of I_{CC} parameter from 2 mA to 2.5 mA and typical value of I_{CC} parameter from 1.5 mA to 2 mA at f = 1 MHz; changed typical value of I_{CC} parameter from 12 mA to 15 mA at f = f_{max}; changed typical value of I_{SB1} and I_{SB2} parameters from 0.7 µA to 1 µA and maximum value of I_{SB1} and I_{SB2} parameters from 2.5 µA to 7 µA). Updated AC Test Loads and Waveforms (Changed the AC test load capacitance value from 50 pF to 30 pF). Updated Data Retention Characteristics (Changed maximum value of I_{CCDR} parameter from 2.5 µA to 7 µA; added typical value of I_{CCDR} parameter). Updated Switching Characteristics (Changed minimum value of t_{LZOE} parameter from 3 ns to 5 ns; changed minimum value of t_{LZCE} and t_{LZWE} parameters from 6 ns to 10 ns; changed maximum value of t_{HZCE} parameter from 22 ns to 18 ns; changed minimum value of t_{PWE} parameter from 30 ns to 35 ns; changed minimum value of t_{SD} from 22 ns to 25 ns). Updated Ordering Information: Updated part numbers. Removed “Package Name” column. Added “Package Diagram” column. Updated Package Diagrams: spec 51-85149 – Changed revision from *B to *C. Added spec 51-85081 *B. Updated to new template.
*C	464503	NXR	05/25/2006	Added Automotive Temperature Range related information in all instances across the document. Updated Ordering Information: Updated part numbers.

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Region	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*D	833080	VKN	03/09/2007	Updated Electrical Characteristics: Added details of V_{IL} parameter corresponding to Test Condition “SOIC package”. Added Note 10 and referred the same note in the maximum value of V_{IL} parameter corresponding to SOIC package.
*E	890962	VKN	03/30/2007	Removed Automotive Temperature Range related information in all instances across the document. Updated Features (Added Note 1 and referred the same note in 32-pin SOIC package). Updated Electrical Characteristics (Added Note 11 and referred the same note in I_{SB2} parameter). Updated Switching Characteristics (Added values for all parameters corresponding to 55 ns Industrial Temperature Range). Updated Ordering Information (Updated part numbers).
*F	987940	VKN	04/18/2007	Updated Electrical Characteristics: Changed maximum value of V_{OL} parameter from 0.4 V to 0.2 V corresponding to Industrial Temperature Range at I_{OL} = 0.1 mA. Changed maximum value of V_{IL} parameter from 0.6 V to 0.4 V corresponding to Industrial Temperature Range, SOIC package at V_{CC} = 2.2 V to 2.7 V. Updated Note 10. Updated Note 11 (made the note applicable for both I_{SB2} and I_{CCDR} parameters).
*G	2548575	NXR	08/05/2008	Added Automotive-A Temperature Range related information in all instances across the document. Updated Ordering Information: Updated part numbers. Updated to new template.
*H	2769239	VKN / AESA	09/25/2009	Updated Ordering Information: Updated part numbers.
*I	2944332	VKN	06/04/2010	Updated Truth Table: Added Note 34 and referred the same note in “$\overline{CE}$” column. Updated Package Diagrams: spec 51-85149 – Changed revision from *C to *D. spec 51-85095 – Changed revision from ** to *A. spec 51-85081 – Changed revision from *B to *C.
*J	3007403	AJU	08/13/2010	Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Updated to new template. Completing Sunset Review.
*K	3110202	PRAS	12/14/2010	Updated Logic Block Diagram. Updated Ordering Information: No change in part numbers. Updated Ordering Code Definitions.
*L	3302901	RAME	07/06/2011	Updated Functional Description: Updated description (Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.”). Updated Ordering Information: No change in part numbers. Updated Ordering Code Definitions. Updated Package Diagrams: spec 51-85095 – Changed revision from *A to *B.

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Region	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*L (cont.)	3302901	RAME	07/06/2011	Updated to new template. Completing Sunset Review.
*M	3363097	AJU	09/07/2011	Updated Data Retention Characteristics: Removed reference of Note 12 in I_{CCDR} parameter. Added Note 14 and referred the same note in I_{CCDR} parameter. Updated Package Diagrams: spec 51-85149 – Changed revision from *D to *E. spec 51-85081 – Changed revision from *C to *D.
*N	3546715	TAVA	03/09/2012	Updated Electrical Characteristics (Updated Note 10 (Removed the line “Refer to AN13470 for details”.)).
*O	3733339	JISH	09/04/2012	Minor text edits. Completing Sunset Review.
*P	4102967	VINI	08/23/2013	Updated Switching Characteristics: Added Note 17 and referred the same note in “Parameter” column. Updated Package Diagrams: spec 51-85081 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*Q	4307881	NILE	04/09/2014	Updated Switching Characteristics: Updated description of t_{PD} parameter (Replaced “$\overline{CE}$ HIGH to power-up” with “$\overline{CE}$ HIGH to power-down”).
*R	4576526	NILE	11/21/2014	Updated Functional Description: Added “For a complete list of related 1documentation, click here.” at the end. Updated Switching Characteristics: Added Note 23 and referred the same note in “Write Cycle”. Updated Switching Waveforms: Added Note 32 and referred the same note in Figure 7.
*S	4802206	NILE	06/18/2015	Updated Package Diagrams: spec 51-85149 – Changed revision from *E to *F. spec 51-85095 – Changed revision from *B to *D. Updated to new template.
*T	5234869	NILE	04/22/2016	Updated Ordering Information: Updated part numbers. Updated Ordering Code Definitions (Added Tape and Reel option). Updated Package Diagrams: spec 51-85149 – Changed revision from *F to *G. Updated to new template.
*U	5480386	VINI	10/18/2016	Updated Thermal Resistance: Replaced “two-layer” with “four-layer” in “Test Conditions” column. Updated values of Θ_{JA} parameter and Θ_{JC} parameter corresponding to all packages. Updated to new template. Completing Sunset Review.
*V	6045156	VINI	01/25/2018	Updated Ordering Information: Updated part numbers. Updated to new template.
*W	6531864	VINI	04/03/2019	Updated to new template.

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