

Features

- Very high speed: 45 ns
- Temperature ranges
 - Industrial: -40 °C to +85 °C
- Wide voltage range: 2.20 V to 3.60 V and 4.5 V to 5.5 V
- Ultra low standby power
 - Typical standby current: 3.5 μA
 - Maximum standby current: 8.7 μA
- Ultra low active power
 - Typical active current: 3.5 mA at f = 1 MHz
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in a 44-pin TSOP II and 48-ball VFBGA Packages

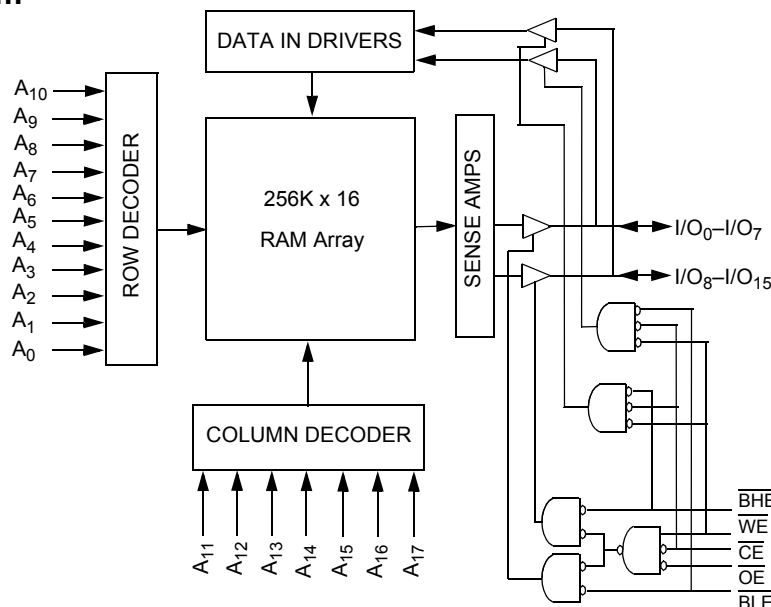
Functional Description

The CY62146GN is a high performance CMOS static RAM organized as 256K words by 16 bits. This device features an advanced circuit design designed to provide an ultra low active current. Ultra low active current is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption by 80 percent when addresses are not toggling. The device can also be put into standby mode reducing power consumption by more than 99 percent when deselected (CE HIGH). The input and output pins (I/O₀ through I/O₁₅) are placed in a high impedance state when the device is deselected (CE HIGH), outputs are disabled (OE HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or a write operation is in progress (CE LOW and WE LOW).

To write to the device, take Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇) is written into the location specified on the address pins (A₀ through A₁₇). If Byte High Enable (BHE) is LOW, then data from the I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₇).

To read from the device, take Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appears on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See the Truth Table on page 11 for a complete description of read and write modes.

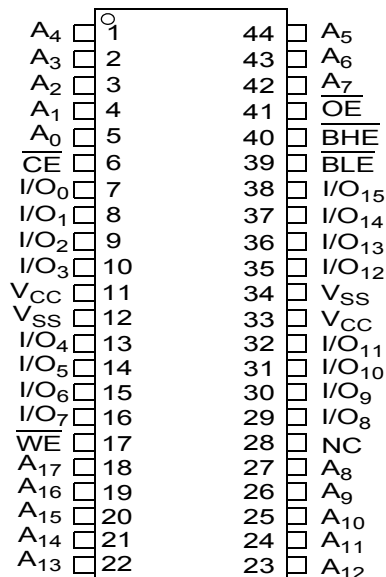
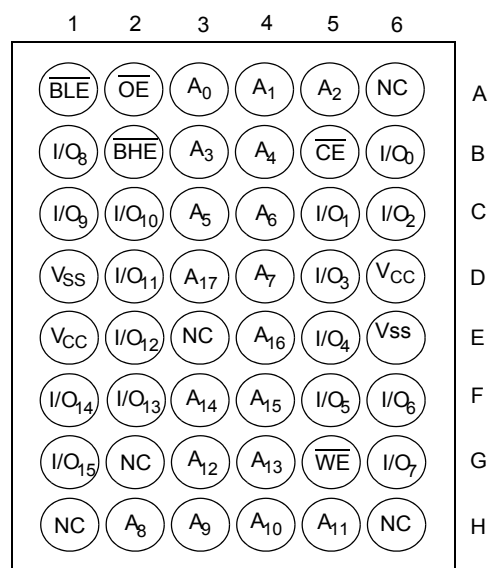
Logic Block Diagram



Contents

| | | | |
|---|-----------|--|-----------|
| Pin Configurations | 3 | Ordering Information | 12 |
| Product Portfolio | 3 | Ordering Code Definitions | 12 |
| Maximum Ratings | 4 | Package Diagrams | 13 |
| Operating Range | 4 | Acronyms | 14 |
| Electrical Characteristics | 4 | Document Conventions | 14 |
| Capacitance | 5 | Units of Measure | 14 |
| Thermal Resistance | 5 | Document History Page | 15 |
| AC Test Loads and Waveforms | 5 | Sales, Solutions, and Legal Information | 16 |
| Data Retention Characteristics | 6 | Worldwide Sales and Design Support | 16 |
| Data Retention Waveform | 6 | Products | 16 |
| Switching Characteristics | 7 | PSoC [®] Solutions | 16 |
| Switching Waveforms | 8 | Cypress Developer Community | 16 |
| Truth Table | 11 | Technical Support | 16 |

Pin Configurations

Figure 1. 44-pin TSOP II Pinout ^[1]

Figure 2. 48-ball VFBGA Pinout ^[1]


Product Portfolio

| Product | Range | V _{CC} Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|-------------|------------|---------------------------|--------------------|----------------------|------------|--------------------------------|-----|--------------------|-----|-------------------------------|-----|
| | | | | | | Operating I _{CC} (mA) | | | | Standby I _{SB2} (μA) | |
| | | f = 1 MHz | | f = f _{max} | | | | | | | |
| | | Min | Typ ^[2] | Max | | Typ ^[2] | Max | Typ ^[2] | Max | Typ ^[2] | Max |
| CY62146GN30 | Industrial | 2.2 | 3.0 | 3.6 | 45 | 3.5 | 6 | 15 | 20 | 3.5 | 8.7 |
| CY62146GN | | 4.5 | 5.0 | 5.5 | | | | | | | |

Notes

1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to + 150 °C

Ambient temperature
with power applied -55 °C to + 125 °C

Supply voltage
to ground potential -0.3 V to + V_{CC} + 0.5 V

DC voltage applied to outputs
in High-Z state^[3, 4] -0.3 V to + V_{CC} + 0.5 V

DC input voltage^[3, 4] -0.3 V to + V_{CC} + 0.5 V

Output current into outputs (LOW) 20 mA

Static Discharge Voltage
(per MIL-STD-883, Method 3015) >2001 V

Latch-up Current >200 mA

Operating Range

| Device | Range | Ambient Temperature | V _{CC} ^[5] |
|-------------|------------|---------------------|-----------------------------------|
| CY62146GN30 | Industrial | -40 °C to +85 °C | 2.2 V to 3.6 V, 4.5 V to 5.5 V |

Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | 45 ns | | | Unit | |
|---------------------------------|---|--|---|--------------------------------------|-----|-----------------------|----|
| | | | Min | Typ ^[6] | Max | | |
| V _{OH} | Output high voltage | 2.2 V to 2.7 V | V _{CC} = Min, I _{OH} = -0.1 mA | 2 | - | - | V |
| | | 2.7 V to 3.6 V | V _{CC} = Min, I _{OH} = -1.0 mA | 2.4 | - | - | |
| | | 4.5 V to 5.5 V | V _{CC} = Min, I _{OH} = -1.0 mA | 2.4 | - | - | |
| | | 4.5 V to 5.5 V | V _{CC} = Min, I _{OH} = -0.1 mA | V _{CC} - 0.5 ^[7] | - | - | |
| V _{OL} | Output low voltage | 2.2 V to 2.7 V | V _{CC} = Min, I _{OL} = 0.1 mA | - | - | 0.4 | V |
| | | 2.7 V to 3.6 V | V _{CC} = Min, I _{OL} = 2.1 mA | - | - | 0.4 | |
| | | 4.5 V to 5.5 V | V _{CC} = Min, I _{OL} = 2.1 mA | - | - | 0.4 | |
| V _{IH} ^[4] | Input high voltage | 2.2 V to 2.7 V | - | 1.8 | - | V _{CC} + 0.3 | V |
| | | 2.7 V to 3.6 V | - | 2.0 | - | V _{CC} + 0.3 | |
| | | 4.5 V to 5.5 V | - | 2.2 | - | V _{CC} + 0.5 | |
| V _{IL} ^[3] | Input LOW Voltage | 2.2 V to 2.7 V | V _{CC} = 2.2 V to 2.7 V | -0.3 | - | 0.6 | V |
| | | 2.7 V to 3.6 V | V _{CC} = 2.7 V to 3.6 V | -0.3 | - | 0.8 | |
| | | 4.5 V to 5.5 V | - | -0.5 | - | 0.8 | |
| I _{IX} | Input leakage current | GND ≤ V _I ≤ V _{CC} | -1 | - | +1 | mA | |
| I _{OZ} | Output leakage current | GND ≤ V _O ≤ V _{CC} , Output disabled | -1 | - | +1 | mA | |
| I _{CC} | V _{CC} operating supply current | f = f _{max} = 1/t _{RC} | V _{CC} = V _{CC(max)} , I _{OUT} = 0 mA | - | 15 | 20 | mA |
| | | f = 1 MHz | CMOS levels | - | 3.5 | 6 | |
| I _{SB1} | Automatic CE power down current – CMOS inputs | $\overline{CE} > V_{CC} - 0.2 V$, $V_{IN} > V_{CC} - 0.2 V$ or $V_{IN} < 0.2 V$, $f = f_{max}$ (Address and data only), $f = 0$ (\overline{OE} , \overline{BHE} , \overline{BLE} and \overline{WE}), $V_{CC} = 3.60 V$ | - | 3.5 | 8.7 | μA | |
| I _{SB2} ^[8] | Automatic CE power down current – CMOS inputs | $\overline{CE} \geq V_{CC} - 0.2 V$, $V_{IN} \geq V_{CC} - 0.2 V$ or $V_{IN} \leq 0.2 V$, $f = 0$, $V_{CC} = 3.60 V$ | - | 3.5 | 8.7 | μA | |

Notes

3. V_{IL(min)} = -2.0 V for pulse durations less than 20 ns.

4. V_{IH(max)} = V_{CC} + 2.0 V for pulse durations less than 20 ns.

5. Full-device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} > 100 μs or stable at V_{CC(min)} > 100 μs.

6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

7. This parameter is guaranteed by design and not tested.

8. Chip enable (CE) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

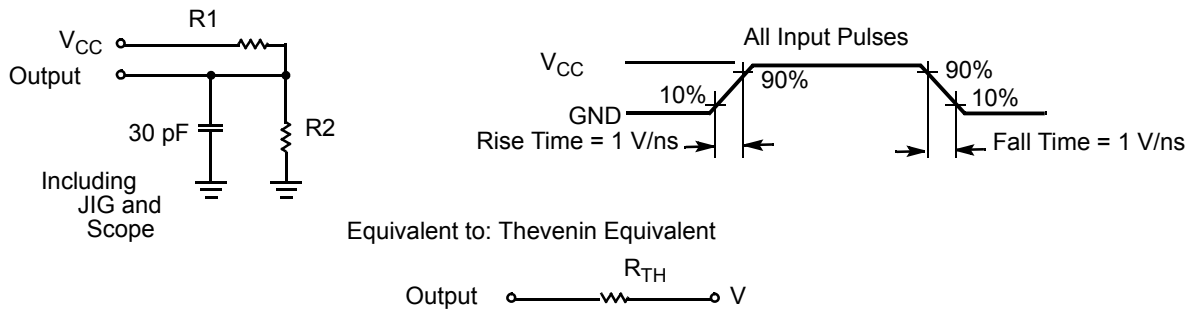
| Parameter ^[9] | Description | Test Conditions | Max | Unit |
|--------------------------|--------------------|---|-----|------|
| C_{IN} | Input capacitance | $T_A = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC(\text{typ})}$ | 10 | pF |
| C_{OUT} | Output capacitance | | 10 | pF |

Thermal Resistance

| Parameter ^[9] | Description | Test Conditions | 48-ball VFBGA | TSOP II | Unit |
|--------------------------|--|--|---------------|---------|--------------------|
| Θ_{JA} | Thermal resistance (junction to ambient) | Still air, soldered on a 3×4.5 inch, four-layer printed circuit board | 31.35 | 68.85 | $^\circ\text{C/W}$ |
| Θ_{JC} | Thermal resistance (junction to case) | | 14.74 | 15.97 | $^\circ\text{C/W}$ |

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms^[10]



| Parameters | 2.50 V | 3.0 V | Unit |
|------------|--------|-------|----------|
| R1 | 16667 | 1103 | Ω |
| R2 | 15385 | 1554 | Ω |
| R_{TH} | 8000 | 645 | Ω |
| V_{TH} | 1.20 | 1.75 | V |

Note

- Tested initially and after any design or process changes that may affect these parameters.
- Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$.

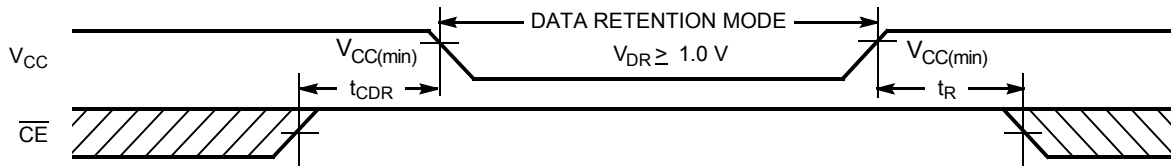
Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------------------|--------------------------------------|---|-----|-----|-----|---------------|
| V_{DR} | V_{CC} for data retention | | 1.0 | – | – | V |
| $I_{CCDR}^{[11, 12]}$ | Data retention current | $V_{CC} = 1.2\text{ V}$, $\overline{CE} \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ | – | – | 13 | μA |
| $t_{CDR}^{[13]}$ | Chip deselect to data retention time | – | 0 | – | – | ns |
| $t_R^{[14]}$ | Operation recovery time | – | 45 | – | – | ns |

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes

11. Chip enable (CE) needs to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
12. I_{CCDR} is guaranteed only after device is first powered up to $V_{CC(min)}$ and then brought down to V_{DR} .
13. Tested initially and after any design or process changes that may affect these parameters.
14. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ > 100 μs or stable at $V_{CC(min)}$ > 100 μs .

Switching Characteristics

Over the Operating Range

| Parameter ^[15, 16] | Description | 45 ns | | Unit |
|---------------------------------------|--|-------|-----|------|
| | | Min | Max | |
| Read Cycle | | | | |
| t_{RC} | Read cycle time | 45 | – | ns |
| t_{AA} | Address to data valid | – | 45 | ns |
| t_{OHA} | Data hold from address change | 10 | – | ns |
| t_{ACE} | \overline{CE} LOW to data valid | – | 45 | ns |
| t_{DOE} | \overline{OE} LOW to data valid | – | 22 | ns |
| t_{LZOE} | \overline{OE} LOW to Low-Z ^[17] | 5 | – | ns |
| t_{HZOE} | \overline{OE} HIGH to High-Z ^[17, 18] | – | 18 | ns |
| t_{LZCE} | \overline{CE} LOW to Low-Z ^[17] | 10 | – | ns |
| t_{HZCE} | \overline{CE} HIGH to High-Z ^[17, 18] | – | 18 | ns |
| t_{PU} | \overline{CE} LOW to power up | 0 | – | ns |
| t_{PD} | \overline{CE} HIGH to power down | – | 45 | ns |
| t_{DBE} | \overline{BLE} / \overline{BHE} LOW to data valid | – | 22 | ns |
| t_{LZBE} | \overline{BLE} / \overline{BHE} LOW to Low-Z ^[17] | 5 | – | ns |
| t_{HZBE} | \overline{BLE} / \overline{BHE} HIGH to High-Z ^[17, 18] | – | 18 | ns |
| Write Cycle^[19, 20] | | | | |
| t_{WC} | Write cycle time | 45 | – | ns |
| t_{SCE} | \overline{CE} LOW to write end | 35 | – | ns |
| t_{AW} | Address setup to write end | 35 | – | ns |
| t_{HA} | Address hold from write end | 0 | – | ns |
| t_{SA} | Address setup to write start | 0 | – | ns |
| t_{PWE} | \overline{WE} pulse width | 35 | – | ns |
| t_{BW} | \overline{BLE} / \overline{BHE} LOW to write end | 35 | – | ns |
| t_{SD} | Data setup to write end | 25 | – | ns |
| t_{HD} | Data hold from write end | 0 | – | ns |
| t_{HZWE} | \overline{WE} LOW to High-Z ^[17, 18] | – | 18 | ns |
| t_{LZWE} | \overline{WE} HIGH to Low-Z ^[17] | 10 | – | ns |

Notes

15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the [Figure 3 on page 5](#).
16. These parameters are guaranteed by design.
17. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
18. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
19. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
20. The minimum write pulse width for Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) should be sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 5. Read Cycle 1 (Address Transition Controlled)^[21, 22]

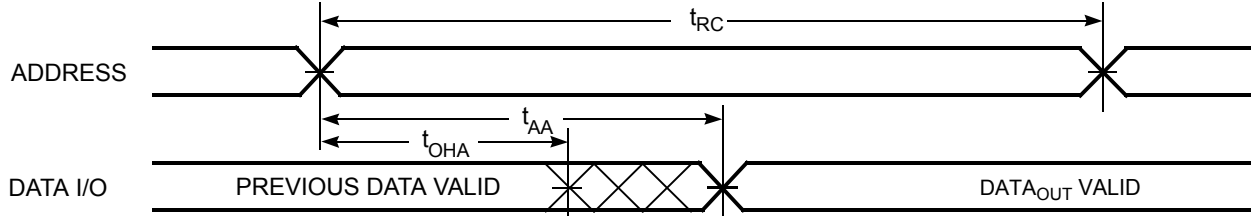
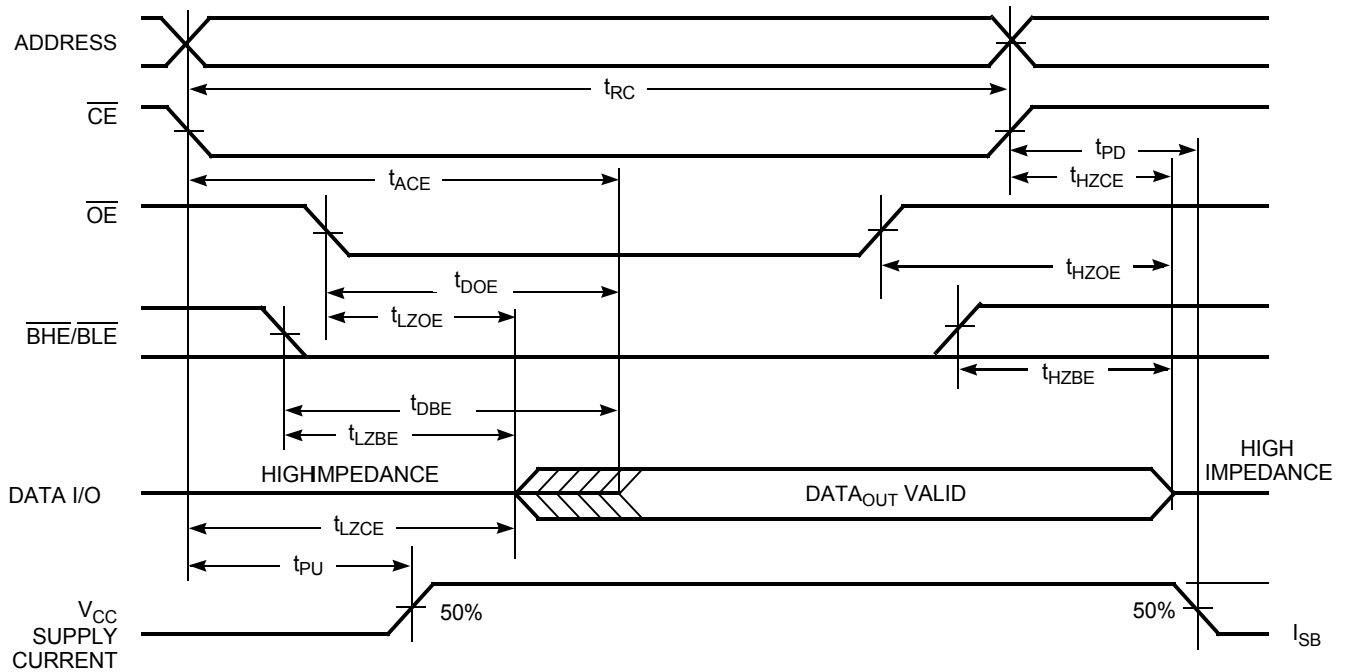


Figure 6. Read Cycle No. 2 (\overline{OE} Controlled)^[22, 23]



Notes

- 21. The device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$.
- 22. \overline{WE} is HIGH for read cycle.
- 23. Address valid before or similar to \overline{CE} .

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 (\overline{WE} Controlled)^[24, 25, 26]

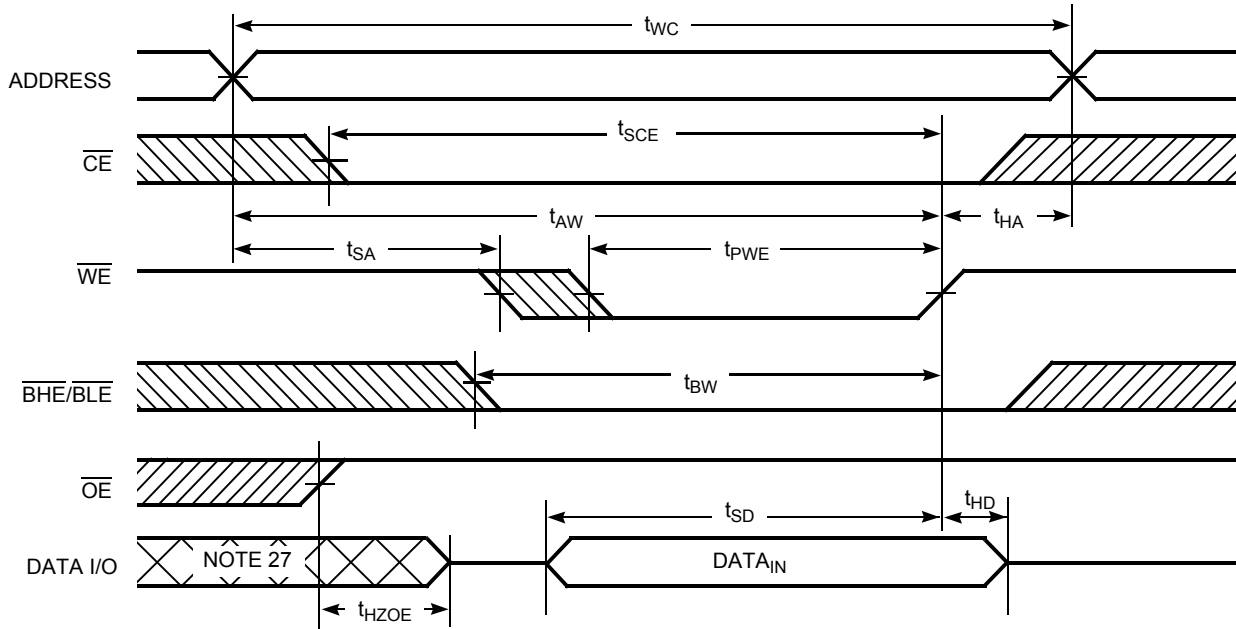
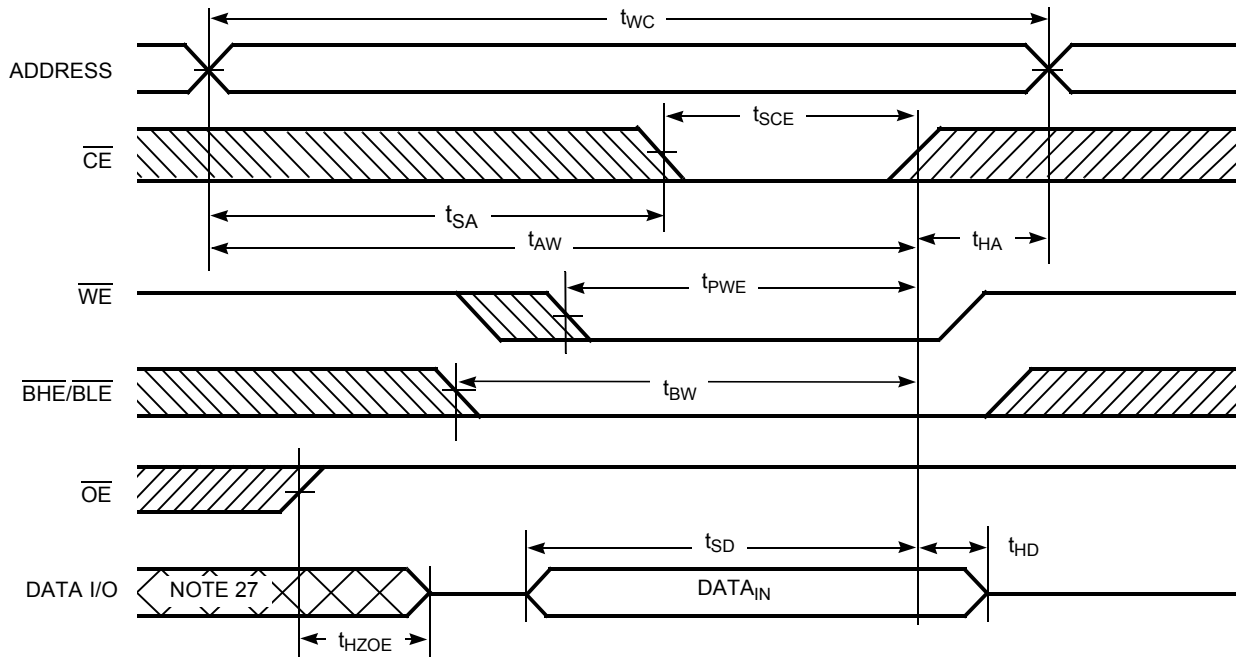


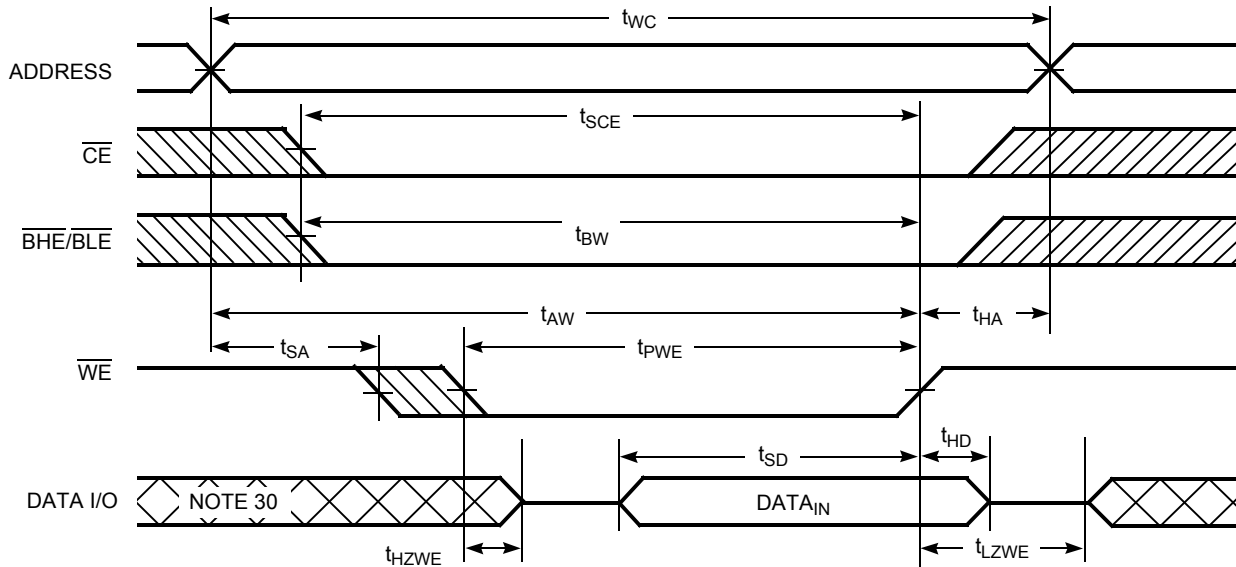
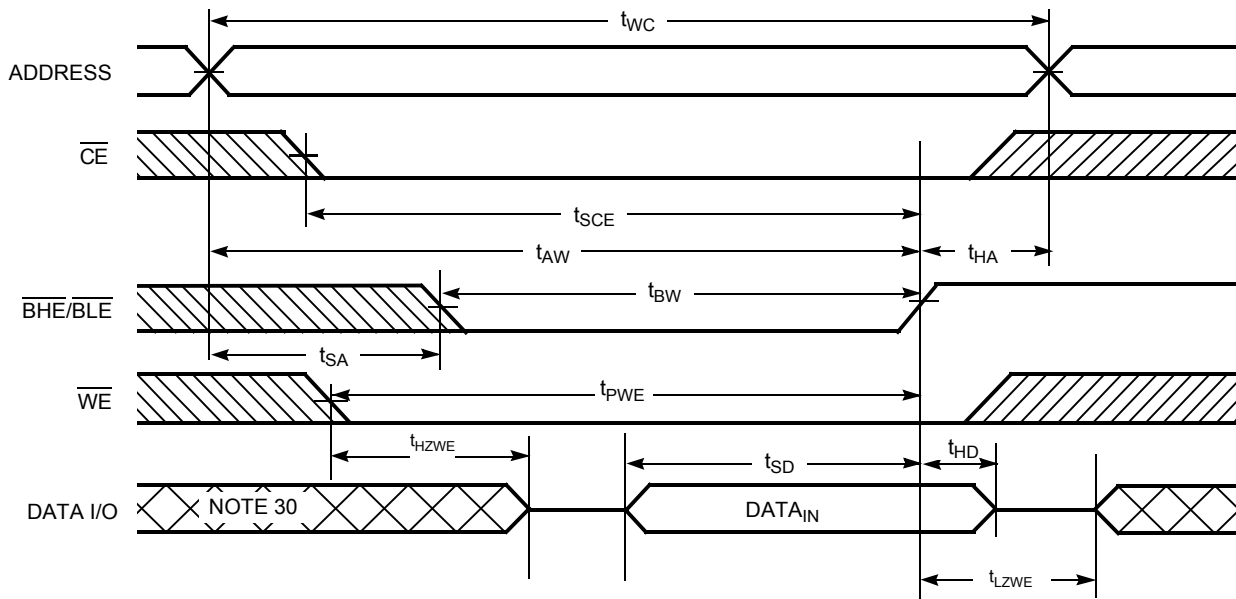
Figure 8. Write Cycle No. 2 (\overline{CE} Controlled)^[24, 25, 26]



Notes

- 24. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
- 25. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 26. If \overline{CE} goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 27. During this period, the I/Os are in output state and input signals must not be applied.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[28, 29]

Figure 10. Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ Controlled, \overline{OE} LOW)^[28]

Notes

28. If \overline{CE} goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.

29. The minimum write pulse width for Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) should be sum of t_{HZWE} and t_{SD} .

30. During this period, the I/Os are in output state and input signals must not be applied.

Truth Table

| CE ^[31] | WE | OE | BHE | BLE | Inputs/Outputs | Mode | Power |
|--------------------|----|----|-----|-----|--|---------------------|----------------------------|
| H | X | X | X | X | High-Z | Deselect/power-down | Standby (I _{SB}) |
| L | X | X | H | H | High-Z | Output disabled | Active (I _{CC}) |
| L | H | L | L | L | Data out (I/O ₀ –I/O ₁₅) | Read | Active (I _{CC}) |
| L | H | L | H | L | Data out (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High-Z | Read | Active (I _{CC}) |
| L | H | L | L | H | Data out (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High-Z | Read | Active (I _{CC}) |
| L | H | H | X | X | High-Z | Output disabled | Active (I _{CC}) |
| L | L | X | L | L | Data in (I/O ₀ –I/O ₁₅) | Write | Active (I _{CC}) |
| L | L | X | H | L | Data in (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High-Z | Write | Active (I _{CC}) |
| L | L | X | L | H | Data in (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High-Z | Write | Active (I _{CC}) |

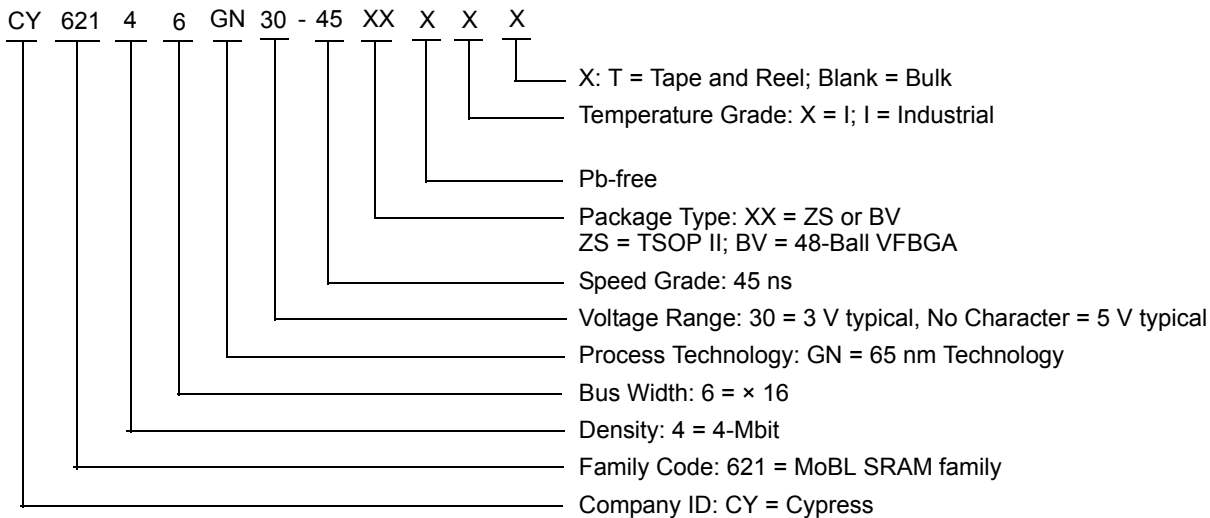
Note

31. Chip enable must be at CMOS levels (not floating). Intermediate voltage levels on this pin is not permitted.

Ordering Information

| Speed (ns) | Voltage Range (V) | Ordering Code | Package Diagram | Package Type (Pb-free) | Operating Range |
|------------|-------------------|---------------------|-----------------|---|-----------------|
| 45 | 2.2 V–3.6 V | CY62146GN30-45ZSXI | 51-85087 | 44-pin TSOP II | Industrial |
| | | CY62146GN30-45ZSXIT | 51-85087 | 44-pin TSOP II, Tape & Reel | |
| | | CY62146GN30-45BVXI | 51-85150 | 48-ball VFBGA (6 × 8 × 1 mm) | |
| | | CY62146GN30-45BVXIT | 51-85150 | 48-ball VFBGA (6 × 8 × 1 mm), Tape & Reel | |
| | 4.5 V–5.5 V | CY62146GN-45ZSXI | 51-85087 | 44-pin TSOP II | |
| | | CY62146GN-45ZSXIT | 51-85087 | 44-pin TSOP II, Tape & Reel | |

Ordering Code Definitions



Package Diagrams

Figure 11. 44-pin TSOP Z44-II Package Outline, 51-85087

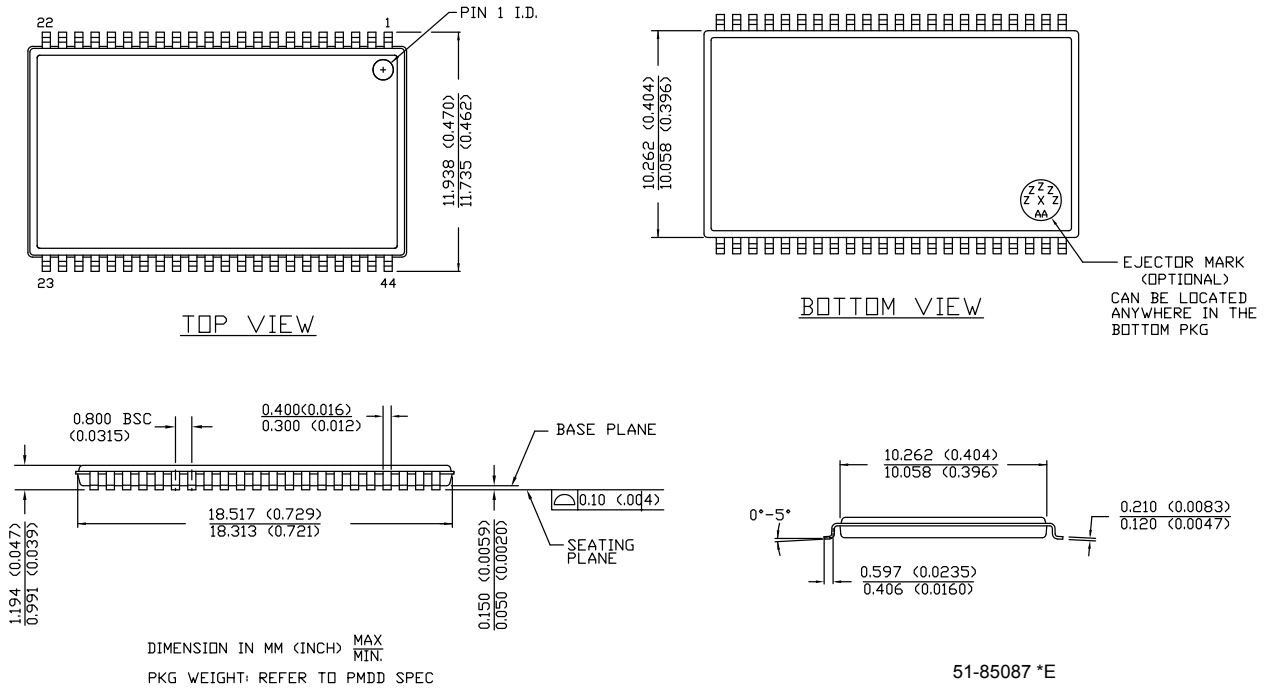
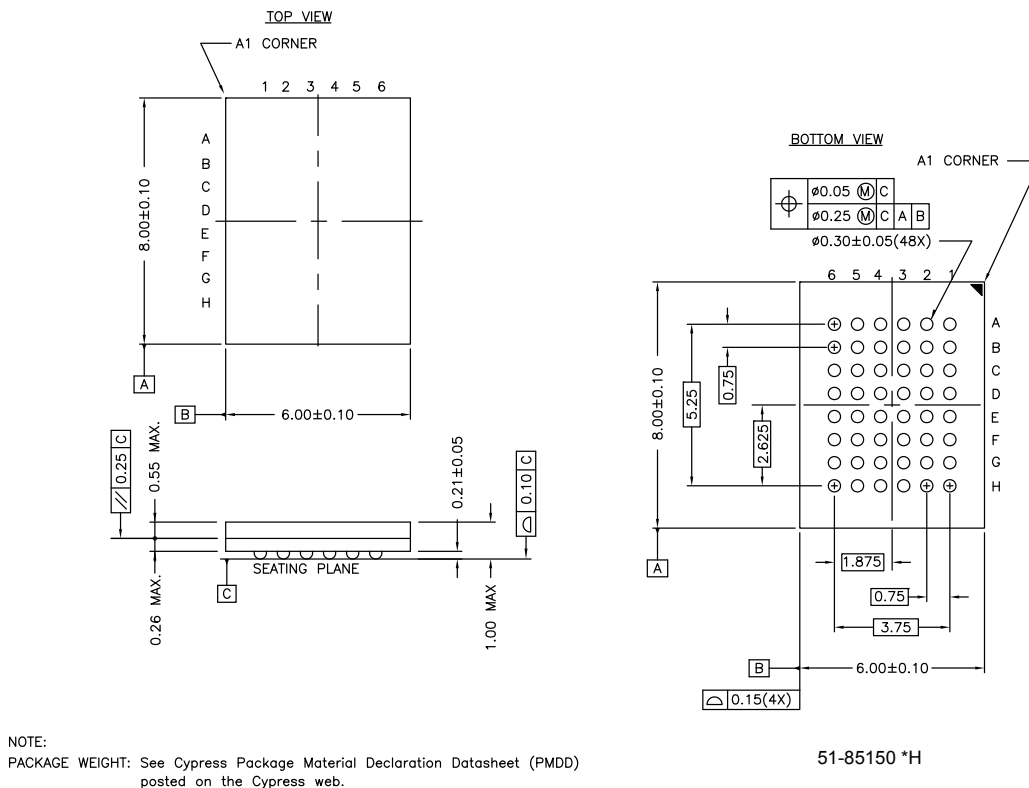


Figure 12. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



Acronyms

Table 1. Acronyms Used in this Document

| Acronym | Description |
|-------------------------|---|
| $\overline{\text{BHE}}$ | byte high enable |
| $\overline{\text{BLE}}$ | byte low enable |
| CMOS | complementary metal oxide semiconductor |
| $\overline{\text{CE}}$ | chip enable |
| I/O | input/output |
| $\overline{\text{OE}}$ | output enable |
| SRAM | static random access memory |
| TSOP | thin small outline package |
| VFBGA | very fine-pitch ball grid array |
| $\overline{\text{WE}}$ | write enable |

Document Conventions

Units of Measure

Table 2. Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | Degrees Celsius |
| MHz | megahertz |
| μA | microamperes |
| mA | milliamperes |
| ns | nanoseconds |
| Ω | ohms |
| pF | picofarads |
| V | volts |
| W | watts |

Document History Page

| Document Title: CY62146GN MoBL [®] , 4-Mbit (256K × 16) Static RAM Document Number: 001-95417 | | | | |
|---|---------|-----------------|-----------------|---|
| Rev. | ECN No. | Orig. of Change | Submission Date | Description of Change |
| ** | 5048897 | NILE | 12/14/2015 | New data sheet. |
| *A | 5072822 | NILE | 01/05/2016 | Added "4.5 V to 5.5 V" voltage range related information in all instances across the document. Updated Ordering Information : Updated part numbers. |
| *B | 5092237 | NILE | 01/21/2016 | Added 48-ball VFBGA package related information in all instances across the document. Updated Ordering Information : Updated part numbers. Updated Package Diagrams : Added spec 51-85150 *H (Figure 12). |
| *C | 5142534 | NILE | 02/18/2016 | Updated Ordering Code Definitions under Ordering Information (Replaced "GN = 90 nm" with "GN = 65 nm Technology"). Updated to new template. |
| *D | 5555156 | NILE | 12/15/2016 | Updated Ordering Information : Updated part numbers. Updated Electrical Characteristics : Enhance V_{IH} for 2.2V - 2.7V operating range from 2.0V to 1.8V. Enhance V_{OH} for 2.7V - 3.6V operating range from 2.2V to 2.4V. Updated Notes 3 and 4 . Updated Thermal Resistance . Updated Sales Support, Copyright and Disclaimer. |
| *E | 5995870 | AESATMP9 | 12/15/2017 | Updated logo and copyright. |

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

| | |
|---|--|
| Arm [®] Cortex [®] Microcontrollers | cypress.com/arm |
| Automotive | cypress.com/automotive |
| Clocks & Buffers | cypress.com/clocks |
| Interface | cypress.com/interface |
| Internet of Things | cypress.com/iot |
| Memory | cypress.com/memory |
| Microcontrollers | cypress.com/mcu |
| PSoC | cypress.com/psoc |
| Power Management ICs | cypress.com/pmic |
| Touch Sensing | cypress.com/touch |
| USB Controllers | cypress.com/usb |
| Wireless Connectivity | cypress.com/wireless |

PSoC[®] Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support



© Cypress Semiconductor Corporation, 2015-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View CY62146GN30-45ZSXI on WIN SOURCE](#)
-  [Cypress Semiconductor Corp Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management