



**THE DATASHEET OF  
CS2082EDWR20**



# CS2082

## Dual Airbag Deployment ASIC

The CS2082 controls and monitors two airbag firing loops. The independent firing loops are low- and high-side controlled. Device communication is through a Serial Peripheral Interface (SPI) port, and includes frame error detection circuitry for data reliability.

Diagnostics include squib resistance measurement and continuous monitoring for shorts to ground, shorts to battery, and for open loops. The high- and low-side drivers can be individually activated to guarantee function and to identify shorts between firing loops. Additional features include power on reset, overtemperature protection, a charge pump, high-side safing sensor closure detection, an analog multiplexer, a monitor to ensure battery potential, and a programmable monitor to ensure firing potential.

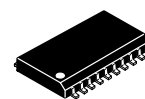
### Features

- Serial Input Bus
- Two Squib Outputs
- Low- and High-Side Control
- Monitors
  - Squib Resistance
  - Short to Ground or Battery
  - Battery Potential
  - Firing Potential
- Safing Sensor Detection
- 60 V Peak Transient Voltage



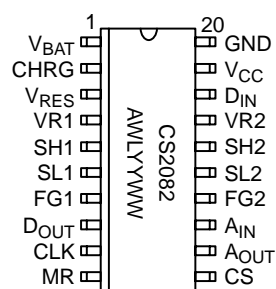
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SO-20L  
DW SUFFIX  
CASE 751D

### PIN CONNECTIONS AND MARKING DIAGRAM



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
CS2082EDW20	SO-20L	37 Units/Rail
CS2082EDWR20	SO-20L	1000 Tape & Reel

# CS2082

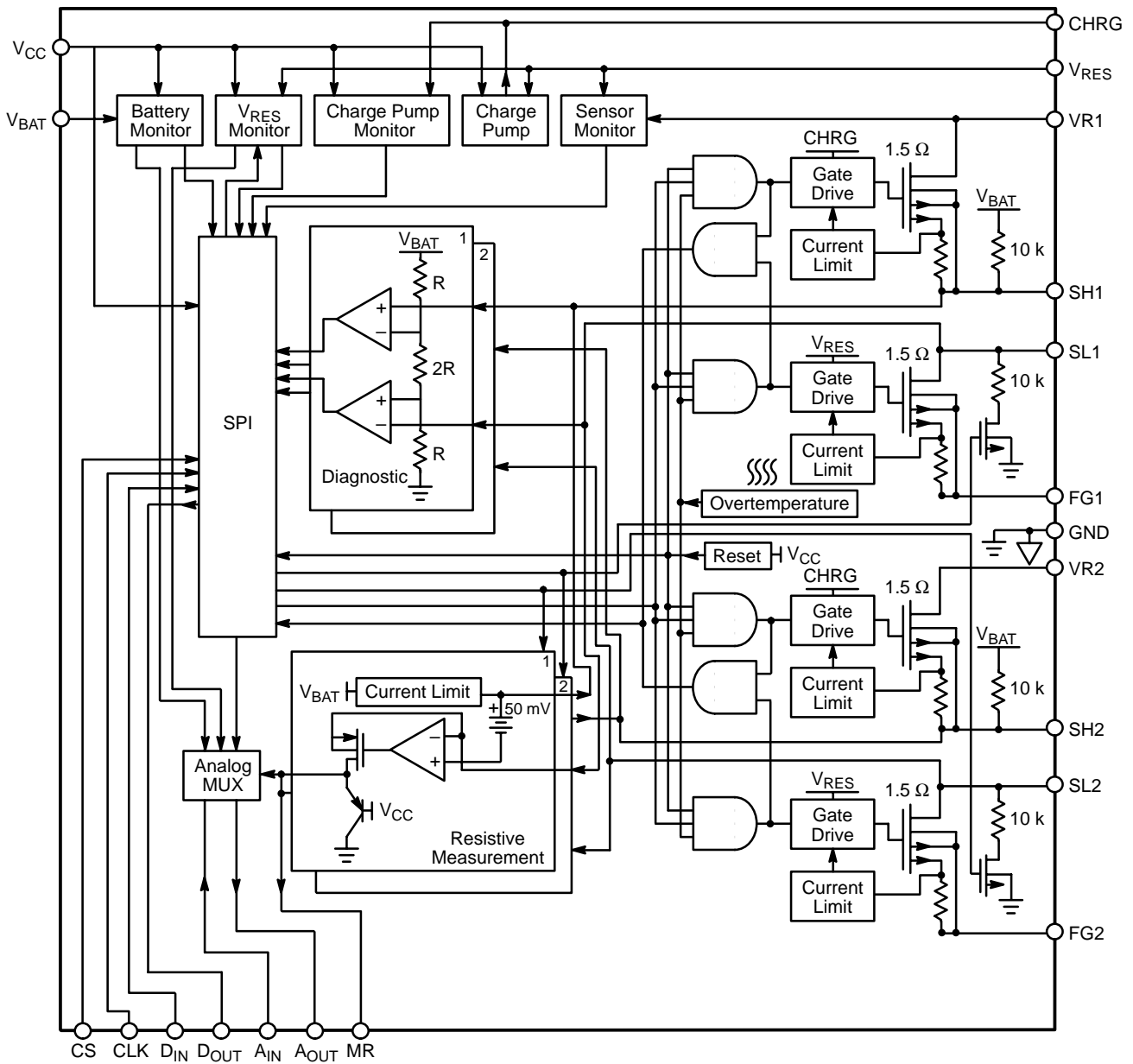


Figure 1. Block Diagram

## MAXIMUM RATINGS\*

Rating	Value	Unit
Storage Temperature	-40 to 150	°C
V <sub>BAT</sub>	-0.3 to 24	V
V <sub>RES</sub>	-0.3 to 30	V
V <sub>CC</sub>	-0.3 to 6.0	V
ESD Susceptibility (Human Body Model)	500	V
Power Dissipation (Non-Firing)	0.15	W
Power Dissipation (Both Firing Loops With Squibs Shorted)	140	W
Power Dissipation (Squib Resistance Measurement)	1.6	W
Peak Transient Voltage (46 V Load Dump @ 14 V V <sub>BAT</sub> )	60	V
Lead Temperature Soldering:	Reflow: (SMD styles only) (Note 1)	230 peak

1. 60 second maximum above 183°C.

\*The maximum package power dissipation must be observed.

**ELECTRICAL CHARACTERISTICS** (4.75 V < V<sub>CC</sub> < 5.25 V, 8.0 V < V<sub>RES</sub> < 30 V, 9.0 V < V<sub>BAT</sub> < 18 V, -40°C < T<sub>A</sub> < +85°C; unless otherwise stated.)

Parameter	Test Conditions	Min	Typ	Max	Unit
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**Supply Requirements**

V <sub>CC</sub> Quiescent Current	V <sub>CC</sub> = 5.25 V	-	2.0	4.0	mA
V <sub>BAT</sub> Quiescent Current	V <sub>BAT</sub> = 18 V	-	2.5	5.0	mA
V <sub>BAT</sub> Measurement Current	V <sub>BAT</sub> = 18 V, R <sub>SQUIB</sub> = 1.0 Ω	-	-	80	mA
V <sub>RES</sub> Quiescent Current	V <sub>RES</sub> = 30 V	-	-	1.0	mA
V <sub>RES</sub> Firing Current	V <sub>RES</sub> = 30 V	-	-	3.0	mA

**Power on Reset**

V<sub>BAT</sub> = 9.0 V, V<sub>RES</sub> = 10 V

Power Reset Active Voltage	V <sub>CC</sub> Falling	3.50	4.00	4.25	V
Power Reset Off Voltage	V <sub>CC</sub> Rising	3.65	4.20	4.50	V
Hysteresis	-	50	-	-	mV

**Low Side Driver**

V<sub>RES</sub> = 8.0 V = V<sub>RX</sub>, V<sub>CC</sub> = 5.0 V, V<sub>BAT</sub> = 8.0 V

Saturation Voltage	I = 1.2 A	-	-	1.8	V
Current Limit (I <sub>LIMIT</sub> )	V <sub>SLX</sub> - V <sub>FGX</sub> = 5.0 V	1.2	1.6	2.0	A
Turn-on Delay Time	From CS falling Edge, I <sub>D</sub> = 0.9 × I <sub>LIMIT(MIN)</sub>	-	-	75	μs
Turn-off Delay Time	From CS falling Edge, I <sub>D</sub> = 0.1 × I <sub>LIMIT(MIN)</sub>	-	-	25	μs

**High Side Driver**

V<sub>RES</sub> = 8.0 V = V<sub>RX</sub>, V<sub>CC</sub> = 5.0 V, V<sub>BAT</sub> = 8.0 V

Saturation Voltage	I = 1.2 A	-	-	1.8	V
Current Limit (I <sub>LIMIT</sub> )	V <sub>RX</sub> - V <sub>SHX</sub> = 5.0 V	1.2	2.0	2.5	A
V <sub>R1</sub> Quiescent Current Drivers off	V <sub>RX</sub> = V <sub>RES</sub> = 30 V	-	-	1.0	mA
V <sub>R2</sub> Quiescent Current Drivers off	V <sub>RX</sub> = V <sub>RES</sub> = 30 V	-	-	100	μA
Turn-on Delay Time	From CS falling Edge, I <sub>D</sub> = 0.9 × I <sub>LIMIT(MIN)</sub>	-	-	100	μs
Turn-off Delay Time	From CS falling Edge, I <sub>D</sub> = 0.1 × I <sub>LIMIT(MIN)</sub>	-	-	25	μs

**Thermal Shut Down**

Thermal Shutdown Temp	Guaranteed by Design	150	180	210	°C
Thermal Hysteresis	Guaranteed by Design	30	40	60	°C

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**ELECTRICAL CHARACTERISTICS (continued)** (4.75 V < V<sub>CC</sub> < 5.25 V, 8.0 V < V<sub>RES</sub> < 30 V, 9.0 V < V<sub>BAT</sub> < 18 V, -40°C < T<sub>A</sub> < +85°C; unless otherwise stated.)

Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Thermal Shut Down</b>					
Time to Thermal Shutdown	R <sub>SQUIB</sub> = 0, V <sub>RX</sub> = 30 V, T = 85°C, Guaranteed by Design	7.0	–	–	ms
<b>Squib Resistive Measurements</b> V <sub>CC</sub> = 5.0 V, R <sub>MR</sub> = 49.9 Ω, V <sub>RES</sub> = 30 V					
Squib Differential Voltage	V <sub>DIFF</sub> = SHx – SLx, R <sub>SQUIB</sub> = 1.0 Ω to 10 Ω	46	53	60	mV
Difference Between SHx & MR current – SHx reference	I <sub>SQUIB</sub> = 50 mA	–1.0	–	1.0	%
SHx Current Limit	R <sub>SQUIB</sub> = 0	67	100	133	mA
SLx Current Limit	R <sub>MR</sub> = 0	77	115	153	mA
MR Voltage Clamp	–	V <sub>CC</sub> – 0.3	–	V <sub>CC</sub> + 0.3	V
Turn On Delay Time excluding external Capacitors	–	–	–	100	μs
Turn off Delay Time	–	–	–	50	μs
<b>Short Measurements</b> V <sub>CC</sub> = 5.0 V, V <sub>RES</sub> ≥ V <sub>BAT</sub> , V <sub>RX</sub> ≥ V <sub>BAT</sub>					
SHx pull-up resistance to V <sub>BAT</sub> SLx pull-down resistance	V <sub>BAT</sub> = 18 V	4.0 4.0	10 10	17 17	kΩ kΩ
Pull-up resistor matching	–	–5.0	–	5.0	%
Pull-down resistor matching	–	–5.0	–	5.0	%
Short to V <sub>BAT</sub> Trip	SHx short to Battery SLx bit set to 1	0.73 × V <sub>BAT</sub>	0.75 × V <sub>BAT</sub>	0.77 × V <sub>BAT</sub>	V
Short to GND Trip	SHx short to GND SGx bit set to 1	0.23 × V <sub>BAT</sub>	0.25 × V <sub>BAT</sub>	0.27 × V <sub>BAT</sub>	V
<b>V<sub>BAT</sub> Monitoring</b> V <sub>CC</sub> = 5.0 V, External V <sub>BAT</sub> Diode not included, V <sub>RES</sub> = 30 V					
V <sub>BAT</sub> Low Trip	BL bit set to 1 when below trip	7.5	8.5	9.5	V
V <sub>BAT</sub> High Trip	BL bit set to 0 when above trip	8.0	9.0	10	V
<b>V<sub>RES</sub> Monitoring</b> V <sub>CC</sub> = 5.0 V, V <sub>BAT</sub> = 18 V					
V <sub>RES</sub> Low Trip	\$6d AUX register b0 = 0	15.7	17.5	19.3	V
V <sub>RES</sub> High Trip	\$6d AUX register b0 = 0	16.5	18.5	20.5	V
V <sub>RES</sub> Low Trip	\$6d AUX register b0 = 1	21.5	24.0	26.5	V
V <sub>RES</sub> High Trip	\$6d AUX register b0 = 1	22.5	25	27.5	V
<b>Safing Sensor Monitor</b>					
External Resistance Trip Range	SSC bit set when resistance is less	30	400	600	Ω
<b>Charge Pump and Monitor</b> V <sub>CC</sub> = 5.0 V, V <sub>BAT</sub> = 10 V					
Oscillator Frequency	V <sub>RES</sub> = 10 V	200	–	800	kHz
Charge Pump charge time	C <sub>CHG</sub> = 0.1 μF, V <sub>RES</sub> = 8.0 V, Chrg from 8.0 V to 14 V	–	–	20	ms
Charge Pump Low Voltage	CL bit set to 1 when below trip	14.5	16.0	17.5	V
Charge Pump High Voltage	CL bit set to 0 when above trip	15.0	17.5	18.0	V
<b>Analog MUX</b> V <sub>CC</sub> = 5.0 V					
A <sub>OUT</sub> Output Range	–	0.1	–	V <sub>CC</sub> – 0.1	V
A <sub>IN</sub> Input Range	–	0	–	V <sub>CC</sub>	V

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**ELECTRICAL CHARACTERISTICS (continued)** (4.75 V < V<sub>CC</sub> < 5.25 V, 8.0 V < V<sub>RES</sub> < 30 V, 9.0 V < V<sub>BAT</sub> < 18 V, -40°C < T<sub>A</sub> < +85°C; unless otherwise stated.)

Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Analog MUX</b> V <sub>CC</sub> = 5.0 V					
MUX internal voltage drop	I <sub>OUT</sub> = 100 μA	–	–	100	mV
Proportion of V <sub>BAT</sub> on A <sub>OUT</sub> with V <sub>BAT</sub> selected	–	23	25	27	%
A <sub>OUT</sub> Impedance with V <sub>BAT</sub> selected	–	6.0	15.0	35	kΩ
Proportion of V <sub>RES</sub> on A <sub>OUT</sub> with V <sub>RES</sub> selected	–	15	17	19	%
A <sub>OUT</sub> Impedance with V <sub>RES</sub> selected	–	6.0	12.5	25.5	kΩ

<b>Digital Inputs – D<sub>IN</sub>, CLK, CS</b> V <sub>CC</sub> = 5.25 V, V <sub>BAT</sub> = 18 V, V <sub>RES</sub> = 30 V					
Input Low Voltage (V <sub>IL</sub> )	–	0	–	0.3 × V <sub>CC</sub>	V
Input High Voltage (V <sub>IH</sub> )	–	0.7 × V <sub>CC</sub>	–	V <sub>CC</sub>	V
Input Voltage Hysteresis	–	100	–	–	mV
Input Pull Down Current (I <sub>IH</sub> )	–	50	100	200	μA

<b>Digital Outputs – D<sub>OUT</sub></b> V <sub>CC</sub> = 4.75 V, V <sub>BAT</sub> = 18 V, V <sub>RES</sub> = 30 V					
Output Low Voltage (V <sub>OL</sub> )	I <sub>SINK</sub> = 1.0 mA	–	–	0.4	V
Output High Voltage (V <sub>OH</sub> )	I <sub>SOURCE</sub> = 1.0 mA	V <sub>CC</sub> – 0.75	–	–	V
Tri-State Pull-up Current	CS = 0, D <sub>OUT</sub> = 0	50	100	200	μA
Rise   Fall Time	C <sub>LOAD</sub> = 200 pF	–	–	50	ns

## PACKAGE PIN DESCRIPTION

Package Lead Number	Pin Symbol	Function
SO-20L		
1	V <sub>BAT</sub>	Battery Supply Voltage.
2	CHRG	Charge pump Storage.
3	V <sub>RES</sub>	Reserve Supply Voltage.
4	VR1	Loop 1 Supply.
5	SH1	Squib 1 High Side.
6	SL1	Squib 1 Low Side.
7	FG1	Loop 1 Return.
8	D <sub>OUT</sub>	Serial Port output.
9	CLK	Serial Port Clock.
10	MR	Squib Resistance Output Current.
11	CS	Serial Port Chip Select.
12	A <sub>OUT</sub>	Analog MUX Output.
13	A <sub>IN</sub>	Analog MUX Input.
14	FG2	Loop 2 Return.
15	SL2	Squib 2 Low Side.
16	SH2	Squib 2 High Side.
17	VR2	Loop 2 Supply.

## PACKAGE PIN DESCRIPTION (continued)

Package Lead Number	Pin Symbol	Function
SO-20L		
18	D <sub>IN</sub>	Serial Port Input.
19	V <sub>CC</sub>	5.0 V Regulated Supply.
20	GND	Signal Ground.

## FUNCTIONAL DESCRIPTION

The CS2082 is an automotive air bag deployment and diagnostic system for up to two independent firing loops. Communication with the ASIC is through a synchronous serial port using Serial Peripheral Interface (SPI) protocol, at CLK rates up to 2.0 MHz.

Data is simultaneously sent from the D<sub>OUT</sub> pin and received at the D<sub>IN</sub> pin under the control of the CS and CLK pins. Error detection logic is included in the SPI to guard against glitches on either the CS or CLK logic signal inputs. A valid CS frame must contain exactly 8 CLK cycles for each CS low-high-low transition. Detection of a frame error will cause input data for that frame to be ignored and an error code (\$FE) to be sent during the next valid CS frame.

The data at D<sub>OUT</sub> is sent MSB first and is guaranteed valid before the rising edge of CLK. The 8 bits sent from D<sub>OUT</sub> after CS goes high will be the previous data received, data from either the status register or the fault register, or the CS frame error code (\$FE).

The data at D<sub>IN</sub> is received MSB first and must be valid before the rising edge of CLK. The 8 bits received at D<sub>IN</sub> before CS goes low will be the current command. Table 1 defines the legal 8-bit SPI commands, where d = four data bits and x = don't care. All other inputs will be ignored.

Table 1. Valid CS2082 SPI Commands

COMMAND	FUNCTION
\$1x	Read Status Register
\$2x	Read Fault Register
\$3d	Squib Resistance Measurements
\$4d	Analog MUX Select
\$5d	Low Side Switch Control
\$6d	Auxiliary Control Register
\$Ad	High Side Switch Control

## Read Status Register – \$1x

The \$1x command causes the data contained in the status register to be sent from D<sub>OUT</sub> during the next valid CS frame. The status register reports the condition of the firing paths, closure detection of an external safing switch between

the V<sub>RES</sub> and VR1 pins, the state of the internal charge pump, and the state of external V<sub>BAT</sub> and V<sub>RES</sub> power supplies. The status register is an 8-bit active-high register with bit definition as shown in Table 2.

Table 2. Status Register Bit Definition

BIT	VALUE	DESCRIPTION
D7	0	Always Logic zero
D6	0	Always Logic zero
D5	F1	SH1 and SL1 switches active
D4	F2	SH2 and SL2 switches active
D3	SSC	Safing Sensor is closed
D2	RL	V <sub>RES</sub> voltage is below trip
D1	BL	V <sub>BAT</sub> voltage is below trip
D0	CL	CHRG voltage is below trip

## Read Fault Register – \$2x

The \$2x command causes the data contained in the fault register to be sent from D<sub>OUT</sub> during the next valid CS frame. The register reports fire path faults by continuously comparing each path to a portion of the voltage at the V<sub>BAT</sub> pin. The fault register is an 8-bit active-high register with bit definition as shown in Table 3.

Table 3. Fault Register Bit Definition

BIT	VALUE	DESCRIPTION
D7	0	Always Logic zero
D6	0	Always Logic zero
D5	0	Always Logic zero
D4	0	Always Logic zero
D3	SB2	High Side of Sqib 2 above 75% V <sub>BAT</sub> trip threshold
D2	SB1	High Side of Sqib 1 above 75% V <sub>BAT</sub> trip threshold
D1	SG2	Low Side of Sqib 2 below 25% V <sub>BAT</sub> trip threshold
D0	SG1	Low Side of Sqib 1 below 25% V <sub>BAT</sub> trip threshold

Each SHx pin is pulled up to V<sub>BAT</sub> while each SLx pin is pulled down to GND through separate nominal 10 kΩ resistors, thus biasing each normal fire path to about 1/2 V<sub>BAT</sub>. An open fire path has been detected if both the SBx and SGx bits are set for that path. To detect faults between fire paths and to test driver function, each driver should be activated individually. The activated driver should cause its respective fault bit to be set. If an activated driver does not set its respective fault bit, a driver fault has been detected. If an activated driver causes the fault bit of an inactivated driver to be set, a fault *between* fire paths has been detected. Table 4 defines the implied ranges over which the various types of faults can be detected.

**Table 4. Implied Resistive Fault Detection Ranges**

Fault	Min	Nom	Max	Unit
Short to Ground	1	5	10	kΩ
Short to Battery	1	5	10	kΩ
Open	5	20	40	kΩ
Driver Open	1	5	10	kΩ
Driver Shorted	1	5	10	kΩ
Squib to Squib	1	5	10	kΩ

### Squib Resistance Measurement – §3d

The §3d command activates squib resistance measurement for the selected firing path. The respective active-high bit definitions are shown in Table 5. At power-up, the default path is 'None.'

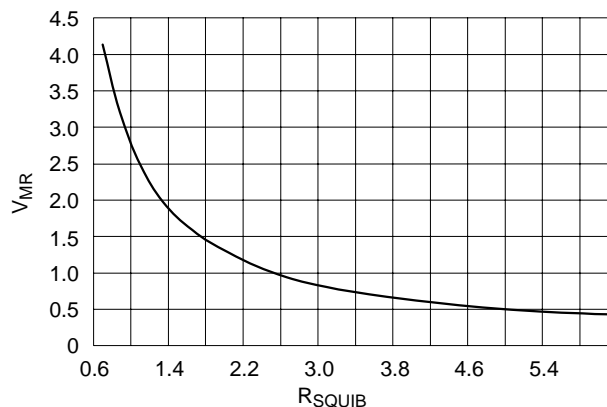
**Table 5. Squib Resistance Path Select**

D3	D2	D1	D0	Path
x	x	0	0	NONE
x	x	0	1	SQUIB 1
x	x	1	0	SQUIB 2
x	x	1	1	NONE

Squib resistance is measured by forcing 50 mV nominal (proportional to V<sub>CC</sub>) across the squib. The resulting squib current is passed to an external load resistor at the MR pin, converting the current back into a voltage. This voltage may be read directly at the MR pin, or passed through the analog multiplexer to be read at the A<sub>OUT</sub> pin. The known values of the squib differential voltage (V<sub>DIFF</sub>) and the MR resistance (R<sub>MR</sub>), and the measured MR voltage (V<sub>MR</sub>) indicate squib resistance such that:

$$RSQUIB = \frac{RMR \times V_{DIFF}}{V_{MR}}$$

Typical MR voltage response for R<sub>MR</sub> = 50 Ω over a squib resistance range of 0.6 Ω to 6.0 Ω is illustrated in Figure 2.



**Figure 2. Typical MR Voltage Response**

Measurement accuracy of the CS2082 with combined tolerances and with an external 1% load resistor at the MR pin can be defined by the equation:

$$RSQ(E) = \frac{V_{DIFF(IDEAL)} \times R_{MR(IDEAL)}}{\left(\frac{V_{DIFF \pm 12\%}}{R_{SQ(A)}}\right) \pm 1\% \times R_{MR} \pm 1\%}$$

$$= RSQ(A) + 12.5\% / -15.94\%$$

where V<sub>DIFF(IDEAL)</sub> and R<sub>MR(IDEAL)</sub> are the assumed values for the squib resistance solution algorithm, R<sub>SQ(A)</sub> is the actual squib resistance, and R<sub>SQ(E)</sub> is the result of the solution algorithm. An additional error may be added if the MR voltage is measured through the analog multiplexer.

In operation, current is sourced from V<sub>BAT</sub> to the SHx pin, through the squib to the SLx pin, and returned to ground through the MR load resistor. Current clamps are provided for both the SHx and SLx pins and a voltage clamp is provided for the MR pin. These clamps along with the resolution of the ADC are the constraining factors for the minimum and maximum measurable squib resistance values.

The minimum measurable squib resistance can be defined as:

$$\frac{V_{DIFF(MIN)}}{I_{LIM(MAX)}} \leq RSQUIB(MIN) \leq \frac{V_{DIFF(MIN)} \times R_{MR(MIN)}}{V_{CLAMP(MAX)}}$$

The maximum measurable squib resistance can be defined as:

$$RSQUIB(MAX) = \frac{V_{DIFF(MAX)} \times R_{MR(MAX)} \times (2^n - 1)}{V_{CC(MIN)}}$$

In the above equations, V<sub>DIFF</sub> is the SHx–SLx forced differential voltage, I<sub>LIM</sub> is the SHx resistive measure current limit, V<sub>CLAMP</sub> is the MR clamp voltage, R<sub>MR</sub> is the toleranced MR load resistor value and n is the number of bits of resolution of the ADC.

It should be noted that during resistive measurements, faults to GND or BAT (dependent on V<sub>BAT</sub> voltage and

squib resistance) may be reported by the fault register and should be ignored.

Power Dissipation during resistive measurement can be calculated as:

$$P = I_{SQUIB}(V_{BAT} - V_{DIFF}) - (I_{SQUIB} \times R_{MR})$$

where  $V_{BAT}$  is the voltage at the CS2082  $V_{BAT}$  pin and  $I_{SQUIB}$  is the measurement current through the squib. A typical value for P is 300 mW when  $V_{BAT} = 13.5$ ,  $V_{DIFF} = 50$  mV,  $R_{SQUIB} = 2.0 \Omega$  and  $R_{MR} = 49.9 \Omega$ .

The resultant increase in power dissipation will cause a corresponding increase in die temperature which will cause a corresponding decrease in time to thermal shutdown of the CS2082. To minimize the impact of squib resistive measurements on time to thermal shutdown a 5% duty cycle is recommended.

**Analog MUX – \$4d**

The \$4d command selects one of five states at the  $A_{OUT}$  pin. The states are: High-Z; MR voltage;  $A_{IN}$  voltage; proportion of  $V_{BAT}$ ; proportion of  $V_{RES}$ . The active-high Analog Mux select register bit definitions are shown in Table 6. All other states will be interpreted as High-Z. At power-up, the default state is ‘High-Z.’

**Table 6. Analog MUX Output Select**

D3	D2	D1	D0	State
0	0	0	0	High-Z
0	0	0	1	MR
0	0	1	0	$A_{IN}$
0	1	0	0	BAT
1	0	0	0	RES

**Low Side Switch Control – \$5d**

The \$5d command activates the low side switches. When a data bit is low that switch is turned on. More than one switch can be activated at a time. Bit assignment is shown in Table 7. At power-up, no switches are active.

**Table 7. Low Side Switch Select**

D3	D2	D1	D0	Active
x	x	0	0	BOTH
x	x	0	1	SL2
x	x	1	0	SL1
x	x	1	1	NONE

**Auxiliary Control Register – \$6d**

The \$6d command selects the  $V_{RES}$  Monitoring trip threshold. The threshold determines when the \$1x Status Register reports  $V_{RES} = 1$ . Bit assignment is shown in Table 8. At power-up, default trip is 17 V.

**Table 8.  $V_{RES}$  Monitor Trip Select**

D3	D2	D1	D0	Trip
x	x	x	0	17 V
x	x	x	1	23 V

**High Side Switch Control – \$Ad**

The \$Ad command activates the high side switches. When a data bit is high, that switch is turned on. More than one switch can be activated at a time. Bit assignment is shown in Table 9. Note that the \$5d and \$Ad commands are binary complements, i.e., by sending 1010xx11, both high side switches are activated, and by sending the complement 0101xx00, both low side switches are activated. At power-up, no switches are active.

**Table 9. High Side Switch Select**

D3	D2	D1	D0	Active
x	x	0	0	NONE
x	x	0	1	SH1
x	x	1	0	SH2
x	x	1	1	BOTH

# CS2082

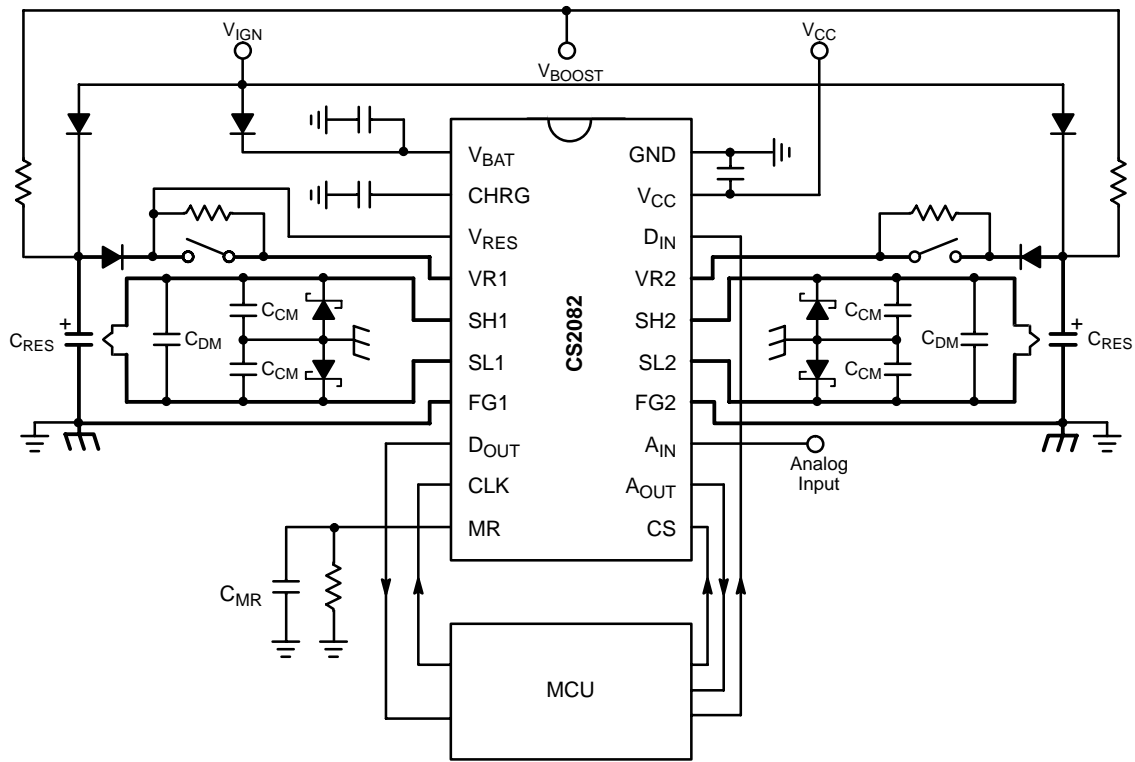



Figure 3. Application Diagram



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