THE DATASHEET OF

CDCE421AEVM

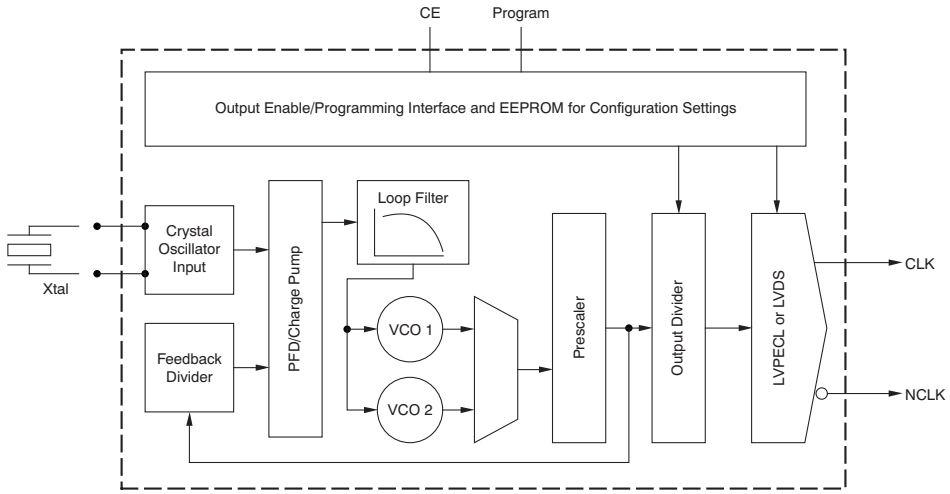
Fully-Integrated, Wide Range, Low-Jitter Crystal Oscillator Clock Generator

FEATURES

- Single Supply at 3.3 V for LVPECL or LVDS Operation
- High-Performance Clock Multiplier, Incorporating Crystal Oscillator Circuitry with Integrated Frequency Synthesizer
- Low Output Jitter: 380 fs RMS typical (from 10 kHz to 20 MHz)
- Low Phase Noise at High Frequency (708-MHz LVPECL):
  - Typically –109 dBc/Hz at 10 kHz and –146dBc/Hz at 10 MHz from the carrier
- Supports Crystal or LVCMOS Input Frequencies from 27.35 MHz to 38.33 MHz
- Output Frequency Ranges from 10.9 MHz to 766.7 MHz and from 875.2 MHz to 1175 MHz
- Low-Voltage Differential Signaling (LVDS) Output, 100-Ω Differential Off-Chip Termination, 10.9-MHz to 400-MHz Frequency Range
- Differential Low-Voltage Positive Emitter Coupled Logic (LVPECL) Outputs, 10.9-MHz to 1.175-GHz Frequency Range
- Two Fully-Integrated Voltage-Controlled Oscillators (VCO) Support Wide Output Frequency Range
- Fully Integrated Programmable Loop Filter
- Typical Power Consumption at 3.3 V:
  - 274 mW in LVDS mode
  - 250 mW in LVPECL mode
- Chip Enable Control Pin
- Simple Serial Interface Allows Programming after Manufacturing
- Integrated On-Chip Nonvolatile Memory (EEPROM) Stores Settings Without Applying High Voltage
- Available in 4-mm × 4-mm QFN-24 Package
- ESD Protection Exceeds 2 kV (HBM)
- Industrial Temperature Range: –40°C to +85°C

APPLICATIONS

- Low-Cost, High-Frequency Crystal Oscillator



DESCRIPTION

The CDCE421A is a high-performance, low phase noise clock generator. It has two fully-integrated, low-noise, LC-based voltage-controlled oscillators (VCOs) that operate in the 1.750-GHz to 2.350-GHz frequency range(1). It also features an integrated crystal oscillator that operates in conjunction with an external AT-cut crystal to produce a stable frequency reference for the phase-locked loop (PLL) based frequency synthesizer.

The output frequency (f_{OUT}) is proportional to the frequency of the input crystal (f_{XTAL}). The prescaler divider, feedback divider, output divider, and VCO selection set the output frequency with respect to f_{XTAL}. Table 2 provides the look-up information for a desired frequency, f_{OUT}, and the corresponding settings for the dividers and VCO selection. To calculate the exact crystal oscillator frequency required for the desired output, use the formula in Equation 1.

$$f_{XTAL} = \left(\frac{\text{Output Divider}}{\text{Feedback Divider}} \right) \times f_{OUT} \quad (1)$$

Where:

- Output divider(1) = 1, 2, 4, 8, 16, and 32
- Feedback divider(2) = 12, 16, 20, and 32

In the CDCE421A, the feedback divider is set automatically with respect to the prescaler setting. The product of the prescaler and the feedback divider should be between 60 and 64 as shown in Table 2 to maintain a stable control loop.

Figure 1 shows a high-level block diagram of the device. The CDCE421A supports one differential LVDS clock output or one differential LVPECL output. All device settings are programmable through a proprietary simple serial interface (SSI).

The device operates in 3.3-V supply environment for both LVPECL and LVDS outputs and is characterized for operation from –40°C to +85°C. The CDCE421A is available in a QFN-24 4-mm × 4-mm package.

CDCE421 Users:

The CDCE421A provides several device enhancements to the CDCE421. For a complete description of differences between these products, refer to Appendix C: Application Information.

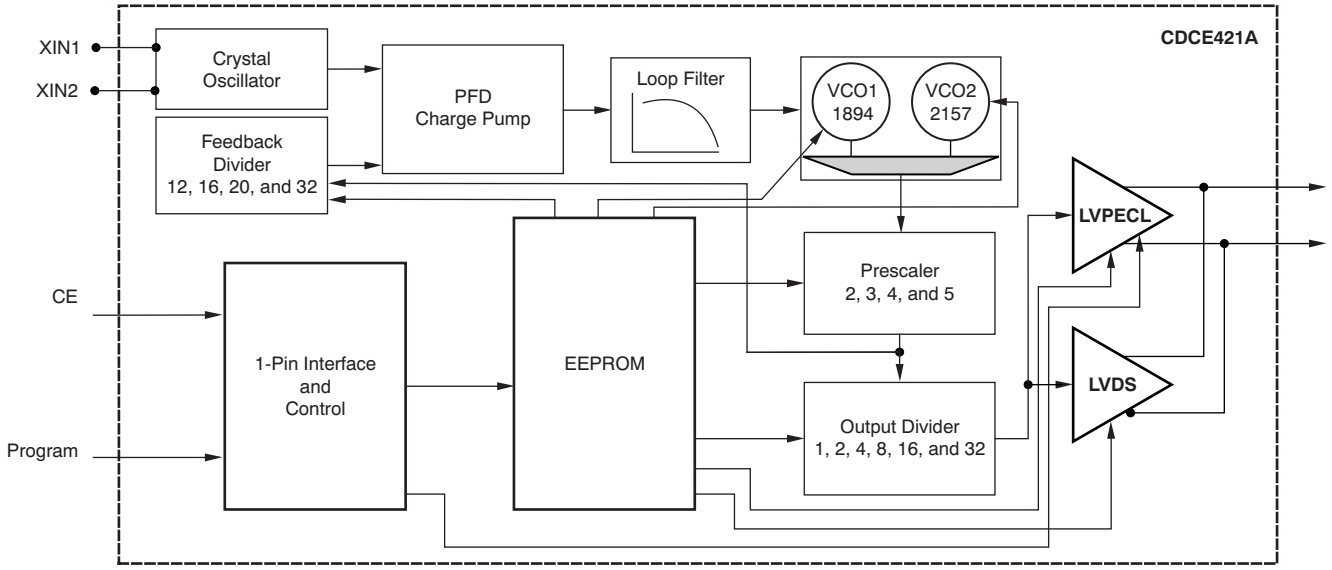


Figure 1. Functional Block Diagram

(1) Output divider and feedback divider should be from the same row in Table 2.
(2) Feedback divider is set automatically with respect to the prescaler setting in Table 2.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS(1)

T_A	PACKAGED DEVICES	FEATURES
–40°C to +85°C	CDCE421ARGET	24-pin QFN (RGE) package, small tape and reel
	CDCE421ARGER	24-pin QFN (RGE) package, tape and reel

(1) For the most current specifications and package information, see the Package Option Addendum located at the end of this data sheet or refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted).(1)

		CDCE421A	UNIT
V_{DD}	Supply voltage(2)	–0.5 to 4.6	V
V_I	Voltage range for all other input pins(2)	–0.5 to V_{CC} to +0.5	V
I_O	Output current for LVPECL	–50	mA
ESD	Electrostatic discharge (HBM)	2	kV
T_A	Specified free-air temperature range (no airflow)	–40 to +85	°C
T_J	Maximum junction temperature	+125	°C
T_{STG}	Storage temperature range	–65 to +150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating condition* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3.0	3.30	3.60	V
T_A	Ambient temperature (no airflow, no heatsink)	–40		+85	°C

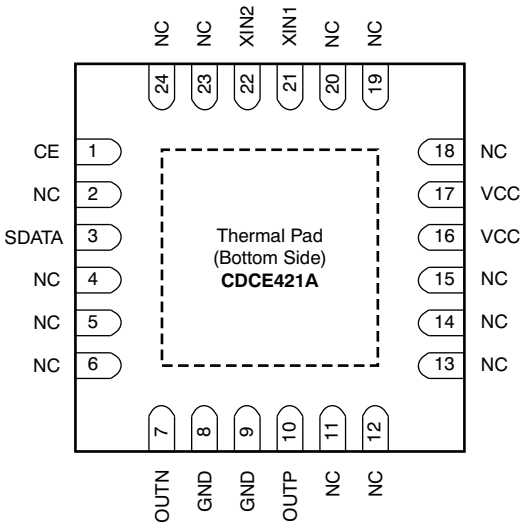
ELECTRICAL CHARACTERISTICS

Over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	CDCE421A			UNIT
			MIN	TYP	MAX	
V_{DD}	Supply voltage		3.00	3.30	3.60	V
I_{VDD} (LVDS)	Total current	LVDS Mode		83	103	mA
I_{VDD} (LVPECL)	Total current	LVPECL Mode		91	110	mA
t_S	Start-up time	f_{IN} = 27.35 MHz, f_{OUT} = 109.4 MHz, Power Supply Ramp Time = 1 ms			4	ms
LVDS Output Mode (See Figure 2 and Figure 4)						
f_{CLK}	Output frequency		10.9		400	MHz
$\|V_{OD}\|$	LVDS differential output voltage	R_L = 100 Ω	247		454	mV
ΔV_{OD}	LVDS V_{OD} magnitude change				50	mV
V_{OS}	Offset voltage	–40°C to +85°C	1.1		1.3	V
ΔV_{OS}	V_{OS} magnitude change				50	mV
t_R	Output rise time	20% to 80% of $V_{OUT(PP)}$		230		ps
t_F	Output fall time	20% to 80% of $V_{OUT(PP)}$		230		ps
I_{OS}	Short-circuit output current	Short V_{OUT+} to ground, V_{OUT} = 0 V			30	mA
		Short $V_{OUT–}$ to ground, V_{OUT} = 0 V			30	mA
	Duty cycle of the output waveform		45		55	%
$t_{j,\ RMS}$	RMS jitter	10 kHz to 20 MHz			1	ps, RMS
LVPECL Output Mode (See Figure 3 and Figure 5)						
f_{CLK}	Output frequency		10.9		1175	MHz
V_{OH}	LVPECL high-level output voltage		V_{CC} – 1.2		V_{CC} – 0.81	V
V_{OL}	LVPECL low-level output voltage		V_{CC} – 2.17		V_{CC} – 1.36	V
$\|V_{OD}\|$	LVPECL differential output voltage		407		1076	mV
t_R	Output rise time	20% to 80% of $V_{OUT(PP)}$		230		ps
t_F	Output fall time	20% to 80% of $V_{OUT(PP)}$		230		ps
	Duty cycle of the output waveform		45		55	%
$t_{j,\ RMS}$	RMS jitter	10 kHz to 20 MHz			1	ps, RMS
LVCMOS Input						
$V_{IL,\ CMOS}$	Low-level CMOS input voltage	V_{DD} = 3.3 V			0.3 × V_{CC}	V
$V_{IH,\ CMOS}$	High-level CMOS input voltage	V_{DD} = 3.3 V	0.7 × V_{CC}			V
$I_{L,\ CMOS}$	Low-level CMOS input current	V_{DD} = $V_{DD,\ max}$, V_{IL} = 0.0 V			–200	µA
$I_{H,\ CMOS}$	High-level CMOS input current	V_{DD} = $V_{DD,\ min}$, V_{IH} = 3.7 V			200	µA

DEVICE INFORMATION

RGE PACKAGE
QFN-24
(TOP VIEW)



PIN DESCRIPTIONS

Table 1. CDCE421A Pin Descriptions

TERMINAL NAME	TERMINAL NO.	TYPE	ESD PROTECTION	DESCRIPTION
CE	1	I	Y	Chip enable CE = 1: enable the device and the outputs. CE = 0: disable all current sources; in LVDS mode, LVDSP = LVDSN = Hi-Z; in LVPECL mode, LVPECLP = LVPECLN = Hi-Z.
GND	8, 9	GND	Y	Ground
No connect	2, 4–6, 11–15, 18–20, 23,24			Do not connect these pins. Leave them floating.
OUTN	7	O	Y	High-speed negative differential LVPECL or LVDS outputs. (Outputs are enabled by CE and selected by the EEPROM configuration registers.)
OUTP	10	O	Y	High-speed positive differential LVPECL or LVDS outputs. (Outputs are enabled by CE and selected by the EEPROM configuration registers.)
SDATA	3	I	Y	Programming pin using TI proprietary interface protocol
VCC	16, 17	Power	Y	3.3-V power supply
XIN1 XIN2	21 22	I GND/NC	Y N	In crystal input mode, connect XIN1 to one end of the crystal and XIN2 to the other end of the crystal. In LVCMOS input single-ended driven mode, XIN1 (pin 21) acts as an input reference, and XIN2 should connect to GND or it can be left unconnected.

DEVICE SETUP AND CONFIGURATION

Table 2. Crystal Frequency Selection and Device Settings

DESIRED OUTPUT FREQUENCY (MHz)		REQUIRED INPUT CRYSTAL FREQUENCY (MHz)		VCO SELECTION	OUTPUT DIVIDER	PRESCALER SETTING	FEEDBACK DIVIDER(1)
From	To	From	To				
1020	1175	31.875	36.719	VCO 2	1	2	32
875.2(2)	1020	27.351	31.875	VCO 1	1	2	32
680	766.7(2)	34	38.333	VCO 2	1	3	20
583.5	680	29.174	34	VCO 1	1	3	20
510	587.5	31.875	36.719	VCO 2	1	4	16
437.6	510	27.351	31.875	VCO 1	1	4	16
408	460	34	38.333	VCO 2	1	5	12
350.1	408	29.174	34	VCO 1	1	5	12
340	383.3	34	38.333	VCO 2	2	3	20
291.7	340	29.174	34	VCO 1	2	3	20
255	293.8	31.875	36.719	VCO 2	2	4	16
218.8	255	27.351	31.875	VCO 1	2	4	16
204	230	34	38.333	VCO 2	2	5	12
175	204	29.174	34	VCO 1	2	5	12
170	191.7	34	38.333	VCO 2	4	3	20
145.9	170	29.174	34	VCO 1	4	3	20
127.5	146.9	31.875	36.719	VCO 2	4	4	16
109.4	127.5	27.351	31.875	VCO 1	4	4	16
102	115	34	38.333	VCO 2	4	5	12
87.5	102	29.174	34	VCO 1	4	5	12
85	95.8	34	38.333	VCO 2	8	3	20
72.9	85	29.174	34	VCO 1	8	3	20
63.8	73.4	31.875	36.719	VCO 2	8	4	16
54.7	63.8	27.351	31.875	VCO 1	8	4	16
51	57.5	34	38.333	VCO 2	8	5	12
43.8	51	29.174	34	VCO 1	8	5	12
42.5	47.9	34	38.333	VCO 2	16	3	20
36.5	42.5	29.174	34	VCO 1	16	3	20
31.9	36.7	31.875	36.719	VCO 2	16	4	16
27.4	31.9	27.351	31.875	VCO 1	16	4	16
25.5	28.8	34	38.333	VCO 2	16	5	12
21.9	25.5	29.174	34	VCO 1	16	5	12
21.3	24	34	38.333	VCO 2	32	3	20
18.2	21.3	29.174	34	VCO 1	32	3	20
15.9	18.4	31.875	36.719	VCO 2	32	4	16
13.7	15.9	27.351	31.875	VCO 1	32	4	16
12.8	14.4	34	38.333	VCO 2	32	5	12
10.9	12.8	29.174	34	VCO 1	32	5	12

(1) Feedback divider is set automatically with respect to the prescaler setting.
(2) Discontinuity in frequency range.

Device Setup Example

The following example illustrates the process to calculate the required AT-cut crystal frequency that is needed to generate a desired output frequency.

Assume we need to generate an output frequency of 622.08MHz. We use Table 3 to find that the desired output frequency lies between 583.5 and 680.0MHz.

Table 3. Crystal Frequency Selection and Device Settings (Selection)

DESIRED OUTPUT FREQUENCY (MHz)		REQUIRED INPUT CRYSTAL FREQUENCY (MHz)		VCO SELECTION	OUTPUT DIVIDER	PRESCALER SETTING	FEEDBACK DIVIDER(1)
From	To	From	To				
680.0	766.7	34.000	38.333	VCO 2	1	3	20
583.5	680.0	29.174	34.000	VCO 1	1	3	20
510.0	587.5	31.875	36.719	VCO 2	1	4	16

(1) Feedback divider is set automatically with respect to the prescaler setting.

This frequency value means that the device must be configured in the following way:

VCO: VCO1

Output divider: 1

Prescaler setting: 3

To determine the correct crystal frequency required to achieve 622.08 MHz with these settings, we use Equation 2, explained earlier in this data sheet.

$$f_{XTAL} = \left(\frac{1}{20}\right) \times 622.08 = 31.154 \text{ MHz} \quad (2)$$

Thus, the AT-cut frequency should be 31.154 MHz (that is, between 29.174 MHz and 34.000 MHz, as shown in Table 3).

Serial Interface and Control

The CDCE421A uses a unique, TI-proprietary interface protocol that can be configured and programmed via a single input pin to the device. The architecture enables only writing to the device from this input pin. Reading the content of a register can be achieved by sending a read command on the input pin and monitoring the desired output pins (LVDS or LVPECL). In cases where the output pins cannot be used to read the content, the software that controls the interface must account for what is written to the EEPROM and when it is programmed. Monitoring the outputs verifies the programming modes; cycling the power on the device verifies that the EEPROM contains the proper configuration.

The CDCE421A can be configured and programmed via the SDATA input pin. For this purpose, a pulse-code shaped programming sequence must be written to the device as described in the EEPROM Programming section. During the EEPROM programming phase, the device requires a stable supply voltage (V_{DD}) of 3.3 V ±300 mV for securely writing to the EEPROM cells. After each *Write to WordX* instruction, the written data are latched, made effective, and offer look-ahead before the actual data are stored into the EEPROM.

Table 4 summarizes all valid programming commands for the CDCE421A.

Table 4. CDCE421A Programming Commands

SDATA	FUNCTION
001100	Enter *Programming Mode* (State 1→State 2); bits must be sent in the specified order with the specified timing. Otherwise a *time-out* occurs.
111011	Enter *Register Readback Mode*; bits must be sent in the specified order with the specified timing. Otherwise a *time-out* occurs.
000 xxxx xxxx	*Write to Word0* (State 2)(1)(2)(3)
100 xxxx xxxx	*Write to Word1* (State 2)(1)(2)(3)
010 xxxx xxxx	*Write to Word2* (State 2)(1)(2)(3)
110 xxxx xxxx	*Write to Word3* (State 2)(1)(2)(3)
001 xxxx xxxx	*Write to Word4* (State 2)(1)(2)(3)
101 xxxx xxxx	*Write to Word5* (State 2)(1)(2)(3)
111 xxxx xxxx	State Machine Jump: All other patterns not defined as below cause *Exit to Normal Mode*
111 1111 0000	Jump: *Enter EEPROM programming without EEPROM lock* (State2 →State 3)
111 0101 0101	Jump: *Enter EEPROM programming with EEPROM lock* (State 2→State 4)
111 0000 0000	Jump: *Exit EEPROM programming* (State 3 or State 4→State 1)

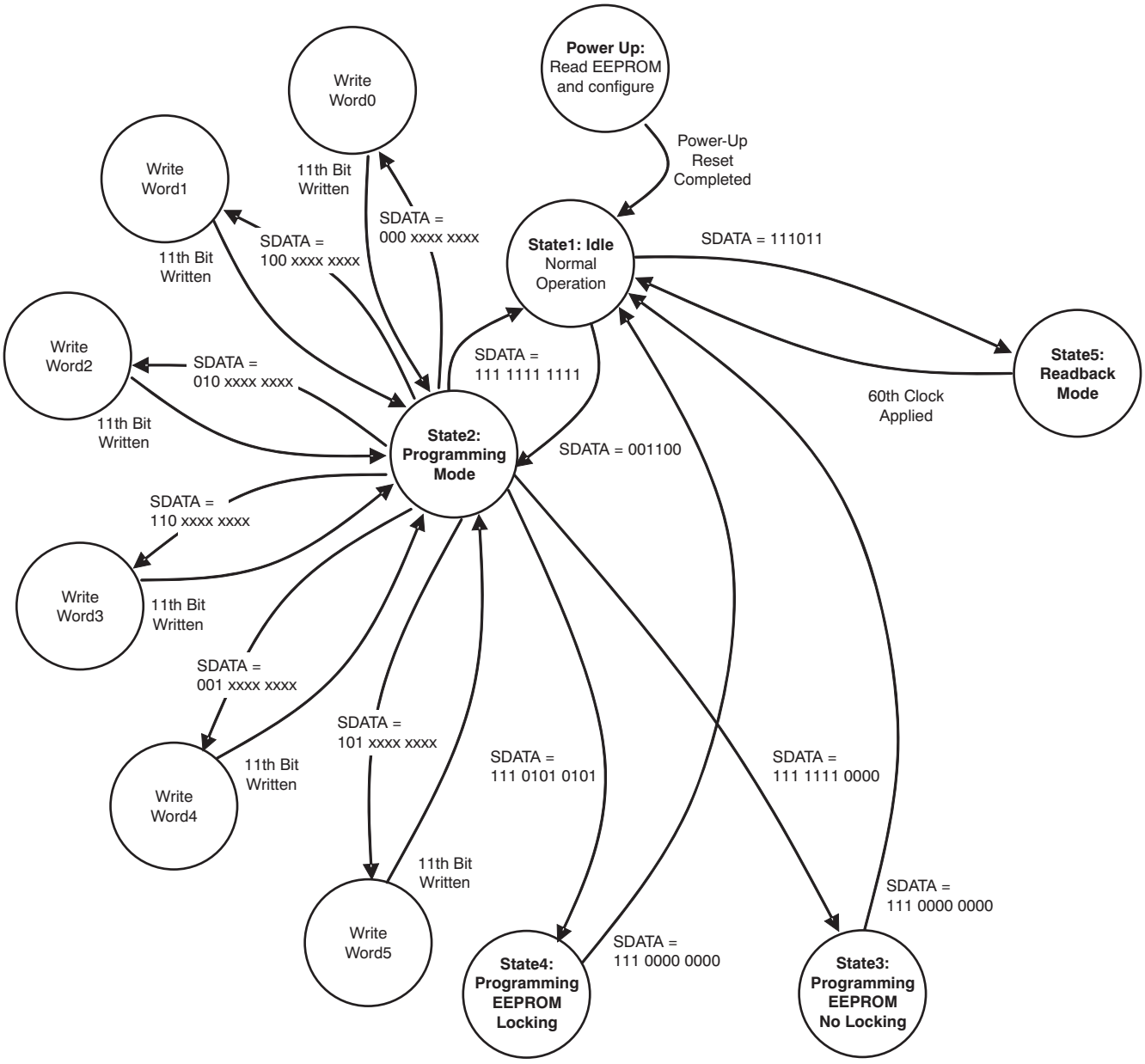
(1) Each rising edge causes a bit to be latched.
(2) In between the bits, some longer time delays can occur, but these delays have no effect on the data.
(3) A *Write to WordX* instruction is expected to be 10 bits long. After the tenth bit, the respective word is latched, and its effect can be observed as a *look-ahead* function.

Outputs (LVPECL or LVDS)

The CDCE421A device has two sets of output drivers, LVPECL and LVDS, where the outputs are wire-ORed together. Only one output can be selected at a given time; the other output goes to a high-impedance (Hi-Z) state.

If the device is configured for LVPECL outputs, the output buffers go to Hi-Z ,and the termination resistors determine the state of the output (LVPECLP = LVPECLN = Hi-Z) in the device disable mode (CE = L). If the device is configured in LVDS mode, the outputs go to a Hi-Z state if the device is disabled (CE = L).

State Flow



(1) In States 2, 3, 4, and 5, the signal pin CE is disregarded and has no influence on power down.

State Flow Diagram of Single Pin Interface

Enter *Programming Mode*

Figure 2 shows the timing behavior of data to be written into SDATA. The sequence shown is '001100'. If the high period is as short as t_1, this period is interpreted as '0'. If the high period is as long as t_3, this period is interpreted as a '1'. This behavior is achieved by shifting the incoming signal SDATA by time t_5 into signal SDATA_DELAYED. As Figure 2 shows, SDATA_DELAYED can be used to latch (or strobe) SDATA. The specification for the timings t_1 through t_7, t_R and t_F are shown in Table 5.

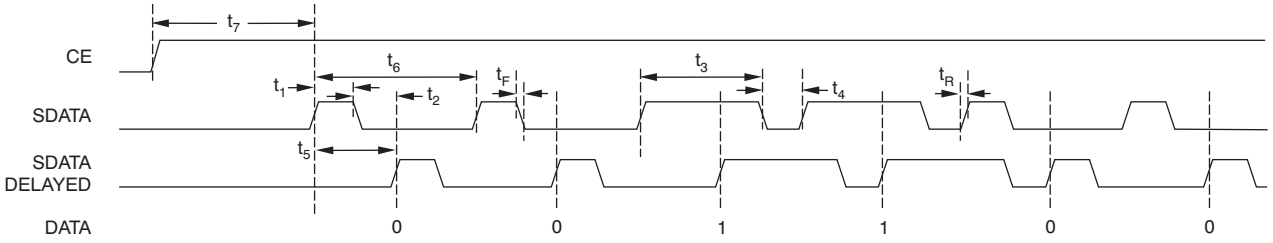


Figure 2. SDATA/CE Timing

Table 5. SDATA/CE Timing Requirements(1)

PARAMETER		MIN	TYP	MAX	UNIT
$f_{SDATACLK}$	Repeat frequency of programming	60	70	80	kHz
t_1	Low signal: High pulse duration		0.2 t		ms
t_2	Low signal: Low pulse duration during *Entering Programming* sequence		0.8 t		ms
	Low signal: Low pulse duration during programming bits		0.8 t		ms
t_3	High signal: High pulse duration		0.8 t		ms
t_4	High signal: Low pulse duration during *Entering Programming* sequence		0.2 t		ms
	High signal: Low pulse duration during programming bits		0.2 t		ms
t_6	Time-out during *Entering Programming Mode* and *Enter Readback Mode* until next bit must occur. High-pulse or low-pulse duration each must be less than this time; otherwise, a time-out results.	16			ms
t_7	EN-high time before first SDATA can be clocked in	3 t			ms
t_R/t_F	Rise and fall time from 20% to 80% of V_{DD}		2		ns

(1) $t = 1/f_{SDATACLK}$.

EEPROM Programming

To program the EEPROM, follow the procedure outlined in this section.

Load all the registers in RAM by writing to Word0 ... Word5. After going back to State 2, then go to State 3 (Programming EEPROM, No Locking) or State 4 (Programming EEPROM with Locking). The contents of Word0 … to Word5 are saved in the EEPROM. Wait 10ms in State 3 or State 4 when programming the EEPROM before moving to State 2 (idle state).

NOTE:

When writing to the device for functionality testing and verification via the serial bus, you are only accessing the RAM. The programming of the CDCE421A can only be performed at V_{CC} = 3.3 V and at room temperature (+25°C).

Programming Cycle of Six Words and Programming Into EEPROM Example

Figure 3 shows an *Enter Programming Mode* sequence and how the different words can be written. The addressing of Word0 … Word5 can be seen in **bold**. After that, the inverted payload for the respective word is clocked in. In this example, this step is followed by a Jump from State 2→State 3 into *Enter EEPROM programming with EEPROM lock*. In the EEPROM programming state, it is required to wait at least 10ms for save programming to occur. The last command is a jump from State 3 back to State 1 (normal operation). Then cycle the power and verify that the device is functioning as programmed.

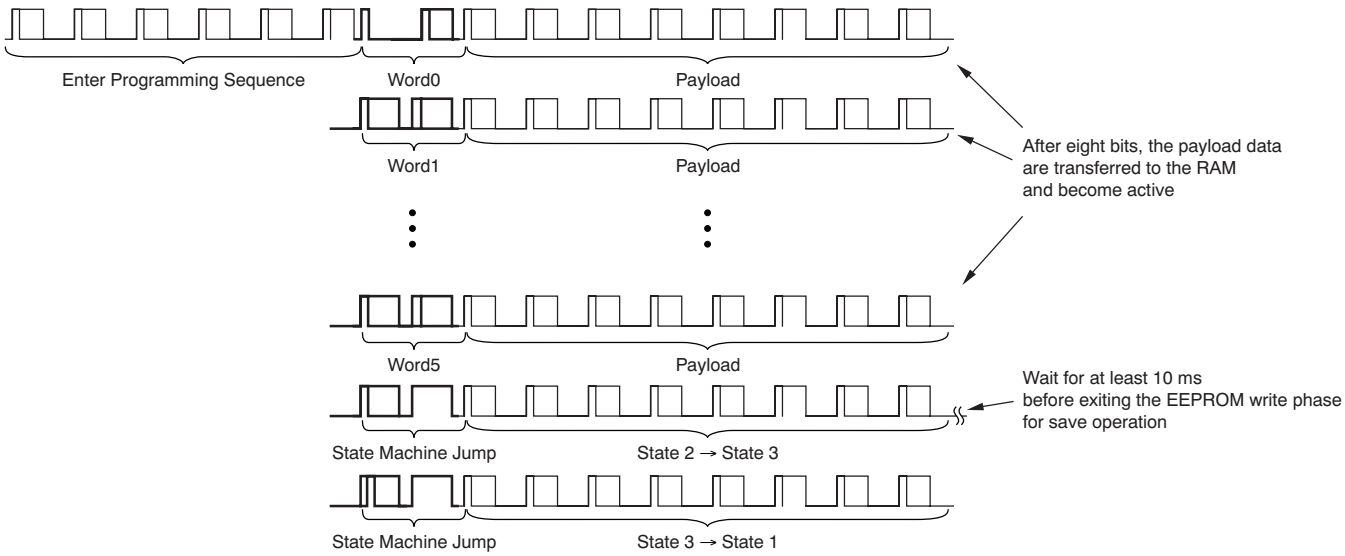


Figure 3. Programming Cycle of Six Words and Programming Into EEPROM

Enter *Register Readback* Mode

Similar to the *Enter Programming Mode* sequence, the *Enter Register Readback Mode* is written into SDATA. After the command has been issued, the SDATA-input is reconfigured as the clock input. By applying one clock, the EEPROM content is read into the shift registers. Then, by applying further clocks at SDATA, the EEPROM content can be clocked out and observed at FOUT. Additionally, FOUT is reconfigured during this operation, as can be seen in Figure 4. There are 59 bits to be clocked out. With the 61st rising clock edge, the FOUR pin is reconfigured for normal operation.

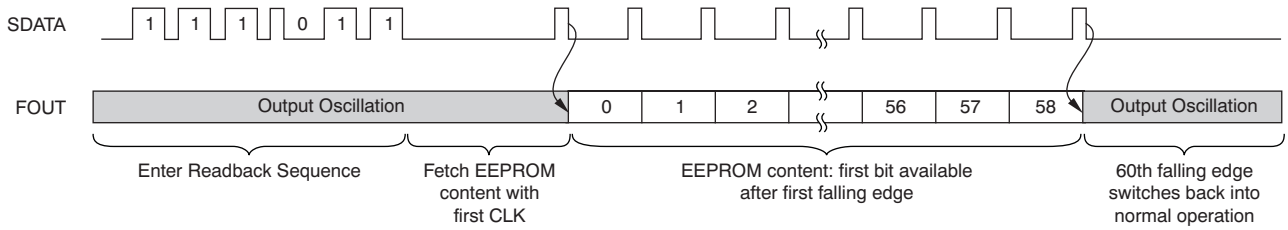


Figure 4. Register Readback Mode Timing Sequence

Table 6 summarizes the contents and functions of the output bit-stream. Note that bit 0 is clocked out first.

Table 6. Register Readback Mode: Output Bit-Stream

OUTPUT BIT-STREAM	FUNCTION
Bit[0:2]	Revision identifier (MSB first)
Bit[3:8]	VCO calibration word
Bit[9]	EEPROM Status: 0 = EEPROM has never been written 1 = EEPROM has been programmed before
Bit[10]	EEPROM Lock: 0 = EEPROM can be rewritten 1 = EEPROM is locked; rewriting the EEPROM is no longer possible
Bit[11:18]	Storage value Word5 (MSB first)
Bit[19:26]	Storage value Word4 (MSB first)
Bit[27:34]	Storage value Word3 (MSB first)
Bit[35:42]	Storage value Word2 (MSB first)
Bit[43:50]	Storage value Word1 (MSB first)
Bit[51:58]	Storage value Word0 (MSB first)

REGISTER DESCRIPTION

Table 7. Word 0

Bit	Name	Description/Function	Type	Recommended Value
0	C0	Register selection	W	0
1	C1	Register selection	W	0
2	C2	Register selection	W	0
3	SELVCO	VCO select: 0 = VCO1 1 = VCO2	W	User
4	SELPRESC	Prescaler setting, Bit 0	W	User
5	SELPRESC	Prescaler setting, Bit 1	W	User
6	OUTSEL	Output divider select, Bit 0	W	User
7	OUTSEL	Output divider select, Bit1	W	User
8	OUTSEL	Output divider select, Bit 2	W	User
9	DRVSEL	Driver select: 0 =LVDS 1=PECL	W	User
10	TITEST1	Reserved	W	1

4	Divide by value (SELPRESC 1, SELPRESC 0)
5	Divide by 5 = (00), 3 = (01), 4 = (10), and 2 = (11)
6	Output divider (OUTSEL2, OUTSEL1, OUTSEL0) Divide by 1 = (000) , 2 = (001), 4 = (010), 8 = (011), 16 = (100), 32 = (101)
7	
8	

Table 8. Word 1

Bit	Name	Description/Function	Type	Recommended Value
0	C0	Register selection	W	1
1	C1	Register selection	W	0
2	C2	Register selection	W	0
3	LFRCSEL	Loop filter control settings, Bit 0	W	1
4	LFRCSEL	Loop filter control settings, Bit 1	W	1
5	LFRCSEL	Loop filter control settings, Bit 2	W	1
6	LFRCSEL	Loop filter control settings, Bit 3	W	1
7	LFRCSEL	Loop filter control settings, Bit 4	W	1
8	LFRCSEL	Loop filter control settings, Bit 5	W	0
9	LFRCSEL	Loop filter control settings, Bit 6	W	1
10	LFRCSEL	Loop filter control settings, Bit 7	W	0

Table 9. Word 2

Bit	Name	Description/Function	Type	Recommended Value
0	C0	Register selection	W	0
1	C1	Register selection	W	1
2	C2	Register selection	W	0
3	LFRCSEL	Loop filter control settings, Bit 8	W	1
4	LFRCSEL	Loop filter control settings, Bit 9	W	1
5	LFRCSEL	Loop filter control settings, Bit 10	W	0
6	LFRCSEL	Loop filter control settings, Bit 11	W	0
7	LFRCSEL	Loop filter control settings, Bit 12	W	0
8	LFRCSEL	Loop filter control settings, Bit 13	W	0
9	LFRCSEL	Loop filter control settings, Bit 14	W	0
10	LFRCSEL	Loop filter control settings, Bit 15	W	0

Table 10. Word 3

Bit	Name	Description/Function	Type	Recommended Value
0	C0	Register selection	W	1
1	C1	Register selection	W	1
2	C2	Register selection	W	0
3	LFRCSEL	Loop filter control settings, Bit 16	W	0
4	LFRCSEL	Loop filter control settings, Bit 17	W	0
5	LFRCSEL	Loop filter control settings, Bit 18	W	0
6	ICPSEL	Charge pump current Sel, Bit 0	W	1
7	ICPSEL	Charge pump current Sel, Bit 1	W	1
8	ICPSEL	Charge pump current Sel, Bit 2	W	1
9	ICPSEL	Charge pump current Sel, Bit 3	W	1
10	TITEST2	Reserved	W	0

Table 11. Word 4

Bit	Name	Description/Function	Type	Recommended Value
0	C0	Register selection	W	0
1	C1	Register selection	W	0
2	C2	Register selection	W	1
3	CALWRD	VCO calibration Word, Bit 0	W	0
4	CALWRD	VCO calibration Word, Bit 1	W	0
5	CALWRD	VCO calibration Word, Bit 2	W	0
6	CALWRD	VCO calibration Word, Bit 3	W	0
7	CALWRD	VCO calibration Word, Bit 4	W	0
8	CALWRD	VCO calibration Word, Bit 5	W	0
9	CALOVR	VCO calibration override	W	0
10	ENCAL	Enable VCO calibration	W	1

Table 12. Word 5

Bit	Name	Description/Function	Type	Recommended Value
0	C0	Register selection	W	1
1	C1	Register selection	W	0
2	C2	Register selectiond	W	1
3	TITSTCFG	TI Test Use, Bit 0	W	0
4	TITSTCFG	TI Test Use, Bit 1	W	0
5	TITSTCFG	TI Test Use, Bit 2	W	0
6	TITSTCFG	TI Test Use, Bit 3	W	0
7	Not used		W	0
8	Not used		W	0
9	Not used		W	0
10	Not used		W	0

Appendix A: Test Configurations

Test setups are used to characterize the CDCE421A device in both ac- and dc-termination. Figure 5 through Figure 8 illustrate all four setups used to terminate the clock signal driven by the device under test.

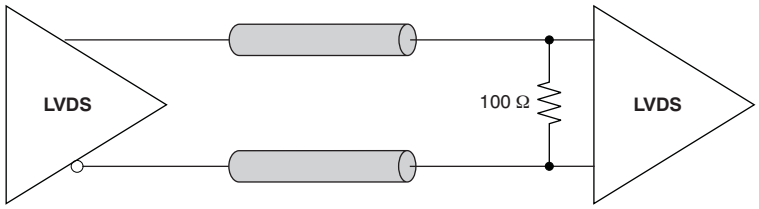


Figure 5. LVDS DC Termination Test Configuration

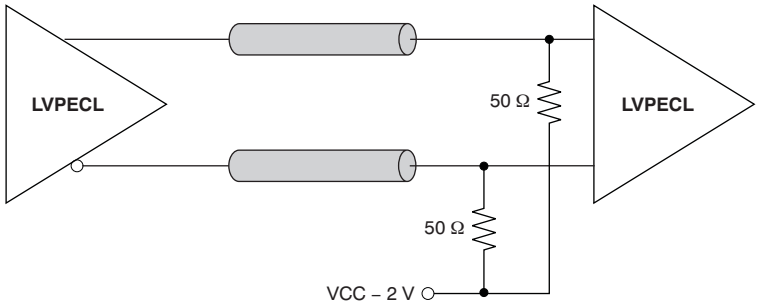


Figure 6. LVPECL DC Termination Test Configuration

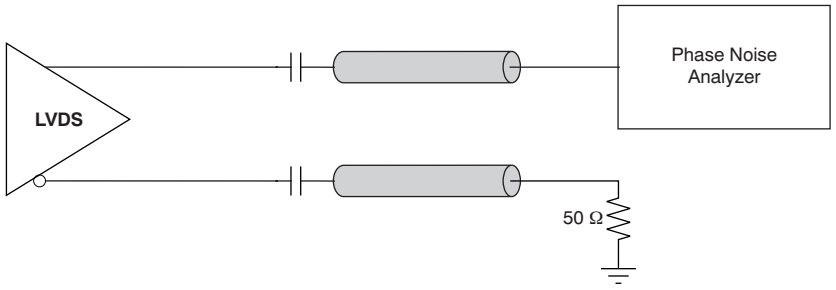


Figure 7. LVDS AC Termination Test Configuration

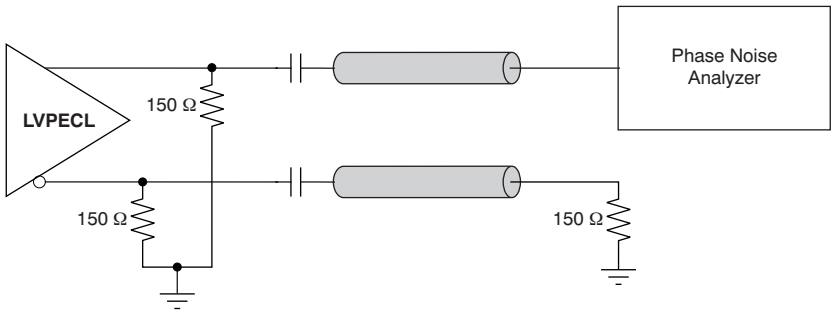


Figure 8. LVPECL AC Termination Test Configuration

Appendix B: Jitter Characteristics in Input Clock Mode

If the CDCE421A is being referenced by an external and cleaner LVCMOS input of 35.42 MHz and 33.33 MHz, respectively, Figure 9 and Table 13 show the SSB phase noise plot and phase noise data of the output at 708 MHz for LVPECL from 100 Hz to 40 MHz from the carrier.

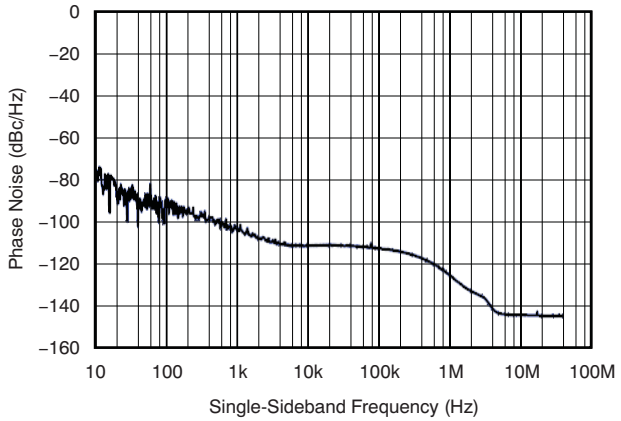


Figure 9. SSB Phase Noise at 708-MHz LVPECL Output with LVCMOS Input of 35.42 MHz

Table 13. Phase Noise Data for LVPECL at 708 MHz with LVCMOS Input of 35.42 MHz(1)

PARAMETER		MIN	TYP	MAX	UNIT
phn100	Phase noise at 100 Hz		–95		dBc/Hz
phn1k	Phase noise at 1 kHz		–105		dBc/Hz
phn10k	Phase noise at 10 kHz		–109		dBc/Hz
phn100k	Phase noise at 100 kHz		–114		dBc/Hz
phn1M	Phase noise at 1 MHz		–126		dBc/Hz
phn10M	Phase noise at 10 MHz		–146		dBc/Hz
phn20M	Phase noise at 20 MHz		–146		dBc/Hz
JRMS	RMS jitter from 10 kHz to 20 MHz		438		fs

(1) Phase noise specifications under following assumptions: input frequency = 35.42 MHz (VCO = 2, prescaler = 3, output divider = 1), output frequency = 708 MHz at LVPECL.

Figure 10 and Table 14 show the SSB phase noise plot and phase noise at 400 MHz for LVDS from 100 Hz to 40 MHz from the carrier. See Figure 7 and Figure 8 for the test configuration setup for LVPECL and LVDS ac termination, respectively.

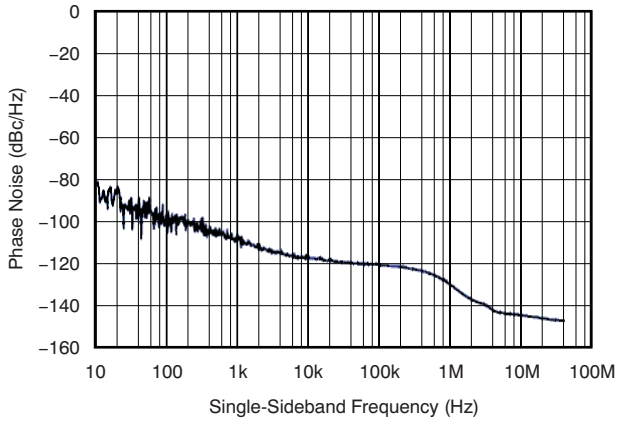


Figure 10. SSB Phase Noise at 400-MHz LVDS Output with LVCMOS Input of 33.33 MHz

Table 14. Phase Noise Data for LVDS at 400 MHz with LVCMOS Input of 33.33 MHz(1)

PARAMETER		MIN	TYP	MAX	UNIT
phn100	Phase noise at 100 Hz		–99		dBc/Hz
phn1k	Phase noise at 1 kHz		–109		dBc/Hz
phn10k	Phase noise at 10 kHz		–119		dBc/Hz
phn100k	Phase noise at 100 kHz		–121		dBc/Hz
phn1M	Phase noise at 1 MHz		–130		dBc/Hz
phn10M	Phase noise at 10 MHz		–147		dBc/Hz
phn20M	Phase noise at 20 MHz		–147		dBc/Hz
JRMS	RMS jitter from 10 kHz to 20 MHz		409		fs

(1) Phase noise specifications under following assumptions: input frequency = 33.33 MHz (VCO = 1, prescaler = 5, output divider = 1), output frequency = 400 MHz at LVDS.

Appendix C: Application Information

CDCE421 User Information

The CDCE421A includes several device enhancements to the CDCE421.

- ***Device Startup***

  The CDCE421A includes an improved device startup circuit that enables the CDCE421A to be used in stand-alone applications (for example, configurations in which the device is not connected to a host system). This design operates over various power-supply ramp time scenarios. For proper operation of the startup circuit, certain register bits must be programmed as specified in Table 15.

Table 15. CDCE421 vs. CDCE421A Register Settings

REGISTER LOCATION	CDCE421	CDCE421A	CDCE421A DATA SHEET REFERENCE
Word 0, Bit 10	Loop filter bias select	TITEST1 (must always be written '1')	Table 7
Word 3, Bit 10	Not used	TITEST2 (must always be written '0')	Table 10

- ***LVDS Output Buffer***

  The CDCE421A incorporates an improved LVDS output buffer. Therefore, the electrical characteristics of the LVDS output buffer on the CDCE421A are different from those of the CDCE421. Refer to the Electrical Characteristics table for the details of the CDCE421A LVDS output buffer.

- ***Product Revision Identification***

  For the product revision identifier bits (bits [2:0]), the value presented by the CDCE421A is '000'. See Table 6 for more details.

Startup Time Estimation

The startup time for the CDCE421A can be estimated based on the parameters defined in Table 16 and illustrated in Figure 11.

Based on these parameters, the CDCE421A startup time limits t_{MAX} and t_{MIN} can be calculated as shown in these equations:

$$t_{MAX} = t_{puh} + t_{rsu} + t_{delay} + t_{VCO\_CAL} + t_{PLL\_LOCK}$$
$$t_{MIN} = t_{pul} + t_{rsu} + t_{delay} + t_{VCO\_CAL} + t_{PLL\_LOCK}$$

Table 16. Timing Definitions: Startup Time Dependencies

Parameter	Definition	Description	Formula/Method of Determination
t_{REF}	Reference Clock Period	The reciprocal of the applied reference frequency (in seconds).	$t_{REF} = \frac{1}{f_{REF}}$
t_{pul}	Power-Up Time (low limit)	Power-supply rise time to low limit of Power On Reset (POR) trip point.	Time required for Power Supply to ramp to 2.27 V.
t_{puh}	Power-Up Time (high limit)	Power-supply rise time to high limit of POR trip point.	Time required for Power Supply to ramp to 2.64 V.
t_{rsu}	Reference Startup Time	After POR releases, the Colpits oscillator is enabled. This startup time is required for the oscillator to generate the requisite signal levels for the delay block to be clocked by the reference input.	Best case: 500 µs Worst case: 800 µs (for a crystal input) 0 s (for an LVCMOS input)
t_{delay}	Delay Time	Internal delay time generated from the reference clock. This delay provides time for the reference oscillator to stabilize.	$t_{delay} = 16384 \times t_{REF}$
t_{VCO_CAL}	VCO Calibration Time	VCO Calibration Time generated from the reference clock. This process selects the operating point for the VCO based on the PLL settings.	$t_{VCO\_CAL} = 550 \times t_{REF}$
t_{PLL_LOCK}	PLL Lock Time	Time required for PLL to lock within ±10 ppm of f_{REF}.	Based on the 400-kHz loop bandwidth, the PLL will settle in 5 τ or 12.5 µs.

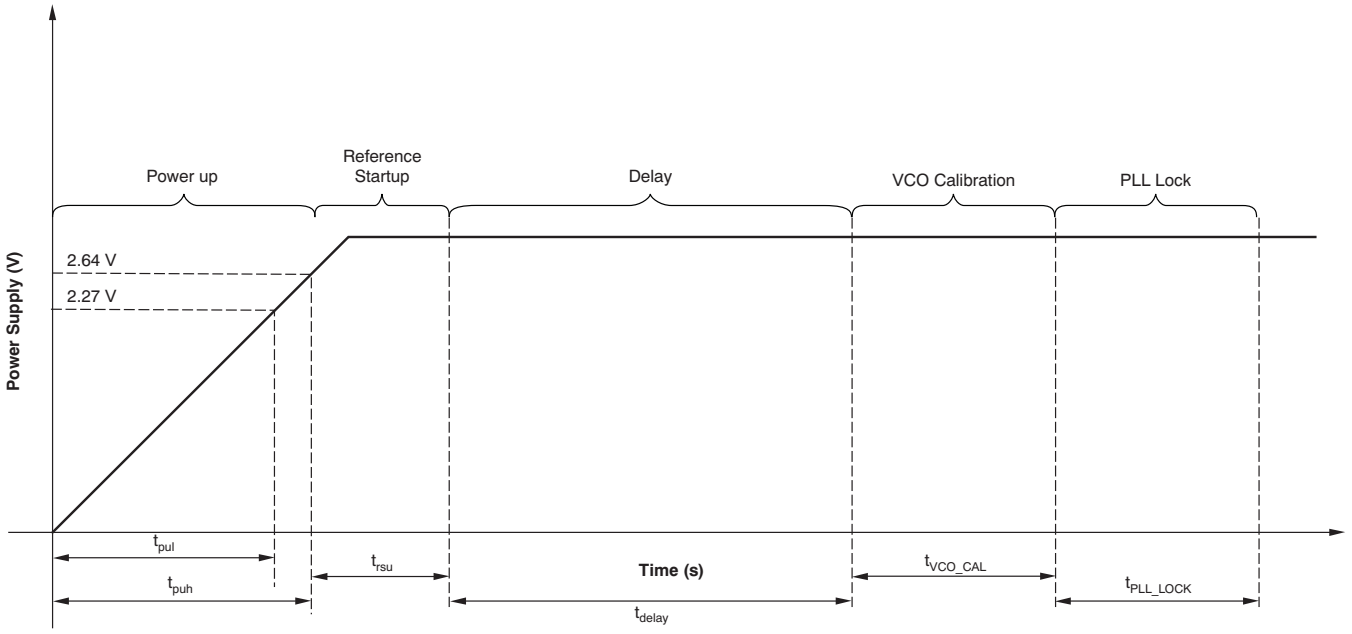


Figure 11. Startup Time Dependencies

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCE421ARGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCE 421A	Samples
CDCE421ARGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCE 421A	Samples
CDCE431YS	ACTIVE	WAFERSALE	YS	0	1	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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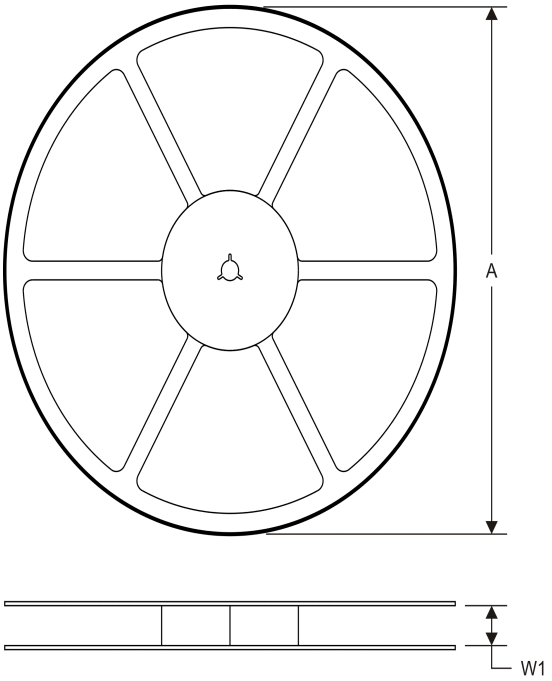
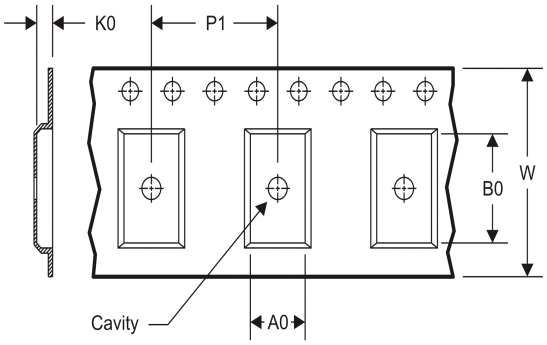
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



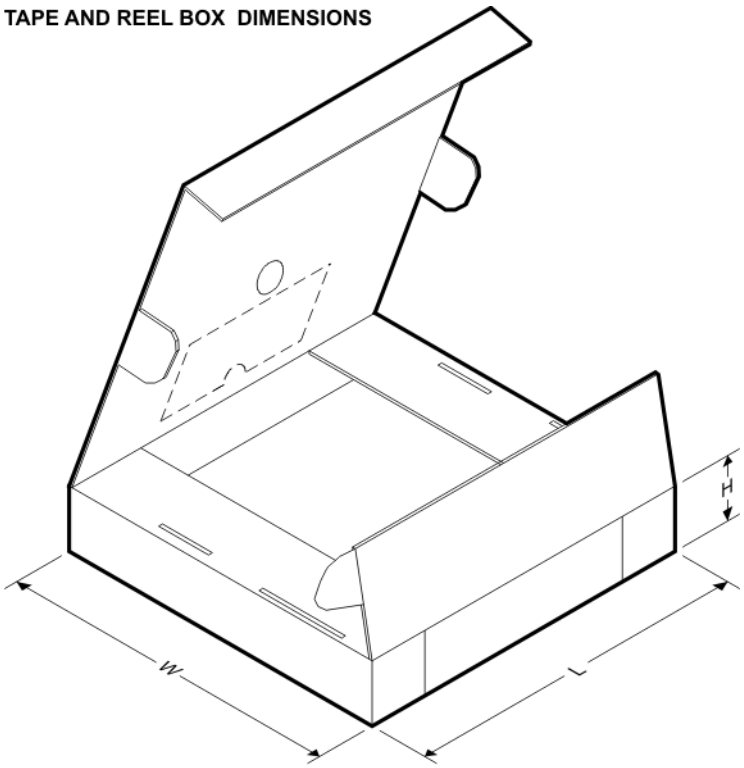
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCE421ARGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
CDCE421ARGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



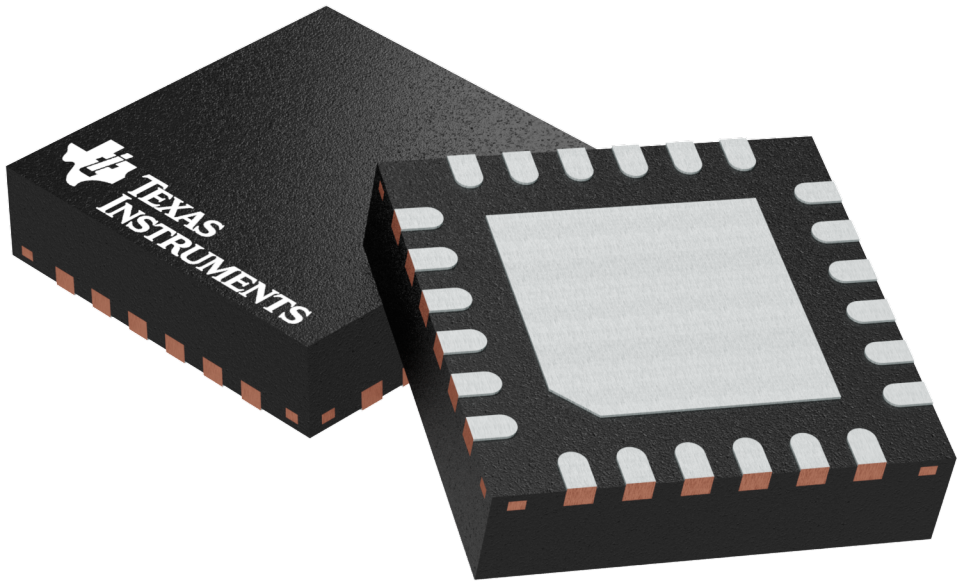
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCE421ARGER	VQFN	RGE	24	3000	367.0	367.0	35.0
CDCE421ARGET	VQFN	RGE	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

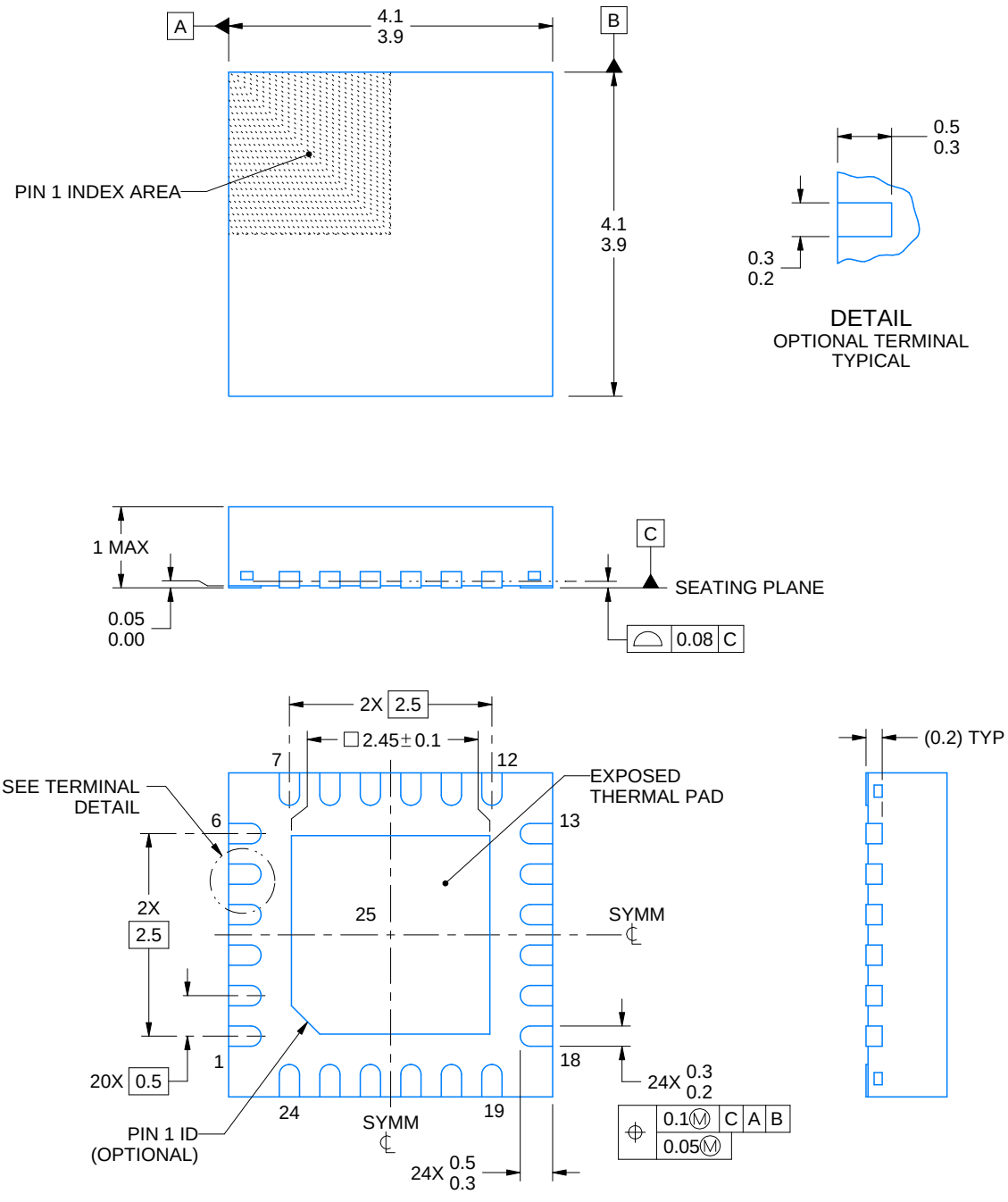
4204104/H

PACKAGE OUTLINE

RGE0024B

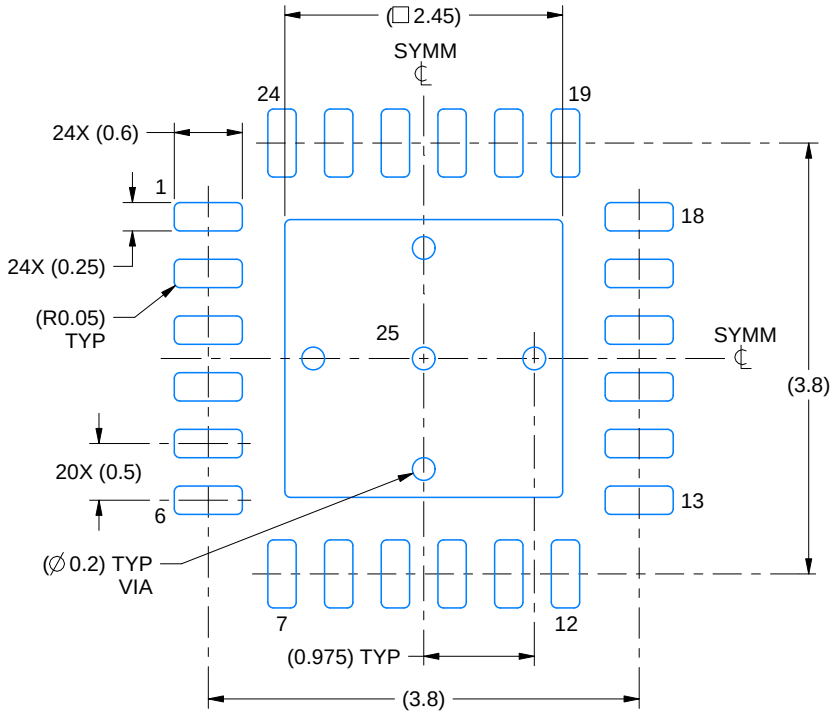
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

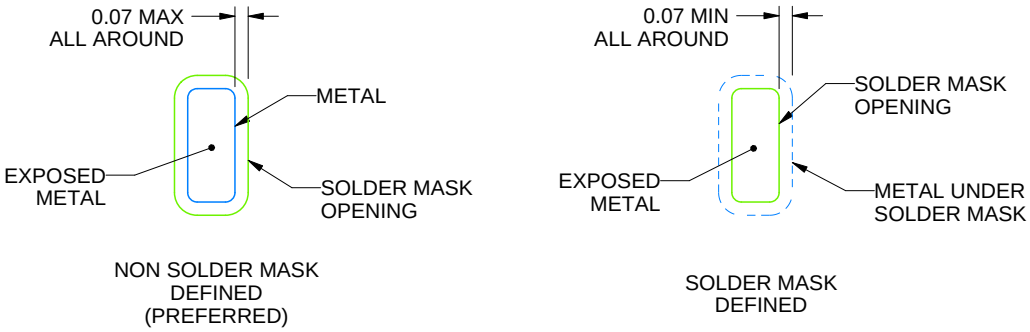


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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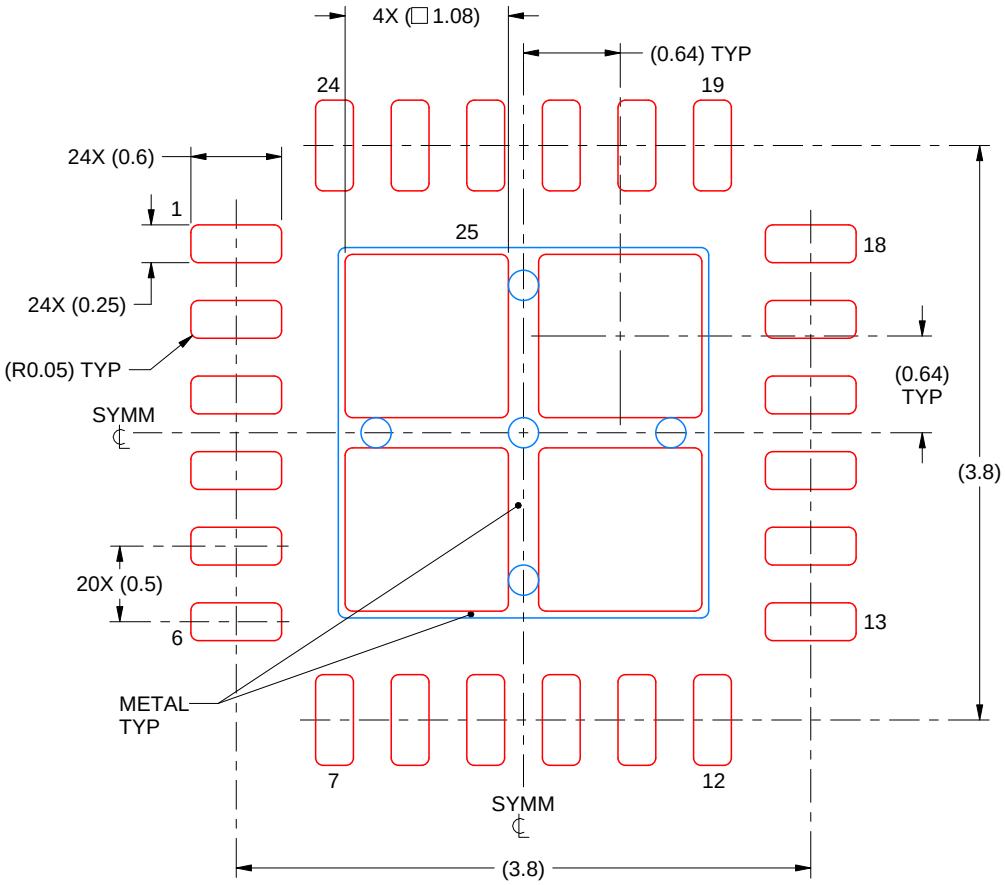
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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