



**THE DATASHEET OF
CC2545RGZT**



System-on-Chip for 2.4-GHz RF Applications

FEATURES

- **RF section**
 - Single-Chip 2.4-GHz RF Transceiver and MCU
 - Supports 250 kbps, 500 kbps, 1 Mbps and 2 Mbps data rates
 - Excellent Link Budget, Enabling Long Range Without External Front-Ends
 - Programmable Output Power up to 4 dBm
 - Excellent Receiver Sensitivity (–90 dBm at 2 Mbps, –98 dBm at 250 kbps)
 - Suitable for Systems Targeting Compliance With Worldwide Radio Frequency Regulations: ETSI EN 300 328 and EN 300 440 Category 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)
 - Accurate RSSI Function
- **Layout**
 - Few External Components
 - Pin Out Suitable for Single Layer PCB Applications
 - Reference Designs Available
 - 48-pin 7-mm × 7-mm QFN (31 General I/O Pins) Package
- **Low Power**
 - Active Mode RX Best Performance: 20.8 mA
 - Active Mode TX (0 dBm): 26.3 mA
 - Power Mode 1 (5 μs Wake-Up): 235 μA
 - Power mode 2 (sleep timer on): 0.9 μA
 - Power mode 3 (External interrupts): 0.4 μA
 - Wide Supply Voltage Range (2V to 3.6V)
 - Full RAM and Register Retention in All Power Modes
- **Microcontroller**
 - High-Performance and Low-Power 8051 Microcontroller Core With Code Prefetch
 - 32-KB Flash Program Memory
 - 1 KB SRAM
 - Hardware Debug Support
 - Extensive Baseband Automation, Including Auto-Acknowledgement and Address Decoding
- **Peripherals**
 - Two-Channel DMA with Access to all Memory Areas and Peripherals
 - General-Purpose Timers (One 16-Bit, Two 8-Bit)
 - Radio Timer, 40-Bit
 - IR Generation Circuitry
 - Several Oscillators:
 - 32MHz XOSC
 - 16MHz RCOSC
 - 32kHz XOSC
 - 32kHz RCOSC
 - 32-kHz Sleep Timer With Capture
 - AES Security Coprocessor
 - UART/SPI/I²C Serial Interface
 - 31 General-Purpose I/O pins (3 × 20-mA Drive Strength, Remaining pins have 4 mA Drive Strength)
 - Watchdog Timer
 - True Random-Number Generator
 - ADC and Analog Comparator

APPLICATIONS

- Proprietary 2.4-GHz Systems
- Human Interface Devices (keyboard, mouse)
- Consumer Electronics



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION

The CC2545 is an optimized system-on-chip (SoC) solution with data rates up to 2Mbps built with low bill-of-material cost. The CC2545 combines the excellent performance of a leading RF transceiver with a single-cycle 8051 compliant CPU, 32-KB in-system programmable flash memory, up to 1-KB RAM, 31 General-Purpose I/O pins and many other powerful features. The CC2545 has efficient power modes with RAM and register retention below 1 μ A, making it highly suited for low-duty-cycle systems where ultralow power consumption is required. Short transition times between operating modes further ensure low energy consumption.

The CC2545 is compatible with the CC2541/CC2543/CC2544. It comes in a 7-mm \times 7-mm QFN48 package, with SPI/UART/I2C interface. The CC2545 comes complete with reference designs from Texas Instruments.

The device targets wireless consumer and HID applications. The CC2545 is tailored for peripheral devices such as wireless keyboards.

For block diagram, see [Figure 7](#)

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|----------------------------|--|------|--------------------|--------------|
| Supply voltage VDD | All supply pins must have the same voltage | -0.3 | 3.9 | V |
| Voltage on any digital pin | | -0.3 | VDD+0.3 \leq 3.9 | V |
| Input RF level | | | 10 | dBm |
| Storage temperature range | | -40 | 125 | $^{\circ}$ C |
| ESD ⁽²⁾ | All pads, according to human-body model, JEDEC STD 22, method A114 (HBM) | | 2000 | V |
| | According to charged-device model, JEDEC STD 22, method C101 (CDM) | | 750 | V |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) CAUTION: ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|---|--|-----|-----|--------------|
| Operating ambient temperature range, T _A | | -40 | 85 | $^{\circ}$ C |
| Operating supply voltage VDD | All supply pins must have same voltage | 2.0 | 3.6 | V |

ELECTRICAL CHARACTERISTICS

 Measured on Texas Instruments CC2545EM reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3.0\text{ V}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--|--|-----|------|-----|---------------|---------------|
| | 2 Mbps, GFSK, 320-kHz deviation | | | | | |
| I_{core} – Core current consumption | RX mode, no peripherals active, low MCU activity | | 20.8 | | mA | |
| | TX mode, 0-dBm output power, no peripherals active, low MCU activity | | 26.3 | | mA | |
| | TX mode, 5-dBm output power, no peripherals active, low MCU activity | | 30.2 | | mA | |
| | Active mode, 16-MHz RCOSC, Low MCU activity | | 3 | | mA | |
| | Active mode, 32-MHz clock frequency, low MCU activity | | 6 | | mA | |
| | Power mode 0, CPU clock halted, all peripherals on, no clock division, 32-MHz crystal selected | | 4.5 | | mA | |
| | Power mode 0, CPU clock halted, all peripherals on, clock division at max (Limits max speed in peripherals except radio), 32-MHz crystal selected | | 3 | | mA | |
| | Power mode 1. Digital regulator ON; 16-MHz RCOSC and 32-MHz crystal oscillator OFF; 32.753-kHz RCOSC, POR, BOD, and sleep timer active; RAM and register retention | | | 235 | | μA |
| | Power mode 2. Digital regulator OFF, 16 MHz RCOSC and 32 MHz crystal oscillator OFF; 32.753 kHz RCOSC, POR and sleep timer active; RAM and register retention | | | 0.9 | | μA |
| | Power mode 3. Digital regulator OFF, no clocks, POR active; RAM and register retention | | | 0.4 | | μA |
| I_{peri} – Peripheral current consumption (Adds to core current I_{core} for each peripheral unit activated) | Timer 1 (16-bit). Timer running, 32-MHz XOSC used | | 90 | | μA | |
| | Radio timer(40 bit). Timer running, 32-MHz XOSC used | | 90 | | μA | |
| | Timer 3 (8-bit). Timer running, 32-MHz XOSC used | | 60 | | μA | |
| | Timer 4 (8-bit). Timer running, 32-MHz XOSC used | | 70 | | μA | |
| | Sleep timer. Including 32.753-kHz RCOSC | | 0.6 | | μA | |

GENERAL CHARACTERISTICS

 Measured on Texas Instruments CC2545EM reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3.0\text{ V}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------------|---|------|-----|------|---------------|
| WAKE-UP AND TIMING | | | | | |
| Power mode 1 → Active | Digital regulator on, 16-MHz RCOSC and 32-MHz crystal oscillator off. Start-up of 16-MHz RCOSC. | | 5 | | μs |
| Power mode 2 or 3 → Active | Digital regulator off, 16 MHz RCOSC and 32 MHz crystal oscillator off. Start-up of regulator and 16 MHz RCOSC. | | 130 | | μs |
| Active → TX or RX | Crystal ESR = 16 Ω . Initially running on 16-MHz RCOSC, with 32-MHz XOSC OFF. | | 500 | | μs |
| | With 32-MHz XOSC initially ON. | | 180 | | μs |
| RX/TX turnaround | RCOSC, with 32MHz XOSC OFF. | | 130 | | μs |
| RADIO PART | | | | | |
| RF frequency range | Programmable in 1-MHz steps | 2379 | | 2496 | MHz |
| Data rates and modulation formats | 2 Mbps, GFSK 320-kHz deviation 2-Mbps, GFSK 500 kHz deviation 1-Mbps, GFSK 250 kHz deviation 1-Mbps, GFSK 160 kHz deviation 500 kbps, MSK 250 kbps, MSK 250 kbps, GSK 160 kHz deviation | | | | |

RF RECEIVE SECTION

Measured on Texas Instruments CC2545EM reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$, and $f_c = 2440\text{ MHz}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|------|-----|-----|------|
| 2 Mbps, GFSK, 320-kHz DEVIATION, 0.1% BER | | | | | |
| Receiver sensitivity | | | -86 | | dBm |
| Saturation | | | -8 | | dBm |
| Co-channel rejection | Wanted signal at -67 dBm | | -13 | | dB |
| In-band blocking rejection | ± 2 -MHz offset, wanted signal at -67 dBm | | -1 | | dB |
| | ± 4 -MHz offset, wanted signal at -67 dBm | | 34 | | |
| | $> \pm 6$ -MHz offset, wanted signal at -67 dBm | | 38 | | |
| Out-of-band blocking rejection | 1-MHz resolution. Wanted signal at -67 dBm, $f < 2\text{ GHz}$ Two exception frequencies with poorer performance | | -32 | | dBm |
| | 1-MHz resolution. Wanted signal at -67 dBm, $2\text{ GHz} > f < 3\text{ GHz}$ Two exception frequencies with poorer performance | | -38 | | |
| | 1-MHz resolution. Wanted signal at -67 dBm, $f > 3\text{ GHz}$ Two exception frequencies with poorer performance | | -12 | | |
| Intermodulation | Wanted signal at -64 dBm, 1 st interferer is CW, 2 nd interferer is GFSK-modulated signal. Offsets of interferers are: 6 and 12 MHz 8 and 16 MHz 10 and 20 MHz | | -43 | | dBm |
| Frequency error tolerance ⁽¹⁾ | Including both initial tolerance and drift. Sensitivity better than -70 dBm. 250 byte payload. | -300 | | 300 | kHz |
| Symbol rate error tolerance ⁽²⁾ | Sensitivity better than -70 dBm. 250 byte payload. | -120 | | 120 | ppm |
| 2 Mbps, GFSK, 500 kHz DEVIATION, 0.1% BER | | | | | |
| Receiver sensitivity | | | -90 | | dBm |
| Saturation | | | -3 | | dBm |
| Co-channel rejection | Wanted signal at -67 dBm | | -10 | | dB |
| In-band blocking rejection | ± 2 MHz offset, wanted signal at -67 dBm | | -3 | | dB |
| | ± 4 MHz offset, wanted signal at -67 dBm | | 36 | | dB |
| | $> \pm 6$ MHz offset, wanted signal at -67 dBm | | 44 | | dB |
| Frequency error tolerance ⁽¹⁾ | Including both initial tolerance and drift. Sensitivity better than -70 dBm. 250 byte payload. | -300 | | 300 | kHz |
| Symbol rate error tolerance ⁽²⁾ | Sensitivity better than -70 dBm. 250 byte payload. | -120 | | 120 | ppm |
| 1 Mbps, GFSK, 250 kHz DEVIATION, 0.1% BER | | | | | |
| Receiver sensitivity | | | -94 | | dBm |
| Saturation | | | 6 | | dBm |
| Co-channel rejection | Wanted signal at -67 dBm | | -7 | | dB |
| In-band blocking rejection | ± 1 MHz offset, wanted signal -67 dBm | | 0 | | dB |
| | ± 2 MHz offset, wanted signal -67 dBm | | 30 | | |
| | ± 3 MHz offset, wanted signal -67 dBm | | 34 | | |
| | $> \pm 5$ MHz offset, wanted signal -67 dBm | | 38 | | |
| Frequency error tolerance | Including both initial tolerance and drift. Sensitivity better than -70 dBm. 250 byte payload. | -250 | | 250 | kHz |
| Symbol rate error tolerance | Sensitivity better than -70 dBm. 250 byte payload. | -80 | | 80 | ppm |

(1) Difference between center frequency of the received RF signal and local oscillator frequency

(2) Difference between incoming symbol rate and the internally generated symbol rate

RF RECEIVE SECTION (continued)

 Measured on Texas Instruments CC2545EM reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$, and $f_c = 2440\text{ MHz}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|------|-----|-----|------|
| 1 Mbps, GFSK, 160 kHz DEVIATION, 0.1% BER | | | | | |
| Receiver sensitivity | | | -91 | | dBm |
| Saturation | | | 6 | | dBm |
| Co-channel rejection | Wanted signal at -67 dBm | | -8 | | dB |
| In band blocking rejection | ± 1 MHz offset, wanted signal at -67 dBm | | 2 | | dB |
| | ± 2 MHz offset, wanted signal at -67 dBm | | 28 | | |
| | ± 3 MHz offset, wanted signal at -67 dBm | | 33 | | |
| | $> \pm 5$ MHz offset, wanted signal at -67 dBm | | 36 | | |
| Frequency error tolerance | Including both initial tolerance and drift, Sensitivity better than -67 dBm | -250 | | 250 | kHz |
| Symbol rate error tolerance | Maximum packet length | -80 | | 80 | ppm |
| 500 kbps, MSK, 0.1% BER | | | | | |
| Receiver sensitivity | | | -98 | | dBm |
| Saturation | | | 6 | | dBm |
| Co-channel rejection | Wanted signal at -67 dBm | | -5 | | dB |
| In band blocking rejection | ± 1 MHz offset, wanted signal at -67 dBm | | 21 | | dB |
| | ± 2 MHz offset, wanted signal at -67 dBm | | 32 | | |
| | $> \pm 2$ MHz offset, wanted signal at -67 dBm | | 33 | | |
| Frequency error tolerance | Including both initial tolerance and drift, Sensitivity better than -67 dBm | -150 | | 150 | kHz |
| Symbol rate error tolerance | Maximum packet length | -60 | | 60 | ppm |
| 250 kbps, GFSK, 160 kHz DEVIATION , 0.1% BER | | | | | |
| Receiver sensitivity | | | -98 | | dBm |
| Saturation | | | 6 | | dBm |
| Co-channel rejection | Wanted signal at -67 dBm | | -2 | | dB |
| In-band blocking rejection | ± 1 MHz offset, wanted signal at -67 dBm | | 22 | | dB |
| | ± 2 MHz offset, wanted signal at -67 dBm | | 32 | | |
| | $> \pm 2$ MHz offset, wanted signal at -67 dBm | | 32 | | |
| Frequency error tolerance | Including both initial tolerance and drift, Sensitivity better than -67 dBm | -150 | | 150 | kHz |
| Symbol rate error tolerance | Maximum packet length | -60 | | 60 | ppm |
| 250 kbps, MSK, 0.1% BER | | | | | |
| Receiver sensitivity | | | -98 | | dBm |
| Saturation | | | 6 | | dBm |
| Co-channel rejection | Wanted signal at -67 dBm | | -5 | | dB |
| In-band blocking rejection | ± 1 MHz offset, wanted signal at -67 dBm | | 21 | | dB |
| | ± 2 MHz offset, wanted signal at -67 dBm | | 32 | | |
| | > 2 MHz offset, wanted signal at -67 dBm | | 33 | | |
| Frequency error tolerance | Including both initial tolerance and drift, Sensitivity better than -67 dBm | -150 | | 150 | kHz |
| Symbol rate error tolerance | Maximum packet length | -60 | | 60 | ppm |
| ALL RATES/FORMATS | | | | | |
| Spurious emission in RX. Conducted measurement | $f < 1\text{ GHz}$ | | -67 | | dBm |
| Spurious emission in RX. Conducted measurement | $f > 1\text{ GHz}$ | | -60 | | dBm |

RF TRANSMIT SECTION

Measured on Texas Instruments CC2545EM reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$, and $f_C = 2440\text{ MHz}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|-----|-----|-----|------|
| Output power, maximum setting | Delivered to a single-ended 50- Ω load through a balun using maximum recommended output power setting. | | 5 | | dBm |
| Output power, minimum setting | Delivered to a single-ended 50- Ω load through a balun using minimum recommended output power setting. | | -20 | | dBm |
| Programmable output power range | Delivered to a single-ended 50- Ω load through a balun. | | 25 | | dB |
| Spurious emission in TX. Conducted measurement | $f < 1\text{ GHz}$ | | -46 | | dBm |
| | $f > 1\text{ GHz}$ | | -44 | | dBm |
| | Suitable for Systems Targeting Compliance With Worldwide Radio Frequency Regulations: ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan) | | | | |

Use a simple LC filter (1.6nH and 1.8pF in parallel to ground) to pass ETSI conducted requirements below 1GHz in restricted bands. For radiated measurements low antenna gain for these frequencies (depending on antenna design) can achieve the same attenuation of these low frequency components (see EM reference design).

32-MHz CRYSTAL OSCILLATOR

Measured on Texas Instruments CC2545EM reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-------------------|------|----------------|----------|
| Crystal frequency | | | 32 | | MHz |
| Crystal frequency accuracy requirement | 250 kbps and 500 kbps data rates 1 Mbps data rate 2 Mbps data rate | -30 -40 -60 | | 30 40 60 | ppm |
| Equivalent series resistance | | 6 | | 60 | Ω |
| Crystal shunt capacitance | | 1 | | 7 | pF |
| Crystal load capacitance | | 10 | | 16 | pF |
| Start-up time | | | 0.25 | | ms |
| Power-down guard time | The crystal oscillator must be in power down for a guard time before it is used again. This requirement is valid for all modes of operation. The need for power-down guard time can vary with crystal type and load. | 3 | | | ms |

32.768-kHz CRYSTAL OSCILLATOR

Measured on Texas Instruments CC2545EM reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------|------|--------|------|----------|
| Crystal frequency | | | 32.768 | | kHz |
| Crystal frequency accuracy requirement ⁽¹⁾ | | -100 | | +100 | ppm |
| Equivalent series resistance | | | 40 | 130 | Ω |
| Crystal shunt capacitance | | | 0.9 | 2 | pF |
| Crystal load capacitance | | | 12 | 16 | pF |
| Start-up time | | | 0.4 | | s |

(1) Crystal frequency accuracy requirement is highly dependent on application. Higher accuracy enables more accurate duty-cycling which in turn will reduce current consumption. The chip can handle much less accurate crystals.

32-kHz RC OSCILLATOR

Measured on Texas Instruments CC2545EM reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------------|-----------------|-----|-------------|-----|---------------------|
| Calibrated frequency | | | 32.753 | | kHz |
| Frequency accuracy after calibration | | | $\pm 0.2\%$ | | |
| Temperature coefficient | | | 0.4 | | $\%/^\circ\text{C}$ |
| Supply-voltage coefficient | | | 3 | | $\%/V$ |
| Calibration time | | | 2 | | ms |

16-MHz RC OSCILLATOR

Measured on Texas Instruments CC2545EM reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------------|-----------------|-----|-------------|-----|---------------|
| Calibrated frequency | | | 16 | | MHz |
| Uncalibrated frequency accuracy | | | $\pm 18\%$ | | |
| Frequency accuracy after calibration | | | $\pm 0.6\%$ | | |
| Start-up time | | | 10 | | μs |
| Initial calibration time | | | 50 | | μs |

RSSI CHARACTERISTICS

Measured on Texas Instruments CC2545EM reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$, unless otherwise noted.

| 2Mbps, GFSK, 320-kHz Deviation, 0.1% BER and 2 Mbps, GFSK, 500-kHz Deviation, 0.1% BER | | | | |
|--|-------------------------------|--|---------|-----|
| RSSI range ⁽¹⁾ | Reduced gain by AC algorithm | | 64 | dB |
| | High gain by AGC algorithm | | 64 | |
| RSSI offset ⁽¹⁾ | Reduced gain by AGC algorithm | | 79 | dBm |
| | High gain by AGC algorithm | | 99 | |
| Absolute uncalibrated accuracy ⁽¹⁾ | | | ± 3 | dB |
| Step size (LSB value) | | | 1 | dB |
| All Other Rates/Formats | | | | |
| RSSI range ⁽¹⁾ | | | 64 | dB |
| RSSI offset ⁽¹⁾ | | | 99 | dBm |
| Absolute uncalibrated accuracy | | | ± 3 | dB |
| Step size (LSB value) | | | 1 | dB |

(1) Assuming CC2545 EM reference design. Other RF designs give an offset from the reported value.

FREQUENCY SYNTHESIZER CHARACTERISTICS

Measured on Texas Instruments CC2545EM reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|------------------------------------|-----|------|-----|--------|
| Phase noise, unmodulated carrier | At $\pm 1\text{ MHz}$ from carrier | | -112 | | dBc/Hz |
| | At $\pm 3\text{ MHz}$ from carrier | | -119 | | |
| | At $\pm 5\text{ MHz}$ from carrier | | -122 | | |

ANALOG TEMPERATURE SENSOR

Measured on Texas Instruments CC2545EM reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$ unless otherwise noted

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------------|--|-----|------|-----|---------|
| Output | Measured using integrated ADC, internal band-gap voltage reference, and maximum resolution | | 1480 | | 12-bit |
| Temperature coefficient | | | 4.5 | | / 0.1°C |
| Voltage coefficient | | | 1 | | / 0.1V |
| Initial accuracy without calibration | | | ±10 | | °C |
| Accuracy using 1-point calibration | | | ±5 | | °C |
| Current consumption when enabled | | | 0.5 | | mA |

COMPARATOR CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$. All measurement results are obtained using the CC2545 reference designs, post-calibration.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|-----------------|-----|------|-----|------------------------------|
| Common-mode maximum voltage | | | VDD | | V |
| Common-mode minimum voltage | | | -0.3 | | |
| Input offset voltage | | | 1 | | mV |
| Offset vs temperature | | | 16 | | $\mu\text{V}/^\circ\text{C}$ |
| Offset vs operating voltage | | | 4 | | mV/V |
| Supply current | | | 230 | | nA |
| Hysteresis | | | 0.15 | | mV |

ADC CHARACTERISTICS

 $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|---|--|-----|-------|-----|---------------|
| | Input voltage | VDD is voltage on AVDD5 pin | 0 | | VDD | V |
| | External reference voltage | VDD is voltage on AVDD5 pin | 0 | | VDD | V |
| | External reference voltage differential | VDD is voltage on AVDD5 pin | 0 | | VDD | V |
| | Input resistance, signal | Simulated using 4-MHz clock speed | | 197 | | k Ω |
| | Full-scale signal ⁽¹⁾ | Peak-to-peak, defines 0 dBFS | | 2.97 | | V |
| ENOB ⁽¹⁾ | Effective number of bits | Single-ended input, 7-bit setting | | 5.7 | | bits |
| | | Single-ended input, 9-bit setting | | 7.5 | | |
| | | Single-ended input, 10-bit setting | | 9.3 | | |
| | | Single-ended input, 12-bit setting | | 10.3 | | |
| | | Differential input, 7-bit setting | | 6.5 | | |
| | | Differential input, 9-bit setting | | 8.3 | | |
| | | Differential input, 10-bit setting | | 10 | | |
| | | Differential input, 12-bit setting | | 11.5 | | |
| | | 10-bit setting, clocked by RCOSC | | 9.7 | | |
| | | 12-bit setting, clocked by RCOSC | | 10.9 | | |
| | Useful power bandwidth | 7-bit setting, both single and differential | | 0–20 | | kHz |
| THD | Total harmonic distortion | Single ended input, 12-bit setting, –6 dBFS ⁽¹⁾ | | –75.2 | | dB |
| | | Differential input, 12-bit setting, –6 dBFS ⁽¹⁾ | | –86.6 | | |
| | Signal to nonharmonic ratio | Single-ended input, 12-bit setting ⁽¹⁾ | | 70.2 | | dB |
| | | Differential input, 12-bit setting ⁽¹⁾ | | 79.3 | | |
| | | Single-ended input, 12-bit setting, –6 dBFS ⁽¹⁾ | | 78.8 | | |
| | | Differential input, 12-bit setting, –6 dBFS ⁽¹⁾ | | 88.9 | | |
| CMRR | Common-mode rejection ratio | Differential input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution | | >84 | | dB |
| | Crosstalk | Single ended input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution | | >84 | | dB |
| | Offset | Midscale | | –3 | | mV |
| | Gain error | | | 0.68% | | |
| DNL | Differential nonlinearity | 12-bit setting, mean ⁽¹⁾ | | 0.05 | | LSB |
| | | 12-bit setting, maximum ⁽¹⁾ | | 0.9 | | |
| INL | Integral nonlinearity | 12-bit setting, mean ⁽¹⁾ | | 4.6 | | LSB |
| | | 12-bit setting, maximum ⁽¹⁾ | | 13.3 | | |
| | | 12-bit setting, mean, clocked by RCOSC | | 10 | | |
| | | 12-bit setting, max, clocked by RCOSC | | 29 | | |
| SINAD (–THD+N) | Signal-to-noise-and-distortion | Single ended input, 7-bit setting ⁽¹⁾ | | 35.4 | | dB |
| | | Single ended input, 9-bit setting ⁽¹⁾ | | 46.8 | | |
| | | Single ended input, 10-bit setting ⁽¹⁾ | | 57.5 | | |
| | | Single ended input, 12-bit setting ⁽¹⁾ | | 66.6 | | |
| | | Differential input, 7-bit setting ⁽¹⁾ | | 40.7 | | |
| | | Differential input, 9-bit setting ⁽¹⁾ | | 51.6 | | |
| | | Differential input, 10-bit setting ⁽¹⁾ | | 61.8 | | |
| | | Differential input, 12-bit setting ⁽¹⁾ | | 70.8 | | |
| | Conversion time | 7-bit setting | | 20 | | μs |
| | | 9-bit setting | | 36 | | |
| | | 10-bit setting | | 68 | | |
| | | 12-bit setting | | 132 | | |

(1) Measured with 300-Hz sine-wave input and VDD as reference.

ADC CHARACTERISTICS (continued)

T_A = 25°C and VDD = 3 V

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------|-----|------|-----|---------|
| Power consumption | | | 1.2 | | mA |
| Internal reference VDD coefficient | | | 4 | | mV/V |
| Internal reference temperature coefficient | | | 0.4 | | mV/10°C |
| Internal reference voltage | | | 1.15 | | V |

DC CHARACTERISTICS

Measured on Texas Instruments CC2545EM reference design with T_A = 25°C, VDD = 3.0 V, unless otherwise noted.⁽¹⁾

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------|-------------------|-----|-----|-----|------|
| Logic-0 input voltage | | | | 0.5 | V |
| Logic-1 input voltage | | 2.5 | | | V |
| Logic-0 input current | | -50 | | 50 | nA |
| Logic-1 input current | | -50 | | 50 | nA |
| I/O pin pullup and pulldown resistors | | | 20 | | kΩ |
| Logic-0 output voltage 4-mA pins | Output load 4 mA | | | 0.5 | V |
| Logic-1 output voltage 4-mA pins | Output load 4 mA | 2.4 | | | V |
| Logic-0 output voltage 20-mA pins | Output load 20 mA | | | 0.5 | V |
| Logic-1 output voltage, 20-mA pins | Output load 20 mA | 2.4 | | | V |

(1) Note that only two of the three 20-mA pins can drive in the same direction at the same time, and toggle at the same time.

CONTROL INPUT AC CHARACTERISTICS

T_A = -40°C to 85°C, VDD = 2 V to 3.6 V.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|-----|-----|-----|------|
| System clock, f _{SYSCLK} t _{SYSCLK} = 1/ f _{SYSCLK} | The undivided system clock is 32 MHz when crystal oscillator is used. The undivided system clock is 16 MHz when calibrated 16-MHz RC oscillator is used. | | 16 | 32 | MHz |
| RESET_N low duration | See item 1, Figure 1. This is the shortest pulse that is recognized as a complete reset pin request. Note that shorter pulses may be recognized but do not lead to complete reset of all modules within the chip. | | 1 | | μs |
| Interrupt pulse duration | See item 2, Figure 1. This is the shortest pulse that is recognized as an interrupt request. | | 20 | | ns |

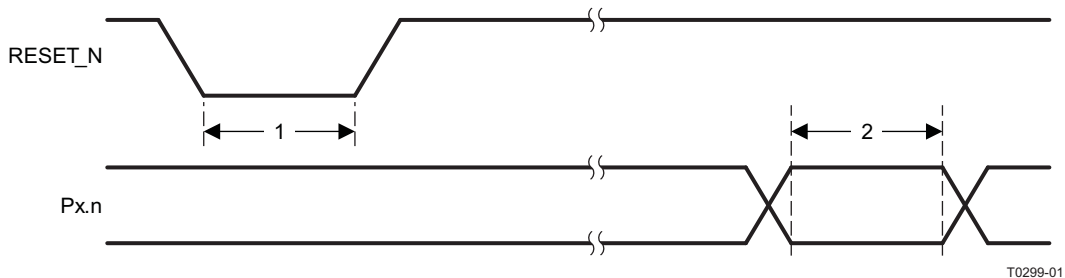
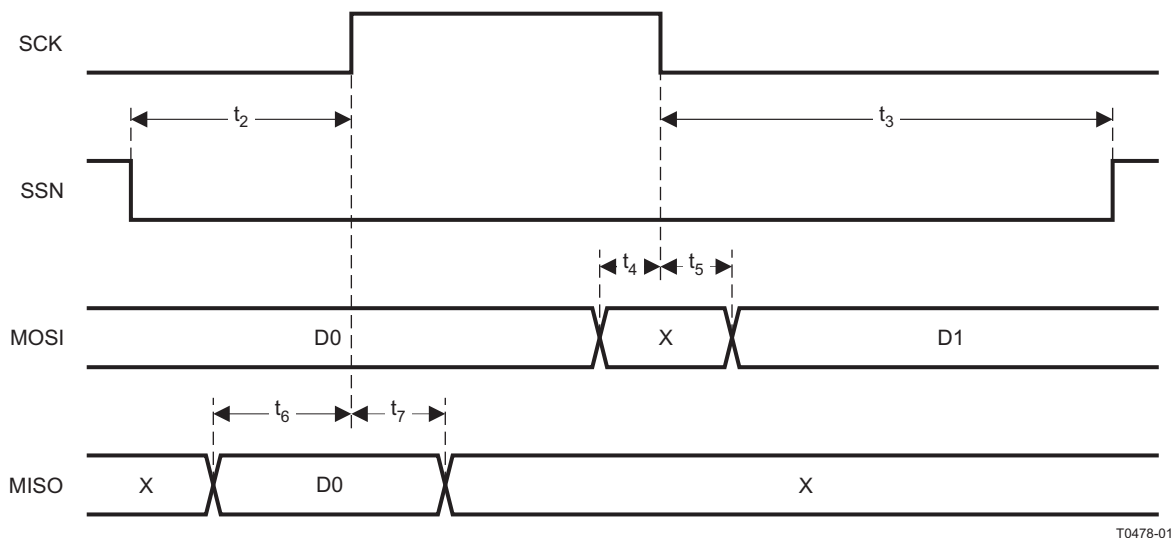


Figure 1. Control Input AC Characteristics

SPI AC CHARACTERISTICS

T_A = -40°C to 85°C, VDD = 2 V to 3.6 V

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|----------------------|-----|-----|-----|------|
| t ₁ SCK period | Master, RX and TX | 250 | | | ns |
| | Slave, RX and TX | 250 | | | |
| SCK duty cycle | Master | | 50% | | |
| t ₂ SSN low to SCK, Figure 2 and Figure 3 | Master | 63 | | | ns |
| | Slave | 63 | | | |
| t ₃ SCK to SSN high | Master | 63 | | | ns |
| | Slave | 63 | | | |
| t ₄ MOSI early out | Master, load = 10 pF | | | 7 | ns |
| t ₅ MOSI late out | Master, load = 10 pF | | | 10 | ns |
| t ₆ MISO setup | Master | 90 | | | ns |
| t ₇ MISO hold | Master | 10 | | | ns |
| SCK duty cycle | Slave | | 50% | | ns |
| t ₁₀ MOSI setup | Slave | 35 | | | ns |
| t ₁₁ MOSI hold | Slave | 10 | | | ns |
| t ₈ MISO early out | Slave, load = 10 pF | | | 0 | ns |
| t ₉ MISO late out | Slave, load = 10 pF | | | 95 | ns |
| Operating frequency | Master, TX only | | | 8 | MHz |
| | Master, RX and TX | | | 4 | |
| | Slave, RX only | | | 8 | |
| | Slave, RX and TX | | | 4 | |



T0478-01

Figure 2. SPI Master AC Characteristics

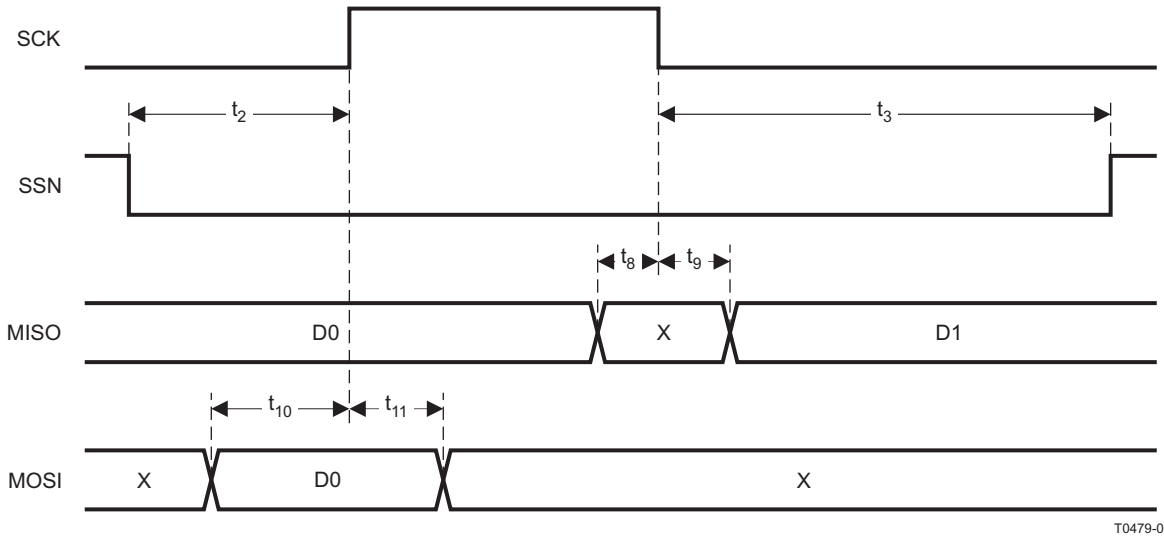


Figure 3. SPI Slave AC Characteristics

T0479-01

DEBUG INTERFACE AC CHARACTERISTICS

$T_A = -40^{\circ}\text{C}$ to 85°C , $V_{DD} = 2\text{ V}$ to 3.6 V

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|-----|-----|-----|------|
| $f_{\text{clk_dbg}}$ | Debug clock frequency (see Figure 4) | | | 12 | MHz |
| t_1 | Allowed high pulse on clock (see Figure 4) | 35 | | | ns |
| t_2 | Allowed low pulse on clock (see Figure 4) | 35 | | | ns |
| t_3 | EXT_RESET_N low to first falling edge on debug clock (see Figure 5) | 167 | | | ns |
| t_4 | Falling edge on clock to EXT_RESET_N high (see Figure 5) | 83 | | | ns |
| t_5 | EXT_RESET_N high to first debug command (see Figure 5) | 83 | | | ns |
| t_6 | Debug data setup (see Figure 6) | 2 | | | ns |
| t_7 | Debug data hold (see Figure 6) | 4 | | | ns |
| t_8 | Clock-to-data delay (see Figure 6) | | | 30 | ns |

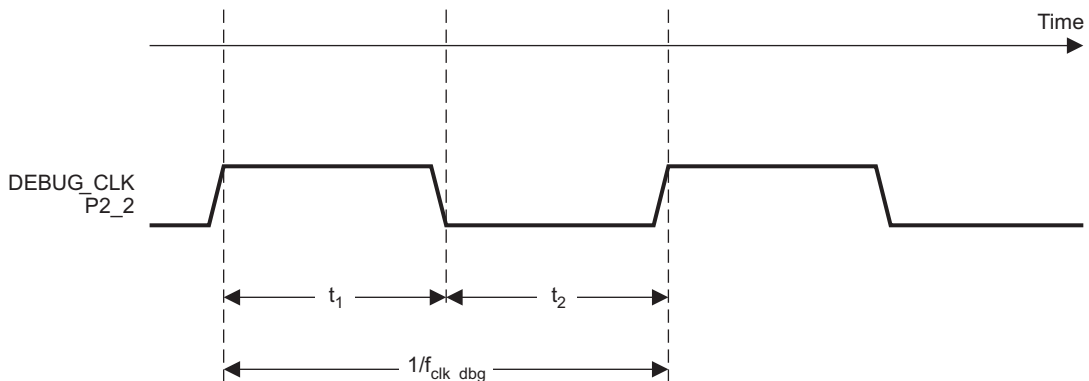
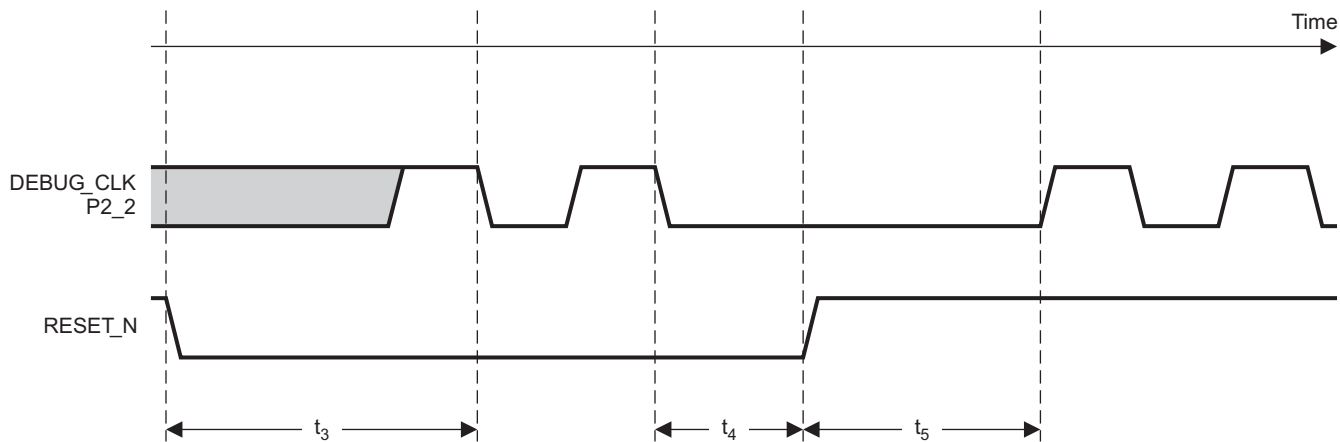


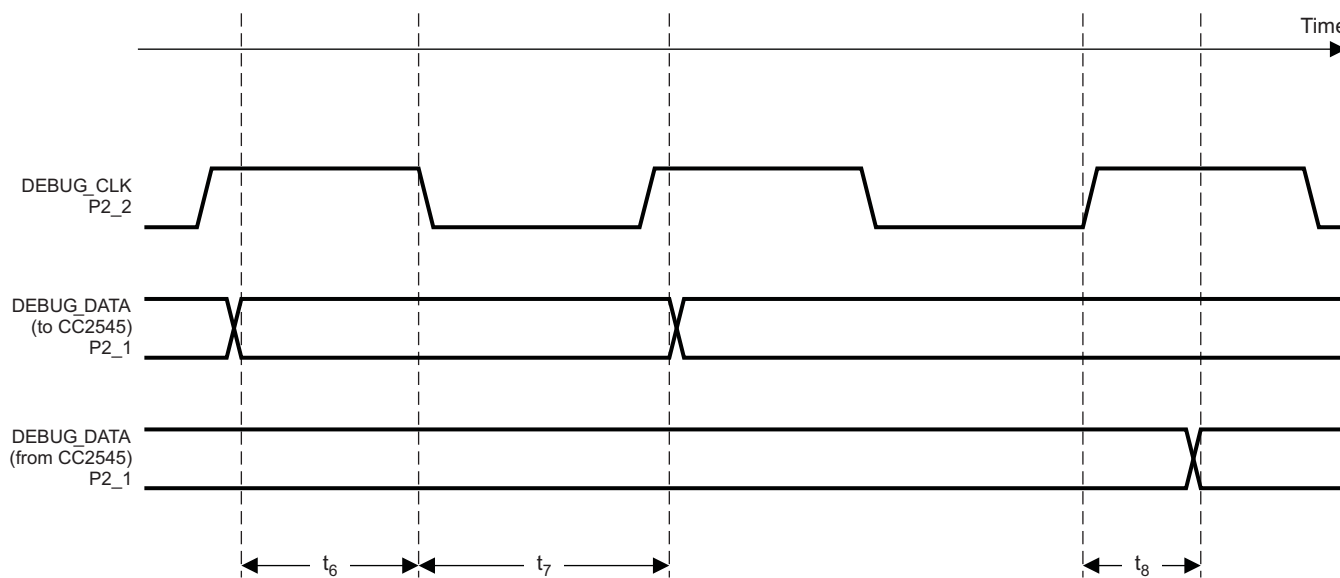
Figure 4. Debug Clock – Basic Timing

T0436-01



T0437-01

Figure 5. Debug Enable Timing



T0438-03

Figure 6. Data Setup and Hold Timing

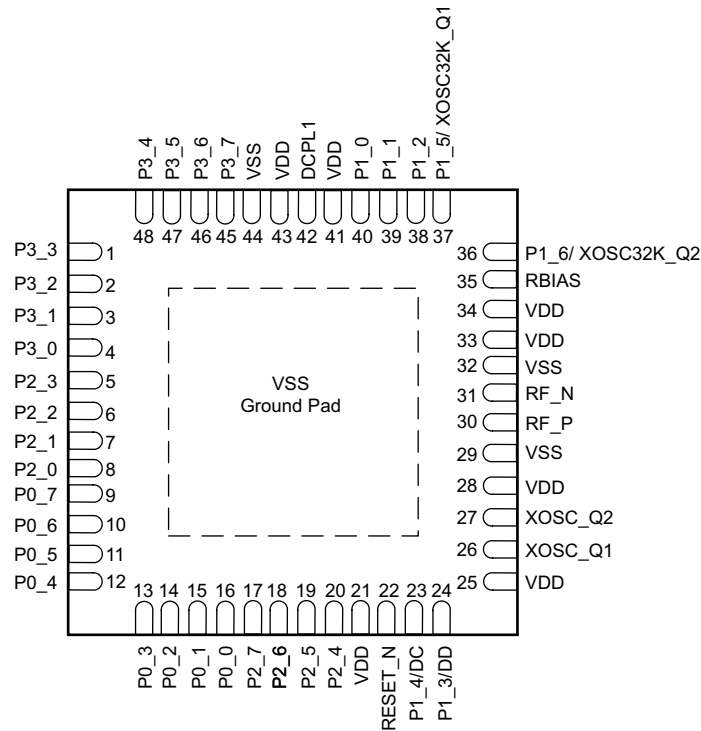
TIMER INPUTS AC CHARACTERISTICS

T_A = -40°C to 85°C, VDD = 2 V to 3.6 V

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|---|-----|-----|-----|--------------------|
| Input capture pulse duration | Synchronizers determine the shortest input pulse that can be recognized. The synchronizers operate at the current system clock rate (16 MHz or 32 MHz). | 1.5 | | | t _{SYCLK} |

DEVICE INFORMATION

**RGZ PACKAGE
(TOP VIEW)**



NOTE: The exposed ground pad must be connected to a solid ground plane; this is the main ground connection for the chip.

Table 1. Pin Description Table

| NAME | PIN | PIN TYPE | DESCRIPTION |
|------|-----|-------------|-------------|
| P3_3 | 1 | Digital I/O | Port 3.3 |
| P3_2 | 2 | Digital I/O | Port 3.2 |
| P3_1 | 3 | Digital I/O | Port 3.1 |
| P3_0 | 4 | Digital I/O | Port 3.0 |
| P2_3 | 5 | Digital I/O | Port 2.3 |
| P2_2 | 6 | Digital I/O | Port 2.2 |
| P2_1 | 7 | Digital I/O | Port 2.1 |
| P2_0 | 8 | Digital I/O | Port 2.0 |
| P0_7 | 9 | Digital I/O | Port 0.7 |
| P0_6 | 10 | Digital I/O | Port 0.6 |
| P0_5 | 11 | Digital I/O | Port 0.5 |
| P0_4 | 12 | Digital I/O | Port 0.4 |
| P0_3 | 13 | Digital I/O | Port 0.3 |
| P0_2 | 14 | Digital I/O | Port 0.2 |
| P0_1 | 15 | Digital I/O | Port 0.1 |
| P0_0 | 16 | Digital I/O | Port 0.0 |
| P2_7 | 17 | Digital I/O | Port 2.7 |
| P2_6 | 18 | Digital I/O | Port 2.6 |
| P2_5 | 19 | Digital I/O | Port 2.5 |
| P2_4 | 20 | Digital I/O | Port 2.4 |

Table 1. Pin Description Table (continued)

| NAME | PIN | PIN TYPE | DESCRIPTION |
|-------------------------|------------|--------------------------|--|
| VDD | 21 | Power (analog) | 2-V-3.6V analog power-supply connection |
| RESET_N | 22 | Digital input | Reset, active-low |
| P1_4/DC | 23 | Digital I/O / Debug | Port 1.4/Debug |
| P1_3/DD | 24 | Digital I/O / Debug | Port 1.3/Debug |
| VDD | 25 | Power (analog) | 2-V-3.6V analog power-supply connection |
| XOSC_Q1 | 26 | Analog I/O | 32-MHz crystal oscillator pin 1 or external-clock input |
| XOSC_Q2 | 27 | Analog I/O | 32-MHz crystal oscillator pin 2 |
| VDD | 28 | Power (analog) | 2-V-3.6V analog power-supply connection |
| VSS | 29 | Unused pin | Connect to ground |
| RF_P | 30 | RF I/O | Positive RF input signal to LNA during RX Positive RF output signal from PA during TX |
| RF_N | 31 | RF I/O | Negative RF input signal to LNA during RX Negative RF output signal from PA during TX |
| VSS | 32 | Unused pin | Connect to ground |
| VDD | 33 | Power (analog) | 2-V-3.6V analog power-supply connection |
| VDD | 34 | Power (analog) | 2-V-3.6V analog power-supply connection |
| RBIAS | 35 | Analog I/O | External precision bias resistor for reference current |
| P1_6/ XOSC32K_ Q2 | 36 | Digital I/O / Analog I/O | Port 1.6/32.768-kHz XOSC |
| P1_5/ XOSC32k_ Q1 | 37 | Digital I/O / Analog I/O | Port 1.5/32.768-kHz XOSC |
| P1_2 | 38 | Digital I/O | Port 1.2, 20mA |
| P1_1 | 39 | Digital I/O | Port 1.1, 20mA |
| P1_0 | 40 | Digital I/O | Port 1.0, 20mA |
| VDD | 41 | Power (analog) | 2-V-3.6V analog power-supply connection |
| DCPL1 | 42 | Power (digital) | 1.8-V digital power-supply decoupling. Do not use for supplying external circuits. |
| VDD | 43 | Power (analog) | 2-V-3.6V analog power-supply connection |
| VSS | 44 | Unused pin | Connect to ground |
| P3_7 | 45 | Digital I/O | Port 3.7 |
| P3_6 | 46 | Digital I/O | Port 3.6 |
| P3_5 | 47 | Digital I/O | Port 3.5 |
| P3_4 | 48 | Digital I/O | Port 3.4 |
| VSS | Ground Pad | Ground | Must be connected to solid ground as this is the main ground connection for the chip. See Pinout Diagram . |

BLOCK DIAGRAM

A block diagram of the CC2545 is shown in Figure 7. The modules can be roughly divided into one of three categories: CPU-related modules; modules related to power, test, and clock distribution; and radio-related modules. In the following subsections, a short description of each module is given. See CC2543/44/45 User's Guide (SWRU283) for more details.

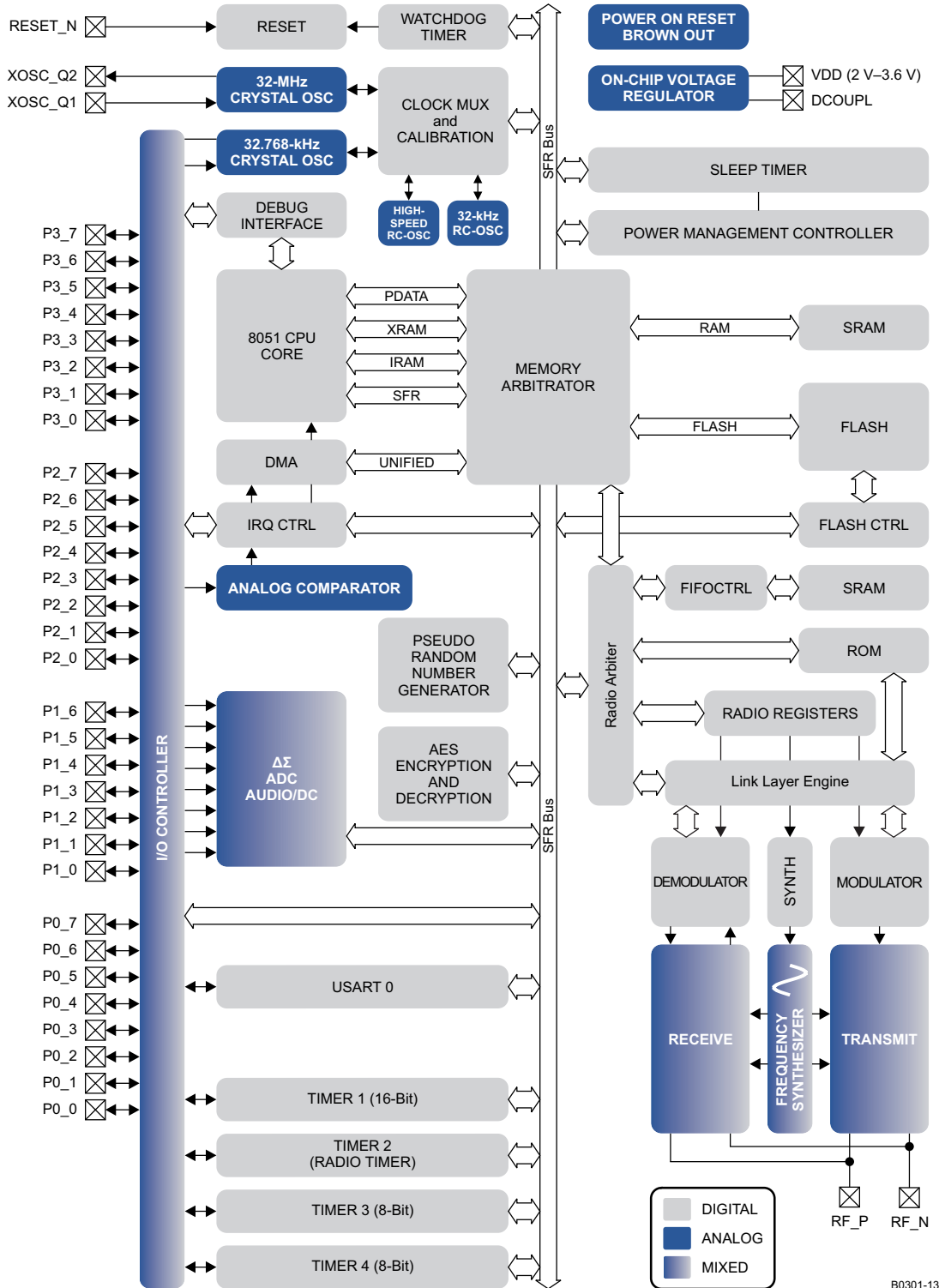


Figure 7. CC2545 Block Diagram

BLOCK DESCRIPTIONS

CPU and Memory

The **8051 CPU core** is a single-cycle 8051-compatible core. It has three different memory access busses (SFR, DATA, and CODE/XDATA), a debug interface, and an 15-input extended interrupt unit.

The **memory arbiter** is at the heart of the system, as it connects the CPU and DMA controller with the physical memories and all peripherals through the SFR bus. The memory arbiter has four memory-access points, access of which can map to one of three physical memories: an SRAM, flash memory, and XREG/SFR registers. It is responsible for performing arbitration and sequencing between simultaneous memory accesses to the same physical memory.

The **SFR bus** is drawn conceptually in [Figure 7](#) as a common bus that connects all hardware peripherals to the memory arbiter. The SFR bus in the block diagram also provides access to the radio registers in the radio register bank, even though these are indeed mapped into XDATA memory space.

The **1-KB SRAM** maps to the DATA memory space and to parts of the XDATA memory spaces.

The **18-KB/32-KB flash block** provides in-circuit programmable non-volatile program memory for the device, and maps into the CODE and XDATA memory spaces.

Peripherals

Writing to the flash block is performed through a **flash controller** that allows page-wise erasure and 4-bitwise programming. See User Guide for details on the flash controller.

A versatile two-channel **DMA controller** is available in the system, accesses memory using the XDATA memory space, and thus has access to all physical memories. Each channel (trigger, priority, transfer mode, addressing mode, source and destination pointers, and transfer count) is configured with DMA descriptors that can be located anywhere in memory. Many of the hardware peripherals (AES core, flash controller, USART, timers, etc.) can be used with the DMA controller for efficient operation by performing data transfers between a single SFR or XREG address and flash/SRAM.

The **interrupt controller** services a total of 17 interrupt sources, divided into six interrupt groups, each of which is associated with one of four interrupt priorities. Any interrupt service request is serviced also when the device is in idle mode by going back to active mode. Some interrupts can also wake up the device from sleep mode (when in sleep mode, the device is in low-power mode PM1, PM2 or PM3).

The **debug interface** implements a proprietary two-wire serial interface that is used for in-circuit debugging. Through this debug interface, it is possible to perform an erasure of the entire flash memory, control which oscillators are enabled, stop and start execution of the user program, execute supplied instructions on the 8051 core, set code breakpoints, and single-step through instructions in the code. Using these techniques, it is possible to perform in-circuit debugging and external flash programming elegantly.

The **I/O controller** is responsible for all general-purpose I/O pins. The CPU can configure whether peripheral modules control certain pins or whether they are under software control, and if so, whether each pin is configured as an input or output and if a pullup or pulldown resistor in the pad is connected. Each peripheral that connects to the I/O pins can choose between several different I/O pin locations to ensure flexibility in various applications.

The **sleep timer** is an ultralow-power timer that can use either an external 32.768-kHz XOSC or an internal 32.753-kHz RC oscillator. The sleep timer runs continuously in all operating modes. Typical applications of this timer are as a real-time counter or as a wake-up timer to get out of power modes 1 or 2.

A built-in **watchdog timer** allows the CC2545 to reset itself if the firmware hangs. When enabled by software, the watchdog timer must be cleared periodically; otherwise, it resets the device when it times out.

Timer 1 is a 16-bit timer with timer/counter/PWM functionality. It has a programmable prescaler, a 16-bit period value, and five individually programmable counter/capture channels, each with a 16-bit compare value. Each of the counter/capture channels can be used as a PWM output or to capture the timing of edges on input signals. It can also be configured in IR generation mode, where it counts timer 3 periods and the output is ANDed with the output of timer 3 to generate modulated consumer IR signals with minimal CPU interaction.

Timer 2 is a 40-bit timer used by the Radio. It has a 16-bit counter with a configurable timer period and a 24-bit overflow counter that can be used to keep track of the number of periods that have transpired. A 40-bit capture register is also used to record the exact time at which a start-of-frame delimiter is received/transmitted or the exact time at which a packet ends. There are two 16-bit timer-compare registers and two 24-bit overflow-compare registers that can be used to give exact timing for start of RX or TX to the radio or general interrupts.

Timer 3 and timer 4 are 8-bit timers with timer/counter/PWM functionality. They have a programmable prescaler, an 8-bit period value, and one programmable counter channel with an 8-bit compare value. Each of the counter channels can be used as PWM output.

USART 0 is configurable as either an SPI master/slave or a UART. It provides double buffering on both RX and TX and hardware flow control and is thus well suited to high-throughput full-duplex applications. The USART has its own high-precision baud-rate generator, thus leaving the ordinary timers free for other uses. When configured as SPI slaves, the USART samples the input signal using SCK directly instead of using some oversampling scheme, and are thus well-suited for high data rates.

I²C module provides a digital peripheral connection with two pins and supports both master and slave operation.

The **AES encryption/decryption core** allows the user to encrypt and decrypt data using the AES algorithm with 128-bit keys. The AES core also supports ECB, CBC, CFB, OFB, CTR, and CBC-MAC, as well as hardware support for CCM.

The ultralow power **analog comparator** enables applications to wake up from PM2 or PM3 based on an analog signal. Both inputs are brought out to pins; the reference voltage must be provided externally. The comparator output is mapped into the digital I/O port and can be treated by the MCU as a regular digital input.

TYPICAL CHARACTERISTICS

All curves are for measurements performed at 2Mbps, GFSK, 320-kHz deviation.

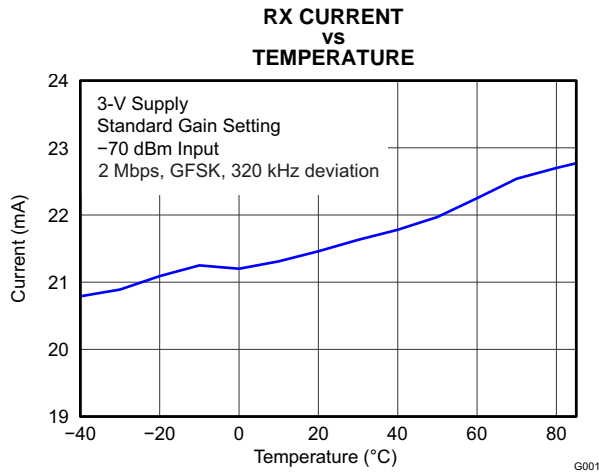


Figure 8.

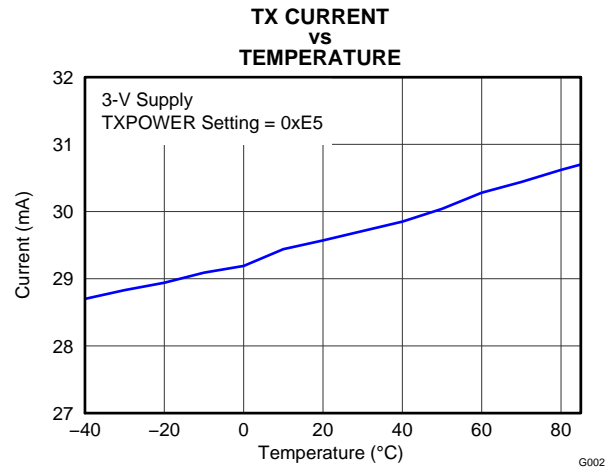


Figure 9.

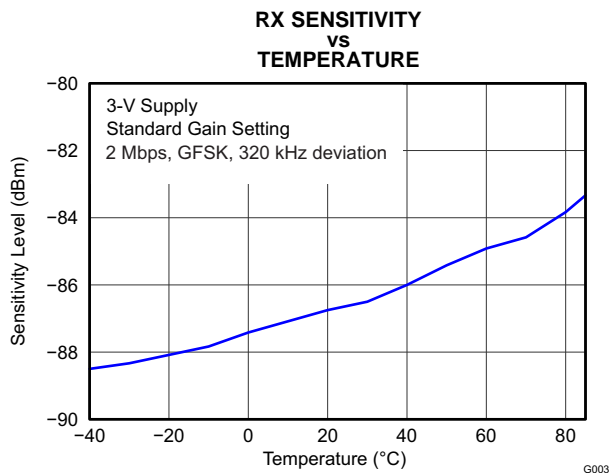


Figure 10.

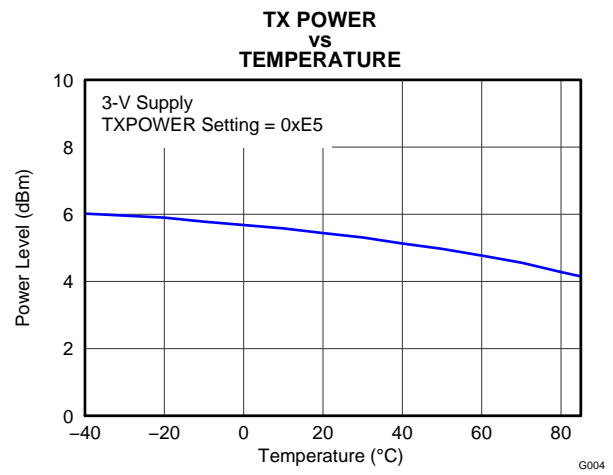


Figure 11.

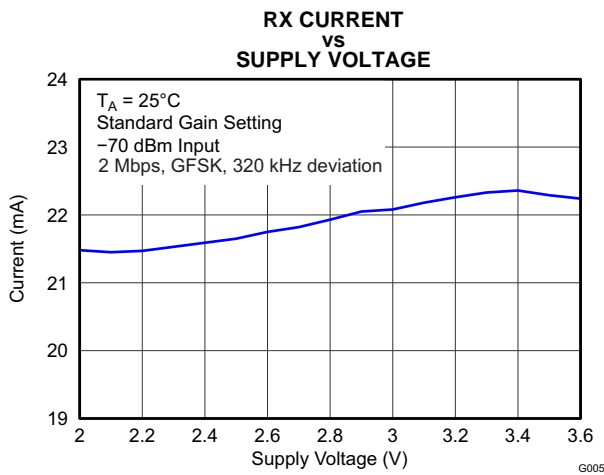


Figure 12.

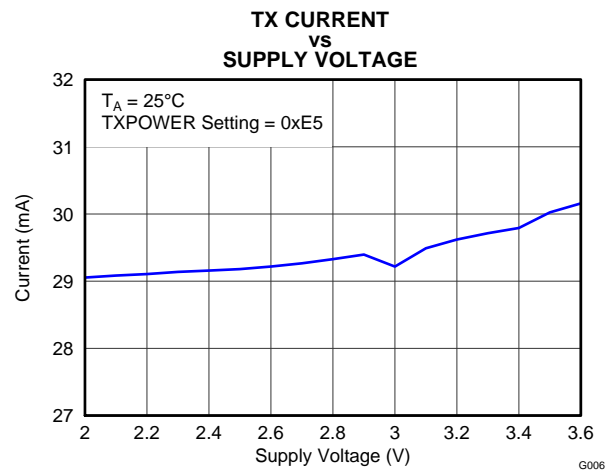


Figure 13.

TYPICAL CHARACTERISTICS (continued)

All curves are for measurements performed at 2Mbps, GFSK, 320-kHz deviation.

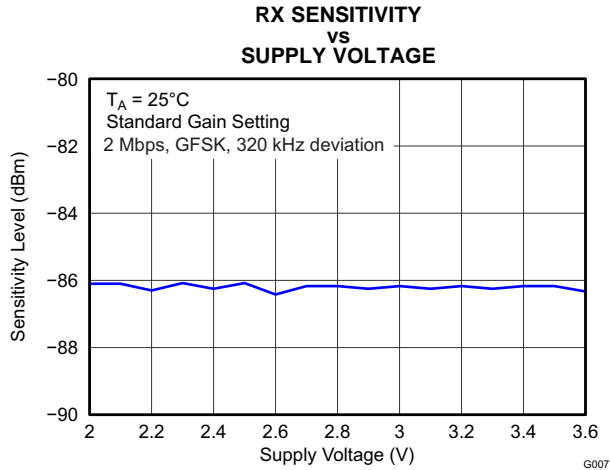


Figure 14.

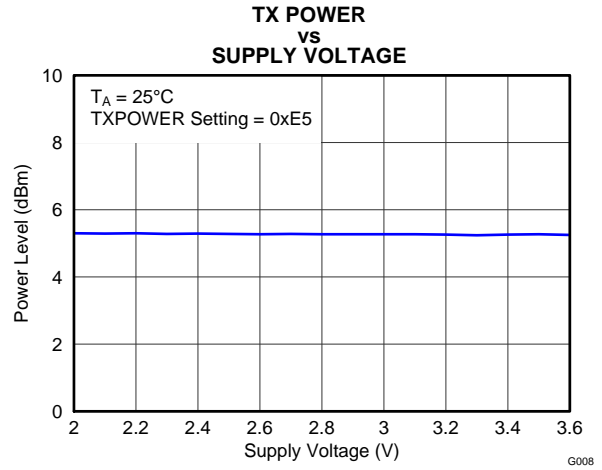


Figure 15.

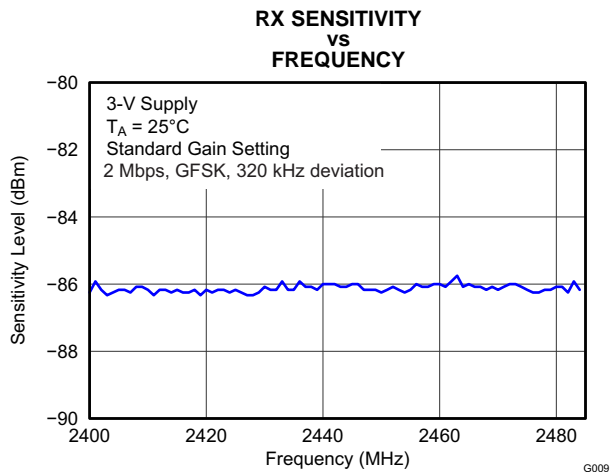


Figure 16.

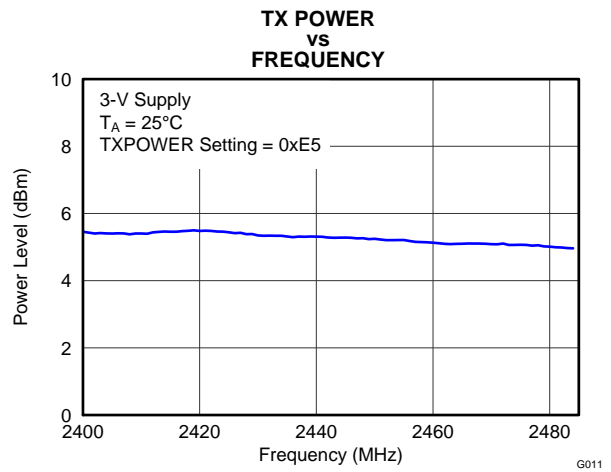


Figure 17.

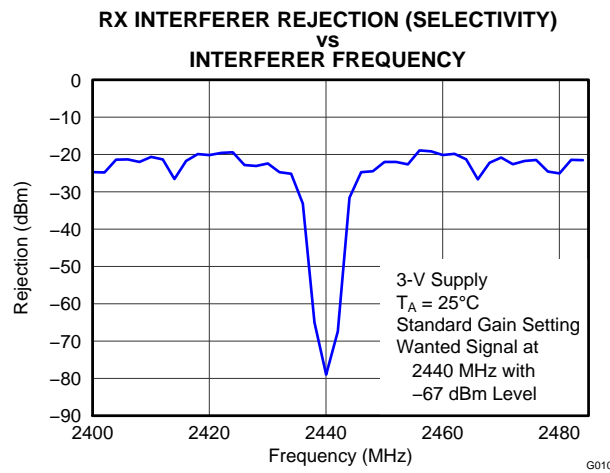


Figure 18.

TYPICAL CHARACTERISTICS (continued)
Table 2. Recommended Output Power Settings⁽¹⁾

| TXPOWER Register Setting | Typical Output Power (dBm) |
|--------------------------|----------------------------|
| 0xE5 | 5 |
| 0xD5 | 4 |
| 0xC5 | 3 |
| 0xB5 | 2 |
| 0xA5 | 0 |
| 0x95 | -2 |
| 0x85 | -3 |
| 0x75 | -4 |
| 0x65 | -6 |
| 0x55 | -8 |
| 0x45 | -11 |
| 0x35 | -13 |
| 0x25 | -15 |
| 0x15 | -17 |
| 0x05 | -20 |

(1) Measured on Texas Instruments CC2545 EM reference design with TA = 25°C, VDD = 3 V, and fc = 2440 MHz. See [SWRU283](#) for recommended register settings.

APPLICATION INFORMATION

APPLICATION INFORMATION

Few external components are required for the operation of the CC2545. A typical application circuit is shown in Figure 19. For suggestions of component values other than those listed in Table 3, see reference design CC2545EM. The performance stated in this data sheet is only valid for the CC2545EM reference design. To obtain similar performance, the reference design should be copied as closely as possible.

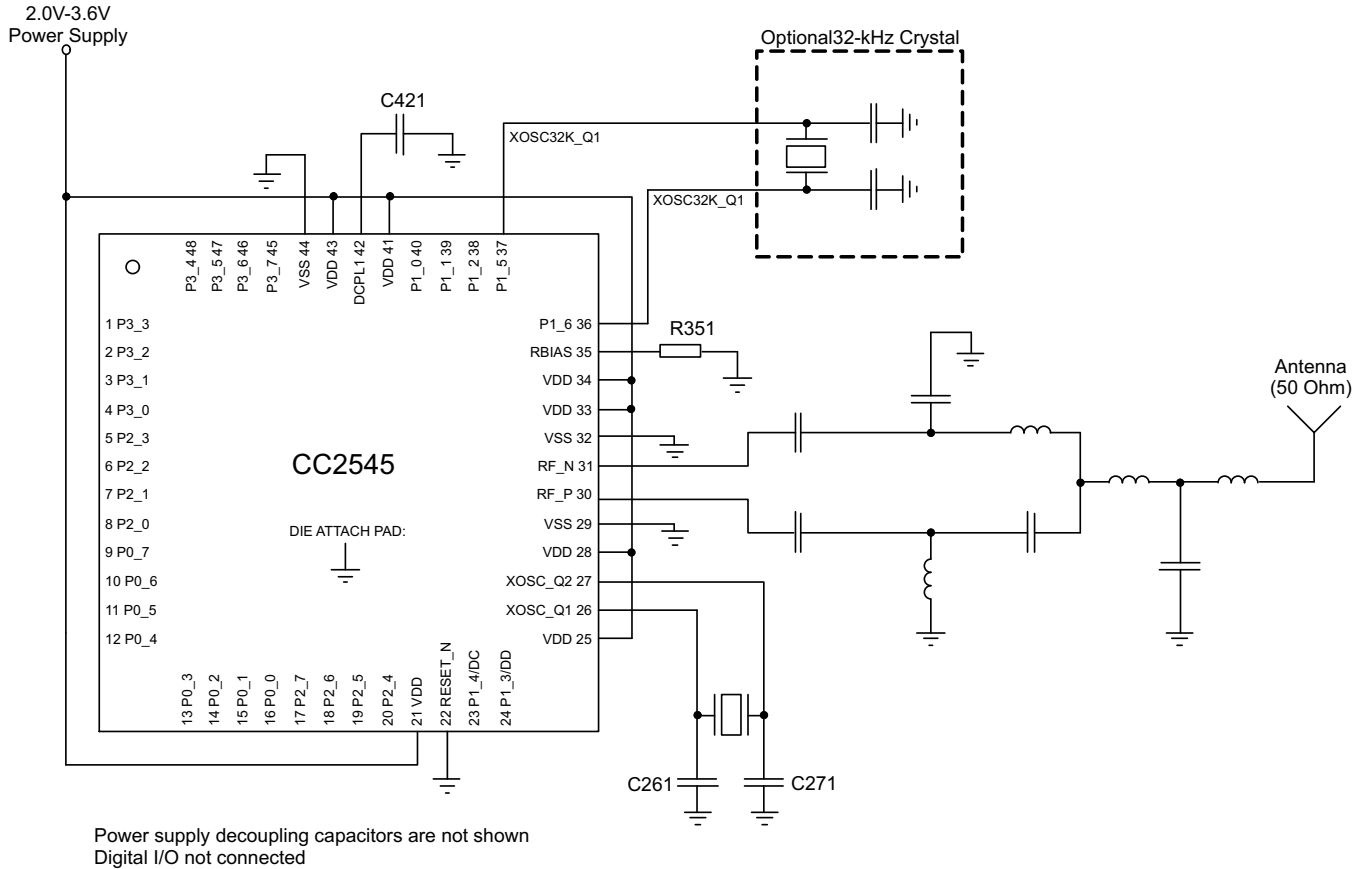


Figure 19. CC2545 Application Circuit

Table 3. Overview of External Components (Excluding Balun, Crystal and Supply Decoupling Capacitors)

| Component | Description | Value |
|-----------|--|---------------|
| C421 | Decoupling capacitor for the internal 1.8V digital voltage regulator | 1 μ F |
| R351 | Precision resistor \pm 1%, used for internal biasing | 56 k Ω |

Input/Output Matching

When using an unbalanced antenna such as a monopole, a balun should be used to optimize performance. The balun can be implemented using low-cost discrete inductors and capacitors. See reference design, CC2545EM, for recommended balun.

Crystal

An external 32-MHz crystal with two loading capacitors is used for the 32-MHz crystal oscillator. The load capacitance seen by the 32-MHz crystal is given by:

$$C_L = \frac{1}{\frac{1}{C_{261}} + \frac{1}{C_{271}}} + C_{\text{parasitic}} \quad (1)$$

A series resistor may be used to comply with ESR requirement.

On-Chip 1.8-V Voltage Regulator Decoupling

The 1.8-V on-chip voltage regulator supplies the 1.8-V digital logic. This regulator requires a decoupling capacitor (C421) for stable operation.

Power-Supply Decoupling and Filtering

Proper power-supply decoupling must be used for optimum performance. The placement and size of the decoupling capacitors and the power supply filtering are very important to achieve the best performance in an application. TI provides a compact reference design that should be followed very closely.

REVISION HISTORY

| Changes from Original (June 2012) to Revision A | Page |
|--|------|
| • Deleted Product Preview banner | 1 |
| • Changed the Temperature coefficient Unit value From: mV/°C To: / 0.1°C | 8 |
| • Changed Figure 19 | 22 |
| Changes from Revision A (August 2012) to Revision B | Page |
| • Changed From: RTC Pin Package To: RGZ Pin Package | 14 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CC2545RGZR | ACTIVE | VQFN | RGZ | 48 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | CC2545 | Samples |
| CC2545RGZT | ACTIVE | VQFN | RGZ | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | CC2545 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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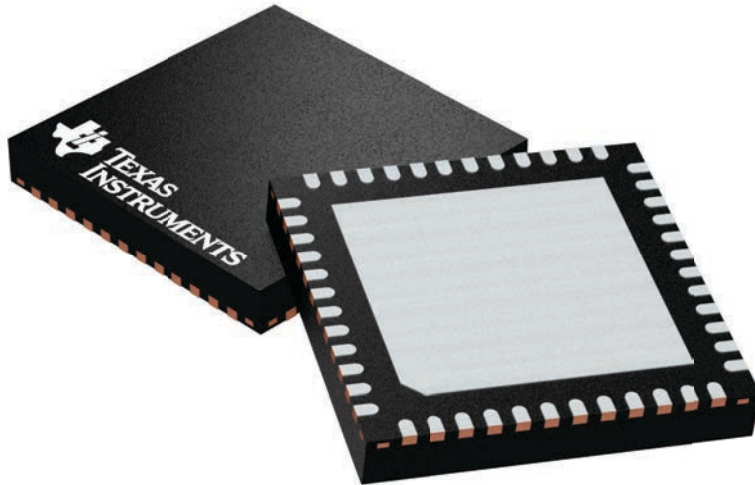
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

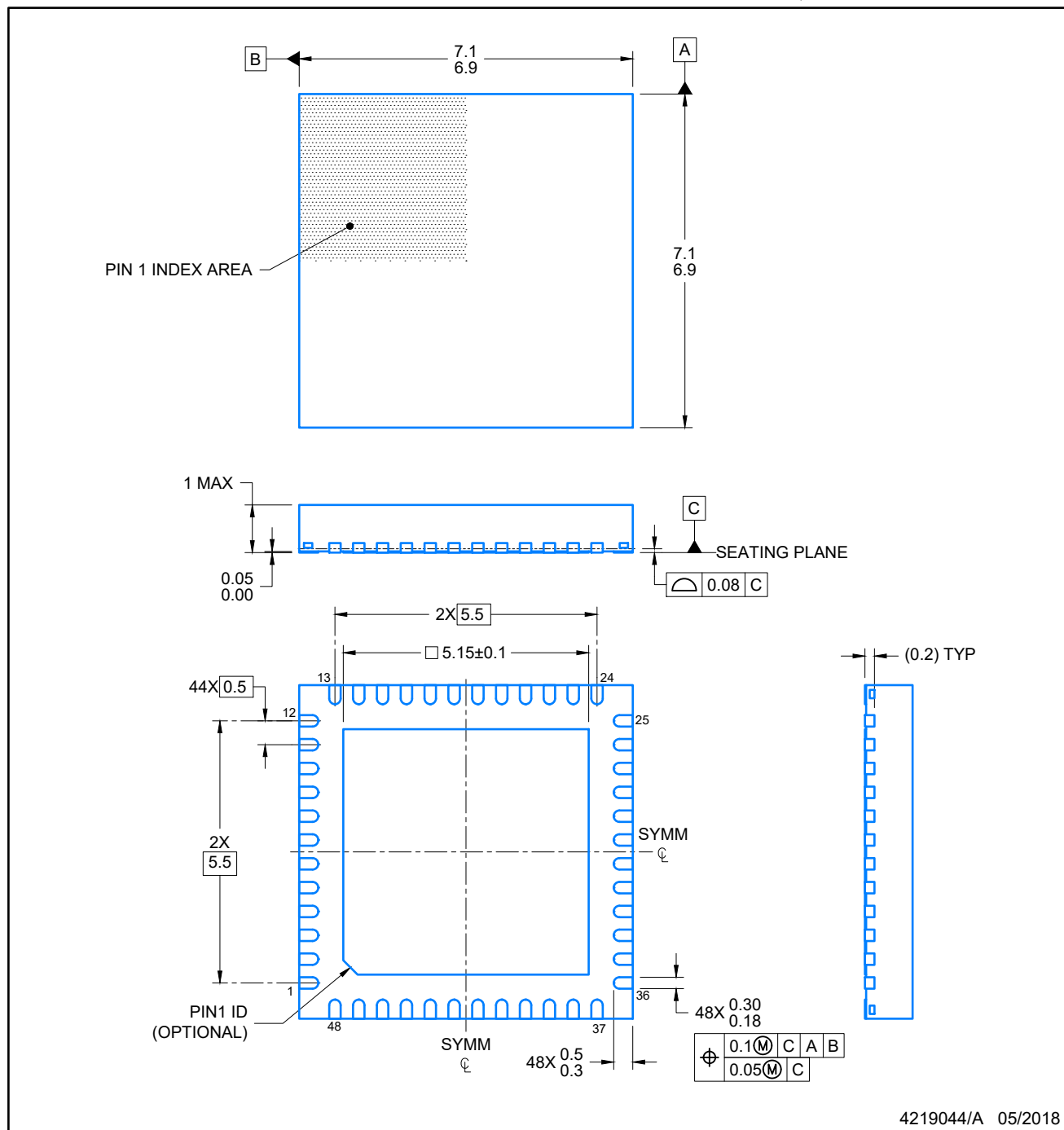
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



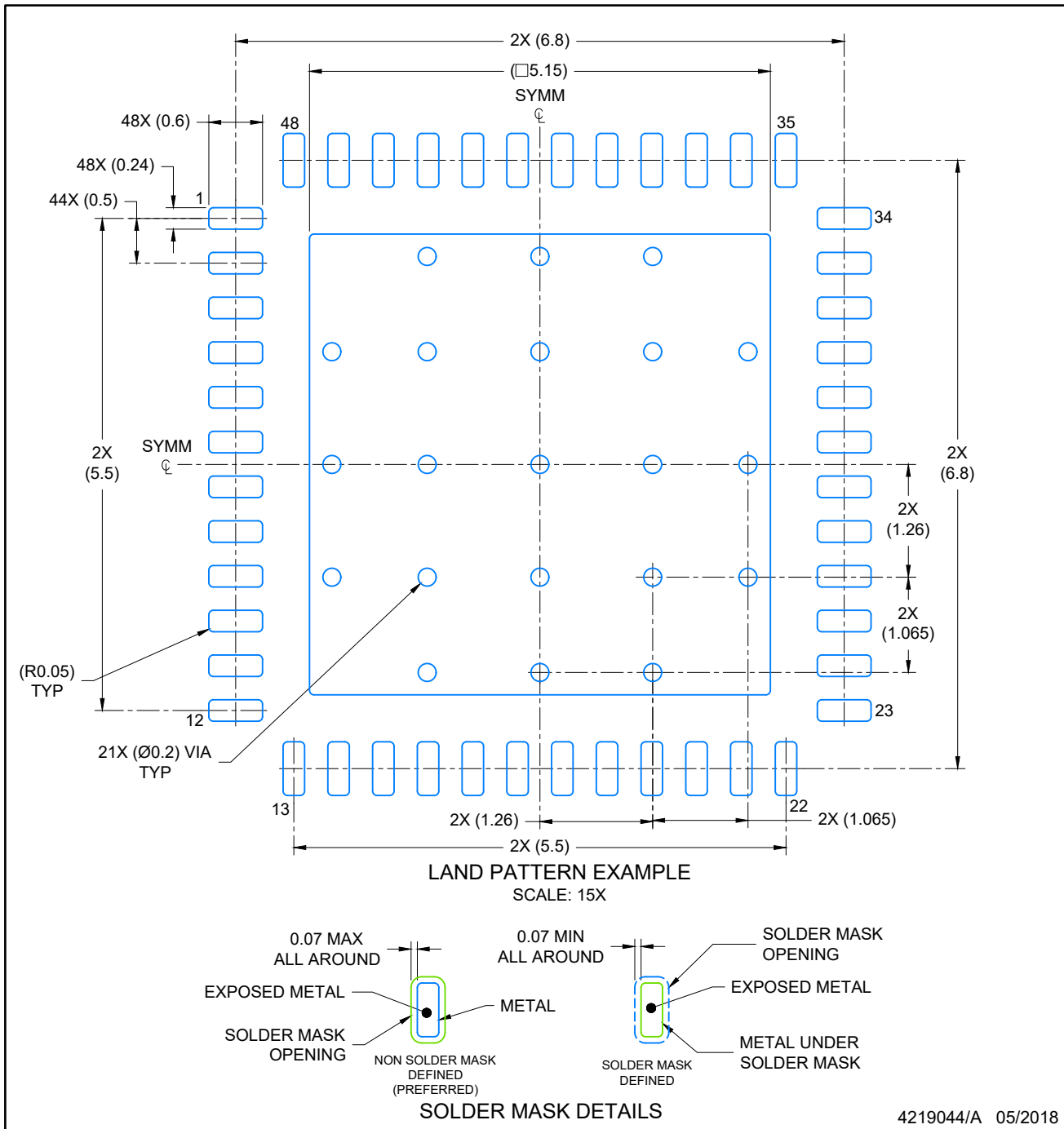
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A



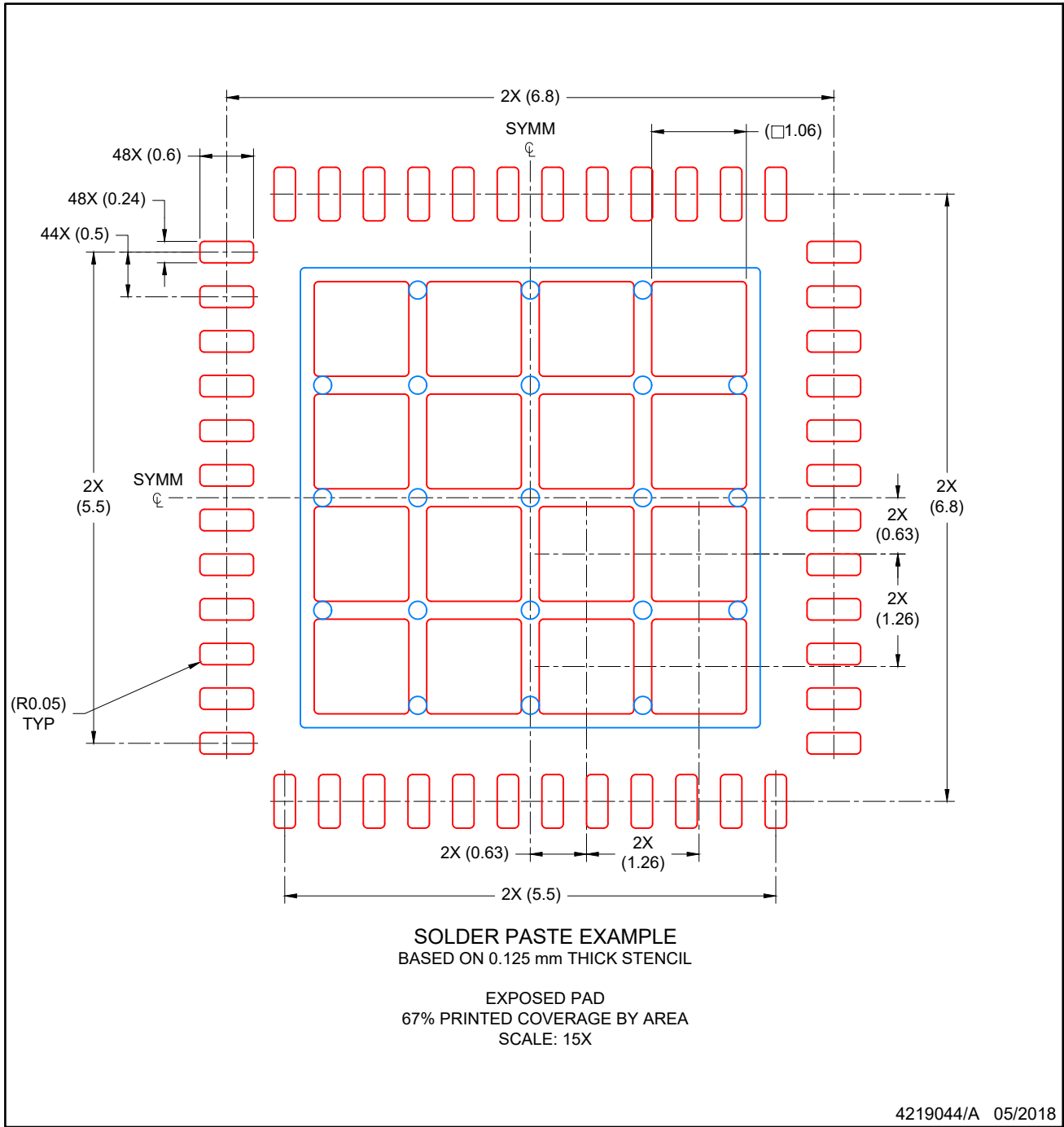
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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