SPOC - BTS5682E

SPI Power Controller

Automotive Power

Never stop thinking

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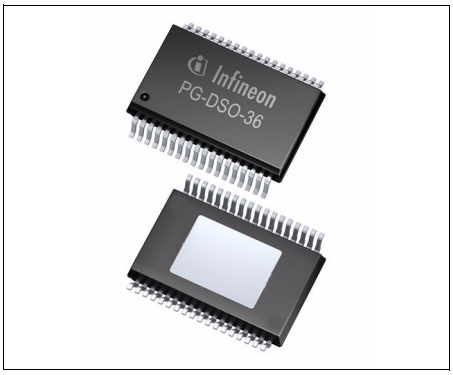
SPI Power Controller **SPOC - BTS5682E**

for Advanced Light Control with Integrated LED Mode and Cranking capable output

AEC Qualified RoHS

1 Overview



PG-DSO-36-36

Features

- 8 bit serial peripheral interface (daisy chain capable SPI) for control and diagnosis
- CMOS compatible parallel input pins for each channel provide direct PWM operation
- Selectable AND- / OR-combination for parallel inputs (PWM control)
- Very low stand-by current
- Enhanced electromagnetic compatibility (EMC) for bulbs as well as LEDs with adjustable slew rate
- Stable behavior at under voltage
- Enhanced relay control supported by cranking capable output
- Device ground independent from load ground
- Green Product (RoHS-Compliant)
- AEC Qualified

Description

The SPOC - BTS5682E is a six channel high-side smart power switch in PG-DSO-36-36 package providing embedded protective functions. It is specially designed to control standard exterior lighting in automotive applications. In order to use the same hardware, the device can be configured to bulb or LED mode. As a result, both load types are optimized in terms of switching and diagnosis behavior.

It is designed to drive lamps up to 3*27W + 2*10W + 5W.

Product Summary

Operating Voltage Power Switch	V_{BB}	5.5 … 28 V
Extended Operating Voltage channel 5	$V_{BB(EXT)}$	3.2 … 5.5 V
Logic Supply Voltage	V_{DD}	3.8 … 5.5 V
Over Voltage Protection	$V_{BB(AZ,min)}$	40 V
Maximum Stand-By Current at 25 °C	$I_{BB(OFF)}$	3 µA
Maximum On-state Resistance at T_j = 150 °C channel 0, 1, 2 channel 3, 4 channel 5	$R_{DS(ON,max)}$	 100 mΩ 260 mΩ 460 mΩ
SPI Access Frequency	$f_{SCLK(max)}$	2 MHz

Type	Package	Marking
SPOC - BTS5682E	PG-DSO-36-36	BTS5682E

Configuration and status diagnosis are done via SPI. An 8 bit serial peripheral interface (SPI) is used. The SPI can be used in daisy chain configuration.

The device provides a current sense signal per channel that is multiplexed to the diagnosis pin IS. It can be enabled and disabled via SPI commands. An over load and over temperature flag is provided in the SPI diagnosis word. A multiplexed switch bypass monitor provides short-circuit to V_{BB} diagnosis.

In order to use the same hardware, channels OUT0, OUT1 and OUT2 can be configured to bulb or LED mode.

Channel 5 is designed to fulfill cranking down to 3.2 V.

The SPOC - BTS5682E provides a fail-safe feature via a limp home input pin.

The power transistors are built by N-channel vertical power MOSFETs with charge pumps. The device is monolithically integrated in SMART technology.

Protective Functions

- Reverse battery protection with external components
- Short circuit protection
- Overload protection
- Multi step current limitation
- Thermal shutdown with latch and dynamic temperature sensor
- Overvoltage protection
- Loss of ground protection
- Electrostatic discharge protection (ESD)

Diagnostic Functions

- Multiplexed proportional load current sense signal (IS)
- Enable function for current sense signal configurable via SPI
- High accuracy of current sense signal at wide load current range
- Current sense ratio (k_{ILIS}) configurable for LEDs or bulbs
- Very fast diagnosis in LED mode (>2% duty cycle at 100 Hz)
- Feedback on over temperature and over load via SPI
- Multiplexed switch bypass monitor provides short circuit to V_{BB} detection

Application Specific Functions

- Fail-safe activation via LHI pin and control via input pins
- Load type configuration via SPI (bulbs or LEDs) for optimized load control
- Enhanced relay control at channel 5 providing cranking capability down to 3.2 V

Applications

- High-side power switch for 12 V grounded loads in automotive applications
- Especially designed for standard exterior lighting like tail light, brake light, parking light, license plate light, indicators and equivalent LEDs
- Enhanced relay control supported by cranking capable output
- Replaces electromechanical relays, fuses and discrete circuits

2 Block Diagram

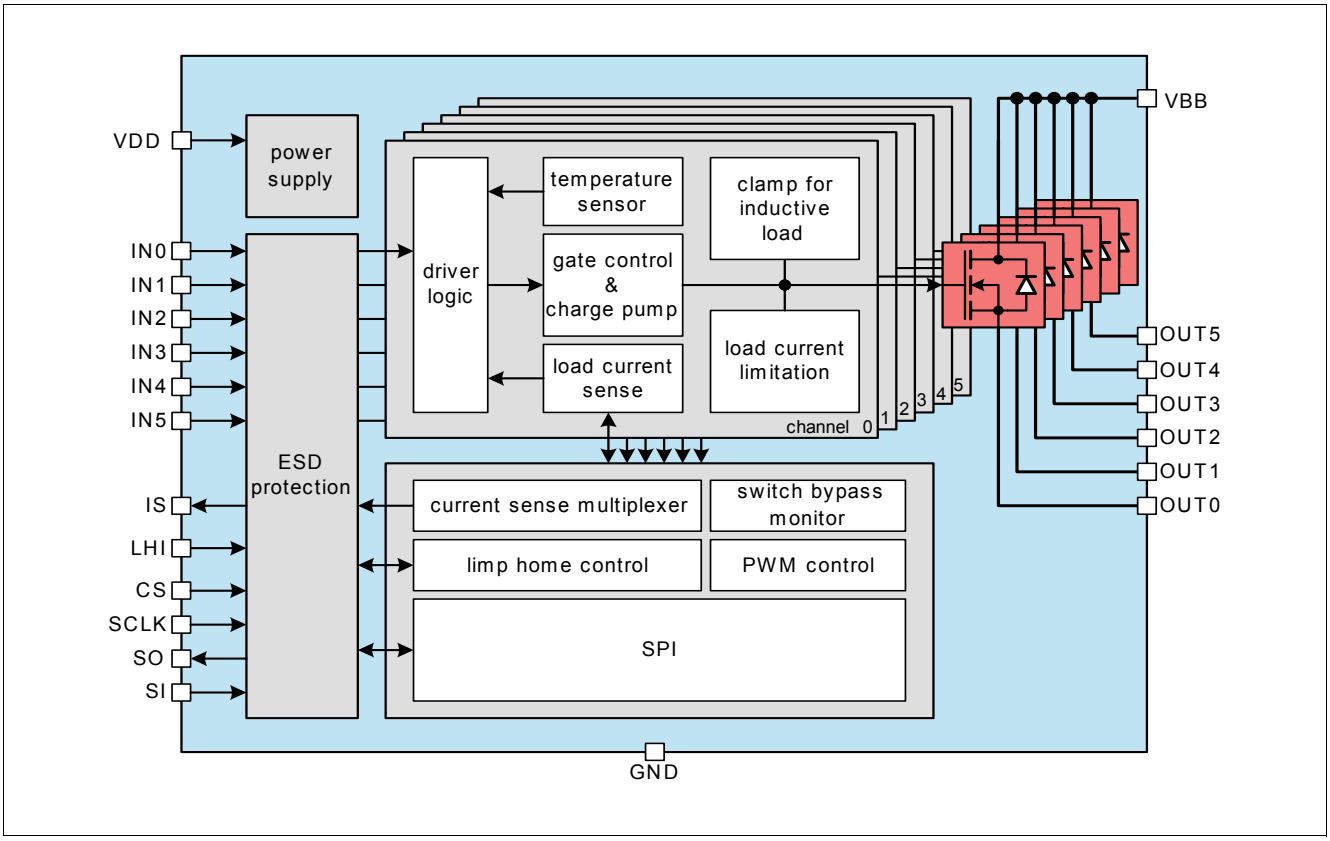


Figure 1 Block Diagram SPOC - BTS5682E

2.1 Terms

The following figure shows all terms used in this data sheet.

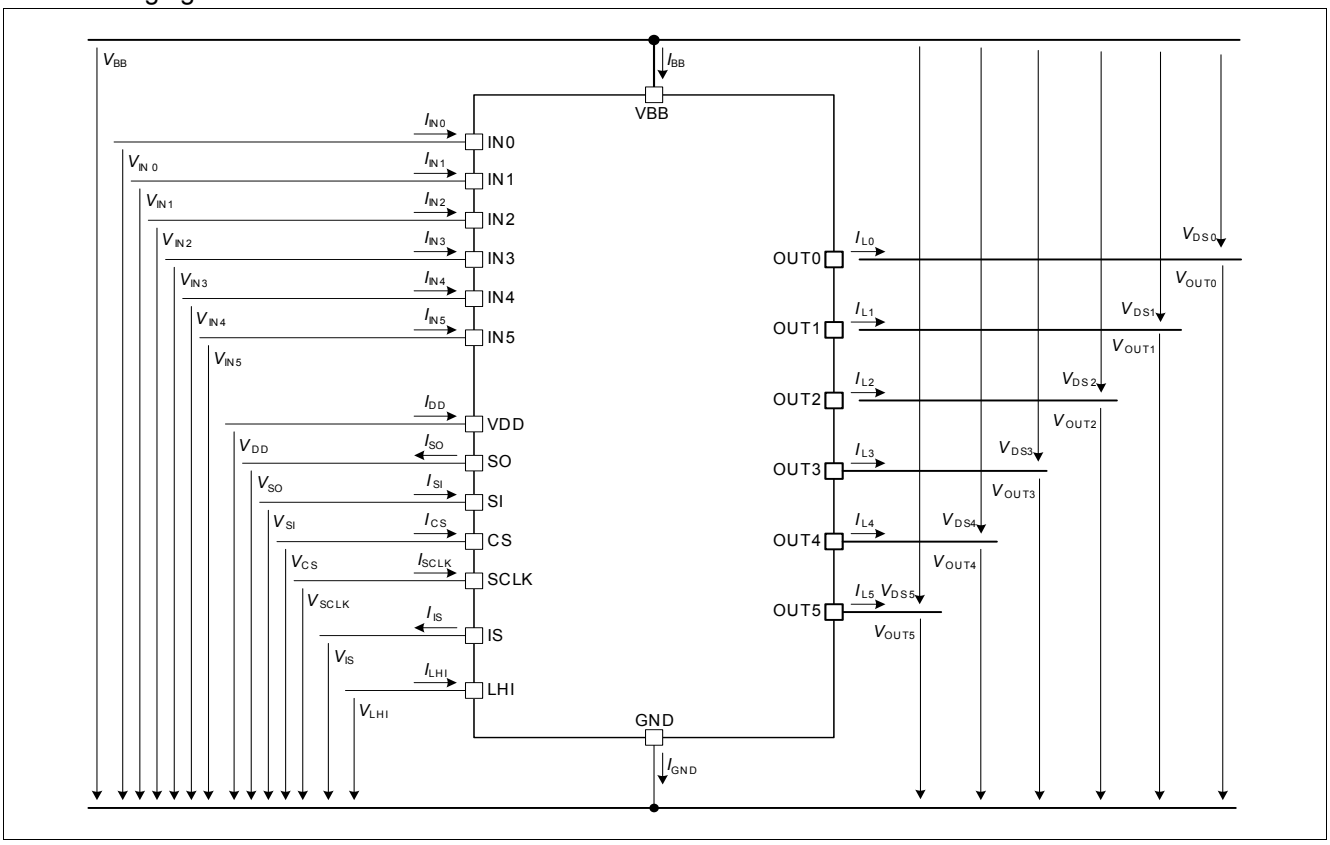


Figure 2 Terms

In all tables of electrical characteristics is valid: Channel related symbols without channel number are valid for each channel separately (e.g. V_{DS} specification is valid for V_{DS0} … V_{DS5}).

All SPI register bits are marked as follows: `ADDR.PARAMETER` (e.g. `HWCR.CTL`). In SPI register description, the values in bold letters (e.g. **0**) are default values.

3 Pin Configuration

3.1 Pin Assignment SPOC - BTS5682E

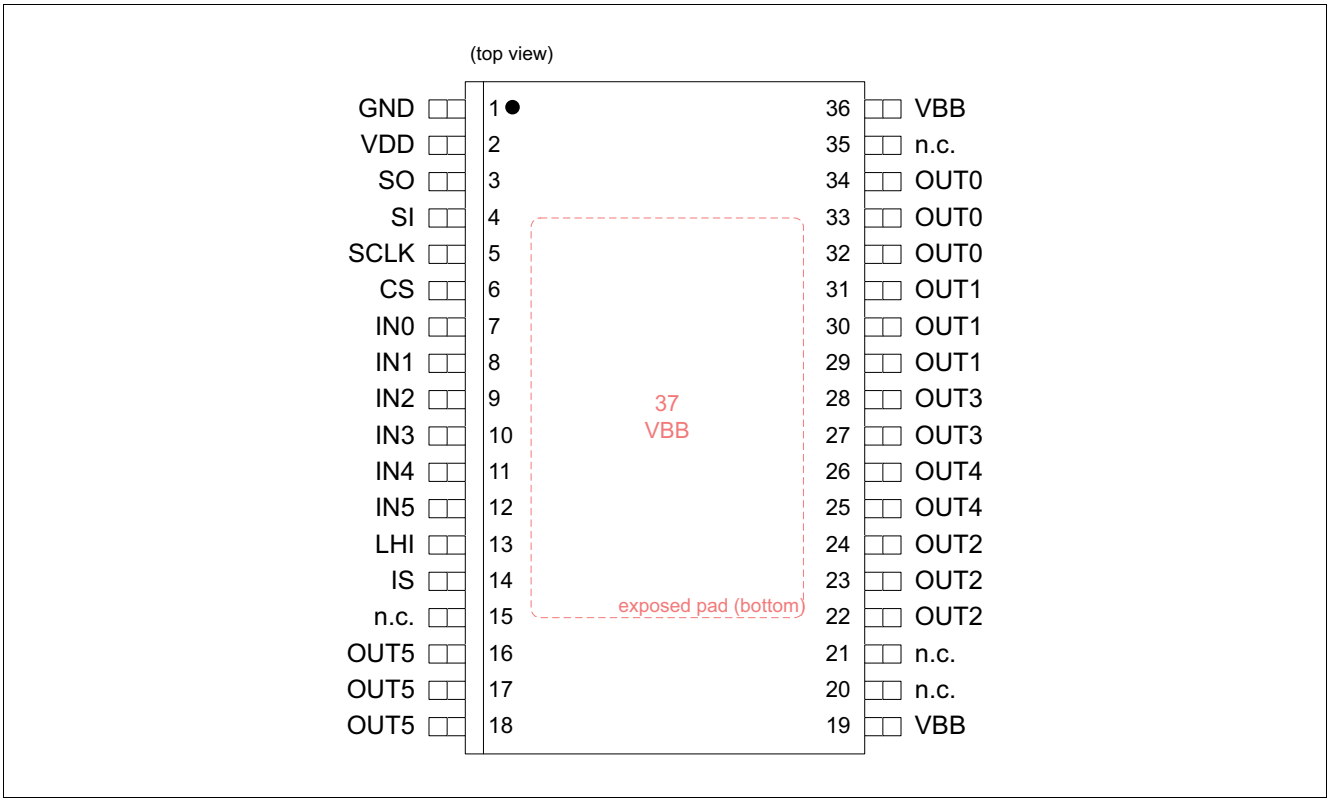


Figure 3 Pin Configuration PG-DSO-36-36

3.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
Power Supply Pins			
19, 36, 37 [1]	VBB	–	Positive power supply for high-side power switch
2	VDD	–	Logic supply (5 V)
1	GND	–	Ground connection
Parallel Input Pins (integrated pull-down, leave unused input pins unconnected)			
7	IN0	I	Input signal of channel 0
8	IN1	I	Input signal of channel 1
9	IN2	I	Input signal of channel 2
10	IN3	I	Input signal of channel 3
11	IN4	I	Input signal of channel 4
12	IN5	I	Input signal of channel 5
Power Output Pins			
32, 33, 34 [2]	OUT0	O	Protected high-side power output of channel 0
29, 30, 31 [2]	OUT1	O	Protected high-side power output of channel 1
22, 23, 24 [2]	OUT2	O	Protected high-side power output of channel 2
27, 28 [2]	OUT3	O	Protected high-side power output of channel 3
25, 26 [2]	OUT4	O	Protected high-side power output of channel 4
16, 17, 18 [2]	OUT5	O	Protected high-side power output of channel 5
SPI & Diagnosis Pins			
6	CS	I	Chip select of SPI interface (low active), Integrated pull up
5	SCLK	I	Serial clock of SPI interface
4	SI	I	Serial input of SPI interface
3	SO	O	Serial output of SPI interface
14	IS	O	Diagnosis output signal
Limp Home Pin (integrated pull-down, leave unused limp home pin unconnected)			
13	LHI	I	Limp home activation signal; Active high
Not connected Pin			
15, 20, 21, 35	n.c.	–	not connected, internally not bonded

1) The exposed pad (pin 37) has to be connected to the power supply with a low impedance connection. The exposed pad must be connected with a low thermal resistance.

2) All outputs pins of each channel have to be connected.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			min.	max.		
Supply Voltage						
4.1.1	Power supply voltage	V_{BB}	-0.3	28	V	–
4.1.2	Logic supply voltage	V_{DD}	-0.3	5.5	V	–
4.1.3	Reverse polarity voltage according **Figure 23**	$-V_{bat(rev)}$	–	16	V	$T_{j(Start)}$ = 25 °C $t \leq$ 2 min. [2)]
4.1.4	Supply voltage for full short circuit protection (single pulse) ($T_{j(0)}$ = -40 °C … 150 °C)	$V_{BB(SC)}$	0	20	V	R_{ECU} = 20mΩ R_{Cable}= 16mΩ/m L_{Cable}= 1µH/m l = 0 or 5m [3)]
4.1.5	Voltage at power transistor	V_{DS}	–	40	V	–
4.1.6	Supply voltage for load dump protection	$V_{BB(LD)}$	–	40	V	R_I = 2 Ω [4)] t = 400ms
4.1.7	Current through ground pin	I_{GND}	-100	25	mA	$t \leq$ 2 min.
4.1.8	Current through V_{DD} pin	I_{DD}	-25	12	mA	$t \leq$ 2 min.
Power Stages						
4.1.9	Load current	I_L	$-I_{L(LIM)}$	$I_{L(LIM)}$	A	[5)]
Diagnosis Pin						
4.1.10	Current through sense pin IS	I_{IS}	-10	10	mA	$t \leq$ 2 min.
Input Pins						
4.1.11	Voltage at input pins	V_{IN}	-0.3	8.0	V	–
4.1.12	Current through input pins	I_{IN}	-0.75 -2.0	0.75 2.0	mA	– $t \leq$ 2 min.
SPI Pins						
4.1.13	Voltage at chip select pin	V_{CS}	-0.3	5.7	V	–
4.1.14	Current through chip select pin	I_{CS}	-0.75 -2.0	0.75 2.0	mA	– $t \leq$ 2 min.
4.1.15	Voltage at serial input pin	V_{SI}	-0.3	5.7	V	–
4.1.16	Current through serial input pin	I_{SI}	-0.75 -2.0	0.75 2.0	mA	– $t \leq$ 2 min.
4.1.17	Voltage at serial clock pin	V_{SCLK}	-0.3	5.7	V	–
4.1.18	Current through serial clock pin	I_{SCLK}	-0.75 -2.0	0.75 2.0	mA	– $t \leq$ 2 min.
4.1.19	Current through serial output pin SO	I_{SO}	-0.75 -2.0	0.75 2.0	mA	– $t \leq$ 2 min.
Limp Home Pin						
4.1.20	Voltage at limp home input pin	V_{LHI}	-0.3	8.0	V	–

Absolute Maximum Ratings (cont'd)[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground
(unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			min.	max.		
4.1.21	Current through limp home input pin	I_{LHI}	-0.75 -2.0	0.75 2.0	mA	– $t \leq 2$ min.
Temperatures						
4.1.22	Junction temperature	T_j	-40	150	°C	–
4.1.23	Dynamic temperature increase while switching	ΔT_j	–	60	K	–
4.1.24	Storage temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
4.1.25	ESD resistivity OUT pins vs. VBB other pins incl. OUT vs. GND	V_{ESD}	 -4 -2	 4 2	kV	HBM [6)] – –

1) Not subject to production test, specified by design.

2) Device mounted on a FR4 2s2p board according to Jedec JESD51-2,-5,-7 at natural convection; The product (chip+package) was simulated on a 76.4 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable, a thermal via array under the package contacted the first inner copper layer.

3) In accordance to AEC Q100-012 and AEC Q101-006.

4) R_I is the internal resistance of the load dump pulse generator.

5) Current limitation is a protection feature. Operation in current limitation is considered as "outside" normal operating range. Protection features are not designed for continuous repetitive operation.

6) ESD resistivity, HBM according to EIA/JESD 22-A 114B (1.5kΩ, 100pF).

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.2.1	Junction to Case [1)]	R_{thJC}	–	–	2	K/W	–
4.2.2	Junction to Ambient [1)]	R_{thJA}	–	22	–	K/W	[2)]

1) Not subject to production test, specified by design.

2) Device mounted on a FR4 2s2p board according to Jedec JESD51-2,-5,-7 at natural convection; The product (chip+package) was simulated on a 76.4 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable, a thermal via array under the package contacted the first inner copper layer.

5 Power Supply

The SPOC - BTS5682E is supplied by two supply voltages V_{BB} and V_{DD}. The V_{BB} supply line is used by the power switches. The V_{DD} supply line is used by the SPI related circuitry and for driving the SO line. A capacitor between pins VDD and GND is recommended as shown in **Figure 23**.

There is a power-on reset function implemented for the V_{DD} logic power supply. After start-up of the logic power supply, all SPI registers are reset to their default values. The SPI interface including daisy chain function is active as soon as V_{DD} is provided in the specified range independent of V_{BB}. The first SPI transmission after a reset contains at pin SO the read information from register `OUT`, the transmission error bit `TER` is set.

5.1 Power Supply Modes

The following table shows all possible power supply modes for V_{BB}, V_{DD} and the pin LHI.

Power Supply Modes	Off	Off	SPI on	Reset	Off [2]	Limp Home mode without SPI	Normal operation	Limp Home mode with SPI [1]
V_{BB}	0 V	0 V	0 V	0 V	13.5 V	13.5 V	13.5 V	13.5 V
V_{DD}	0 V	0 V	5 V	5 V	0 V	0 V	5 V	5 V
LHI	0 V	5 V	0 V	5 V	0 V	5 V	0 V	5 V
PROFET operating	–	–	–	–	✓[2]	✓	✓	✓
Limp home	–	–	–	–	–	✓	–	✓
SPI (logic)	–	–	✓	reset	reset	reset	✓	reset
Stand-by current	–	–	–	–	✓[2]	–	✓[3]	–
Idle current	–	–	–	–	–	–	✓[4]	–
Diagnosis	–	–	–	–	–	–	✓	✓[5]

1) SPI read only.
2) Depending on latched channel 5.
3) When `DCR.MUX` = 111_b and channel 5 in OFF-state.
4) When all channels are in OFF-state and `DCR.MUX`!= 111_b.
5) Current sense disabled in limp home mode.

Stand-by mode is entered as soon as the current sense multiplexer (`DCR.MUX`) is in default (stand-by) position and channel 5 is not latched in ON-state[1]. Additionally, all thermal latches are cleared automatically. As soon as stand-by mode is entered, register `HWCR.STB` is set. The state of channel 5 can be read via `HWCR.CH5`. To wake-up the device, the current sense multiplexer (`DCR.MUX`) is programmed different to default (stand-by) position.

Idle mode parameters are valid, when all channels are switched off, but the current sense multiplexer is not in default position, and V_{DD} supply is available.

Limp home (LHI = high) will wake-up the device and is working without V_{DD} supply. As a result, all channels can be activated via the dedicated input pins. The cranking latch is not available in limp home mode in order to switch to stand-by mode after limp home.

1) Not affected by the inputs state

5.2 Cranking Mode

The SPOC - BTS5682E is designed to support cranking capability at channel 5. It provides an extended operating range specified by parameter **5.4.2** independent of V_{DD} supply.

A latch operating at low V_{BB} voltages was integrated into the gate control of channel 5 in order to keep the channel 5 switched on during supply voltage drop.

The latch mode of channel 5 is activated per default (`HWCR.LCH` = 1). This latch can be set via input pin or via SPI register `OUT.OUT5`. The channel stays in ON-state until the latch is cleared.

For deactivating channel 5 latching operation mode the following steps needs to be performed:

- The channel must not be activated via pin IN5 or `OUT.OUT5`.
- The latch-bit must be cleared (`HWCR.LCH` = 0) via the SPI.

The state of channel 5 can be read via `HWCR.CH5`. As a result, after cranking and micro-controller reset, the state of the device (stand-by or channel 5 in ON-state) can be uniquely identified.

As long as channel 5 is in ON-state, the SPOC - BTS5682E will not enter stand-by mode.

5.3 Reset

There are several reset triggers implemented in the device. They reset the SPI registers and errors flags to their default values. The power stages are not affected by the reset signals.

The first SPI transmission after any kind of reset contains at pin SO the read information from register `OUT`, the transmission error bit `TER` is set.

Power-On Reset

The power-on reset is released, when V_{DD} voltage level is higher than $V_{DD(min)}$. The SPI interface can be accessed after wake up time $t_{WU(PO)}$.

Reset Command

There is a reset command available to reset all register bits of the register bank and the diagnosis registers. As soon as `HWCR.RST` = 1, a reset is triggered equivalent to power-on reset. The SPI interface can be accessed after transfer delay time $t_{CS(td)}$.

Limp Home Mode

In Limp Home mode, the SPI write-registers are reset. Output OUTx will follow the input INx configuration only. For application example see **Figure 23**. The SPI interface is operating normally, so the limp home register bit LHI as well as the error flags can be read, but any write command will be ignored. To activate the Limp Home mode, LHI input pin voltage must be higher than $V_{LHI(H)}$.

5.4 Electrical Characteristics

Electrical Characteristics Power Supply

Unless otherwise specified: V_{BB} = 9 V to 16 V, V_{DD} = 3.8 V to 5.5 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
5.4.1	Operating voltage power switch	V_{BB}	5.5	–	28[1)]	V	–
5.4.2	Extended operating voltage power switch channel 5	$V_{BB(EXT)}$	3.2	–	5.5	V	V_{DS5} < 1.5 V [2)] R_{L5} = 50 Ω
5.4.3	Stand-by current for whole device with loads	$I_{BB(STB)}$	 – – –	 0.5 – –	 3 3 58	µA	V_{DD} = 0 V V_{LHI} = 0 V T_j = 25 °C $T_j \leq$ 85 °C [1)] T_j = 150 °C
5.4.4	Idle current for whole device with loads, all channels off.	$I_{BB(idle)}$	–	3	8	mA	V_{DD} = 5 V DCR.MUX = 110_B
5.4.5	Logic supply voltage	V_{DD}	3.8	–	5.5	V	–
5.4.6	Logic supply current	I_{DD}	–	55	120	µA	V_{CS} = 0 V f_{SCLK} = 0 Hz
5.4.7	Logic idle current	$I_{DD(idle)}$	–	20	50	µA	V_{CS} = V_{DD} f_{SCLK} = 0 Hz Chip in Standby
5.4.8	Operating current for whole device	I_{GND}	–	12	25	mA	f_{SCLK} = 0 Hz
LHI Input Characteristics							
5.4.9	L-input level at pin LHI	$V_{LHI(L)}$	-0.3	–	1.0	V	–
5.4.10	H-input level at pin LHI	$V_{LHI(H)}$	2.6	–	5.5	V	–
5.4.11	L-input current through pin LHI	$I_{LHI(L)}$	3	–	85	µA	V_{LHI} = 0.4 V
5.4.12	H-input current through pin LHI	$I_{LHI(H)}$	7	30	85	µA	V_{LHI} = 5 V

1) Not subject to production test, specified by design.

2) V_{BB} decreasing.

Note: Characteristics show the deviation of parameter at the given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing at V_{BB} = 13.5 V, V_{DD} = 4.3 V and T_j = 25 °C.

5.5 Command Description

HWCR
Hardware Configuration Register

W/$\overline{R}$[1)]	RB[1)]	ADDR[1)]		3	2	1	0
read	**1**	**1**	**0**	**CH5**	**LCH**	**STB**	**CTL**
write	**1**	**1**	**0**	**0**	**LCH**	**RST**	**CTL**

1) W/$\overline{R}$ Write/Read, RB Register Bank, ADDR Address

Field	Bits	Type	Description
RST	1	w	**Reset Command** **0** Normal operation 1 Execute reset command
STB	1	r	**Stand-by** 0 Device is awake **1** Device is in stand-by mode
LCH	2	rw	**Cranking Latch activation** 0 Normal mode (transparent) **1** Latch mode
CH5	3	r	**Channel 5 state** 0 Channel 5 is in OFF-state **1** Channel 5 is in ON-state

6 Power Stages

The high-side power stages are built by N-channel vertical power MOSFETs (DMOS) with charge pumps. There are six channels implemented in the device. Each channel can be switched on via an input pin or via SPI register `OUT`. Channels 0, 1 and 2 provides a load type configuration for bulbs or LEDs in register `PLCR`. The load type configuration is allowed to be changed in OFF-state only.

6.1 Output ON-State Resistance

The on-state resistance $R_{DS(ON)}$ depends on the supply voltage V_{BB} as well as on the junction temperature T_j. **Figure 4** shows those dependencies. The behavior in reverse polarity mode is described in **Section 12**.

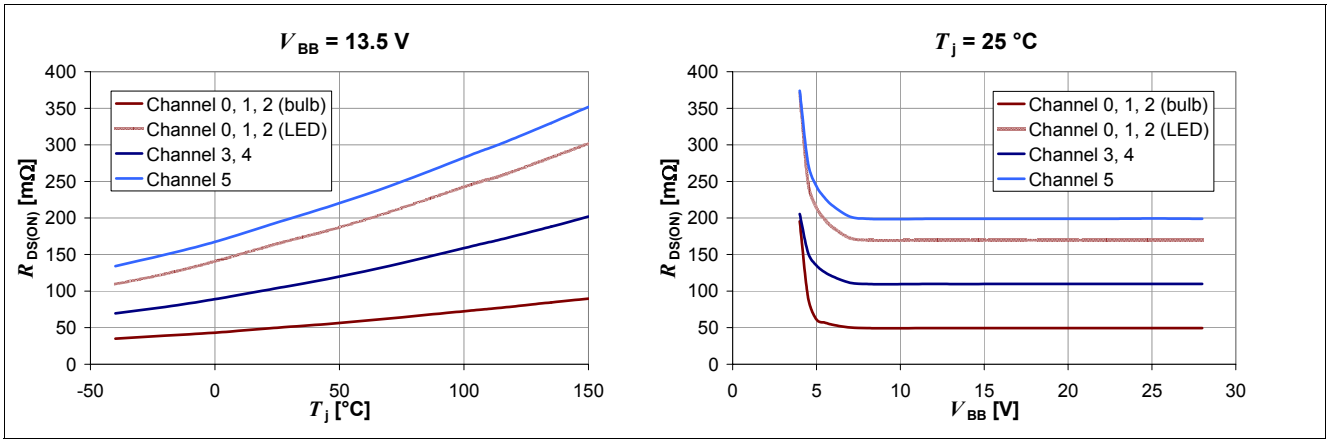


Figure 4 Typical On-State Resistance

6.2 Input Circuit

There are two ways of using the input pins in combination with the OUT register by programming the `HWCR.PWM` parameter.

- `PLCR.PWM` = 0: A channel is switched on either by the according `OUT` register bit or the input pin.
- `PLCR.PWM` = 1: A channel is switched on by the according `OUT` register bit only, when the input pin is high. In this configuration, a PWM signal can be given to the input pin and the channel is activated by the SPI register `OUT`.

Figure 5 shows the complete input switch matrix.

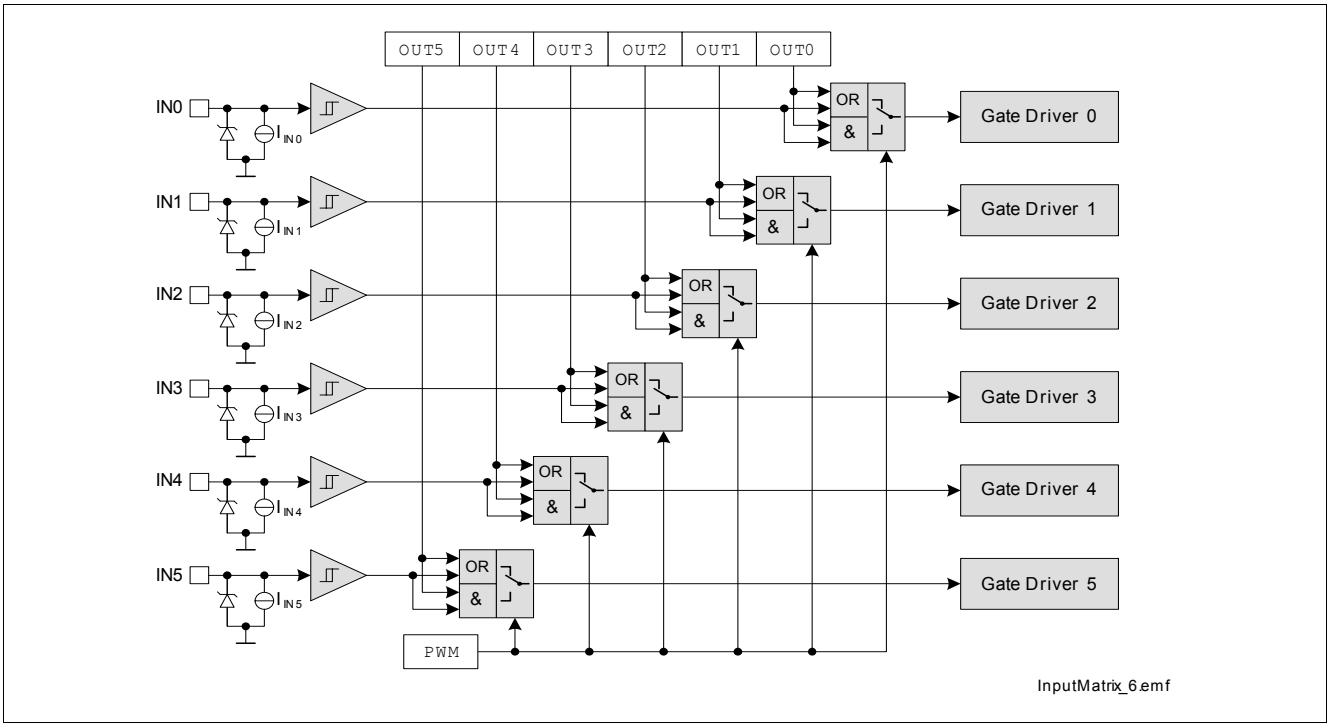


Figure 5 Input Switch Matrix

The current sink to ground ensures that the input signal is low in case of an open input pin. The zener diode protects the input circuit against ESD pulses.

6.3 Power Stage Output

The power stages are built to be used in high side configuration (**Figure 6**).

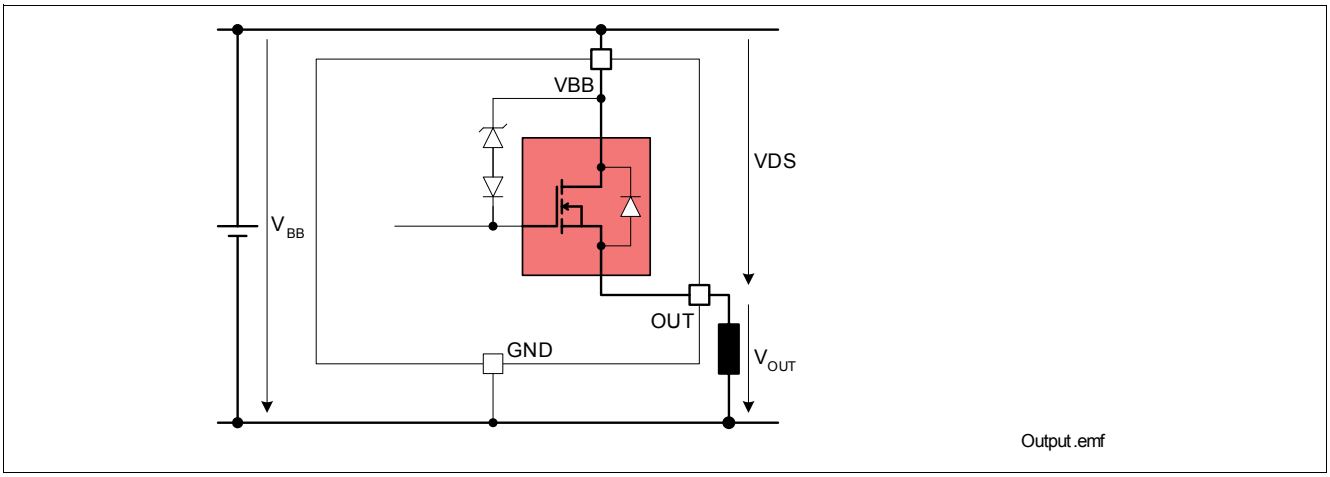


Figure 6 Power Stage Output

The power DMOS switches with a dedicated slope, which is optimized in terms of EMC emission.

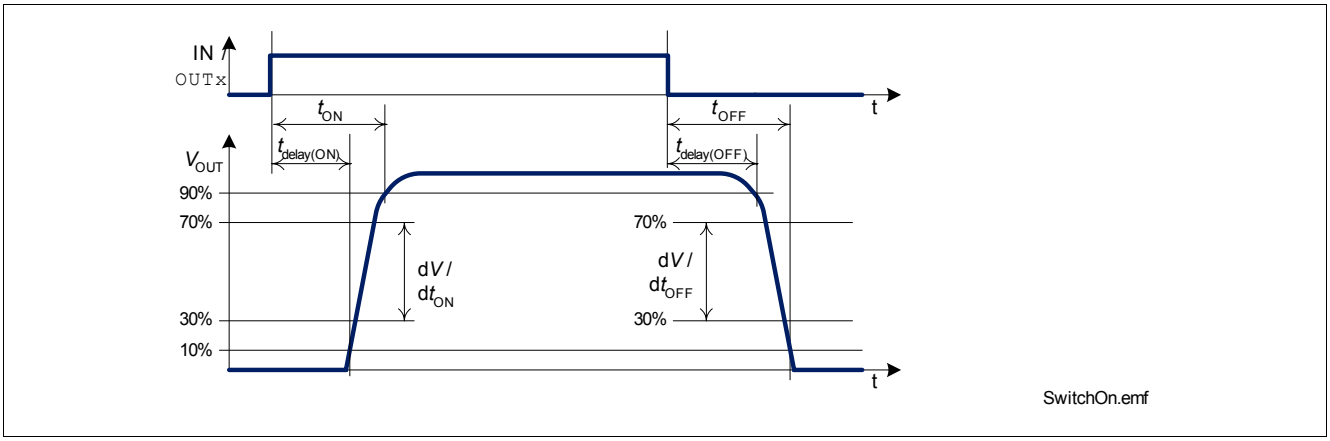


Figure 7 Switching a Load (resistive)

When switching off inductive loads with high-side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent avalanche of the device, there is a voltage clamp mechanism implemented which limits that negative output voltage to a certain level ($V_{DS(CL)}$). See **Figure 6** for details. The maximum allowed load inductance is limited.

6.4 Electrical Characteristics

Electrical Characteristics Power Stages

Unless otherwise specified: V_{BB} = 9 V to 16 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Output Characteristics							
6.4.1	On-State Resistance	$R_{DS(ON)}$				mΩ	
	channel 0, 1, 2						`PLCR.LEDn = 0`
			–	50	–		[1] T_j = 25 °C / I_L = 2.6 A
			–	85	100		T_j = 150 °C / I_L = 2.6 A
							`PLCR.LEDn = 1`
			–	170	–		[1] T_j = 25 °C / I_L = 0.6 A
			–	300	375		T_j = 150 °C / I_L = 0.6 A
	channel 3, 4		–	110	–		[1] T_j = 25 °C / I_L = 1.3 A
			–	200	260		T_j = 150 °C / I_L = 1.3 A
	channel 5		–	200	–		[1] T_j = 25 °C / I_L = 0.6 A
			–	350	460		T_j = 150 °C / I_L = 0.6 A
6.4.2	Output voltage drop limitation at small load currents	$V_{DS(NL)}$				mV	
	channel 0, 1, 2						`PLCR.LEDn = 0`
			–	25	–		I_L = 35 mA
	channel 3, 4, 5		–	25	–		I_L = 35 mA
6.4.3	Output clamp	$V_{DS(CL)}$	40	47	54	V	I_L = 20 mA [2]
6.4.4	Output leakage current per channel	$I_{L(OFF)}$				µA	V_{IN} = 0 V or floating `OUT.OUTn = 0`
	channel 0, 1, 2		–	0.1	10		stand-by
			–	–	40		idle
	channel 3, 4		–	0.1	8		stand-by
			–	–	40		idle
	channel 5		–	0.1	8		stand-by
			–	–	40		idle
6.4.5	Inverse current capability per channel	$-I_{L(IC)}$				A	[3]
	channel 0, 1, 2		–	2.5	–		–
	channel 3, 4		–	1.0	–		–
	channel 5		–	0.5	–		–
Input Characteristics							
6.4.6	L-input level	$V_{IN(L)}$	-0.3	–	1.0	V	–
6.4.7	H-input level	$V_{IN(H)}$	2.6	–	5.5	V	–
6.4.8	L-input current	$I_{IN(L)}$	3	25	75	µA	V_{IN} = 0.4 V
6.4.9	H-input current	$I_{IN(H)}$	10	40	75	µA	V_{IN} = 5 V

Electrical Characteristics Power Stages (cont'd)

Unless otherwise specified: V_{BB} = 9 V to 16 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Timings							
6.4.10	Turn-ON delay to 10% V_{BB} (Logical propagation delay from input INx to output OUTx)	$t_{delay(ON)}$				µs	V_{BB} = 13.5 V [1]
	channel 0, 1, 2						PLCR.LEDn = 0
			–	35	–		R_L = 6.8 Ω
	channel 3, 4		–	20	–		R_L = 18 Ω
	channel 5		–	30	–		R_L = 33 Ω
6.4.11	Turn-OFF delay to 90% V_{BB} (Logical propagation delay from input INx to output OUTx)	$t_{delay(OFF)}$				µs	V_{BB} = 13.5 V [1]
	channel 0, 1, 2						PLCR.LEDn = 0
			–	50	–		R_L = 6.8 Ω
	channel 3, 4		–	30	–		R_L = 18 Ω
	channel 5		–	40	–		R_L = 33 Ω
6.4.12	Turn-ON time to 90% V_{BB}	t_{ON}				µs	V_{BB} = 13.5 V
	channel 0, 1, 2						PLCR.LEDn = 0
			–	–	250		R_L = 6.8 Ω
							PLCR.LEDn = 1
			–	–	100		R_L = 33 Ω
	channel 3, 4		–	–	150		R_L = 18 Ω
	channel 5		–	–	170		R_L = 33 Ω
6.4.13	Turn-OFF time to 10% V_{BB}	t_{OFF}				µs	V_{BB} = 13.5 V
	channel 0, 1, 2						PLCR.LEDn = 0
			–	–	290		R_L = 6.8 Ω
							PLCR.LEDn = 1
			–	–	100		R_L = 33 Ω
	channel 3, 4		–	–	150		R_L = 18 Ω
	channel 5		–	–	170		R_L = 33 Ω
6.4.14	Turn-ON slew rate 30% to 70% V_{BB}	dV/dt_{ON}				V/µs	V_{BB} = 13.5 V
	channel 0, 1, 2						PLCR.LEDn = 0
			0.1	0.2	0.5		R_L = 6.8 Ω
							PLCR.LEDn = 1
			0.1	0.75	1.9		R_L = 33 Ω
	channel 3, 4		0.1	0.45	0.9		R_L = 18 Ω
	channel 5		0.1	0.45	0.9		R_L = 33 Ω

Electrical Characteristics Power Stages (cont'd)

Unless otherwise specified: V_{BB} = 9 V to 16 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
6.4.15	Turn-OFF slew rate 70% to 30% V_{BB}	$-\frac{dV}{dt_{OFF}}$				V/µs	V_{BB} = 13.5 V
	channel 0, 1, 2						PLCR.LEDn = 0
			0.1	0.2	0.5		R_L = 6.8 Ω
							PLCR.LEDn = 1
			0.1	0.75	1.9		R_L = 33 Ω
	channel 3, 4		0.1	0.45	0.9		R_L = 18 Ω
	channel 5		0.1	0.45	0.9		R_L = 33 Ω

1) Not subject to production test, specified by design.
2) The voltage increase until the current is reached.
3) Not subject to production test, specified by design. In case of inverse current (V_{OUT} > V_{BB}), the error flag ERR in the standard diagnosis of the affected channel is cleared (valid for channel 0, 1, 2, 3, 4). The inverse current capability in ON-state and OFF-state is defined for T_j < $T_{j(SC)}$ and channel remains in same state (ON-state or OFF-state). Other channels can be affected (e.g. OUT latch due to junction temperature increase).

6.5 Command Description

OUT
Output Configuration Registers

W/$\overline{R}$	RB	5	4	3	2	1	0
read/write	**0**	**OUT5**	**OUT4**	**OUT3**	**OUT2**	**OUT1**	**OUT0**

Field	Bits	Type	Description
OUTn n = 5 to 0	n	rw	**Set Output Mode for Channel n** **0** Channel n is switched off 1 Channel n is switched on

PLCR
PWM and LED-Mode Configuration Register

W/$\overline{R}$	RB	ADDR		3	2	1	0
read/write	**1**	**0**	**1**	**PWM**	**LED2**	**LED1**	**LED0**

Field	Bits	Type	Description
PWM	3	rw	**PWM Configuration** **0** Input signal OR-combined with according `OUT` register bit 1 Input signal AND-combined with according `OUT` register bit
LEDn n = 2 to 0	n	rw	**Set LED Mode for Channel n** **0** Channel n is in bulb mode 1 Channel n is in LED mode

7 Protection Functions

The device provides embedded protective functions, which are designed to prevent IC destruction under fault conditions described in this data sheet. Fault conditions are considered as “outside” normal operating range. Protective functions are neither designed for continuous nor for repetitive operation.

7.1 Over Load Protection

The load current I_L is limited by the device itself in case of over load or short circuit to ground. There are multiple steps of current limitation which are selected automatically depending on the voltage V_{DS} across the power DMOS. Please note that the voltage at the OUT pin is V_{BB} - V_{DS}. Please refer to following figures for details.

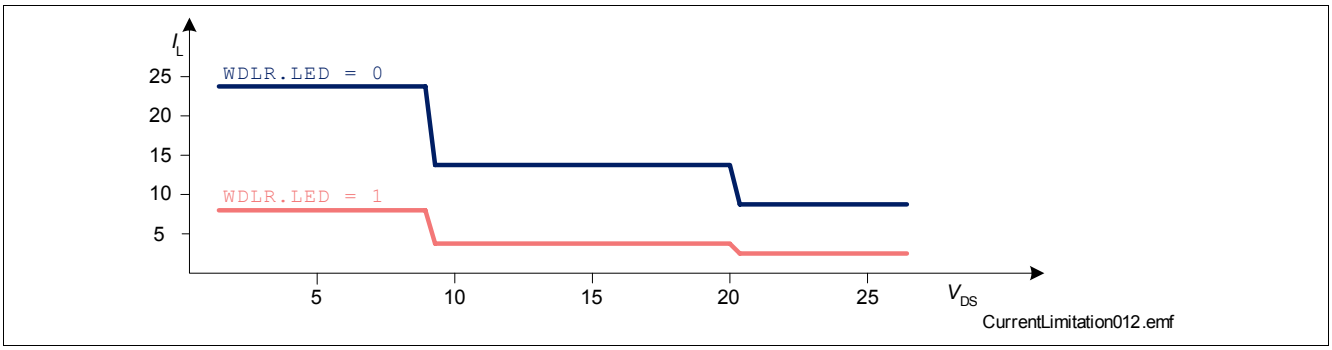


Figure 8 Current Limitation Channels 0, 1, 2 (minimum values)

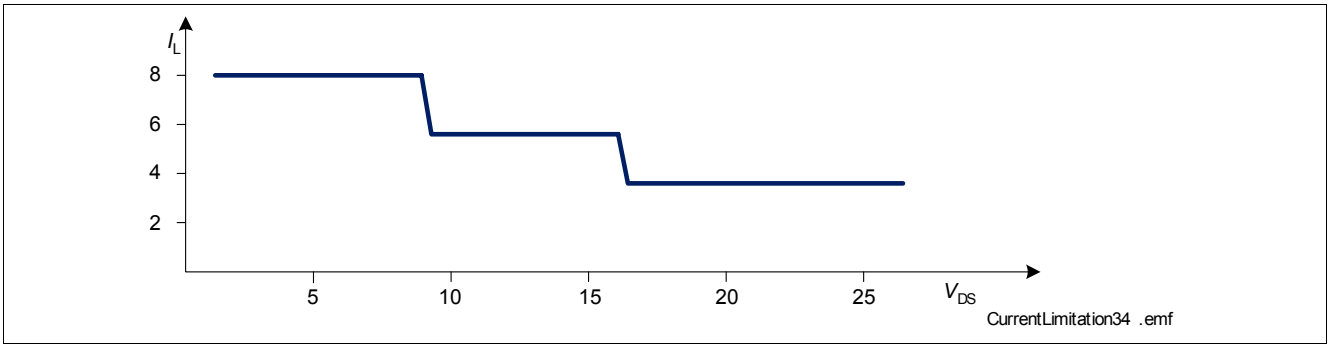


Figure 9 Current Limitation Channels 3, 4 (minimum values)

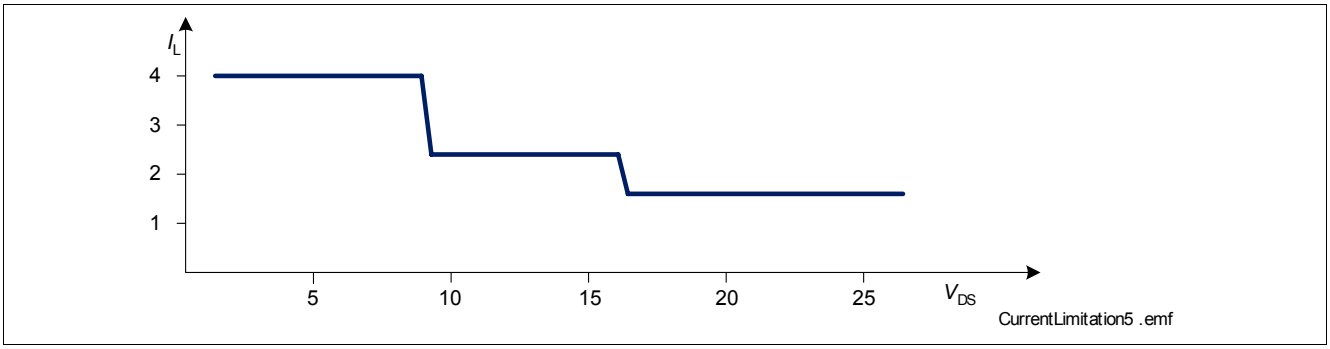


Figure 10 Current Limitation Channels 5 (minimum values)

Current limitation to the value $I_{L(LIM)}$ is realized by increasing the resistance of the output channel, which leads to rapid temperature rise inside.

7.2 Over Temperature Protection

Each channel has its own temperature sensor. If the temperature at the channel exceeds the thermal shutdown temperature $T_{j(SC)}$, the channel will switch off and latch to prevent destruction (also in case of V_{DD} = 0V). In order to reactivate the channel, the temperature at the output must drop by at least the thermal hysteresis ΔT_j and the over temperature latch must be cleared by SPI command `HWCR.CTL` = 1. All over temperature latches are cleared by SPI command `HWCR.CTL` = 1.

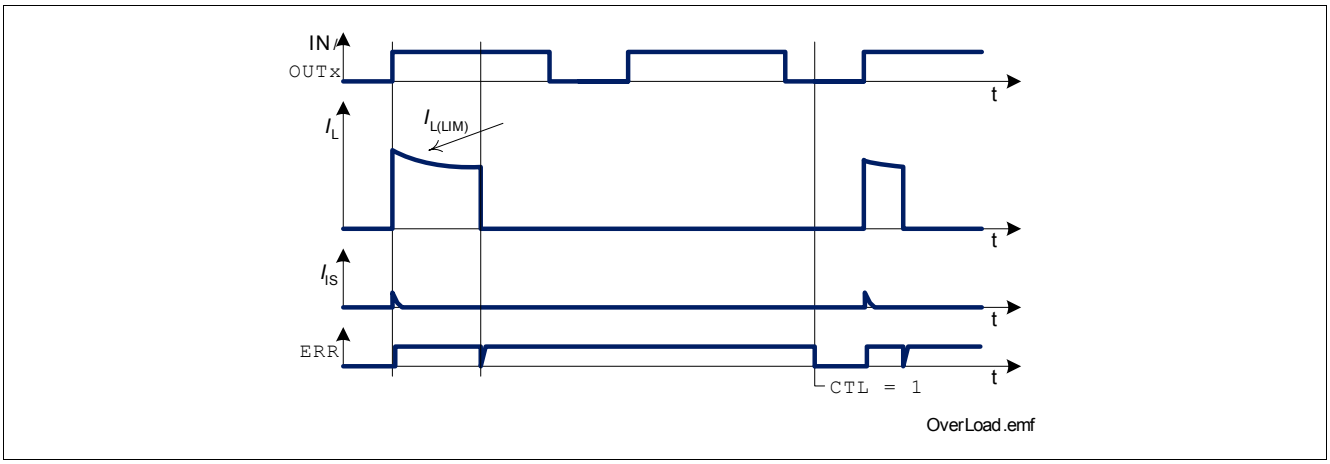


Figure 11 Shut Down by Over Temperature

Additionally, channels 0, 1, 2, 3, 4 have their own dynamic temperature sensors. The dynamic temperature sensor improves short circuit robustness by limiting sudden increases in the junction temperature. The dynamic temperature sensor turns off the channel if its sudden temperature increase exceeds the dynamic temperature sensor threshold $\Delta T_{j(SW)}$. Please refer to the following figure for details.

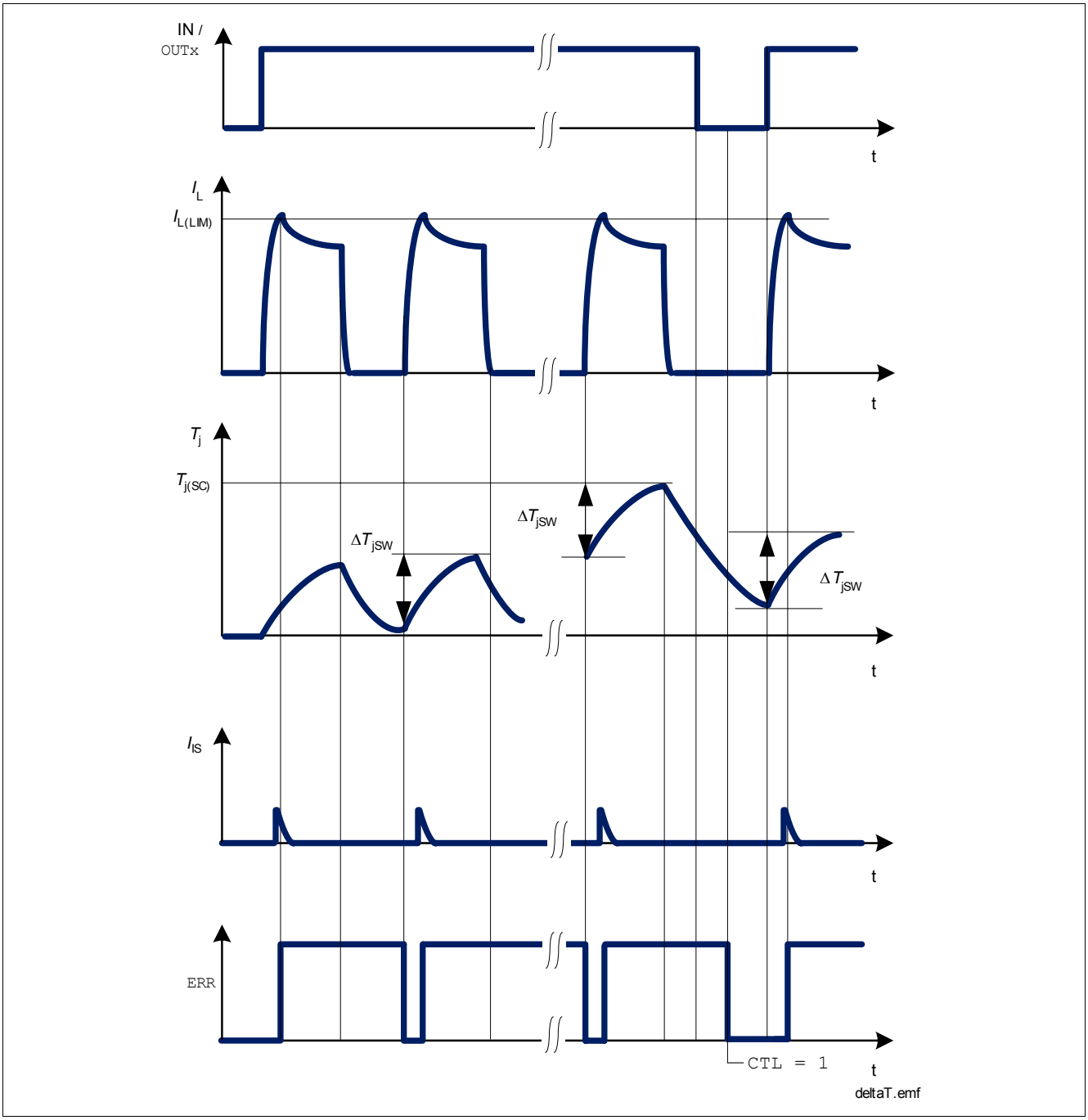


Figure 12 Dynamic Temperature Sensor Operations

The ERR-flag will be set during dynamic temperature sensor shut down. It can be reset by reading the ERR-flag. If the channel is still in dynamic temperature sensor shut down, the ERR-flag will be set again.

7.3 Reverse Polarity Protection

In reverse polarity mode, power dissipation is caused by the intrinsic body diode of each DMOS channel as well as each ESD diode of the logic pins. The reverse current through the channels has to be limited by the connected loads. The current through the ground pin, sense pin IS, the logic power supply pin V_{DD}, the SPI pins and the limp home input pin has to be limited as well (please refer to the maximum ratings listed on **Page 9**).

Note: No protection mechanism like temperature protection or current limitation is active during reverse polarity.

7.4 Over Voltage Protection

In addition to the output clamp for inductive loads as described in **Section 6.3**, there is a clamp mechanism available for over voltage protection. The current through the ground connection has to be limited during over voltage. Please note that in case of over voltage the pin GND might have a high voltage offset to the module ground.

7.5 Loss of Ground

In case of complete loss of the device ground connections, but connected load ground, the SPOC - BTS5682E securely changes to or stays in off-state excepted channel 5. If switched on before, channel 5 will remain in on-state until V_{BB} - V_{DD} > V_{BD}.

7.6 Loss of V_{BB}

In case of loss of V_{BB} connection in on-state, all inductances of the loads have to be demagnetized through the ground connection or through an additional path from V_{BB} to ground. When a diode is used in the ground path for reverse polarity reason, the ground connection is not available for demagnetization. Then for example, a resistor can be placed in parallel to the diode or a suppressor diode can be used between V_{BB} and GND.

7.7 Electrical Characteristics

Electrical Characteristics Protection Functions

Unless otherwise specified: V_{BB} = 9 V to 16 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Over Load Protection							
7.7.1	Load current limitation	$I_{L(LIM)}$				A	V_{DS} = 7 V
	channel 0, 1, 2		24	–	40		PLCR.LEDn = 0 [1]
			6	–	12		PLCR.LEDn = 1 [1]
	channel 3, 4		8	–	18		[1]
	channel 5		4	–	7		–
Over Temperature Protection							
7.7.2	Thermal shut down temperature	$T_{j(SC)}$	150	170	190	°C	[2]
7.7.3	Thermal hysteresis	ΔT_j	–	7	–	K	[2]
7.7.4	Dynamic temperature increase limitation while switching	ΔT_{jsw}	–	60	–	K	[2]
Over Voltage							
7.7.5	Overvoltage protection	$V_{BB(AZ)}$	40	47	54	V	I_{bb} = 4 mA
Loss of Ground							
7.7.6	Operating V_{BB} - V_{DD} voltage for Channel 5	V_{BD}	–	7	–	V	[2]

1) For T_j = 150 °C, not subject to production test. Device will shutdown due to the maximum junction temperature sensor.
2) Not subject to production test, specified by design.

7.8 Command Description

HWCR
Hardware Configuration Register

W/$\overline{R}$	RB	ADDR		3	2	1	0
write	**1**	**1**	**0**	**0**	**LCH**	**RST**	**CTL**

Field	Bits	Type	Description
CTL	0	rw	**Clear Thermal Latch** **0** Thermal latches are untouched 1 Command: Clear all thermal latches

8 Diagnosis

For diagnosis purpose, the SPOC - BTS5682E provides a current sense signal at pin IS and the diagnosis word via SPI. There is a current sense multiplexer implemented that is controlled via SPI. The sense signal can also be disabled by SPI command. A switch bypass monitor allows to detect a short circuit between the output pin and the battery voltage. Please refer to **Figure 13** for details.

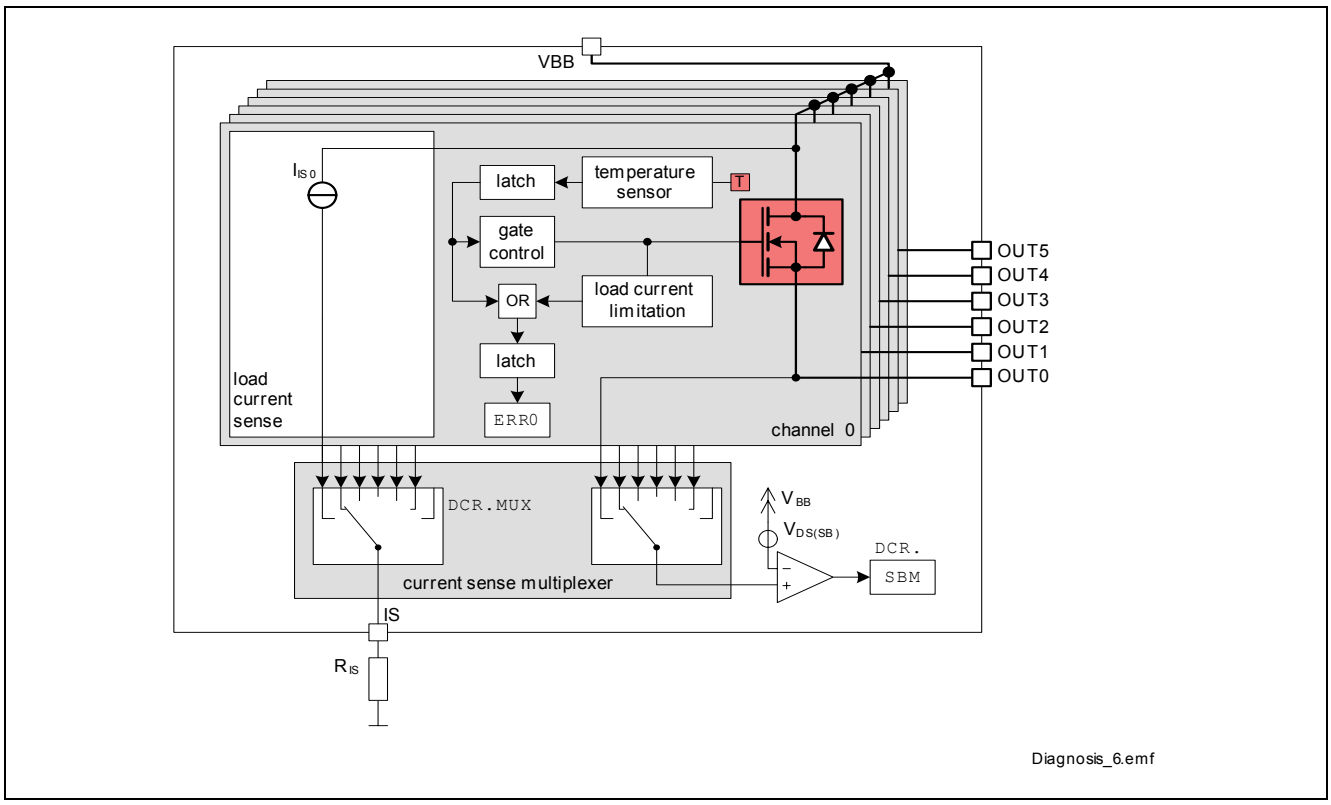


Figure 13 Block diagram: Diagnosis

For diagnosis feedback at different operation modes, please see **Table 1**.

Table 1 Operation Modes [1)]

Operation Mode	Input Level OUT.OUTn	Output Level V_{OUT}	Current Sense I_{IS}	Error Flag ERRn[2)]	DCR.SBM
Normal Operation (OFF)	L / 0 (OFF-state)	GND	Z	0	1
Short Circuit to GND		GND	Z	0	1
Thermal shut down		Z	Z	0[3)]	x
Short Circuit to V_{BB}		V_{BB}	Z	0	0
Open Load		Z	Z	0	x
Normal Operation (ON)	H / 1 (ON-state)	~V_{BB}	I_L / k_{ILIS}	0	0
Current Limitation		< V_{BB}	Z	1	x
Short Circuit to GND		~GND	Z	1	1
Dynamic Temperature Sensor shut down		Z	Z	1	x
Thermal shut down		Z	Z	1[3)]	x
Short Circuit to V_{BB}		V_{BB}	< I_L / k_{ILIS}	0	0
Open Load		V_{BB}	Z	0	0

1) L = low level, H = high level, Z = high impedance, potential depends on leakage currents and external circuit. x = undefined.

2) The error flags are latched until they are transmitted in the standard diagnosis word via SPI.

3) The over temperature flag is set latched (in OFF states also) and can be cleared by SPI command HWCR.CTL.

8.1 Diagnosis Word at SPI

The standard diagnosis at the SPI interface provides information about each channel. The error flags, an OR combination of the over temperature flags and the over load monitoring signals are provided in the SPI standard diagnosis bits ERRn.

The over load monitoring signals are latched in the error flags and cleared each time the standard diagnosis is transmitted via SPI. In detail, they are cleared between the second and third raising edge of the SCLK signal.

The over temperature flags, which cause an overheated channel to latch off, are latched directly at the gate control block. The latches are cleared by SPI command HWCR.CTL.

Please note: The over temperature information is latched twice. When transmitting a clear thermal latch command (HWCR.CTL), the error flag is cleared during command transmission of the next SPI frame and ready for latching after the third raising edge of the SCLK signal. As a result, the first standard diagnosis information after a CTL command will indicate a failure mode at the previously affected channels although the thermal latches have been cleared already. In case of continuous over load, the error flags are set again immediately because of the over load monitoring signal.

8.2 Load Current Sense Diagnosis

There is a current sense signal available at pin IS which provides a current proportional to the load current of one selected channel. The selection is done by a multiplexer which is configured via SPI.

Current Sense Signal

The current sense signal (ratio $k_{ILIS} = I_L / I_S$) is provided as long as no failure mode occurs.The ratio k_{ILIS} can be adjusted to the load type (LED or bulb) via SPI register PLCR for channels 0 to 2. Usually a resistor R_{IS} is connected to the current sense pin. It is recommended to use resistors 2.5 kΩ < R_{IS} < 7 kΩ. A typical value is 3.3 kΩ.

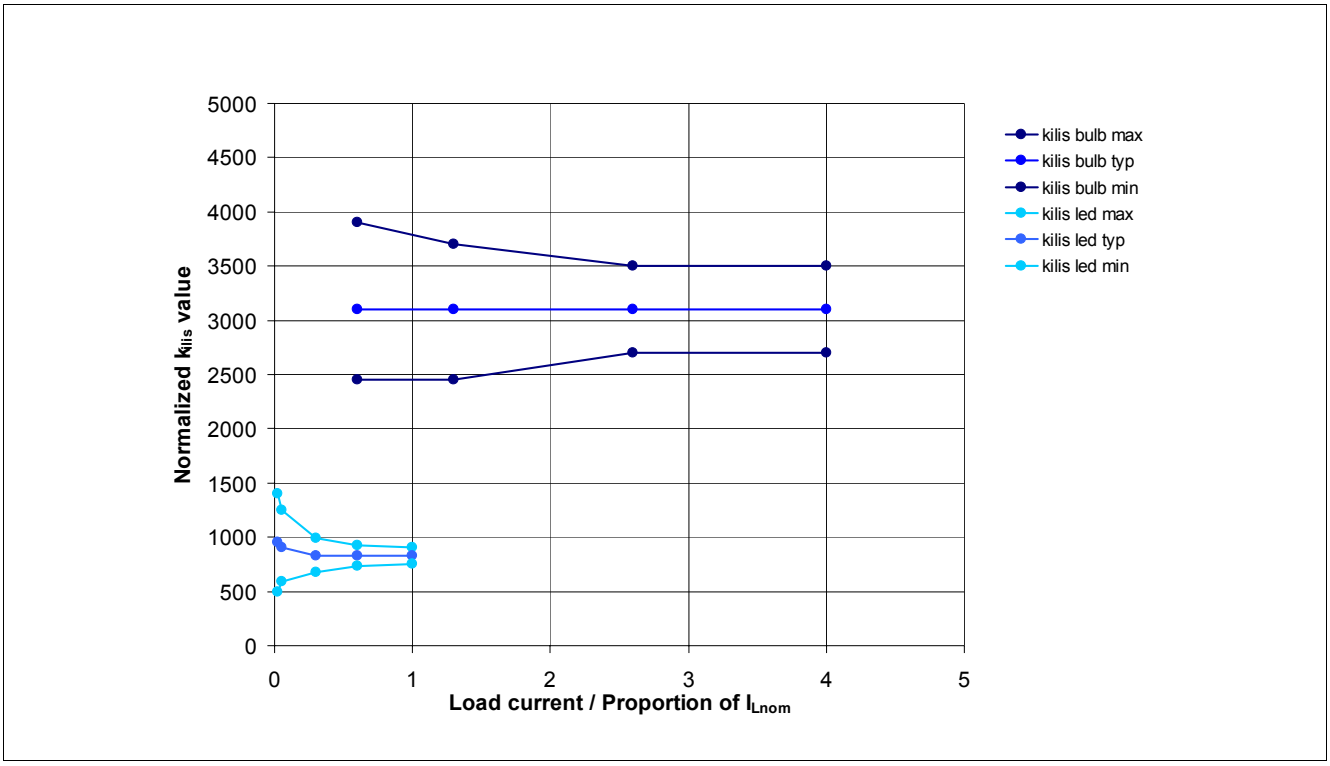


Figure 14 Current Sense Ratio k_{ILIS} Channel 0, 1, 2 Bulb and LED mode [1)]

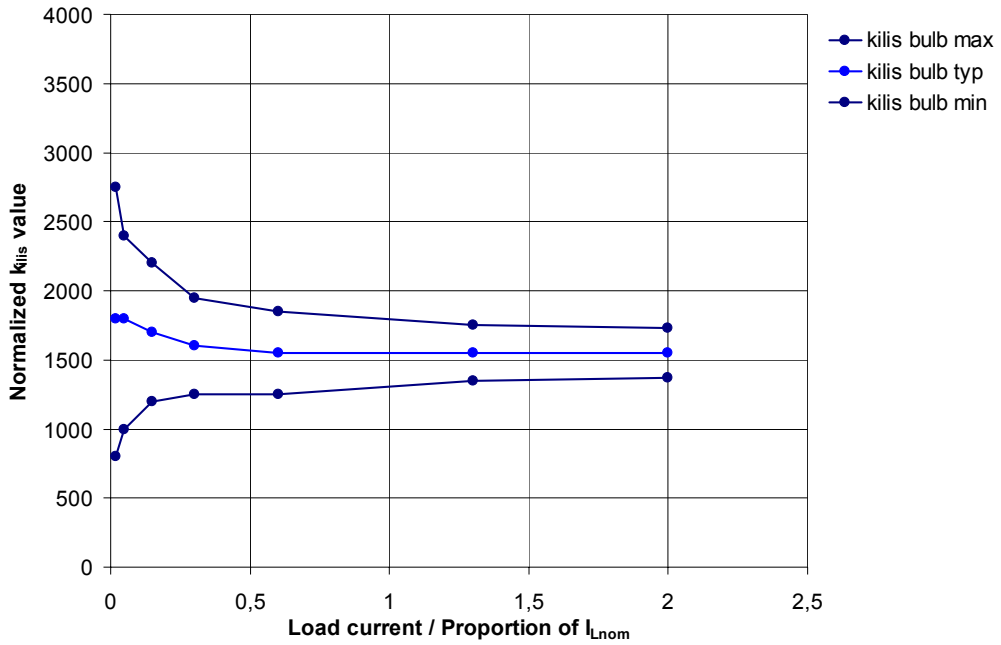


Figure 15 Current Sense Ratio k_{ILIS} Channel 3, 4[1)]

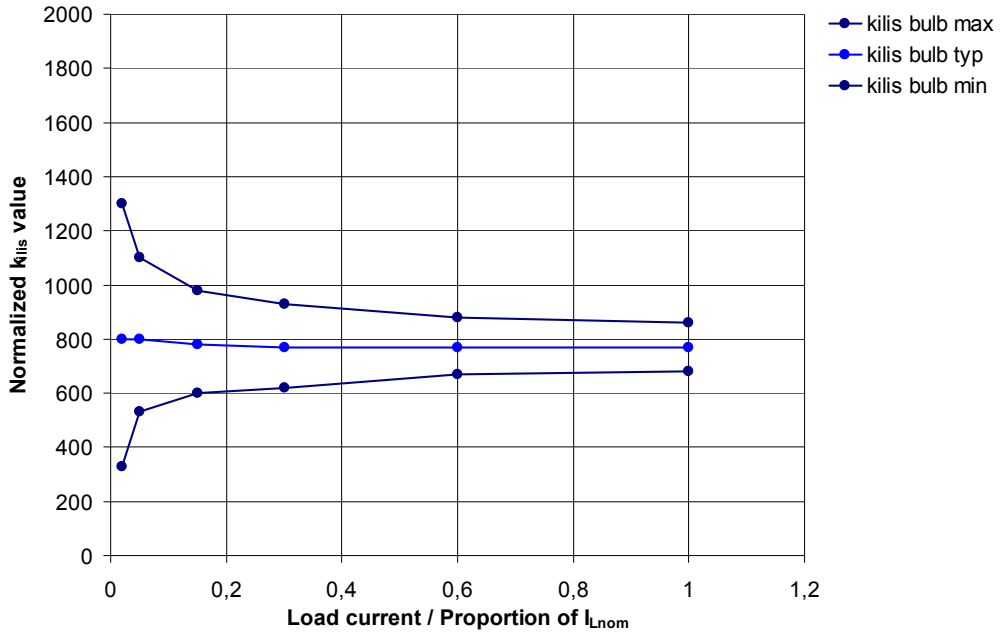


Figure 16 Current Sense Ratio k_{ILIS} Channel 5 [1)]

1) The curves show the behavior based on characterization data. The marked points are guaranteed in this Data Sheet in Section 8.4 (Position 8.4.1).

In case of over current as well as over temperature, the current sense signal of the affected channel is switched off. To distinguish between over temperature and over load, the SPI diagnosis word can be used. Whereas the over load flag is cleared every time the diagnosis is transmitted, the over temperature flag is cleared by a dedicated SPI command (HWCR.CTL).

Details about timings between the current sense signal I_{IS} and the output voltage V_{OUT} and the load current I_L can be found in **Figure 17**.

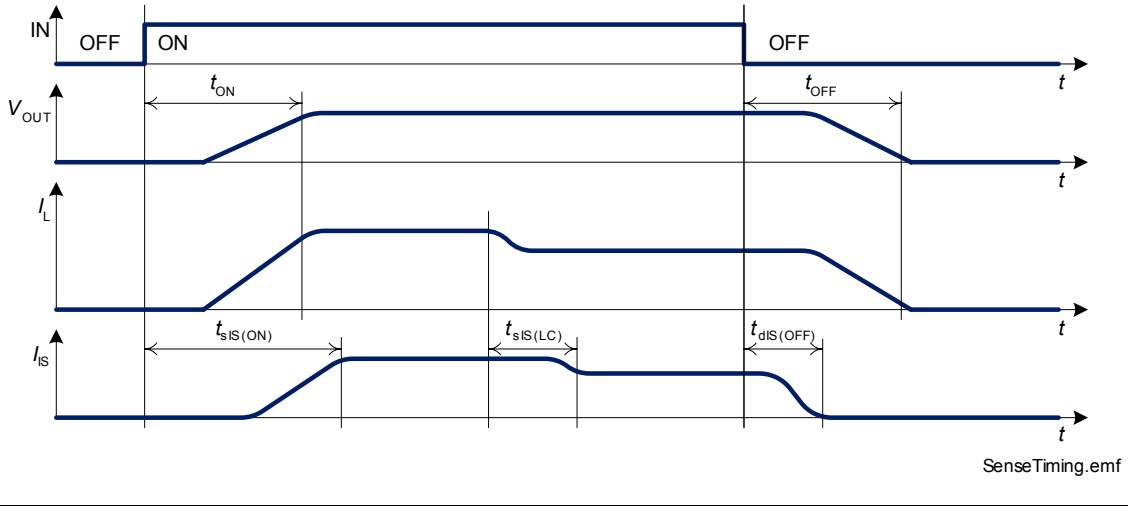


Figure 17 Timing of Current Sense Signal

Current Sense Multiplexer

There is a current sense multiplexer implemented in the SPOC - BTS5682E that routes the sense current of the selected channel to the diagnosis pin IS. The channel is selected via SPI register DCR.MUX. The sense current also can be disabled by SPI register DCR.MUX. For details on timing of the current sense multiplexer, please refer to **Figure 18**.

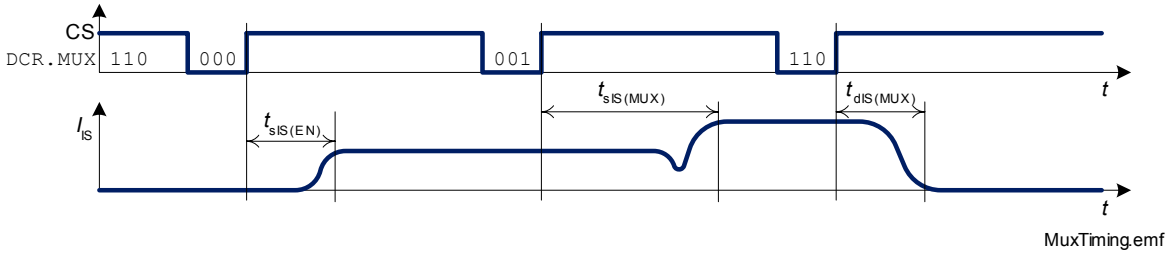


Figure 18 Timing of Current Sense Multiplexer

8.3 Switch Bypass Diagnosis

To detect short circuit to V_{BB}, there is a switch bypass monitor implemented. In case of short circuit between the output pin OUT and V_{BB} in ON-state, the current will flow through the power transistor as well as through the short circuit (bypass) with undefined ratio. As a result, the current sense signal will show lower values than expected by the load current. In OFF-state, the output voltage will stay close to V_{BB} potential which means a small V_{DS}.

The switch bypass monitor compares the voltage V_{DS} across the power transistor of that channel which is selected by the current sense multiplexer (DCR.MUX) with threshold $V_{DS(SB)}$. The result of comparison can be read in SPI register DCR.SBM.

8.4 Electrical Characteristics

Unless otherwise specified: V_{BB} = 9 V to 16 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Load Current Sense							
8.4.1	Current sense ratio	k_{ILIS}					
	channel 0, 1, 2 (bulb):						PLCR.LEDn = 0
	0.600 A		2450	3100	3900		–
	1.3 A		2450	3100	3700		–
	2.6 A		2700	3100	3500		–
	4.0 A		2700	3100	3500		–
	channel 0, 1, 2 (LED):						PLCR.LEDn = 1
	0.020 A		500	950	1400		–
	0.050 A		590	910	1250		–
	0.300 A		680	830	990		–
	0.600 A		730	830	930		–
	1.0 A		750	830	910		–
	channel 3, 4:						
	0.020 A		800	1800	2750		–
	0.050 A		1000	1800	2400		–
	0.150 A		1200	1700	2200		–
	0.300 A		1250	1600	1950		–
	0.600 A		1250	1550	1850		–
	1.3 A		1350	1550	1750		–
	2.0 A		1370	1550	1730		–
	channel 5:						
	0.020 A		330	800	1300		–
	0.050 A		530	800	1100		–
	0.150 A		600	780	980		–
	0.300 A		620	770	930		–
	0.600 A		670	770	880		–
	1.0 A		680	770	860		–
8.4.2	Current sense voltage limitation	$V_{IS(LIM)}$	$0.9V_{DD}$	V_{DD}	$1.1V_{DD}$	V	I_{IS} = 1 mA

Unless otherwise specified: V_{BB} = 9 V to 16 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
8.4.3	Current sense leakage / offset current	$I_{IS(en)}$	–	–	1	µA	I_L = 0 DCR.MUX = 000_B
8.4.4	Current sense leakage, while diagnosis disabled	$I_{IS(dis)}$	–	–	1	µA	DCR.MUX = 110_B
8.4.5	Current sense settling time after channel activation	$t_{sIS(ON)}$				µs	V_{BB} = 13.5 V R_{IS} = 3.3 kΩ
	channel 0, 1, 2						PLCR.LEDn = 0
			–	–	300		R_L = 6.8 Ω
							PLCR.LEDn = 1
			–	–	115		R_L = 33 Ω
	channel 3, 4		–	–	180		R_L = 18 Ω
	channel 5		–	–	180		R_L = 33 Ω
8.4.6	Current sense desettling time after channel deactivation	$t_{dIS(OFF)}$				µs	V_{BB} = 13.5 V [1] R_{IS} = 3.3 kΩ
			–	–	25		PLCR.LEDn = 0
			–	–	25		PLCR.LEDn = 1
8.4.7	Current sense settling time after change of load current	$t_{sIS(LC)}$				µs	V_{BB} = 13.5 V [1] R_{IS} = 3.3 kΩ
	channel 0, 1, 2						PLCR.LEDn = 0
			–	–	30		I_L = 2.6 A to 1.3 A
	channel 3, 4		–	–	30		I_L = 1.3 A to 0.6 A
	channel 5		–	–	30		I_L = 0.6 A to 0.3 A
8.4.8	Current sense settling time after current sense activation	$t_{sIS(EN)}$	–	–	25	µs	R_{IS} = 3.3 kΩ DCR.MUX: 110_B -> 000_B
8.4.9	Current sense settling time after multiplexer channel change	$t_{sIS(MUX)}$	–	–	30	µs	R_{IS} = 3.3 kΩ DCR.MUX: 000_B -> 001_B
8.4.10	Current sense deactivation time	$t_{dIS(MUX)}$	–	–	25	µs	R_{IS} = 3.3 kΩ DCR.MUX: [1] 001_B -> 110_B
Switch Bypass Monitor							
8.4.11	Switch bypass monitor threshold	$V_{DS(SB)}$	0.7	–	2.5	V	–

1) Not subject to production test, specified by design.

8.5 Command Description

DCR
Diagnosis Control Register

W/$\overline{R}$	RB	ADDR		3	2	1	0
read	**1**	**1**	**1**	**SBM**	**MUX**		
write	**1**	**1**	**1**	**0**	**MUX**		

Input Level `OUT.OUTn`	**Field**	**Bits**	**Type**	**Description**
L / `0` (OFF-state)	MUX	2:0	rw	**Set Current Sense Multiplexer Configuration** 000 IS pin is high impedance 001 IS pin is high impedance 010 IS pin is high impedance 011 IS pin is high impedance 100 IS pin is high impedance 101 IS pin is high impedance 110 IS pin is high impedance **111** Stand-by mode (IS pin is high impedance)
	SBM	3	r	**Switch Bypass Monitor**[1)] 0 $V_{DS} < V_{DS(SB)}$ 1 $V_{DS} > V_{DS(SB)}$
H / `1` (ON-state)	MUX	2:0	rw	**Set Current Sense Multiplexer Configuration** 000 current sense of channel 0 is routed to IS pin 001 current sense of channel 1 is routed to IS pin 010 current sense of channel 2 is routed to IS pin 011 current sense of channel 3 is routed to IS pin 100 current sense of channel 4 is routed to IS pin 101 current sense of channel 5 is routed to IS pin 110 IS pin is high impedance **111** Stand-by mode (IS pin is high impedance)
	SBM	3	r	**Switch Bypass Monitor**[1)] 0 $V_{DS} < V_{DS(SB)}$ 1 $V_{DS} > V_{DS(SB)}$

1) Invalid in stand-by mode

Standard Diagnosis

CS	7	6	5	4	3	2	1	0
TER	**0**	**LHI**	**ERR5**	**ERR4**	**ERR3**	**ERR2**	**ERR1**	**ERR0**

Field	Bits	Type	Description
ERRn n = 5 to 0	n	r	**Error flag Channel n** 0 normal operation 1 failure mode occurred

9 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and $\overline{CS}$. Data is transferred by the lines SI and SO at the rate given by SCLK. The falling edge of $\overline{CS}$ indicates the beginning of an access. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of $\overline{CS}$. A modulo 8 counter ensures that data is taken only, when a multiple of 8 bit has been transferred. The interface provides daisy chain capability.

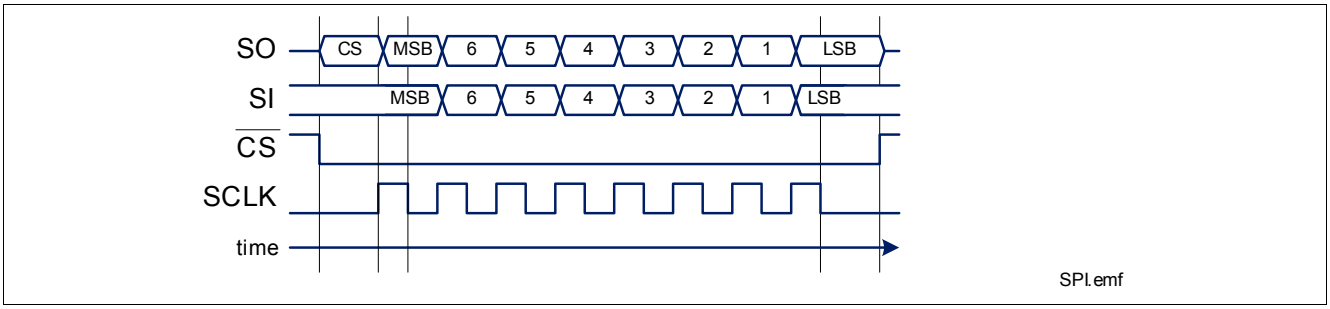


Figure 19 Serial Peripheral Interface

9.1 SPI Signal Description

$\overline{CS}$ - Chip Select:

The system micro controller selects the SPOC - BTS5682E by means of the $\overline{CS}$ pin. Whenever the pin is in low state, data transfer can take place. When $\overline{CS}$ is in high state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

$\overline{CS}$ High to Low transition:

- The requested information is transferred into the shift register.
- SO changes from high impedance state to high or low state depending on the logic OR combination between the transmission error flag (TER) and the signal level at pin SI. As a result, even in daisy chain configuration, a high signal indicates a faulty transmission. This information stays available to the first rising edge of SCLK.

$\overline{CS}$ Low to High transition:

- Command decoding is only done, when after the falling edge of $\overline{CS}$ exactly a multiple (1, 2, 3, …) of eight SCLK signals have been detected. In case of faulty transmission, the transmission error flag (TER) is set and the command is ignored.
- Data from shift register is transferred into the addressed register.

SCLK - Serial Clock:

This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in low state whenever chip select $\overline{CS}$ makes any transition.

SI - Serial Input:

Serial input data bits are shift-in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. The input data consists of two parts, control bits followed by data bits. Please refer to **Section 9.5** for further information.

SO Serial Output:

Data is shifted out serially at this pin, the most significant bit first. SO is in high impedance state until the $\overline{CS}$ pin goes to low state. New data will appear at the SO pin following the rising edge of SCLK. Please refer to **Section 9.5** for further information.

9.2 Daisy Chain Capability

The SPI of SPOC - BTS5682E provides daisy chain capability. In this configuration several devices are activated by the same $\overline{CS}$ signal $\overline{MCS}$. The SI line of one device is connected with the SO line of another device (see **Figure 20**), in order to build a chain. The ends of the chain are connected with the output and input of the master device, MO and MI respectively. The master device provides the master clock MCLK which is connected to the SCLK line of each device in the chain.

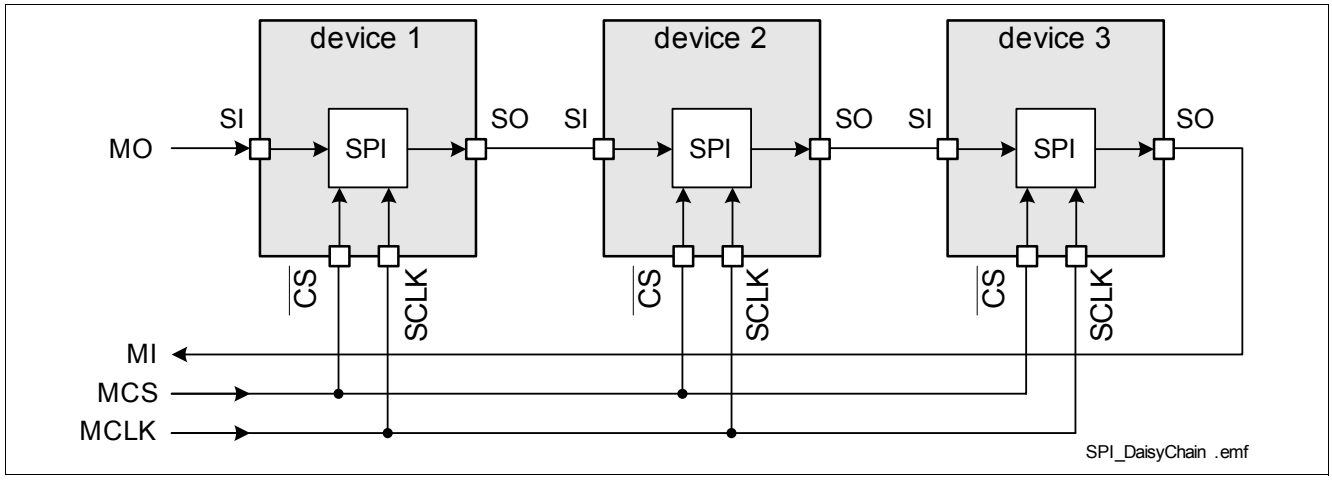


Figure 20 Daisy Chain Configuration

In the SPI block of each device, there is one shift register where one bit from SI line is shifted in each SCLK. The bit shifted out occurs at the SO pin. After eight SCLK cycles, the data transfer for one device has been finished. In single chip configuration, the $\overline{CS}$ line must turn high to make the device accept the transferred data. In daisy chain configuration, the data shifted out at device 1 has been shifted in to device 2. When using three devices in daisy chain, three times eight bits have to be shifted through the devices. After that, the $\overline{MCS}$ line must turn high (see **Figure 21**).

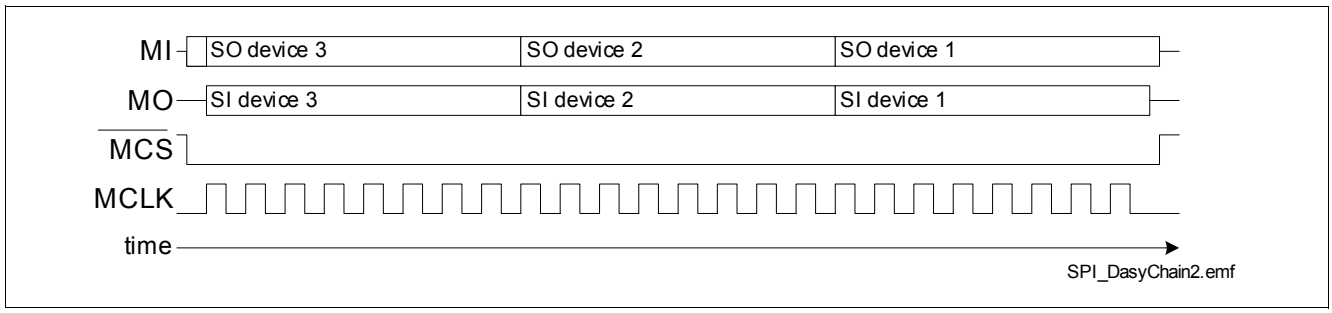


Figure 21 Data Transfer in Daisy Chain Configuration

9.3 Timing Diagrams

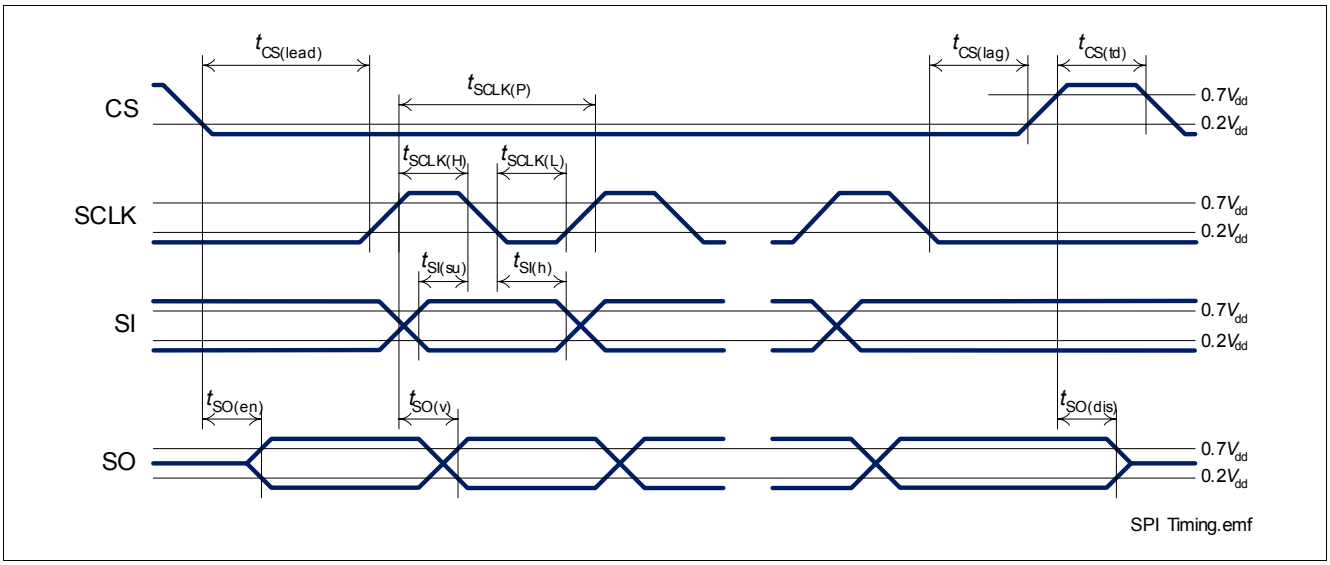


Figure 22 Timing Diagram SPI Access

9.4 Electrical Characteristics

Unless otherwise specified: V_{BB} = 9 V to 16 V, T_j = -40 °C to +150 °C, V_{DD} = 3.8 V to 5.5 V
typical values: V_{BB} = 13.5 V, T_j = 25 °C, V_{DD} = 4.3 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Input Characteristics ($\overline{CS}$, SCLK, SI)							
9.4.1	L level of pin					V	V_{DD} = 4.3 V
	$\overline{CS}$	$V_{CS(L)}$	-0.3	–	1.0		–
	SCLK	$V_{SCLK(L)}$	-0.3	–	1.0		–
	SI	$V_{SI(L)}$	-0.3	–	1.0		–
9.4.2	H level of pin					V	V_{DD} = 4.3 V
	$\overline{CS}$	$V_{CS(H)}$	2.6	–	5.5		–
	SCLK	$V_{SCLK(H)}$	2.6	–	5.5		–
	SI	$V_{SI(H)}$	2.6	–	5.5		–
9.4.3	L-input pull-up current at $\overline{CS}$ pin	$-I_{CS(L)}$	10	30	85	µA	V_{DD} = 4.3 V V_{CS} = 0 V
9.4.4	H-input pull-up current at $\overline{CS}$ pin	$-I_{CS(H)}$	3	–	85	µA	V_{DD} = 4.3 V V_{CS} = 2.6 V
9.4.5	L-input pull-down current at pin					µA	V_{DD} = 4.3 V
	SCLK	$I_{SCLK(L)}$	3	–	75		V_{SCLK} = 0.4 V
	SI	$I_{SI(L)}$	3	–	75		V_{SI} = 0.4 V
9.4.6	H-input pull-down current at pin					µA	V_{DD} = 4.3 V
	SCLK	$I_{SCLK(H)}$	10	30	75		V_{SCLK} = 4.3 V
	SI	$I_{SI(H)}$	10	30	75		V_{SI} = 4.3 V
Output Characteristics (SO)							
9.4.7	L level output voltage	$V_{SO(L)}$	0	–	0.5	V	I_{SO} = -0.5 mA

Unless otherwise specified: V_{BB} = 9 V to 16 V, T_j = -40 °C to +150 °C, V_{DD} = 3.8 V to 5.5 V
typical values: V_{BB} = 13.5 V, T_j = 25 °C, V_{DD} = 4.3 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
9.4.8	H level output voltage	$V_{SO(H)}$	V_{DD} - 0.5 V	–	V_{DD}	V	I_{SO} = 0.5 mA V_{DD} = 4.3 V
9.4.9	Output tristate leakage current	$I_{SO(OFF)}$	-10	–	10	µA	V_{CS} =V_{DD}
Timings							
9.4.10	Serial clock frequency	f_{SCLK}	0	–	2	MHz	–
9.4.11	Serial clock period	$t_{SCLK(P)}$	500	–	–	ns	–
9.4.12	Serial clock high time	$t_{SCLK(H)}$	250	–	–	ns	–
9.4.13	Serial clock low time	$t_{SCLK(L)}$	250	–	–	ns	–
9.4.14	Enable lead time (falling $\overline{CS}$ to rising SCLK)	$t_{CS(lead)}$	1	–	–	µs	–
9.4.15	Enable lag time (falling SCLK to rising $\overline{CS}$)	$t_{CS(lag)}$	1	–	–	µs	–
9.4.16	Transfer delay time (rising $\overline{CS}$ to falling $\overline{CS}$)	$t_{CS(td)}$	1	–	–	µs	–
9.4.17	Data setup time (required time SI to falling SCLK)	$t_{SI(su)}$	100	–	–	ns	–
9.4.18	Data hold time (falling SCLK to SI)	$t_{SI(h)}$	100	–	–	ns	–
9.4.19	Output enable time (falling $\overline{CS}$ to SO valid)	$t_{SO(en)}$	–	–	1	µs	C_L = 20 pF [1)]
9.4.20	Output disable time (rising $\overline{CS}$ to SO tri-state)	$t_{SO(dis)}$	–	–	1	µs	C_L = 20 pF [1)]
9.4.21	Output data valid time with capacitive load	$t_{SO(v)}$	–	–	250	ns	C_L = 20 pF [1)]

1) Not subject to production test, specified by design.

9.5 SPI Protocol

	CS[1]	7	6	5	4	3	2	1	0
		Write OUT Register							
SI		1	0	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
		Read OUT Register							
SI		0	0	x	x	x	x	x	0
		Write Configuration Register							
SI		1	1	ADDR		DATA			
		Read Configuration Register							
SI		0	1	ADDR		x	x	x	0
		Read Standard Diagnosis							
SI		0	x	x	x	x	x	x	1
		Standard Diagnosis							
SO	TER	0	LHI	ERR5	ERR4	ERR3	ERR2	ERR1	ERR0
		Second Frame of Read Command							
SO	TER	1	0	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
SO	TER	1	1	ADDR		DATA			

1) The SO pin shows this information between $\overline{CS}$ hi -> lo and first SCLK lo -> hi transition.

Note: Reading a register needs two SPI frames. In the first frame the RD command is sent. In the second frame the output at SPI signal SO will contain the requested information. A new command can be executed in the second frame.

Field	Bits	Type	Description
RB	6	rw	**Register Bank** **0** Read / write to the OUTx channel 1 Read / write to the other register
TER	CS	r	**Transmission Error** **0** Previous transmission was successful (modulo 8 clocks received) 1 Previous transmission failed or first transmission after reset
OUTx x = 5 to 0	x	rw	**Output Control Register of Channel x** **0** OFF 1 ON
ADDR	5:4	rw	**Address** Pointer to register for read and write command
DATA	3:0	rw	**Data** Data written to or read from register selected by address ADDR
LHI	6	r	**Limp Home Enable** **0** L-input signal at pin LHI 1 H-input signal at pin LHI
ERRx x = 5 to 0	x	r	**Diagnosis of Channel x** **0** No failure 1 Over temperature, over load or short circuit

9.6 Register Overview

Name	W/$\overline{R}$	RB	5	4	3	2	1	0	default[1)]
OUT	W/R	0	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0	00_H

Name	W/$\overline{R}$	RB	ADDR		3	2	1	0	default[1)]
PLCR	W/R	1	0	1	PWM	LED2	LED1	LED0	00_H
HWCR	R	1	1	0	CH5	LCH	STB	CTL	06_H
	W	1	1	0	0	LCH	RST	CTL	-
DCR	R	1	1	1	SBM	MUX			07_H
	W	1	1	1	0	MUX			-

1) The default values are set after reset.

10 Application Description

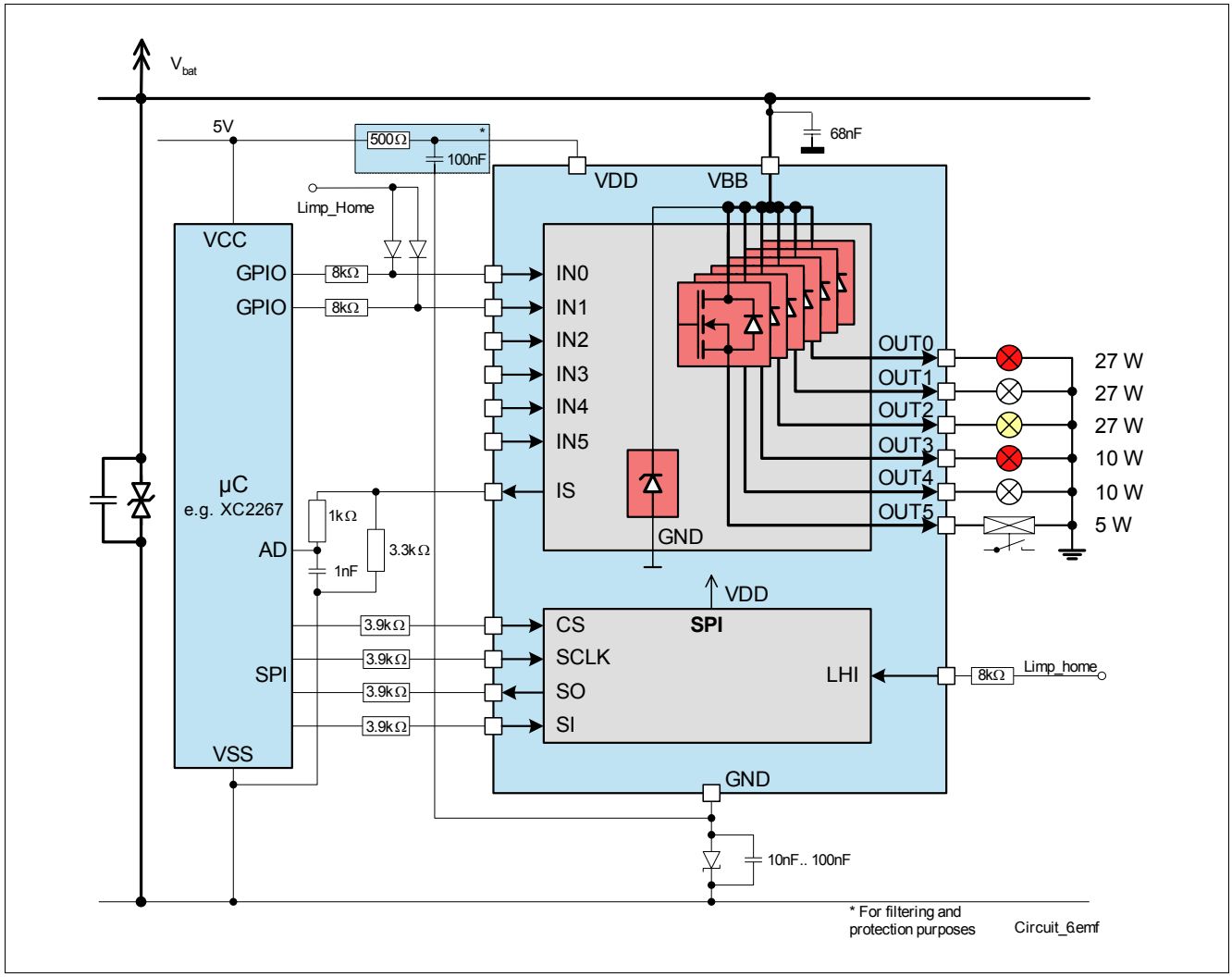
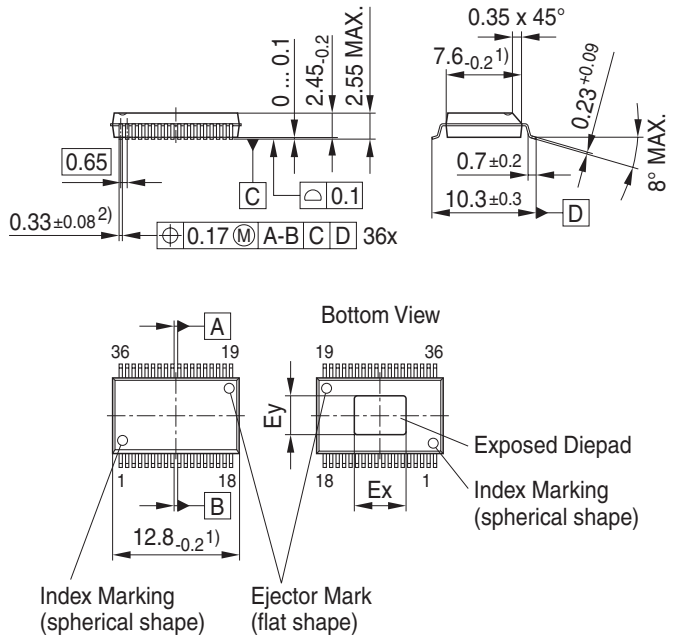


Figure 23 Application Circuit Example

11 Package Outlines SPOC - BTS5682E



Exposed Diepad Dimensions			
Package	Leadframe	Ex	Ey
PG-DSO-36-36	C66065-A6940-C016	6.8	4.2

1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side

PG-DSO-36-36-PO V01

Figure 24 PG-DSO-36-36 (Plastic Dual Small Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

12 Revision History

Revision	Date	Changes
1.0	08-01-22	Initial revision

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