



**THE DATASHEET OF  
BQ77PL900EVM-001**



## Five to Ten Series Cell Lithium-Ion or Lithium-Polymer Battery Protector and Analog Front End

### FEATURES

- 5, 6, 7, 8, 9, or 10 Series-Cell Primary Protection
- PMOS FET Drive for Charge and Discharge FETs
- Capable of Operation with 1-m $\Omega$  Sense Resistor
- Supply Voltage Range from 7 V to 50 V
- Low Supply Current of 450  $\mu$ A Typical
- Integrated 5-V, 25-mA LDO
- Integrated 3.3-V, 25-mA LDO
- Stand-Alone Mode
  - Pack Protection Control and Recovery
  - Individual Cell Monitoring
  - Integrated Cell Balancing
  - Programmable Threshold and Delay Time for
    - Overvoltage
    - Undervoltage
    - Overcurrent in Discharge
    - Short Circuit in Discharge
  - Fixed Overtemperature Protection
- Host Control Mode
  - I<sup>2</sup>C Interface to Host Controller
  - Analog Interface for Host Cell Measurement and System Charge/Discharge Current
  - Host-Controlled Protection Recovery
  - Host-Controlled Cell Balancing

### APPLICATIONS

- Cordless Power Tools
- Power Assisted Bicycle/Scooter
- Uninterruptible Power Supply (UPS) Systems
- Medical Equipment
- Portable Test Equipment

### DESCRIPTION

The bq77PL900 is a five to ten series cell lithium-ion battery pack protector. The integrated I<sup>2</sup>C communications interface allows the bq77PL900 also to be as an analog front end (AFE) for a Host controller. Two LDOs, one 5-V, 25-mA and one 3.3-V, 25-mA, are also included and may be used to power a host controller or support circuitry.

The bq77PL900 integrates a voltage translation system to extract battery parameters such as individual cell voltages and charge/discharge current. Variables such as voltage protection thresholds and detection delay times can be programmed by using the internal EEPROM.

The bq77PL900 can act as a stand-alone self-contained battery protection system (stand-alone mode). It can alternatively be combined with a host microcontroller to offer fuel gauge or other battery management capabilities to the host system (host-control mode).

The bq77PL900 provides full safety protection for overvoltage, undervoltage, overcurrent in discharge, and short circuit in discharge conditions. When the EEPROM programmable safety thresholds are reached, the bq77PL900 turns off the FET drive autonomously. No external components are needed to configure the protection features.

The analog front end (AFE) outputs allow a host controller to observe individual cell voltages and charge/discharge currents. The host controller's analog-to-digital converter connects to the bq77PL900 to acquire these values.

Cell balancing can be performed autonomously, or the host controller can activate it individually via a cell bypass path integrated into the bq77PL900. Internal control registers accessible via the I<sup>2</sup>C interface configure this operation. The maximum balancing bypass current is set via an external series resistor and the internal FET-on resistance (typically 400  $\Omega$ ). Optionally, external bypass cell balance FETs can be used for increased current capability.

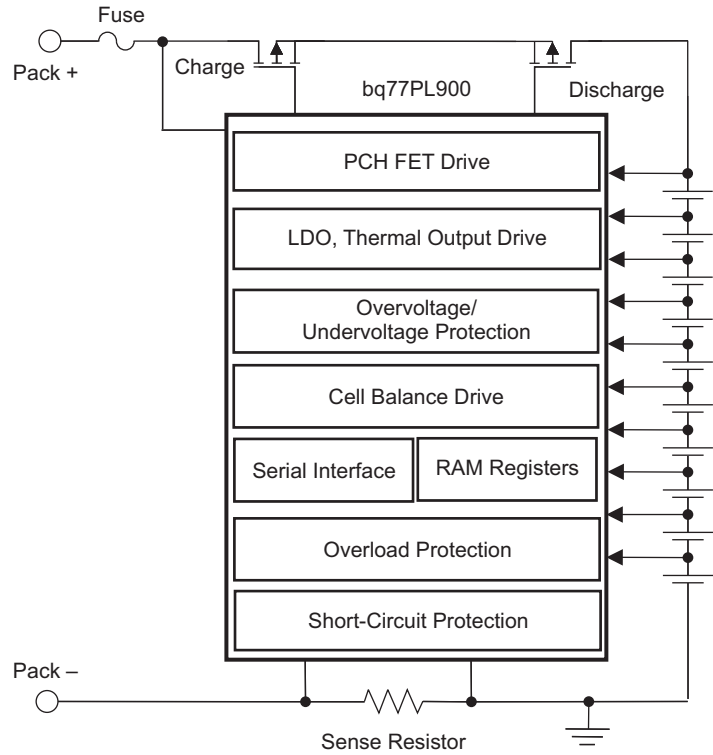


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



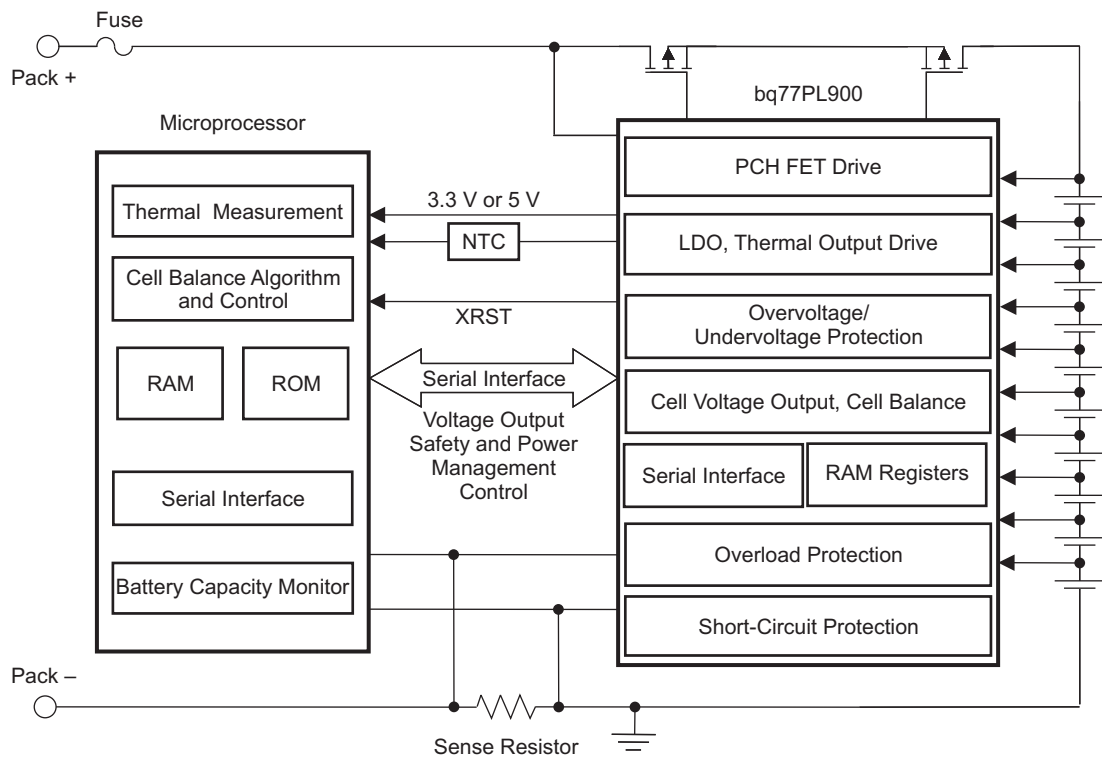
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**TYPICAL IMPLEMENTATION**



B0323-01

**Figure 1. Stand-Alone Mode**



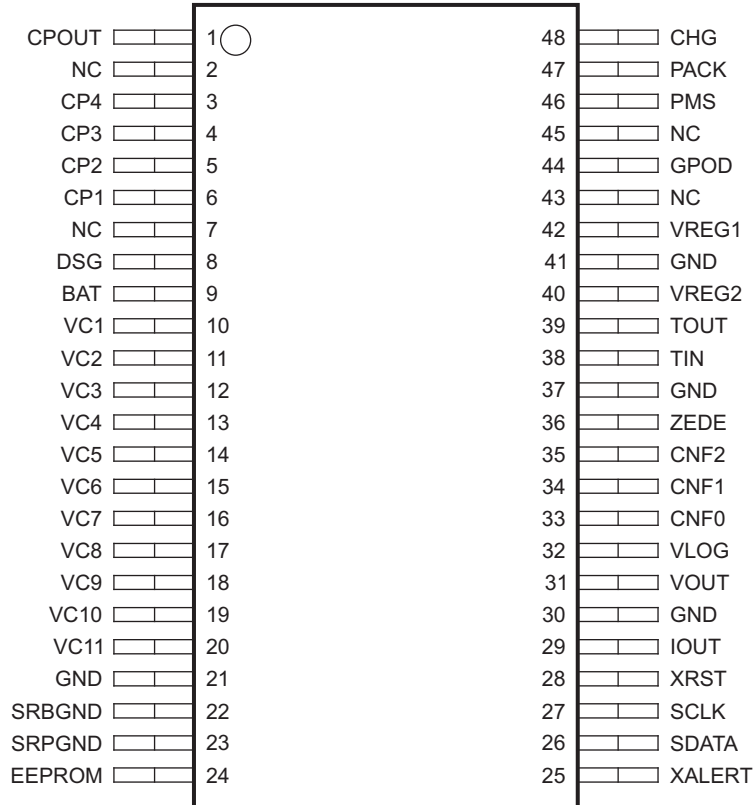
B0324-01

Figure 2. Host-Control Mode

## PIN DETAILS

### Pin Out Diagram

DL Package  
(Top View)



P0084-01

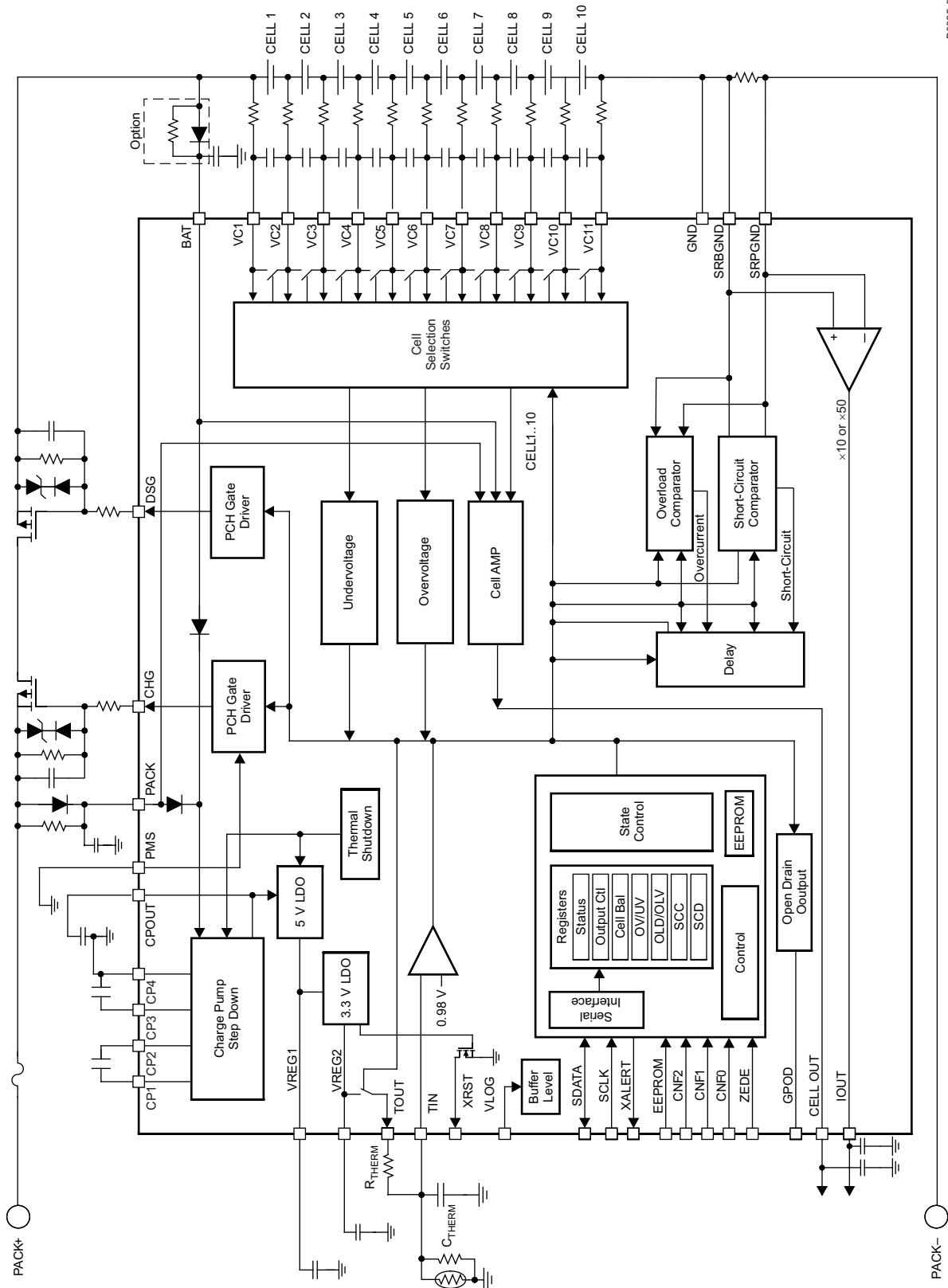
### TERMINAL FUNCTIONS

NAME	PIN #	DESCRIPTION
BAT	9	Power supply voltage
CHG	48	Charge FET gate drive
CNF0	33	Used cell for number determination in combination with CNF1 and CNF2
CNF1	34	Used cell for number determination in combination with CNF0 and CNF2
CNF2	35	Used cell for number determination in combination with CNF0 and CNF1
CP1	6	Charge pump capacitor 2 connection terminal
CP2	5	Charge pump capacitor 2 connection terminal
CP3	4	Charge pump capacitor 1 connection terminal
CP4	3	Charge pump capacitor 1 connection terminal (GND)
CPOUT	1	Charge pump output and internal power source.
DSG	8	Discharge FET gate drive
EEPROM	24	Active-high EEPROM write-enable pin. During normal operation, should be connected to GND
GND	21, 30, 37	Power-supply ground
GPOD	44	General-purpose N-CH FET open-drain output
GND	41	Should be connected to GND
IOUT	29	Amplifier output for charge/discharge current measurement

**TERMINAL FUNCTIONS (continued)**

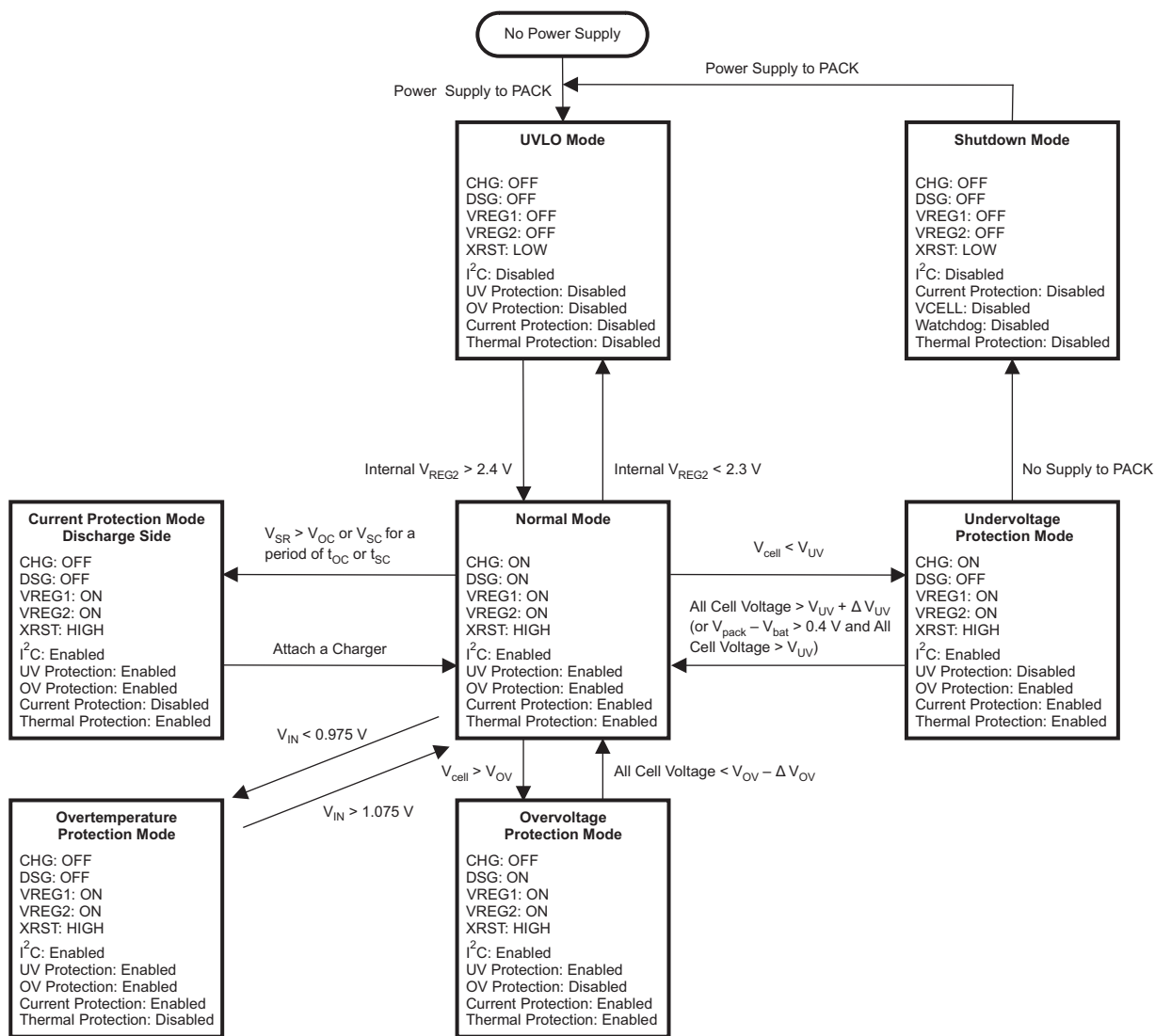
NAME	PIN #	DESCRIPTION
NC	2, 7, 43, 45	No connect (not electrically connected)
PACK	47	PACK positive terminal and alternative power source
PMS	46	Determines CHG output state for zero-volt charge
SCLK	27	Open-drain bidirectional serial interface clock with an internal 10-k $\Omega$ pullup to V <sub>LOG</sub>
SDATA	26	Open-drain bidirectional serial interface data with an internal 10-k $\Omega$ pullup to V <sub>LOG</sub>
SRBGND	22	Current sense terminal (Connect Battery to cell's GND)
SRPGND	23	Current-sense positive terminal when discharging relative to SRNGND, current-sense negative terminal when charging relative to SRGND. (Connect to pack GND)
TIN	38	Temperature sensing input
TOUT	39	Thermistor bias current source
VC1	10	Sense voltage input terminal for most positive cell, balance current input for most positive cell, and battery stack measurement input
VC2	11	Sense voltage input terminal for second-most positive cell, balance current input for second-most positive cell, and return balance current for most positive cell
VC3	12	Sense voltage input terminal for third-most positive cell, balance current input for third-most positive cell, and return balance current for second-most positive cell
VC4	13	Sense voltage input terminal for fourth-most positive cell, balance current input for fourth-most positive cell, and return balance current for third-most positive cell
VC5	14	Sense voltage input terminal for fifth-most positive cell, balance current input for fifth-most positive cell, and return balance current for fourth-most positive cell
VC6	15	Sense voltage input terminal for sixth-most positive cell, balance current input for sixth-most positive cell, and return balance current for fifth-most positive cell
VC7	16	Sense voltage input terminal for seventh-most positive cell, balance current input for seventh-most positive cell, and return balance current for sixth-most positive cell
VC8	17	Sense voltage input terminal for eighth-most positive cell, balance current input for eighth-most positive cell, and return balance current for seventh-most positive cell
VC9	18	Sense voltage input terminal for ninth-most positive cell, balance current input for ninth-most positive cell, and return balance current for eighth-most positive cell
VC10	19	Sense voltage input terminal for tenth-most positive cell, balance current input for tenth-most positive cell, and return balance current for ninth-most positive cell
VC11	20	Sense voltage input terminal for most negative cell, return balance current for least positive cell
VLOG	32	Data I/O voltage set by connecting either VREG1 or VREG2
VOUT	31	Amplifier output for cell voltage measurement
VREG1	42	Integrated 5-V regulator output
VREG2	40	Integrated 3.3-V regulator output
XALERT	25	Open-drain output used to indicate status register change. (Includes an internal 100-k $\Omega$ pullup to V <sub>LOG</sub> .)
XRST	28	Power-on-reset output. Active-low open-drain output with an internal 3-k $\Omega$ pullup to V <sub>LOG</sub>
ZEDE	36	Protection delay test pin. Minimizes protection delay times when connected to V <sub>LOG</sub> . Programmed delay times used when pulled to GND, normal operation.

FUNCTIONAL BLOCK DIAGRAM



B0325-01

### 4 SAFETY STATE OVERVIEW

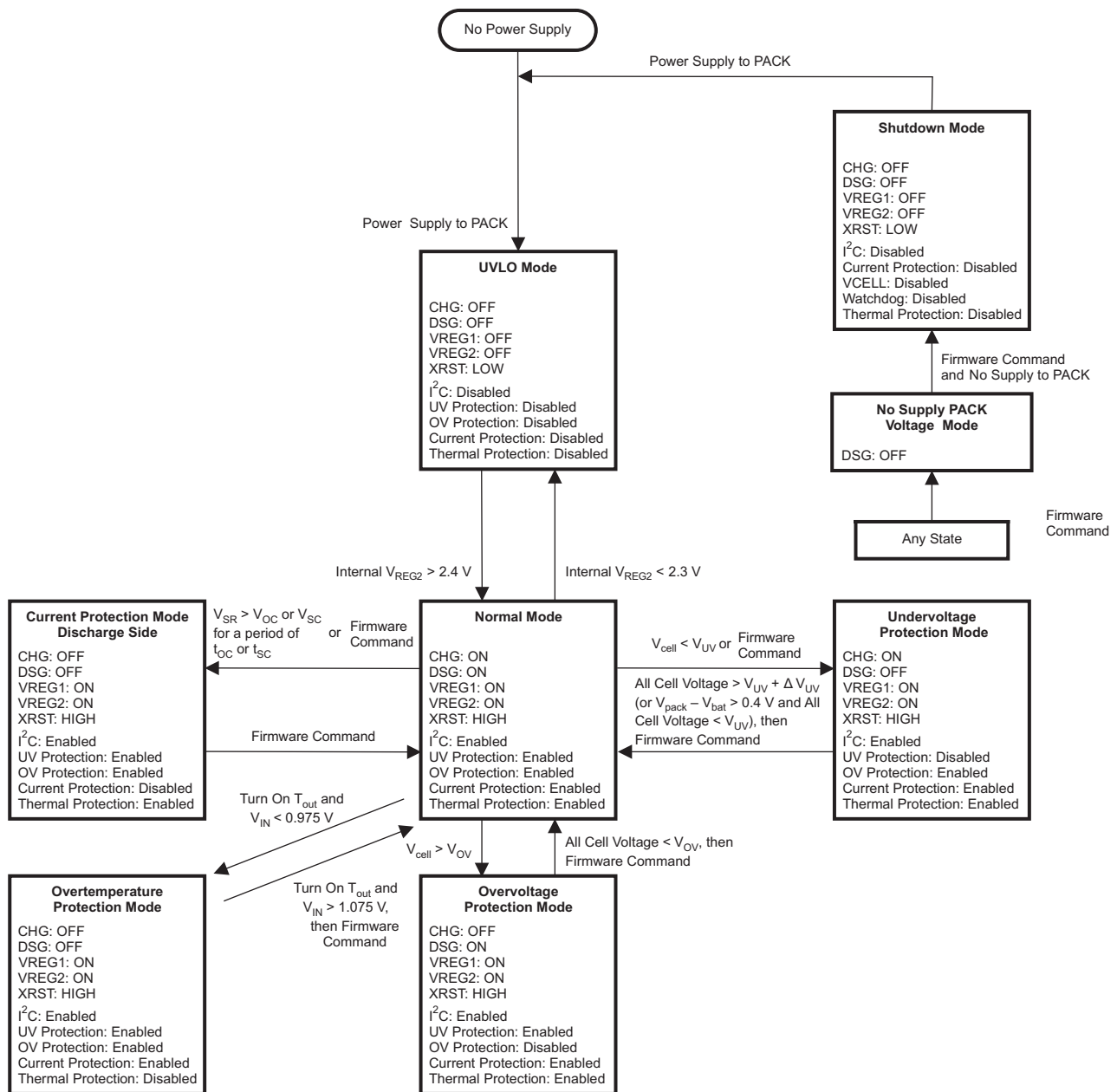


B0326-01

Figure 3. Stand-Alone Mode

Table 1. Stand-Alone STATUS Bit, XALERT and FET Transition Summary

MODE TRANSITION	STATUS BIT	XALERT	FET ACTIVITY
Normal to current protection	SCD or OCD = 1	H to L	DSG and CHG off
Current protection to normal	SCD or OCD = 0	L to H	DSG and CHG on
Normal to overvoltage protection	OVP = 1	H to L	CHG off
Overtemperature protection to normal	OVP = 0	L to H	CHG on
Normal to undervoltage protection (when VPACK goes down to 0 V, move to shutdown mode)	UVP = 1	H to L	DSG off
Undervoltage protection to normal	UVP = 0	L to H	DSG on
Normal to overtemperature	OVT = 1	H to L	DSG and CHG off
Overtemperature to normal	OVT = 0	L to H	DSG and CHG on



B0327-01

Figure 4. Host-Control Mode

**Table 2. Host Control Summary**

MODE TRANSITION		FUNCTION AND FIRMWARE PROCEDURE
Normal to current protection		Vsr > Voc or Vsc for period of toc or tsc Automatically, DSG and CHG turn off, SCD or OCD status changes = 1, XALERT = L
Current protection to normal		<ol style="list-style-type: none"> <li>1. Send commands to transition LTCLR from 0 to 1 to 0</li> <li>2. Read status bit. XALERT would change to H.</li> <li>3. Set CHG and DSG FET ON to enable normal operation</li> </ol>
Normal to overvoltage protection		Vcell > Vov for period of tov Automatically, CHG turns off, UV status changes = 1, XALERT = L
Overvoltage protection to normal		<ol style="list-style-type: none"> <li>1. Confirm the OVP protection status is cleared</li> <li>2. Send command LTCLR from 1 to 0</li> <li>3. Read status bit. XALERT changes to H.</li> <li>4. Set CHG FET ON to enable normal operation</li> </ol>
Normal to undervoltage protection	UVFET_DIS = 0	Vcell < Vuv for period of tuv Automatically, DSG turns off, UV status changes = 1, XALERT = L
	UVFET_DIS = 1	<ol style="list-style-type: none"> <li>1. Vcell &lt; Vuv or for period of tuv, UV status changes = 1, XALERT = L</li> <li>2. Send commands to turn off DSG.</li> </ol>
Undervoltage protection to normal	UVFET_DIS = X	<ol style="list-style-type: none"> <li>1. Confirm the OVP protection status is cleared</li> <li>2. Send command LTCLR from 1 to 0</li> <li>3. Set DSG FET ON to enable normal operation</li> <li>4. Read status bit. XALERT changes to H.</li> </ol>
Normal to overtemperature		<ol style="list-style-type: none"> <li>1. Send commands to turn on TOUT</li> <li>2. If TIN voltage &lt; 0.975 V, DSG and CHG turn off, OVTEMP status changes = 1, XALERT = L</li> </ol>
Overtemperature to normal		<ol style="list-style-type: none"> <li>1. Send commands to turn on TOUT (To return to normal mode, bq77PL900 must acknowledge Vth &gt; 1.075 V)</li> <li>2. Send commands to transition LTCLR from 1 to 0</li> <li>3. Set CHG and DSG FET ON</li> <li>4. Read status bit. XALERT changes to H.</li> </ol>
Any mode to shutdown		<ol style="list-style-type: none"> <li>1. Set DSG FET OFF</li> <li>2. Wait until PACK voltage decreases to 0 V</li> <li>3. SET shutdown bit to 1</li> </ol>

**ORDERING INFORMATION**

T <sub>A</sub>	PACKAGED SSOP48
–40°C to 100°C	bq77PL900DL <sup>(1)</sup>

(1) The bq77PL900 can be ordered in tape and reel by adding the suffix R to the orderable part number, i.e., bq77PL900DLR.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

			VALUE	UNIT
V <sub>MAX</sub>	Supply voltage range	BAT, PACK	–0.3 to 60	V
V <sub>IN</sub>	Input voltage range	VC1–VC10	–0.3 to 60	V
		VC11	–0.3 to 0.3	
		VCn to VCn + 1, n = 1 to 10	–0.3 to 8	
		PMS	–0.3 to 60	
		SRP, SRN	–0.5 to 1	
		SDATA, SCLK, EEPROM, VLOG, ZEDE, CNF0, CNF1, CNF2, TIN	–0.3 to 7	
V <sub>O</sub>	Output voltage range	CHG	PACK – 20 to 60	V
		DSG	BAT – 20 to 60	
		TOUT, VOUT, IOUT, XRST, XALERT, SDATA, SCLK	–0.3 to 7	
		CP1, CP2, CP3, CP4, CPOUT, GPOD	–0.3 to 60	
		VREG1	–0.3 to 8	
		VREG2	–0.3 to 3.6	
I <sub>CB</sub>	Current for cell balancing		10	mA
T <sub>STG</sub>	Storage temperature range		–65 to 150	°C
T <sub>SOLDER</sub>	Lead temperature (soldering, 10 s)		300	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground of this device except VCn – VC(n+1), where n=1 to 10 cell voltage.

## DISSIPATION RATINGS

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> ≥ 70°C	T <sub>A</sub> = 85°C POWER RATING	T <sub>A</sub> = 100°C POWER RATING
DL	1388 mW	11.1 mW/°C	720 mW	555 mW

**RECOMMENDED OPERATING CONDITIONS**

			MIN	NOM	MAX	UNIT
Supply Voltage		PACK, BAT	7		50	V
$V_{I(STARTUP)}$		Start-up voltage PACK	7.5			V
$V_{LOG}$	Logic supply voltage		$0.8 \times V_{REG2}$		$1.2 \times V_{REG1}$	V
$V_I$	Input voltage range	VC1 to VC10	0		BAT	V
		VC11	0		0.5	
		SRP, SRN	-0.3		0.5	
		$VC_n - VC_{(n+1)}$ , (n = 1 to 10)	0		7	
		PACK, BAT			50	
$V_{IH}$	Logic level input voltage high	SCLK, SDATA, EEPROM, VLOG (VLOG = VREG1 or VREG2)	$0.8 \times V_{LOG}$		$V_{LOG}$	
$V_{IL}$	Logic level input voltage low		0		$0.2 \times V_{LOG}$	
$V_O$	Output voltage range	XALERT, SDATA			$V_{LOG}$	V
		VOUT, IOUT	VGAIN = High	1.2		
			VGAIN = Low	0.975		
GPOD				45	V	
$R_{VCX}$				400		$\Omega$
$I_{REGOUT}$		I(reg1 + reg2)			25	mA
$C_{REG1}$	External 5-V REG capacitor		2.2			$\mu F$
$C_{REG2}$	External 3.3-V REG capacitor		2.2			$\mu F$
$C_{CP1}, C_{CP2}$	Charge pump flying capacitor		1			$\mu F$
$C_{CPOUT}$	Charge pump output capacitor		4.7			$\mu F$
$C_{VOUT}$	Output capacitance		0.1			$\mu F$
$C_{IOUT}$	Output capacitance		0.1			$\mu F$
$I_{OL}$		GPOD, XRST			1	mA
$f_{SCLK}$	Input frequency	SCLK			100	kHz
	EEPROM number of writes				3	
$T_{OPR}$	Operating temperature		-25		85	$^{\circ}C$
$T_{FUNC}$	Functional temperature		-40		100	$^{\circ}C$

### ELECTRICAL CHARACTERISTICS

BAT = PACK = 7 V to 50 V, T<sub>A</sub> = –25°C to 85°C, typical values stated where T<sub>A</sub> = 25°C and BAT = PACK = 36 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>SUPPLY CURRENT</b>							
I <sub>CC1</sub>	Supply current 1	No load at REG1, REG2, TOUT, SCLK, SDIN, XALERT, CELLAMP, CURRENTAMP = off CHG, DSG = on, cell balance = off, I <sub>REG1</sub> = I <sub>REG2</sub> = 0 mA, Charge pump = off <sup>(1)</sup> , BAT = PACK = 35 V	T <sub>A</sub> = 25°C	450	550	μA	
			T <sub>A</sub> = –40°C to 100°C		600		
I <sub>CC2</sub>	Supply current 2	No load at REG1, REG2, TOUT, SCLK, SDIN, XALERT, CELLAMP, CURRENTAMP = on, CHG, DSG = on, Cell balance = off, I <sub>REG1</sub> = I <sub>REG2</sub> = 0 mA, Charge pump = off, BAT = PACK = 35 V	T <sub>A</sub> = 25°C	650	750	μA	
			T <sub>A</sub> = –40°C to 100°C		800		
I <sub>SHUTDOWN</sub>	Shutdown mode	CHG, DSG = off, VREG1 = VREG2 = off, PACK = 0 V, BAT = 35 V	T <sub>A</sub> = 25°C	0.1	1.2	μA	
			T <sub>A</sub> = –40°C to 100°C		2		
<b>VREG1, INTEGRATED 5-V LDO</b>							
V <sub>(REG1)</sub>	Output voltage	8.5 V < PACK or BAT ≤ 50 V, I <sub>OUT</sub> ≤ 25 mA	T <sub>A</sub> = –40°C to 100°C	4.55	5	5.45	V
		7 V < PACK or BAT ≤ 8.5 V, I <sub>OUT</sub> ≤ 3 mA		4.55	5	5.45	
ΔV <sub>(REG1)</sub>	Output temperature drift	PACK or BAT = 50 V, I <sub>OUT</sub> = 2 mA	T <sub>A</sub> = 25°C	±0.2%			
ΔV <sub>(REG1LINE)</sub>	Line regulation	10 V ≤ PACK or BAT ≤ 50 V, I <sub>OUT</sub> = 2 mA	T <sub>A</sub> = 25°C	10	20	mV	
ΔV <sub>(REG1LOAD)</sub>	Load regulation	PACK or BAT = 36 V, 0.2 mA ≤ I <sub>OUT</sub> ≤ 2 mA	T <sub>A</sub> = 25°C	7	15	mV	
		PACK or BAT = 36 V, 0.2 mA ≤ I <sub>OUT</sub> ≤ 25 mA		40	100		
I <sub>REG1MAX</sub>	Current limit	PACK or BAT = 36 V, VREG1 = 4.5 V	T <sub>A</sub> = 25°C	35	75	125	mA
		PACK or BAT = 36 V, VREG1 = 0 V		5	20	35	
<b>VREG2, INTEGRATED 3.3-V LDO</b>							
V <sub>(REG2)</sub>	Output voltage	8.5 V < PACK or BAT ≤ 50 V, I <sub>OUT</sub> ≤ 25 mA	T <sub>A</sub> = –40°C to 100°C	3.05	3.3	3.55	V
		7 V < PACK or BAT ≤ 8.5 V, I <sub>OUT</sub> ≤ 10 mA		3.05	3.3	3.55	
		7 V < PACK or BAT ≤ 50 V, I <sub>OUT</sub> = 0.2 mA		–2%	3.3	2%	
ΔV <sub>(REG2)</sub>	Output temperature drift	PACK or BAT = 50 V, I <sub>OUT</sub> = 2 mA	T <sub>A</sub> = –40°C to 100°C	±0.2%			
	Line regulation	7 V ≤ PACK or BAT ≤ 50 V, I <sub>OUT</sub> = 2 mA	T <sub>A</sub> = 25°C	10	20	mV	
	Load regulation	PACK or BAT = 36 V, 0.2 mA ≤ I <sub>OUT</sub> ≤ 2 mA	T <sub>A</sub> = 25°C	7	15	mV	
PACK or BAT = 36 V, 0.2 mA ≤ I <sub>OUT</sub> ≤ 25 mA		40		100			
I <sub>REG2MAX</sub>	Current limit	PACK or BAT = 36 V, VREG2 = 3 V	T <sub>A</sub> = 25°C	25	50	100	mA
		PACK or BAT = 36 V, VREG2 = 0 V		10	20	30	
<b>TOUT, THERMISTOR POWER SUPPLY</b>							
V <sub>TOUT</sub>		I <sub>OUT</sub> = 0 mA	T <sub>A</sub> = –40°C to 100°C	3.05	3.55	V	
R <sub>DS(ON)</sub>	Pass-element series resistance	I <sub>OUT</sub> = –1 mA at TOUT pin, I <sub>REG2</sub> = –0.2 mA R <sub>DS(ON)</sub> = (V <sub>REG2</sub> – V <sub>TOUT</sub> )/1 mA	T <sub>A</sub> = –40°C to 100°C		50	100	Ω
V <sub>TINS</sub>	Thermistor sense voltage	T <sub>A</sub> = –40°C to 100°C		–5%	0.975	5%	V
V <sub>TINSHYS</sub>	Thermistor sense hysteresis voltage	T <sub>A</sub> = –40°C to 100°C		50	100	150	mV
<b>THERMAL SHUTDOWN</b>							
T <sub>therm</sub>	Shutdown threshold	PACK or BAT = 36 V <sup>(2)</sup>		150		°C	
<b>PMS, PRECHARGE MODE SELECT DISABLE</b>							
V <sub>PMSDISABLE</sub>	PMS disable threshold of BAT	PACK = PMS = 20 V, VREG2 = 0 V, CHG = ON → OFF		8	13	16	V
<b>POR, POWER-ON RESET</b>							
V <sub>POR–</sub>	Negative-going voltage input	VLOG = VREG1(5 V) V		3.85	4.05	4.25	V
		VLOG = VREG2(3.3 V) V		2.45	2.65	2.8	

(1) Charge pump starts working when (I<sub>REG33</sub> + I<sub>REG5</sub>) > 3 mA.

(2) Not 100% tested, assured by design up to 125°C

**ELECTRICAL CHARACTERISTICS (continued)**

 BAT = PACK = 7 V to 50 V,  $T_A = -25^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , typical values stated where  $T_A = 25^{\circ}\text{C}$  and BAT = PACK = 36 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>POR_HYS</sub>	Positive-going hysteresis	VLOG = 3.3 V	50	150	250	mV
		VLOG = 5 V	100	250	400	
t <sub>RST</sub>	Reset delay time		1		5	ms
<b>CELL VOLTAGE MONITOR</b>						
V <sub>CELL_OUT</sub>	CELL output	VCn – VCn + 1 = 0 V, 20 V ≤ BAT ≤ 50 V, VGAIN = Low	0.925	0.975	1.025	V
		VCn – VCn + 1 = 0 V, 20 V ≤ BAT ≤ 50 V, VGAIN = High	1.12	1.2	1.28	
		VCn – VCn + 1 = 4.5 V, 20 V ≤ BAT ≤ 50 V		0.3		
REF 1	CELL output	Mode <sup>(3)</sup> , 20 V ≤ BAT or PACK ≤ 50 V, VGAIN = Low	–2%	0.975	2%	V
REF 2	CELL output	Mode <sup>(4)</sup> , 20 V ≤ BAT or PACK ≤ 50 V, VGAIN = High	–2%	1.2	2%	V
PACK	CELL output	Mode <sup>(5)</sup>	–5%	PACK/50	5%	V
BAT	CELL output	Mode <sup>(6)</sup>	–5%	BAT/50	5%	V
CMRR	Common-mode rejection	CELL max to CELL min, 20 V ≤ BAT ≤ 50 V	40			dB
K1	CELL scale factor 1	K = {CELL output (VC11 = 0 V, VC10 = 4.5 V) – CELL output (VC11 = VC10 = 0 V)} / 4.5 <sup>(7)</sup>	0.147	0.15	0.153	
		K = {CELL output (VC2 = 40.5 V, VC1 = 45 V) – CELL output (VC2 = VC1 = 40.5 V)} / 4.5 <sup>(7)</sup>	0.147	0.15	0.153	
K2	CELL scale factor 2	K = {CELL output (VC11 = 0 V, VC10 = 4.5 V) – CELL output (VC11 = VC10 = 0 V)} / 4.5 <sup>(8)</sup>	0.197	0.201	0.205	
		K = {CELL output (VC2 = 40.5 V, VC1 = 45 V) – CELL output (VC2 = VC1 = 40.5 V)} / 4.5 <sup>(8)</sup>	0.197	0.201	0.205	
I <sub>VCELLOUT</sub>	Drive current	VCn – VCn + 1 = 0 V, Vcell = 0 V, T <sub>A</sub> = –40 to 100°C	12	18		μA
V <sub>ICR</sub>	CELL output offset error	CELL output (VC2 = 45 V, VC1 = 45 V) – CELL output (VC2 = VC1 = 0 V)		–1		mV
R <sub>BAL</sub>	Cell balance internal resistance	RDS <sub>(ON)</sub> for internal FET switch at V <sub>DS</sub> = 2 V, BAT = PACK = 35 V	–50%	400	50%	Ω
<b>CURRENT MONITOR</b>						
V <sub>IOUT</sub>	Output voltage	VSRP = VSRN = 0 V <sup>(9)</sup>		1.2		V
V <sub>OFFSET</sub>	Input offset voltage	VSRP = VSRN = 0 V <sup>(9)</sup> , T <sub>A</sub> = 25°C	–3		3	mV
		VSRP = VSRN = 0 V <sup>(9)</sup> , T <sub>A</sub> = –40°C to 100°C	–4		4	
	DC gain, low	–100 mV < SRP < 100 mV <sup>(10)</sup>	–2%	10	2%	
	DC gain, high	–20 mV < SRP < 20 mV <sup>(11)</sup>	–2%	50	2%	
I <sub>IOUT</sub>	Drive current	V <sub>IOUT</sub> = 0 V, T <sub>A</sub> = –40°C to 100°C	12	18		μA

(3) STATE\_CONTROL [VGAIN] = 0, FUNCTION\_CONTROL [VAEN] = 1, CELL\_SEL[CAL2] = 0, [CAL0] = 1, [CAL0] = 1

(4) STATE\_CONTROL [VGAIN] = 1, FUNCTION\_CONTROL [VAEN] = 1, CELL\_SEL[CAL2] = 0, [CAL0] = 1, [CAL0] = 1

(5) STATE\_CONTROL [VGAIN] = X, FUNCTION\_CONTROL [PACK] = 1, [VAEN] = 1

(6) STATE\_CONTROL [VGAIN] = X, FUNCTION\_CONTROL [BAT] = 1, [VAEN] = 1

(7) STATE\_CONTROL [VGAIN] = 0, FUNCTION\_CONTROL [VAEN] = 1, CELL\_SEL[CAL2] = 0, [CAL0] = 0, [CAL0] = 0

(8) STATE\_CONTROL [VGAIN] = 1, FUNCTION\_CONTROL [VAEN] = 1, CELL\_SEL[CAL2] = 0, [CAL0] = 0, [CAL0] = 0

(9) STATE\_CONTROL [IGAIN] = X, FUNCTION\_CONTROL [IAEN] = 1, [IACAL] = 1

(10) STATE\_CONTROL [IGAIN] = 0, FUNCTION\_CONTROL [IAEN] = 1, [IACAL] = 0

(11) STATE\_CONTROL [IGAIN] = 1, FUNCTION\_CONTROL [IAEN] = 1, [IACAL] = 0

**ELECTRICAL CHARACTERISTICS (continued)**

BAT = PACK = 7 V to 50 V, T<sub>A</sub> = –25°C to 85°C, typical values stated where T<sub>A</sub> = 25°C and BAT = PACK = 36 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>BATTERY PROTECTION THRESHOLDS</b>						
V <sub>OV</sub>	OV detection threshold range	Default	4.15		4.5	V
ΔV <sub>OV</sub>	OV detection threshold program step			50		mV
V <sub>OVH</sub>	OV detection hysteresis voltage range	Default	0		0.3	V
ΔV <sub>OVH</sub>	OV detection hysteresis program step			0.1		V
V <sub>UV</sub>	UV detection threshold range	Default	1.4		2.9	V
ΔV <sub>UV</sub>	UV detection threshold program step			100		mV
V <sub>UVH</sub>	UV detection hysteresis voltage	Default	0.2		1.2	V
ΔV <sub>UVH</sub>	UV detection threshold program step			200		mV
V <sub>OCDT</sub>	OCD detection threshold range	Default	10		85	mV
ΔV <sub>OCDT</sub>	OCD detection threshold program step			5		mV
V <sub>SCDT</sub>	SCD detection threshold range	Default	60		135	mV
ΔV <sub>SCDT</sub>	SCD detection threshold program step			5		mV
V <sub>OV_acr</sub>	OV detection threshold accuracy	Default (T <sub>A</sub> = 0°C to 85°C)	–50	0	50	mV
V <sub>UV_acr</sub>	UV detection threshold accuracy	Default	–100	0	100	mV
V <sub>OCD_acr</sub>	OCD detection threshold accuracy	V <sub>OCD</sub> = 10 mV or 15 mV	–4	0	4	mV
		V <sub>OCD</sub> > 20 mV	–20%	0	20%	
V <sub>SCD_acr</sub>	SCD detection threshold accuracy	Default	–20%	0	20%	
<b>BATTERY PROTECTION DELAY TIMES</b>						
t <sub>OV</sub>	OV detection delay time range	Default	500		2250	ms
Δt <sub>OV</sub>	OV detection delay time step			250		ms
t <sub>UV</sub>	UV detection delay time range	Default	0		8000	ms
Δt <sub>UV</sub>	UV detection delay time step		1.25		1000	ms
t <sub>OCD</sub>	OCD detection delay time range	Default	20		1600	ms
Δt <sub>OCD</sub>	OCD detection delay time step		20		100	ms
t <sub>SCD</sub>	SCD detection delay time range	Default	0		900	μs
Δt <sub>SCD</sub>	SCD detection threshold program step			60		μs
t <sub>OV_acr</sub>	OV detection delay time accuracy	Default	–15%	0%	15%	
t <sub>UV_acr</sub>	UV detection delay time accuracy	Default	–15%	0%	15%	
t <sub>OC_acr</sub>	OC detection delay time accuracy	Default	–15%	0%	15%	
V <sub>SCD_acr</sub>	SC detection delay time accuracy	t <sub>SCD</sub> Max	–15%	0%	15%	

**ELECTRICAL CHARACTERISTICS (continued)**

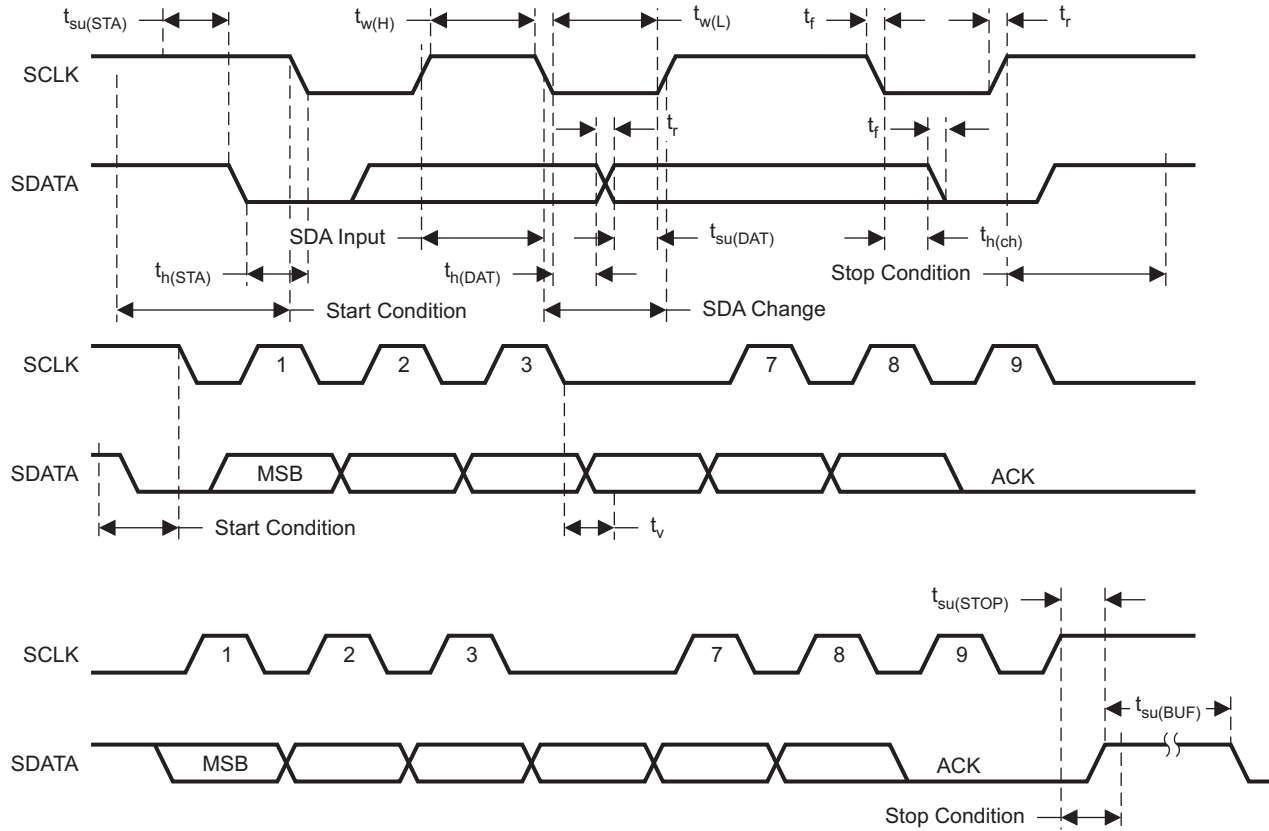
 BAT = PACK = 7 V to 50 V,  $T_A = -25^\circ\text{C}$  to  $85^\circ\text{C}$ , typical values stated where  $T_A = 25^\circ\text{C}$  and BAT = PACK = 36 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\text{SRC}}$	OC/SC recovery timing in stand-alone mode		-15%	12.8 s	15%	
<b>BATTERY PROTECTION RECOVERY</b>						
$V_{\text{RECSC}}$	SC, OC recovery voltage		1	1.4	2	V
$V_{\text{RECUV}}$	Undervoltage recover voltage	$V_{\text{RECUV}} = V_{\text{PACK}} - V_{\text{BAT}}$ , $V_{\text{UV}} + V_{\text{UVH}} > V_{\text{CELL}} > V_{\text{UV}}$	0.05	0.1	0.3	V
<b>FET DRIVE</b>						
$V_{\text{(FETON)}}$	Output voltage, charge and discharge FETs on	$V_{\text{O(FETONDSG)}} = V_{\text{(BAT)}} - V_{\text{(DSG)}}$ , VGS connect 1 M $\Omega$ , BAT = PACK = 35 V	8	12	16	V
		$V_{\text{O(FETONCHG)}} = V_{\text{(PACK)}} - V_{\text{(CHG)}}$ , VGS connect 1 M $\Omega$ , BAT = PACK = 35 V	8	12	16	
$V_{\text{(FETOFF)}}$	Output voltage, charge and discharge FETs off	$V_{\text{O(FETOFFDSG)}} = V_{\text{(PACK)}} - V_{\text{(DSG)}}$ , BAT = PACK = 35 V			0.2	V
		$V_{\text{O(FETOFFCHG)}} = V_{\text{(BAT)}} - V_{\text{(CHG)}}$ , BAT = PACK = 35 V			0.2	
$t_r$	Rise time	$C_L = 20$ nF, BAT = PACK = 35 V	$V_{\text{DSG}}$ : 10% to 90%	5	15	$\mu\text{s}$
			$V_{\text{CHG}}$ : 10% to 90%	5	15	
$t_f$	Fall time	$C_L = 20$ nF, BAT = PACK = 35 V	$V_{\text{DSG}}$ : 90% to 10%	90	140	$\mu\text{s}$
			$V_{\text{CHG}}$ : 90% to 10%	90	140	
<b>LOGIC</b>						
$V_{\text{OL}}$	Logic-level output voltage	XALERT, $I_{\text{OUT}} = 200$ $\mu\text{A}$ , $T_A = -40^\circ\text{C}$ to $100^\circ\text{C}$			0.4	V
		SDATA, SCLK, XRST, $I_{\text{OUT}} = 1$ mA, $T_A = -40^\circ\text{C}$ to $100^\circ\text{C}$			0.4	
		GPOD, $I_{\text{OUT}} = 1$ mA, $T_A = -40^\circ\text{C}$ to $100^\circ\text{C}$			0.6	
$I_{\text{LEAK}}$	Leakage current	GPOD $V_{\text{OUT}} = 1$ V, $T_A = -40^\circ\text{C}$ to $100^\circ\text{C}$			1	$\mu\text{A}$
$V_{\text{IH}}$	SCLK (hysteresis input)	Hysteresis		400		mV
$R_{\text{UP}}$	Pullup resistance	XALERT, $T_A = -40^\circ\text{C}$ to $100^\circ\text{C}$	60	100	200	k $\Omega$
		DATA, SCLK, $T_A = -40^\circ\text{C}$ to $100^\circ\text{C}$	6	10	20	
		XRST, $T_A = -40^\circ\text{C}$ to $100^\circ\text{C}$	1	3	6	
$I_{\text{DOWN}}$	Pulldown current	CNF0, CNF1, CNF2 = VREG2		2	4	$\mu\text{A}$

### I<sup>2</sup>C COMPATIBLE INTERFACE

BAT = PACK = 7 V to 50 V, T<sub>A</sub> = –25°C to 85°C, typical values stated where T<sub>A</sub> = 25°C and BAT = PACK = 36 V (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
t <sub>r</sub>	SCLK, SDATA rise time		1000	ns
t <sub>f</sub>	SCLK, SDATA fall time		300	ns
t <sub>w(H)</sub>	SCLK pulse duration high	4		μs
t <sub>w(L)</sub>	SCLK pulse duration low	4.7		μs
t <sub>su(STA)</sub>	Setup time for START condition	4.7		μs
t <sub>h(STA)</sub>	START condition hold time after which first clock pulse is generated	4		μs
t <sub>su(DAT)</sub>	Data setup time	250		ns
t <sub>h(DAT)</sub>	Data hold time	0		μs
t <sub>su(STOP)</sub>	Setup time for STOP condition	4		μs
t <sub>su(BUF)</sub>	Time the bus must be free before new transmission can start	4.7		μs
t <sub>v</sub>	Clock low to data-out valid		900	ns
t <sub>h(CH)</sub>	Data-out hold time after clock low	0		ns
f <sub>SCL</sub>	Clock frequency	0	100	kHz



T0369-01

Figure 5. I<sup>2</sup>C-Like I/F Timing Chart

## GENERAL OPERATIONAL OVERVIEW

### Stand-Alone Mode and Host Control Mode

The bq77PL900 has two operational modes, stand-alone mode and host-control mode. The mode is switched by *STATE\_CONTROL [HOST]*. In stand-alone mode, the battery protection is managed by the bq77PL900 without the need for any external control. In this mode, the CHG and DSG FETs are driven ON and OFF automatically and cell balancing is processed by a fixed algorithm if enabled by *OCDELAY[CBEN]*. In this mode, I<sup>2</sup>C communication is enabled, and a host can read the registers and set *STATE\_CONTROL [HOST]* but cannot control any output or function such as Vcell AMP enable.

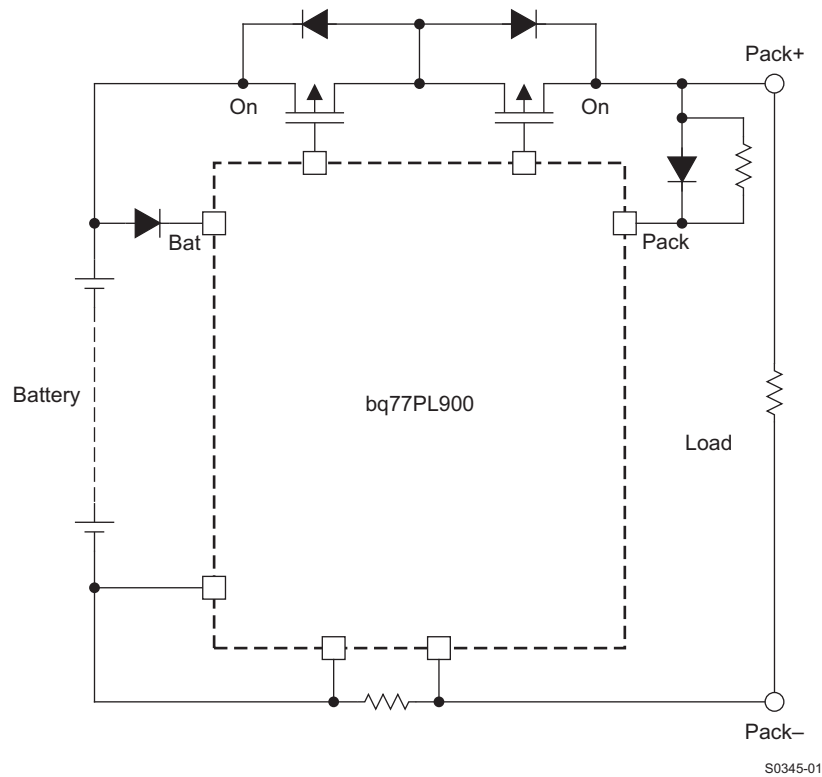
In host control mode, a host microcontroller can obtain battery information such as voltage and current from the bq77PL900 analog interface. This allows the host, such as a microcontroller, to calculate remaining capacity or implement an alternative cell balancing algorithm. In this mode, the bq77PL900 still detects cell protection faults and acts appropriately, although the recovery method is different from that in stand-alone mode. The host controller has control over the recovery method and FET action after the protection state has been entered. [Table 3](#) contains further details of the protection action differences.

**Table 3. Stand-Alone Mode and Host Control Mode Protection Summary**

FUNCTION	MODE	Stand-Alone Mode (HOST = L)	Host-Control Mode (HOST = H)	
OV protection	Detection	<b>Automatic</b> The bq77PL900 detects and recovers from protection states and controls the FETs.	<b>Automatic</b> The bq77PL900 detects an OV voltage and turns OFF the CHG FET. Must turn off cell balancing for correct voltage detection.	
	Recovery		<b>Host Control</b>	
UV protection	Detection		<b>Host Control</b> The bq77PL900 detects a UV voltage but no FET action is taken. Must turn off cell balancing for correct voltage detection.	
	Recovery		<b>Host Control</b>	
OCD/SCD protection	Detection		<b>Automatic</b> The bq77PL900 detects OCD and turns CHG and DSG FETs OFF.	
	Recovery		<b>Host Control</b>	
Overtemperature protection	Detection		Host must turn ON.	
	Recovery		<b>Host Control</b>	
CHG/DSG FET control	—		<b>Automatic</b> Host cannot drive the FETs	<b>Host Control</b> The bq77PL900 cannot release from protection state automatically.
Cell balancing	—		CBEN = 1: <b>Automatic</b> CBEN = 0: <b>No function</b>	<b>Host Control</b> The host can balance any cells at any time CBEN = Don't care
Zero-volt charge1	PMS = High, ZVC = X	<b>Automatic</b> <b>(0-V charge current flows through CHG FET)</b>	<b>Automatic</b>	
Zero-volt charge2	PMS = Low, ZVC = 0	<b>No support for 0-V charge</b>	<b>Host Control</b>	
Zero-volt charge3	PMS = Low, ZVC = 1	<b>Automatic</b> <b>(0-V charge current flows through FET that is driven by GPOD)</b>	Host should control precharge FET by using GPOD pin.	

**Normal Operation Mode**

When all cell voltages are within the range of  $V_{UV}$  to  $V_{OV}$ , and the CHG and DSG FETs are turned ON, the cells are charged and discharged at any time.



**Figure 6. Normal Operation Mode**

## Battery Protection

The bq77PL900 fully integrates battery protection circuits including cell overvoltage, undervoltage, and overcurrent in discharge and short circuit in discharge detection. Each detection voltage can be adjusted by programming the integrated EEPROM. Also, the detection delay time can be programmed as shown in [Table 4](#).

### CAUTION:

**Only a maximum of three programming cycles should be performed to ensure data stability.**

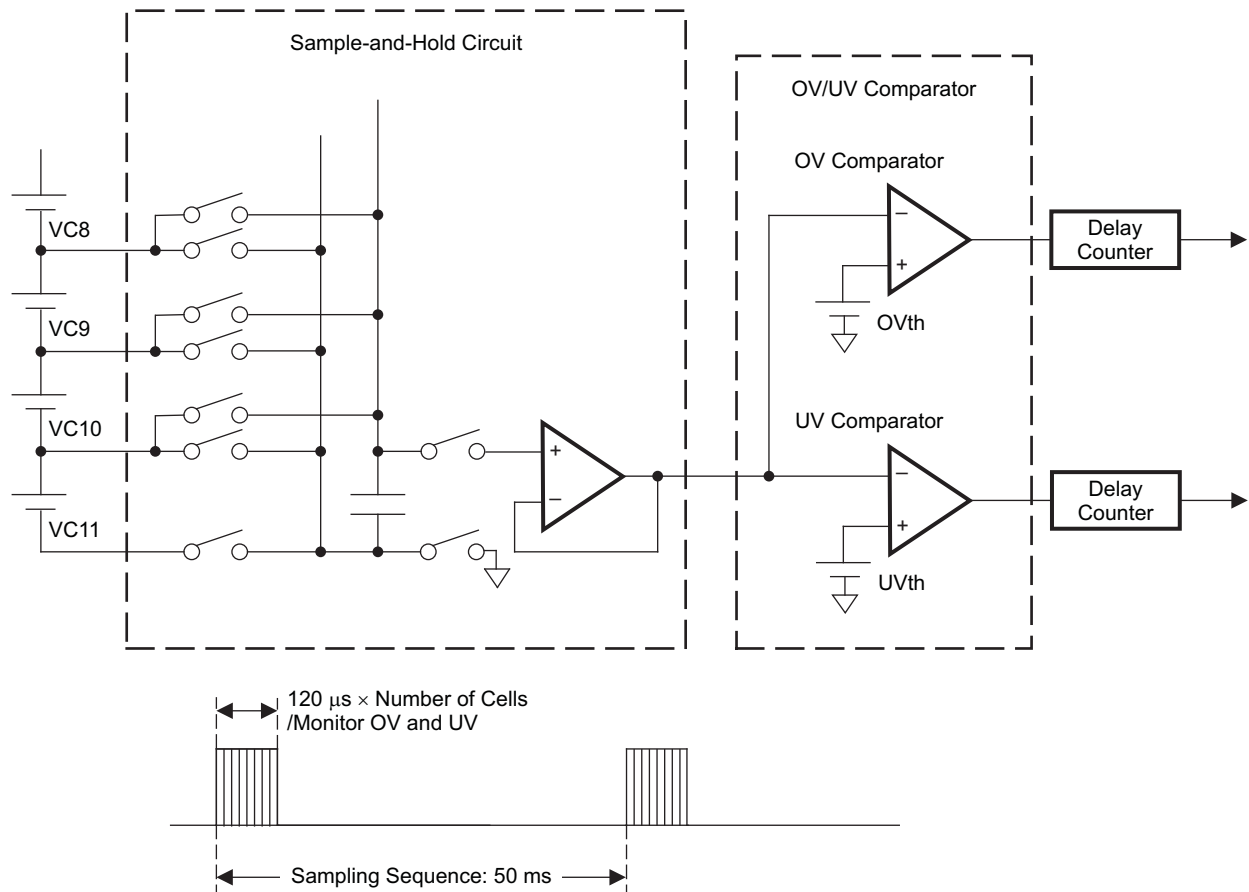
**Table 4. Detection Voltage, Detection Delay Time Summary**

PARAMETER		MIN	MAX	STEP	BITS
Overvoltage	Voltage	4.15 V	4.5 V	50 mV	3
	Delay	0.5 s	2.25 s	0.25 s	3
	Hysteresis	100 mV	400 mV	50 mV	2
Undervoltage	Voltage	1.4 V	2.9 V	100 mV	4
	Delay	0 ms	30 ms	1.25 ms–10 ms	4
		1 s	8 s	1 s	
	Hysteresis	100 mV	1200 mV	0.2 V, 0.4 V	2
Overcurrent in discharge	Voltage	10 mV	85 mV	5 mV	4
	Delay	20 ms	1600 ms	20 ms or 100 ms	5
Short circuit in discharge	Voltage	60 mV	135 mV	5 mV	4
	Delay	0 $\mu$ s	900 $\mu$ s	60 $\mu$ s	4

## Cell Overvoltage and Cell Undervoltage Detection

The cell overvoltage and cell undervoltage detection circuit consists of a sample-and-hold (S/H) circuit and two comparators.

The S/H period is about 120  $\mu$ s for each cell, and S/H is performed sequentially on each cell. Once all of the cells are checked, the bq77PL900 waits about 50 mS for the next S/H.



S0346-01

**Figure 7. Cell Voltage Monitoring Circuit**

### Cell Overvoltage Detection and Recovery

Cell overvoltage detection is the same as host control mode for the FET OFF state, but the recovery conditions are different. The CHG FET is turned OFF if any one of the cell voltages remains higher than  $V_{OV}$  for a period greater than  $t_{OV}$ . As a result, the cells are protected from an overcharge condition. Also XLAERT changes from High to Low. Both  $V_{OV}$  and  $t_{OV}$  can be programmed in the internal EEPROM.

### Recovery in Host Control Mode

The recovery condition is as follows:

1. All cell voltages become lower than  $V_{OV}$  ( $\Delta V_{OVH}$  is ignored).
2. Additionally, the host must send a sequence of firmware commands to the bq77PL900 to turn ON the CHG FET.

The command sequence required is as follows:

1. The host must toggle LTCLR from 0 to 1 and then back to 0.
2. Then set the CHG control bit to 1. To reset XLAERT high, the host must read the status register.

Figure 8 illustrates the circuit schematic in overvoltage protection mode in Host Control Mode. Figure 9 illustrates the timing of this protection mode.

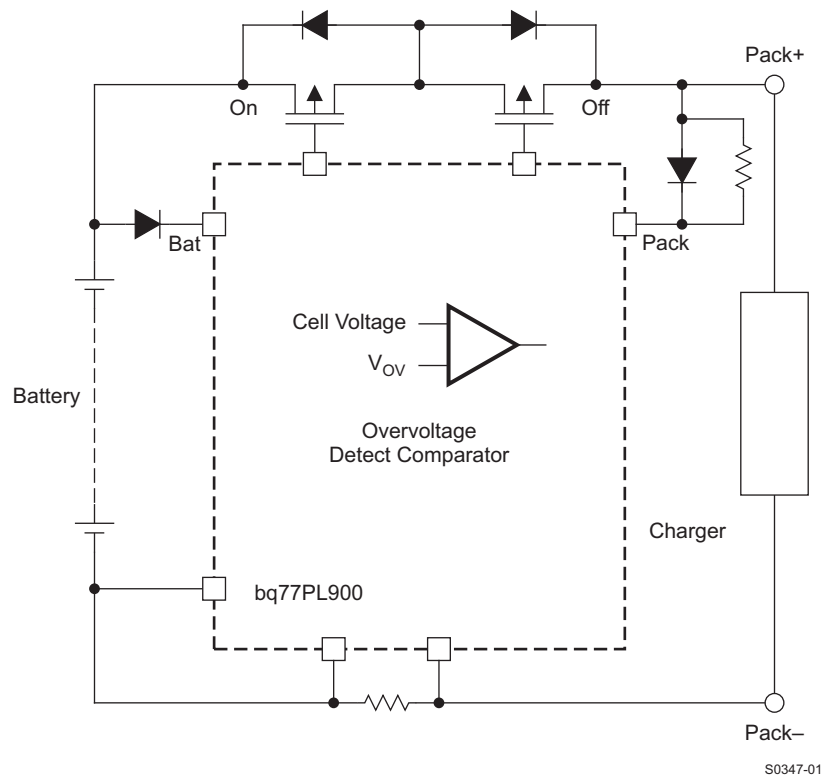
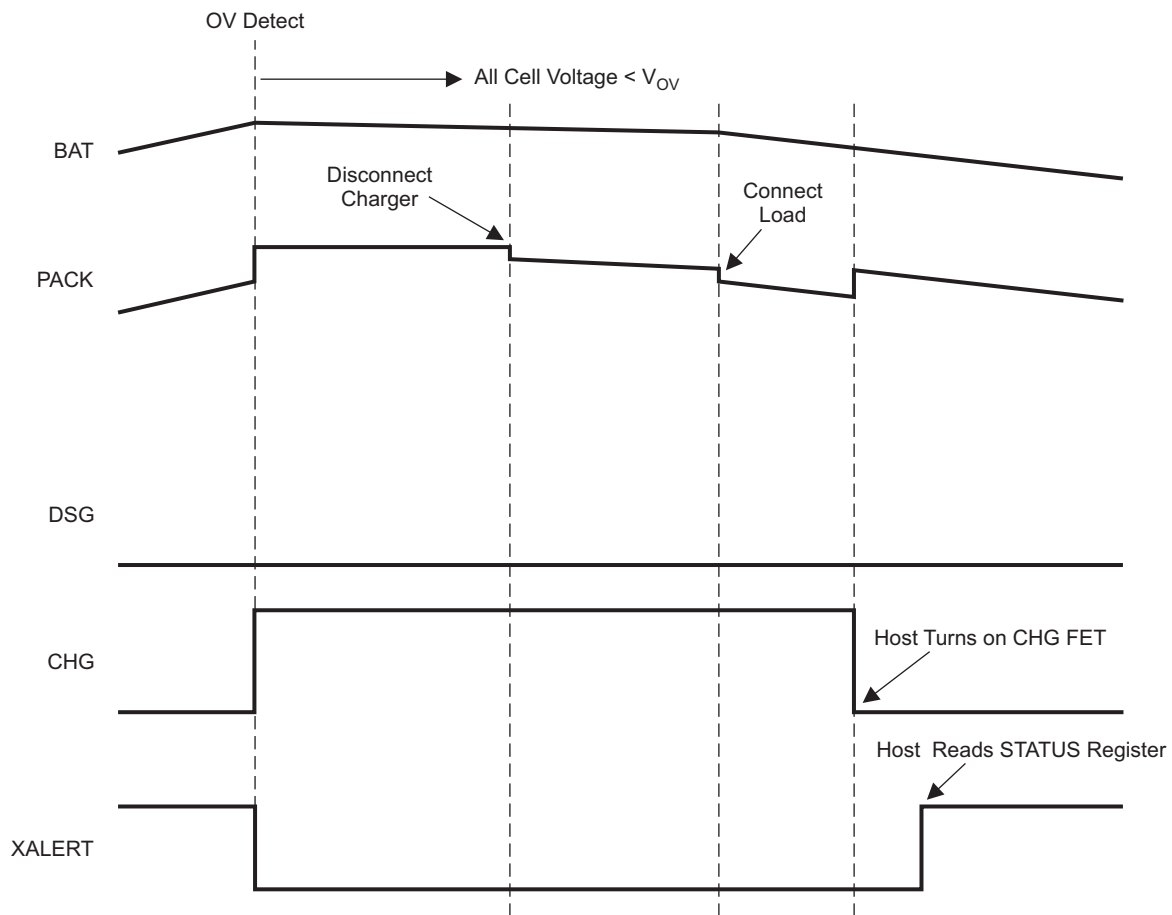


Figure 8. Overvoltage in Host-Control Mode



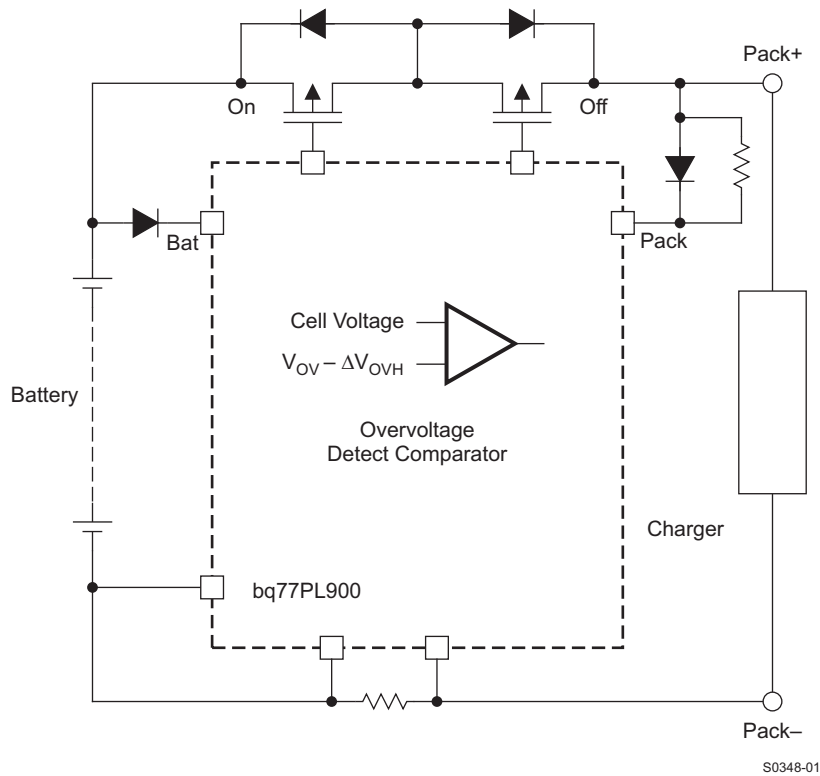
T0370-01

Figure 9. OV and OV Recovery Timing in Host-Control Mode

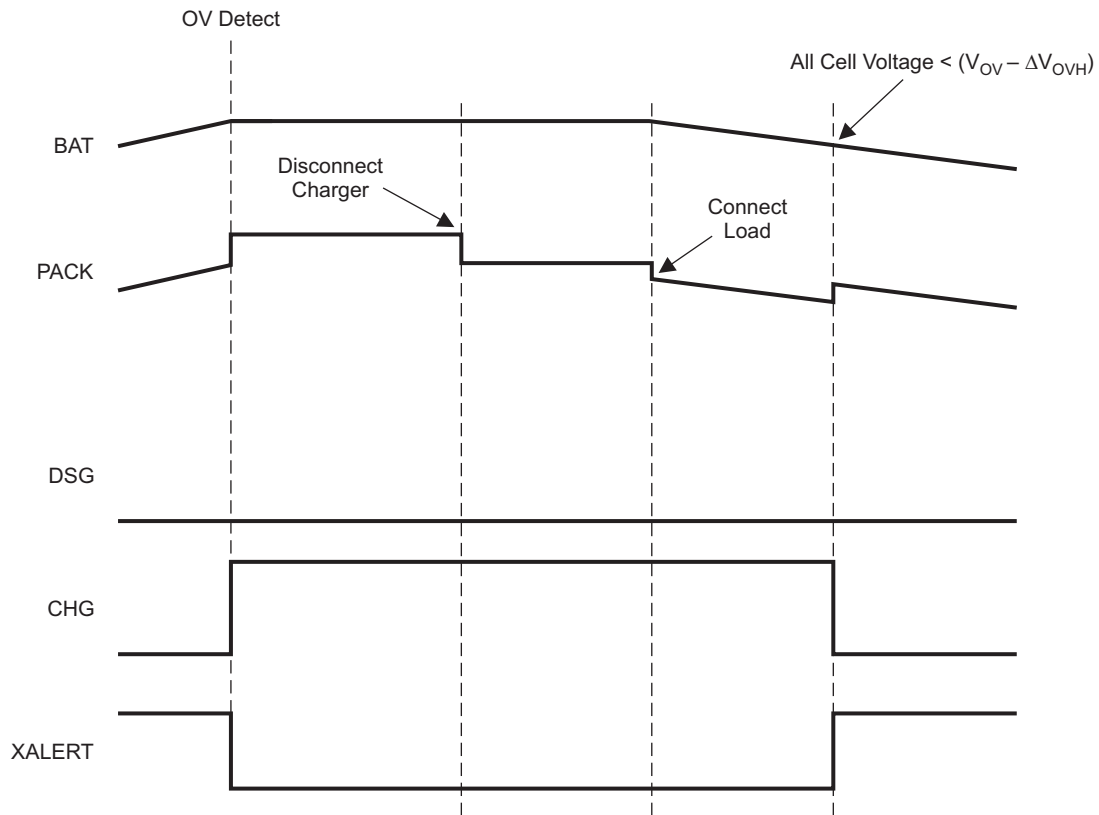
**Recovery in Stand-Alone Mode**

The recovery condition occurs when all cell voltages become lower than  $(V_{OV} - \Delta V_{OVH})$ .

Figure 10 illustrates the circuit schematic in overvoltage protection mode in stand-alone mode. Figure 11 illustrates the timing of this protection mode.



**Figure 10. Cell Overvoltage Protection Mode in Stand-Alone Mode**



T0371-01

Figure 11. OV and OV Recovery Timing in Stand-Alone Mode

### 7.14.1 Cell Undervoltage Detection and Recovery

When any one of the cell voltages falls below  $V_{UV}$  for a period of  $t_{UV}$ , the bq77PL900 enters the undervoltage mode. At this time, the DSG FET is turned OFF and XALERT driven low. Both  $V_{UV}$  and  $t_{UV}$  can be programmed in the internal EEPROM.

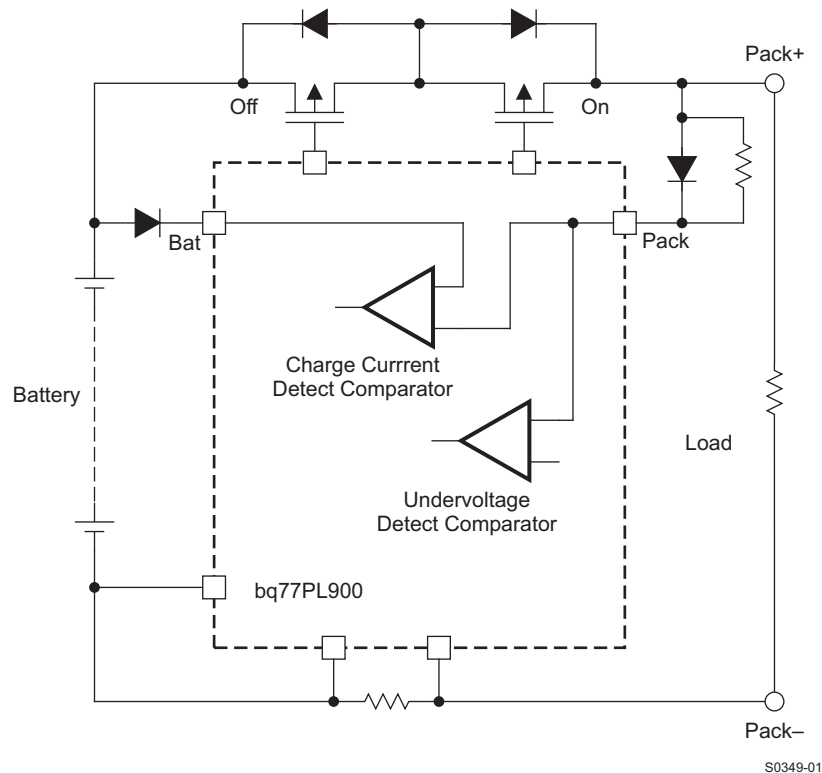


Figure 12. Cell Undervoltage Protection Mode in Host Mode and Stand-Alone Mode (Attaching a Charger)

#### In Host-Control Mode

Cell undervoltage protection recovery conditions are when:

1. All cell voltages become higher than  $(V_{UV} + \Delta V_{UVH})$ , or
2. All cell voltages are higher than  $V_{UV}$  AND a charger is connected between PACK+ and PACK-, noting that PACK+ voltage must be higher than BAT due to the diode forward voltage.

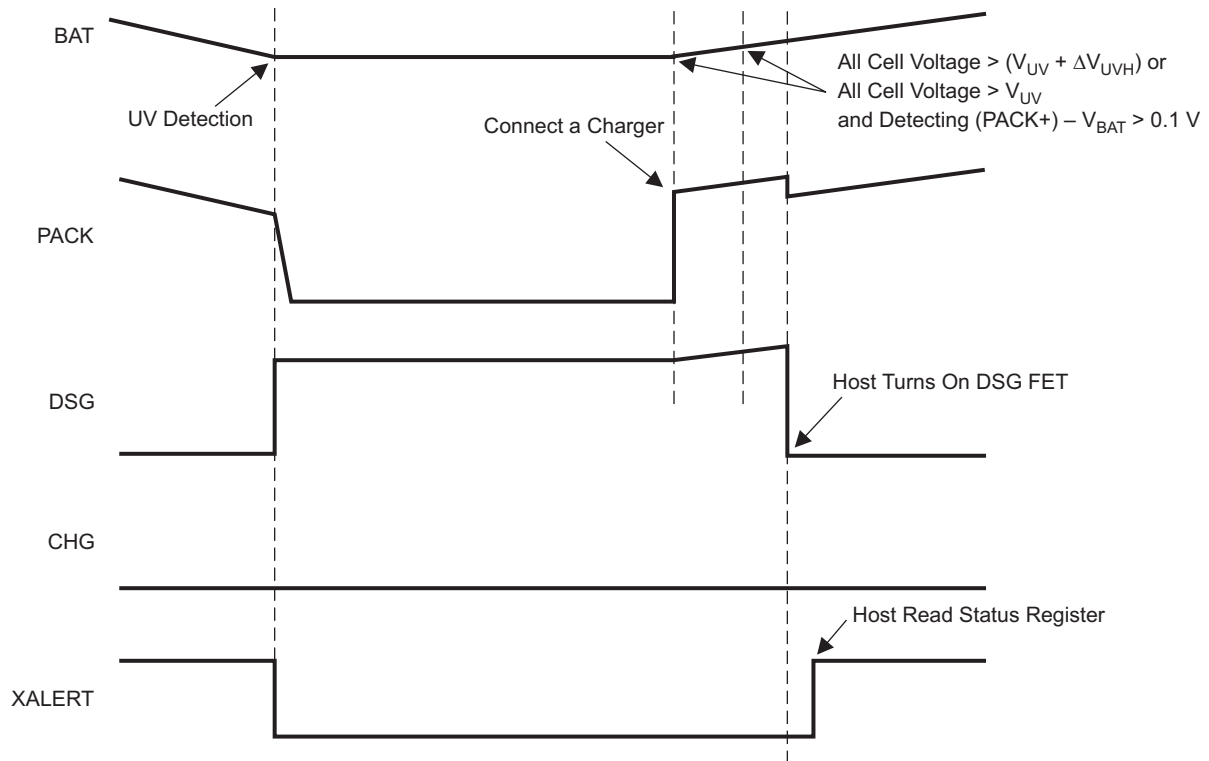
The bq77PL900 monitors the voltage difference between the PACK+ and BAT pins. When a difference higher than 0.4V (typ.) is seen, it is interpreted that a charger has been connected.

Figure 12 illustrates the circuit schematic in undervoltage protection mode.

In some applications, it is required not to turn OFF the DSG FET suddenly. In these cases, by setting **UVLEVLE [UVFET\_DIS] = 1**, only XALERT is driven low in response to entering an undervoltage condition. The host can turn OFF the DSG FET to protect the undervoltage condition. When the bq77PL900 recovery condition is satisfied, the host must send a sequence of firmware commands to the bq77PL900. The firmware command sequence to turn ON the DSG FET is as follows:

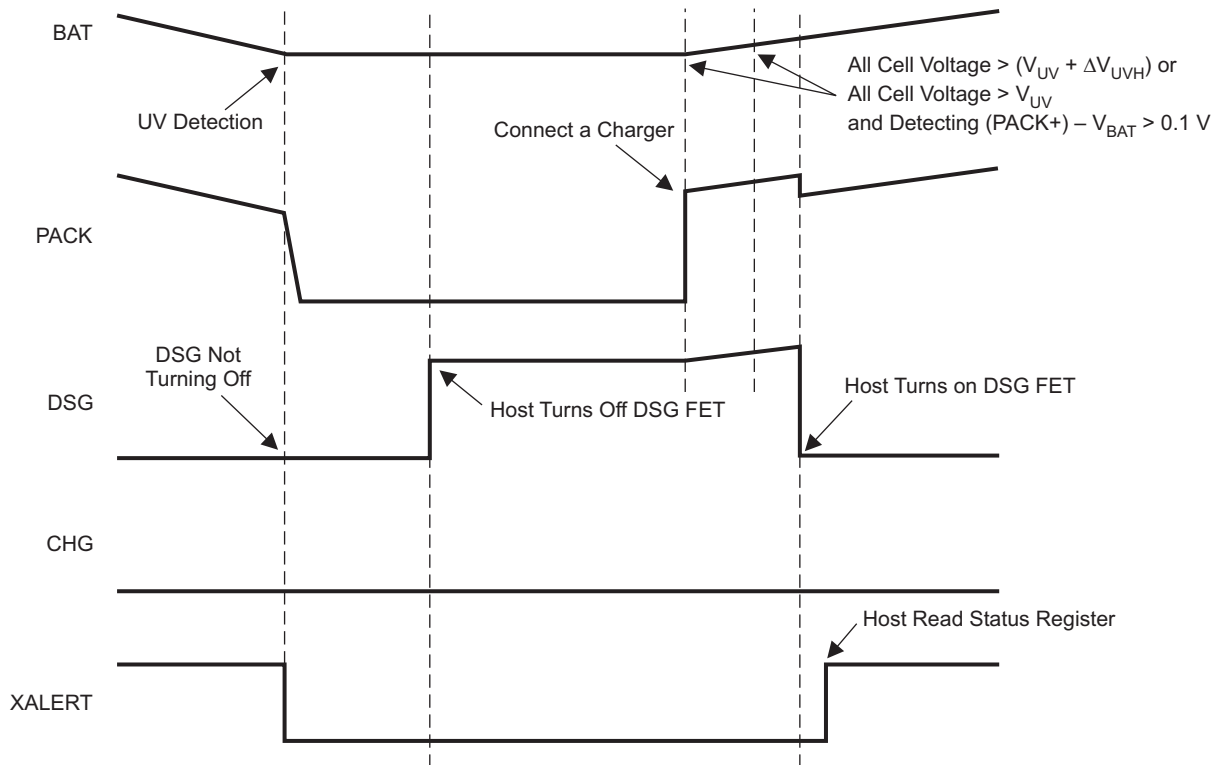
1. The host must toggle LTCLR from 0 to 1 and back to 0.
2. Then the host must set the DSG ON bit to 1.
3. Then the host can read the status register to reset XALERT high.

Figure 13 and Figure 14 illustrate the timing chart of protection mode.



T0372-01

Figure 13. UV and UV Recovery Timing Host-Control Mode (UVFET\_DIS = 0)



T0373-01

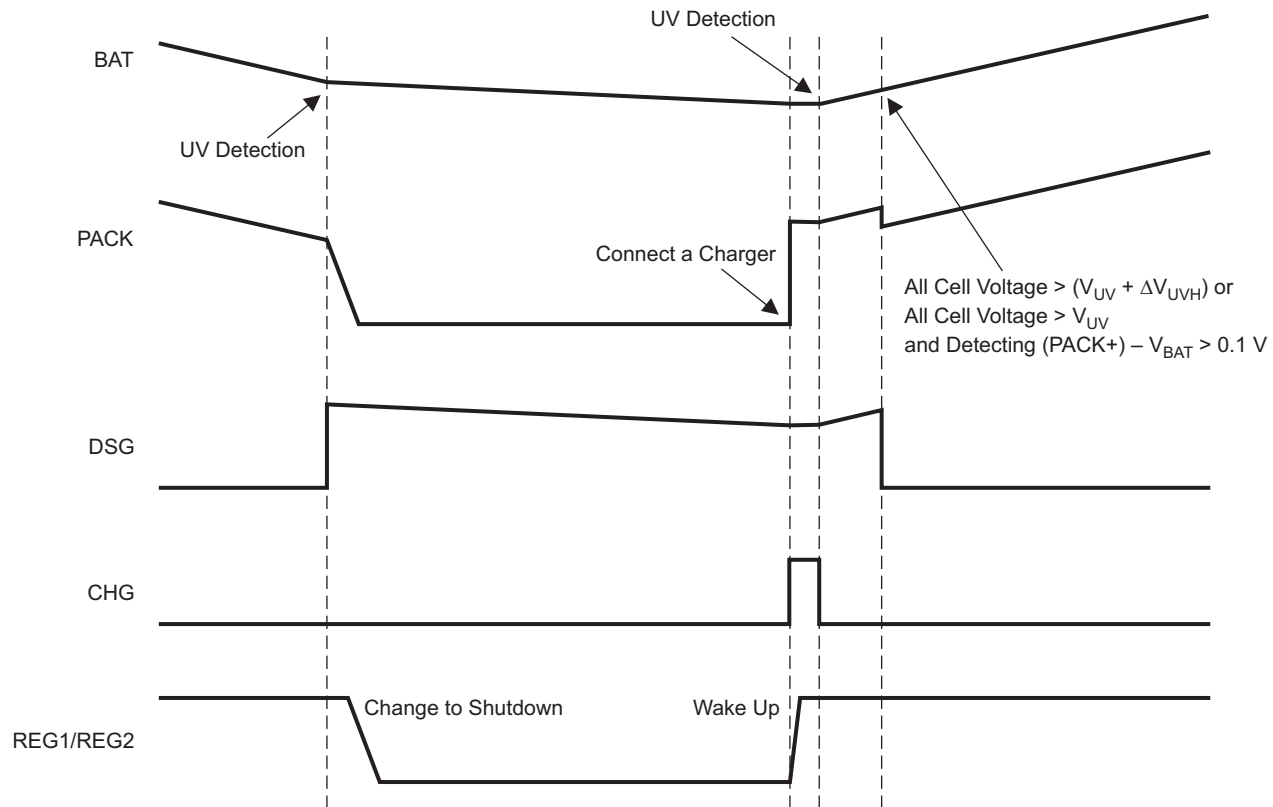
Figure 14. UV and UV Recovery Timing Host Control Mode (UVFET\_DIS = 1)

### In Stand-Alone Mode

On detecting entry to undervoltage mode, the bq77PL900 moves to the *shutdown* power mode.

When a charger is attached, the bq77PL900 wakes up from shutdown mode. If cell voltages are lower than the undervoltage condition, the DSG FET is turned OFF and XALERT driven low. During periods when a charger is attached, the bq77PL900 never changes to shutdown mode.

When the undervoltage recovery condition is satisfied, the DSG FET turns ON and XLAERT is reset high.



T0374-01

Figure 15. UV and UV Recovery in Stand-Alone Mode

### Overcurrent in Discharge (OCD) Detection

The overcurrent in discharge detection feature detects abnormal currents in the discharge direction via measuring the voltage across the sense resistor ( $V_{OCD}$ ) and is used to protect the pass FETs, cells, and any other inline components from abnormal discharge current conditions. The detection circuit also incorporates a blanking delay period ( $t_{OCD}$ ) before turning OFF the pass FETs. Both  $V_{OCD}$  and  $t_{OCD}$  can be programmed in internal EEPROM.

### Short Circuit in Discharge (SCD) Detection

The short circuit in discharge detection feature detects severe discharge current via measuring the voltage across the sense resistor ( $V_{SCD}$ ) and is used to protect the pass FETs, cells, and any other inline components from severe current conditions. The detection circuit also incorporates a blanking delay period ( $t_{SCD}$ ) before turning OFF the pass FETs. Both  $V_{SCD}$  and  $t_{SCD}$  can be programmed in the internal EEPROM.

**7.14.1 Overcurrent in Discharge and Short Circuit in Discharge Recovery**

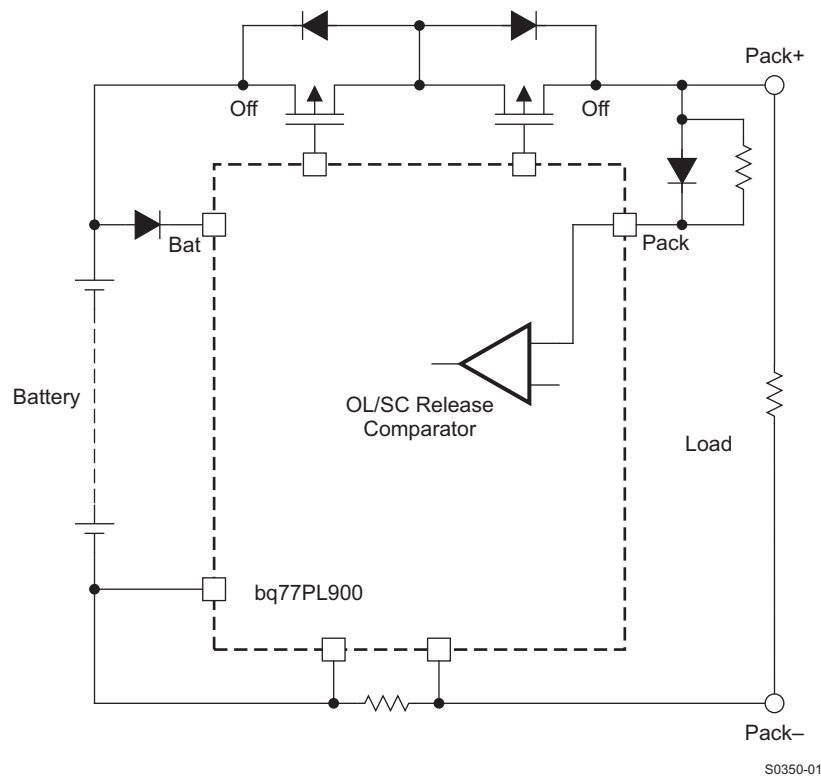
In host-control mode, the host must send a sequence of firmware commands to the bq77PL900 to recover from overcurrent and short-circuit currents. The command sequence to turn ON the DSG and CHG FETs is as follows:

1. The host must toggle LTCLR from 0 to 1 and back to 0.
2. Then set the DSG and CHG control bits to 1. To reset XALERT high, the STATUS register must be read.

In stand-alone mode, the bq77PL900 has two methods to recover from overcurrent and short-circuit conditions by setting the SOR bit of OCD\_CFG.

SOR = 0: Recover comparator is active after 12.8 s. An internal comparator monitors the PACK+ voltage and when the PACK+ voltage reaches  $V_{RECSC}$ , the overcurrent in discharge recovers. When the bq77PL900 detects a charger is attached, the DSG and CHG FETs turn ON and XALERT is reset High.

SOR = 1: After 12.8 s, the bq77PL900 automatically recovers from OC and SC. The DSG and CHG FETs turn ON and XALERT is reset high. If the OC or SC condition is still present, OC and SC is detected again and the recovery/detection cycle continues until the fault is removed.



**Figure 16. Overcurrent and Short-Circuit Protection Modes**

**Table 5. Detection and Recovery Condition Summary (Stand-Alone Mode)**

	CELL OVERVOLTAGE	CELL UNDERVOLTAGE	OVERCURRENT IN DISCHARGE	SHORT CIRCUIT IN DISCHARGE
Detection condition	Any cell voltage > $V_{OV}$	Any cell voltage < $V_{UV}$	$(V_{SRP} - V_{SRN}) > V_{OCD}$	$(V_{SRP} - V_{SRN}) > V_{SCD}$
CHG FET	ON → OFF	ON	ON → OFF	ON → OFF
DSG FET	ON	ON → OFF	ON → OFF	ON → OFF
Recovery condition 1	All cell voltage < $(V_{OV} - \Delta V_{OVH})$	All cell voltages > $(V_{UV} + \Delta V_{UVH})$	SOR = 0: Attach a charger SOR = 1: OC condition is released	SOR = 0: Attach a charger SOR = 1: SC condition is released
Recovery condition 2		All cell voltages > $V_{UV}$ AND $PACK+ - V_{BAT} > 0.1 V$		
CHG FET	OFF → ON	ON	OFF → ON	OFF → ON
DSG FET	ON	OFF → ON	OFF → ON	OFF → ON

**Table 6. Detection and Recovery Condition Summary (Host-Control Mode)**

	CELL OVERVOLTAGE	CELL UNDERVOLTAGE	OVERCURRENT IN DISCHARGE	SHORT CIRCUIT IN DISCHARGE
Detection condition	Any cell voltage > $V_{OV}$	Any cell voltage < $V_{UV}$	$(V_{SRP} - V_{SRN}) > V_{OCD}$	$(V_{SRP} - V_{SRN}) > V_{SCD}$
CHG FET	ON → OFF	ON	ON → OFF	ON → OFF
DSG FET	ON	ON → OFF (UVFET_DIS = 0)	ON → OFF	ON → OFF
Recovery condition 1	All cell voltage < $V_{OV}$ (ignore the hysteresis)	All cell voltage > $(V_{UV} + \Delta V_{UVH})$	None	None
Recovery condition 2		All cell voltage > $V_{UV}$ AND $V_{PACK} - V_{BAT} > 0.1 V$		
CHG FET <sup>(1)</sup>	OFF → ON	ON	OFF → ON	OFF → ON
DSG FET <sup>(1)</sup>	ON	OFF → ON	OFF → ON	OFF → ON

(1) Host is required to set and clear LTCLR, then turn on the FETs.

## Low-Dropout Regulators (REG1 and REG2)

The bq77PL900 has two low dropout (LDO) regulators that provide power to both internal and external circuitry. The inputs for these regulators can be derived from the PACK or BAT terminals (see the [Initialization](#) section for further details). The output of REG1 is typically 5 V, with a minimum output capacitance of 2.2  $\mu$ F required for stable operation. It is also internally current-limited. During normal operation, the regulator limits the output current, typically to 25 mA. The output of REG2 is typically 3.3 V, also with a minimum output capacitance of 2.2  $\mu$ F for stable operation, and it is also internally current-limited.

Until the internal regulator circuit is correctly powered, the DSG and CHG FETs are driven OFF.

## Initialization

From a shutdown situation, the bq77PL900 requires a voltage greater than the start-up voltage ( $V_{STARTUP}$ ) applied to the PACK pin to enable its integrated regulator and provide the regulator power source. Once the REG1 and REG2 outputs become stable, the power source of the regulator is switched to BAT.

After the regulators have started, they then continue to operate through the BAT input. If the BAT input is below the minimum operating range, then the bq77PL900 does not operate until the supply to the PACK input is applied.

If the voltage at REG2 falls, the internal circuit turns off the CHG and DSG FETs and disables all controllable functions, including the REG1, REG2, and TOUT outputs.

## Series Configuration of Five to Ten Cells

Unused cell inputs are required to be shorted to the uppermost-voltage-connected terminal. For example, in a five-cell configuration, VC1 to VC5 are shorted to VC6. In a 9-cell configuration, VC1 is shorted to VC2.

The CNF0, CNF1, and CNF2 pins should be connected to VLOG = logic 1 (through a 10-kΩ resistance) or GND = logic 0 (directly) according to the desired cell configuration as seen in [Table 7](#).

**Table 7. Cell Configuration**

CNF2 PIN	CNF1 PIN	CNF0 PIN	CELL CONFIGURATION
0	0	0	10-cell
0	0	1	9-cell
0	1	0	8-cell
0	1	1	7-cell
1	0	0	6-cell
1	0	1	5-cell
All other combinations			10-cell

## Delay Time Zero

The ZEDE pin enables EEPROM-programmed detection delay times when connected with GND (normal operation). The detection delay time is set to 0 when this pin is connected with VLOG. This is typically used in battery manufacturing test only.

## Cell Voltage Measurement

The cell voltage is translated to allow a host controller to measure individual series elements of the battery. The series element voltage is presented on the VOUT terminal. The cell voltage amplifier gain can be selected as one of the following two equations. The VOUT voltage gain is selected by *STATE\_CONTROL [VGAIN]*. VOUT is internally connected to ground when disabled.

$$V_{OUT1} = 0.975 - \{(\text{Cell voltage}) \times 0.15\} \text{ when } VGAIN = 0$$

or

$$V_{OUT2} = 1.2 - \{(\text{Cell voltage}) \times 0.20\} \text{ when } VGAIN = 1$$

The total pack voltage can also be monitored. The PACK voltage output is enabled or disabled by *FUNCTION\_CONTROL [PACK]*.

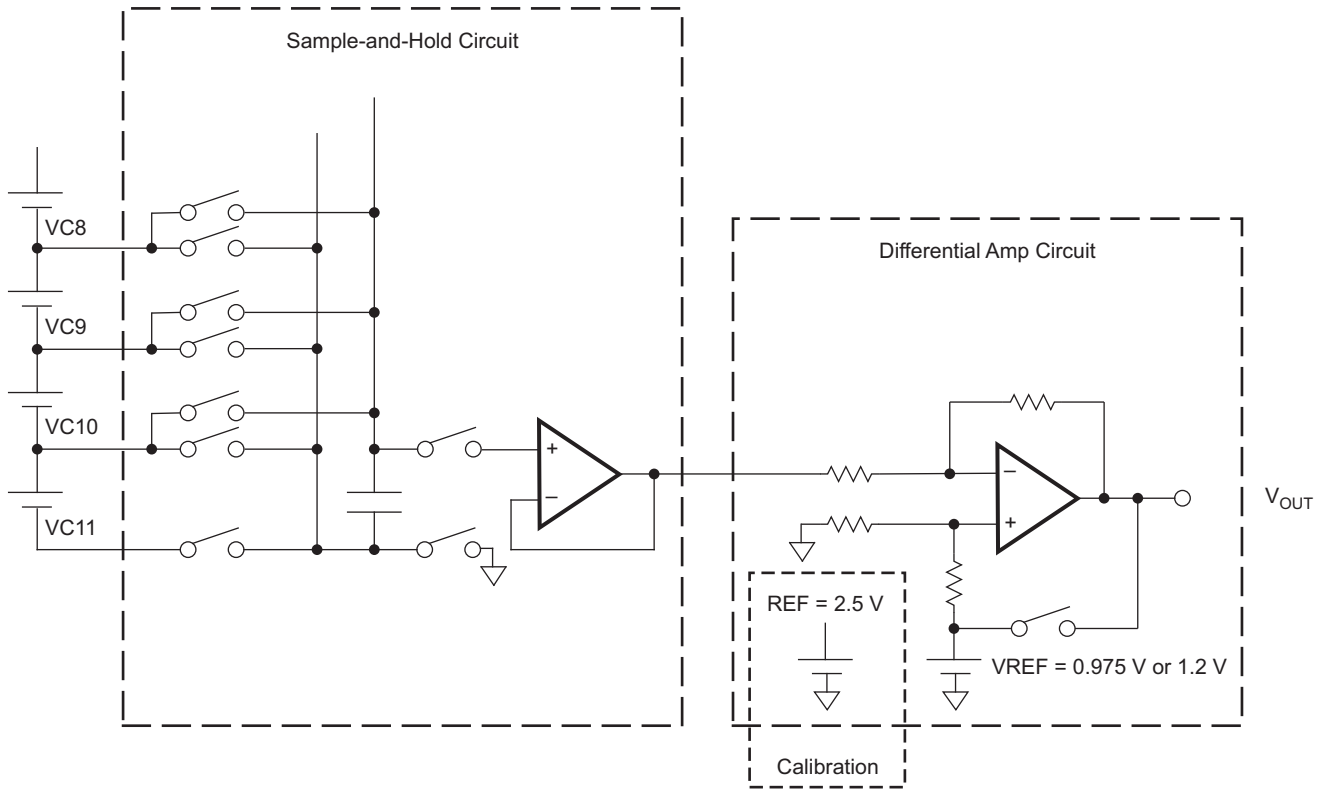
$$V_{OUT3} = (\text{Total pack voltage}) \times 0.02 \text{ when } PACK = 1$$

The total pack voltage can also be monitored. The BAT voltage output is enabled or disabled by *FUNCTION\_CONTROL [BAT]*.

$$V_{OUT4} = (\text{Total battery voltage}) \times 0.02 \text{ when } BAT = 1$$

## Cell Voltage Measurement Calibration

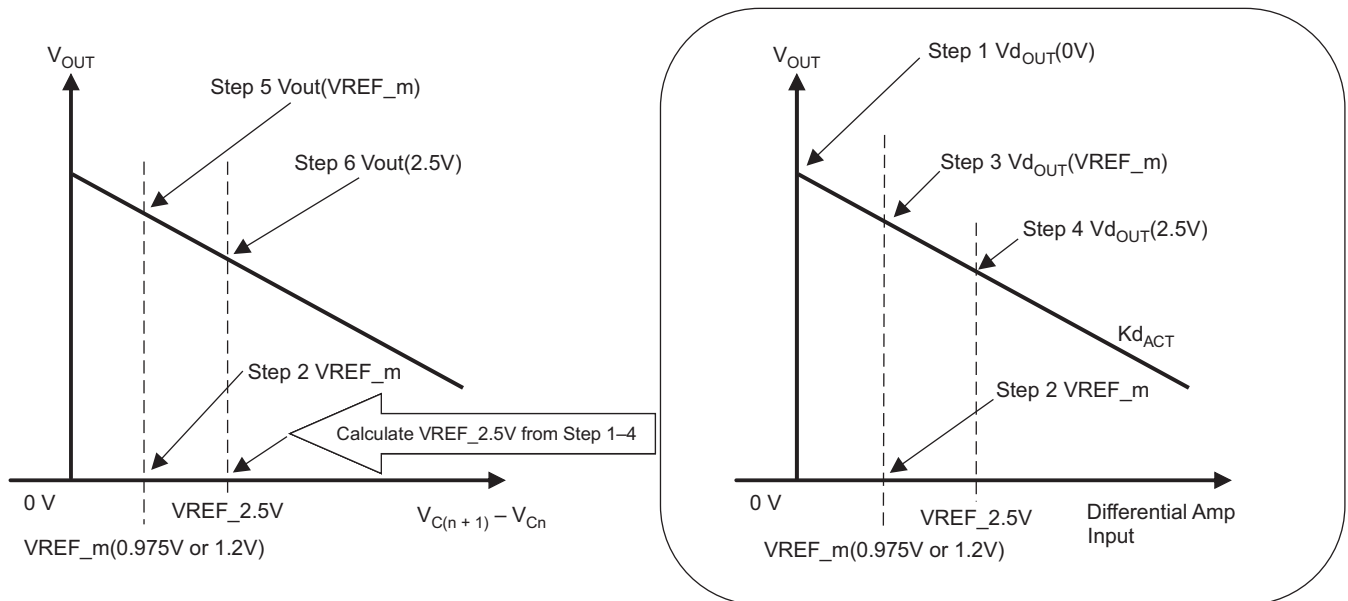
The bq77PL900 cell-voltage monitor consists of a sample-and-hold (S/H) circuit and differential amplifier.



S0351-01

Figure 17. Cell Voltage Monitoring Circuit

To calibrate the VCELL output, it must measure a 2.5-V signal, but 2.5 V is beyond the ADC input range of most analog-to-digital converters used in these applications. The bq77PL900 is designed to measure the 2.5 V through a differential amplifier first, which is where the calibration procedure starts.



M0122-01

Figure 18. Calibration Method

**Step 1**

Set CAL2 = 0, CAL1 = 0, CAL0 = 1, CELL[4:1] = 0, VAEN = 1

Measure the output voltage of the differential amplifier at 0-V input (both inputs of the differential amplifier are connected to GND). The output voltage includes the offset and is represented by:

$V_{dOUT}(0V)$  = measured output voltage of differential amplifier at 0-V input  
(This value includes an offset voltage ( $V_{OS}$ ) and a reference voltage.)

**Step 2**

Set CAL2 = 0, CAL1 = 1, CAL0 = 1, VAEN = 1

VREF is trimmed to 0.975 V or 1.2 V within  $\pm 2\%$ . Then measure internal reference voltage VREF directly from VOUT:

$V_{REF\_m}$  = measured reference voltage (0.975 V or 1.2 V)

**Step 3**

Set CAL2 = 0, CAL1 = 1, CAL0 = 0, CELL[4:1] = 0, VAEN = 1

Measure the scaled REF voltage through the differential amplifier.

$V_{dOUT}(V_{REF\_m})$  = The output voltage, including the scale factor error and offset  
 $= V_{REF} + (1 + K) \times V_{OS} - K \times V_{REF}$   
 $= V_{REF\_m} + (1 + K_{dACT}) \times V_{OS} - K_{dACT} \times V_{REF\_m}$

where:  $V_{REF\_m} + (1 + K_{dACT}) \times V_{OS} = V_{dOUT}(0V)$

$K_{dACT} = (V_{dOUT}(0V) - V_{dOUT}(V_{REF\_m})) / V_{REF\_m}$

= (measured value at step 1 – measured value at step 3) / measured value at step 2

Calibrated differential voltage is calculated by:

$V_{dout} = V_{REF} + (1 + K) \times V_{OS} - K \times V_{din}$   
 $= V_{dOUT}(0V) - K_{dACT} \times V_{din}$

Where:  $V_{din}$  = input voltage of differential amp lifier

**Step 4**

Set CAL2 = 1, CAL1 = 0, CAL0 = 0, CELL[4:1] = 0, VAEN = 1

Measure scaled REF(2.5V) though differential amp,

Some TI-Benchmark gas gauges cannot measure 2.5 V directly, because the ADC input voltage is 1 V. So to measure the 2.5-V internal reference voltage, use a differential amplifier as a method to scale down the measurement value.

$V_{dout}(2.5V)$  = measured differential amp output voltage at the 2.5-V input

Already, differential amplifier calibration was performed in steps 1, 2, and 3.

So  $V_{REF\_2.5V}$  is presented by

$V_{REF\_2.5V} = \{ V_{dOUT}(0V) - V_{dout}(2.5V) \} / K_{dACT}$

**Step 5**

Set CAL2 = 1, CAL1 = 0, CAL0 = 1, CELL2 = 0, CELL1 = 0, VAEN = 1

$V_{out}(0.975V \text{ or } 1.2V)$  = Measure scaled REF (0.975-V or 1.2-V) output voltage S/H and differential amplifier.

**Step 6**

Set CAL2 = 1, CAL1 = 1, CAL0 = 0, CELL[4:1] = 0, VAEN = 1

$V_{out}(2.5V)$  = Measure scaled REF (2.5-V) output voltage S/H and differential amp.

Scale factor

$K_{ACT} = -(V_{OUT}(2.5V) - V_{OUT}(0.975V \text{ or } 1.2V)) / (V_{REF\_2.5V} - V_{REF\_m})$

$$V_{out(0V)} = V_{OUT(2.5V)} + K_{ACT} \times V_{REF\_2.5V}$$

OR

$$V_{out(0V)} = V_{OUT(0.975V \text{ or } 1.2V)} + K_{ACT} \times V_{REF\_m}$$

Cell voltage is calculated by as follows:

$$V_{Cn} - V_{C(n+1)} = \{V_{out(0V)} - V_{OUT}\} / K_{ACT}$$

## Current Monitor

Discharge and charge currents are translated to allow a host controller to measure accurately current, which measurement can then be used for additional safety features or calculating the remaining capacity of the battery. The sense resistor voltage is converted using the following equation. The typical offset voltage is  $V_{CELL\_OFF}$  (1.2 V typical), although it can be presented on the IOUT pin for measurement, if required.

The output voltage increases when current is positive (discharging) and decreases when current is negative (charging).

$$V_{CURR} = 1.2 + (I_{PACK} \times R_{SENSE}) \times (IGAIN)$$

where

$$\text{State\_Control [IGAIN]} = 1 \text{ then } IGAIN = 50$$

$$\text{State\_Control [IGAIN]} = 0 \text{ then } IGAIN = 10$$

The current monitor amplifier can present the offset voltage as shown in [Table 8](#). The IOUT pin is enabled or disabled by *FUNCTION\_CONTROL* [*IACAL*, *IAEN*] and has a default state of OFF. IOUT is internally connected to ground when disabled.

**Table 8. IACAL and IAEN Configuration**

IACAL	IAEN	CONDITION
0	1	NORMAL
1	1	OFFSET
X	0	OFF

## Cell Balance Control

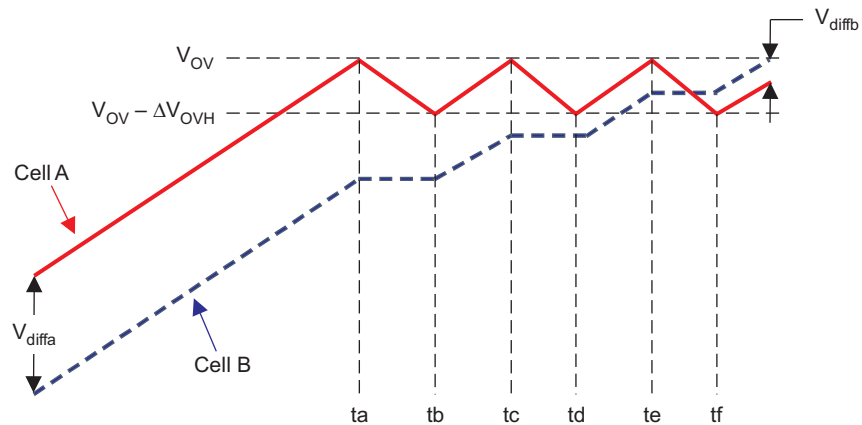
The integrated cell balance FETs allow a bypass path to be enabled for any one series element. The purpose of this bypass path is to reduce the current into any one cell during charging to bring the series elements to the same voltage. Series resistors placed between the input pins and the positive series element nodes limits the bypass current value. Series input resistors between 500 Ω and 1 kΩ are recommended for effective cell balancing.

In host-control mode, individual series element selection is made via *CELL\_BALANCE* [*CBAL1*, *CBAL2*, *CBAL3*, *CBAL4*, *CBAL5*, *CBAL6*, *CBAL7*, and *CBAL8*] and *FUNCTION\_CONTROL* [*CBAL9*, *CBAL10*].

In stand-alone mode, cell balancing works as shown in [Figure 19](#). When a certain cell (cell A) voltage reaches cell overvoltage, the battery charging stops and then cell balance starts working at  $t_a$ . The cell-A voltage decreases by the bypass current until the voltage reaches  $(V_{OV} - \Delta V_{OVH})$ . Cell-B voltage does not change during the period because cell balancing works only for the cell that reached  $V_{OV}$ . At  $t_b$ , battery charging starts again. Cell A and cell B have been charged in this period until cell-A voltage reaches  $V_{OV}$  again. The voltage difference between cell A and cell B becomes smaller when the bq77PL900 repeats the foregoing cycle. The bq77PL900 stops cell balance when cell overvoltage protection has released.

The bq77PL900 is designed to prevent cell balancing on adjacent cells or on every other cell. For example, if cell overvoltage happened to cell 8, cell 7 (cell 7 is next to cell 8) and cell 3 (cell 3 is **not** next to cell 8 or cell 7), then cell balancing starts for cell 8 and cell 3 first. When the cell-8 voltage is back to normal, then cell balancing starts for cell 7.

While the bq77PL900 monitors the overvoltage and undervoltage, cell balancing is automatically turned off. This configuration is supported for both modes (host-control and stand-alone modes).



T0375-01

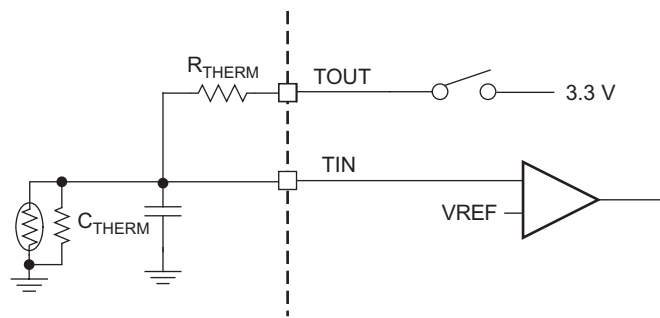
Figure 19. Cell Balancing Timing Chart (Automatic)

**Thermistor Drive Circuit (TOUT), Thermistor Input (TIN)**

The TOUT pin is powered by REG2, can be enabled via *FUNCTION\_CONTROL [TOUT]* to drive an external thermistor, and is OFF by default. A 10-kΩ, 25°C NTC (e.g., Semitec 103AT) thermistor is typical. The maximum output impedance is 100 Ω.

The bq77PL900 monitors the battery temperature as shown in Figure 20. A voltage divided by the NTC thermistor and reference resistor is connected to TIN. The bq77PL900 compares the TIN voltage with the internal reference voltage (0.975V), and when  $V_{TIN} < V_{REF}$  the bq77PL900 turns OFF the CHG and DSG FETs and sets *STATUS [OVTEMP]*.

In host-control mode, the host should enable and disable TOUT.



S0352-01

Figure 20. Temperature Monitoring Circuit

**General-Purpose Open-Drain Drive (GPOD)**

The GPOD output is enabled or disabled by *OUTPUT\_CONTROL [GPOD]* and has a default state of OFF.

In stand-alone mode, this pin is used for driving the 0-V/precharge FET for zero-voltage battery charging by *OCD\_CFG [ZVC] = 1*.

**Alerting the Host (XALERT)**

In both modes, the XALERT pin is available and is driven low when faults are detected. The method to clear the XALERT pin is different in stand-alone mode than in host-control mode. In stand-alone mode, XLAERT is cleared when all of the faults are cleared. In host-control mode, the host must toggle (from 0, set to 1, then reset to 0) *OUTPUT\_CONTROL [LTCLR]* and then read the *STATUS* register.

### Alerting the Host (LTCLR)

In host-control mode, when a protection fault occurs, the state is latched. The fault flag is unlatched by toggling (from 0, set to 1 then reset to 0) *OUTPUT\_CONTROL [LTCLR]*. The OCD, SCD, OV, and UV bits are unlatched by this function. Now the FETs can be controlled by programming the *OUTPUT\_CONTROL* register, and the XALERT output can be cleared by reading the *STATUS* register. When detecting overvoltage or undervoltage faults, LTCTR changes are ignored. After a period of 1 ms, it must send an LTCLR command.

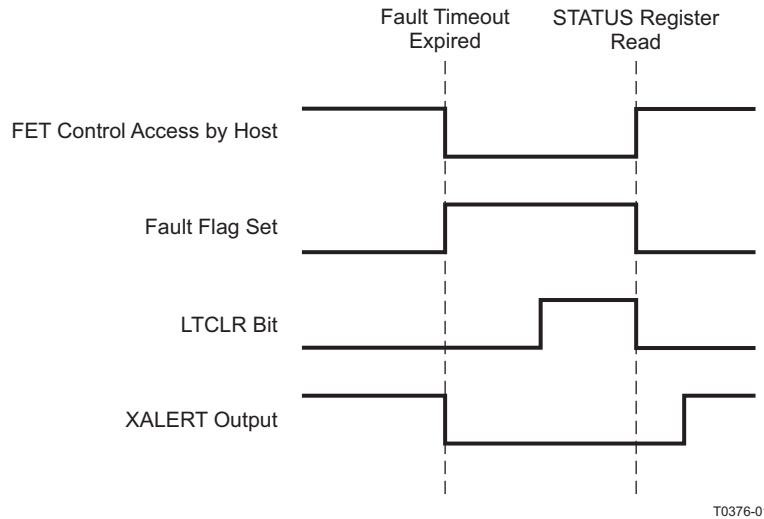


Figure 21. LTCLR and XLAERT Clear Timing (Host-Control Mode)

### POR

The XRST open-drain output pin is triggered on activation of the VREG1 or VREG2 output. This holds the host controller in reset for  $t_{RST}$ , allowing  $V_{VREG1}$  or  $V_{VREG2}$  to stabilize before the host controller is released from reset.

The XRST output and monitoring voltage is supplied by the source of VLOG. When VLOG is connected to VREG1, the XRST output level is  $V_{VREG1}$  and monitors the activation of VREG1. When VLOG is connected to VREG2, the XRST output level is  $V_{VREG2}$  and monitors the activation of VREG2.

When  $V_{VREG1}$  or  $V_{VREG2}$  voltage is below the output specifications, XRST is active-low ( $0.8 \times VLOG$ ). When  $V_{BAT}$  is below 7 V, VREG1 and VREG2 stop, then XRST goes low. If a host has a problem with a sudden reset signal, it is recommended monitoring the battery voltage to avoid it, e.g., burnout detection.

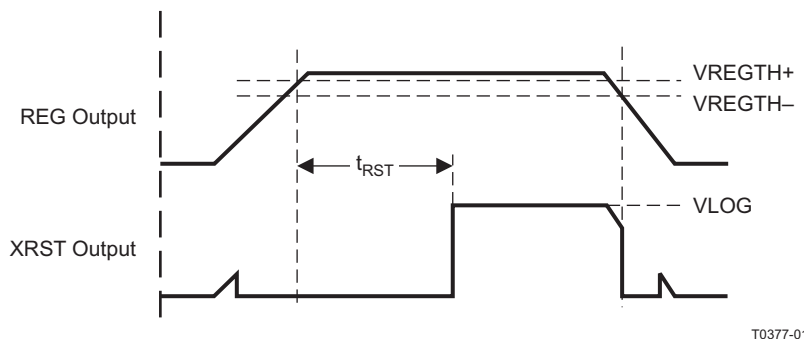


Figure 22. XRST Timing Chart – Power Up and Power Down

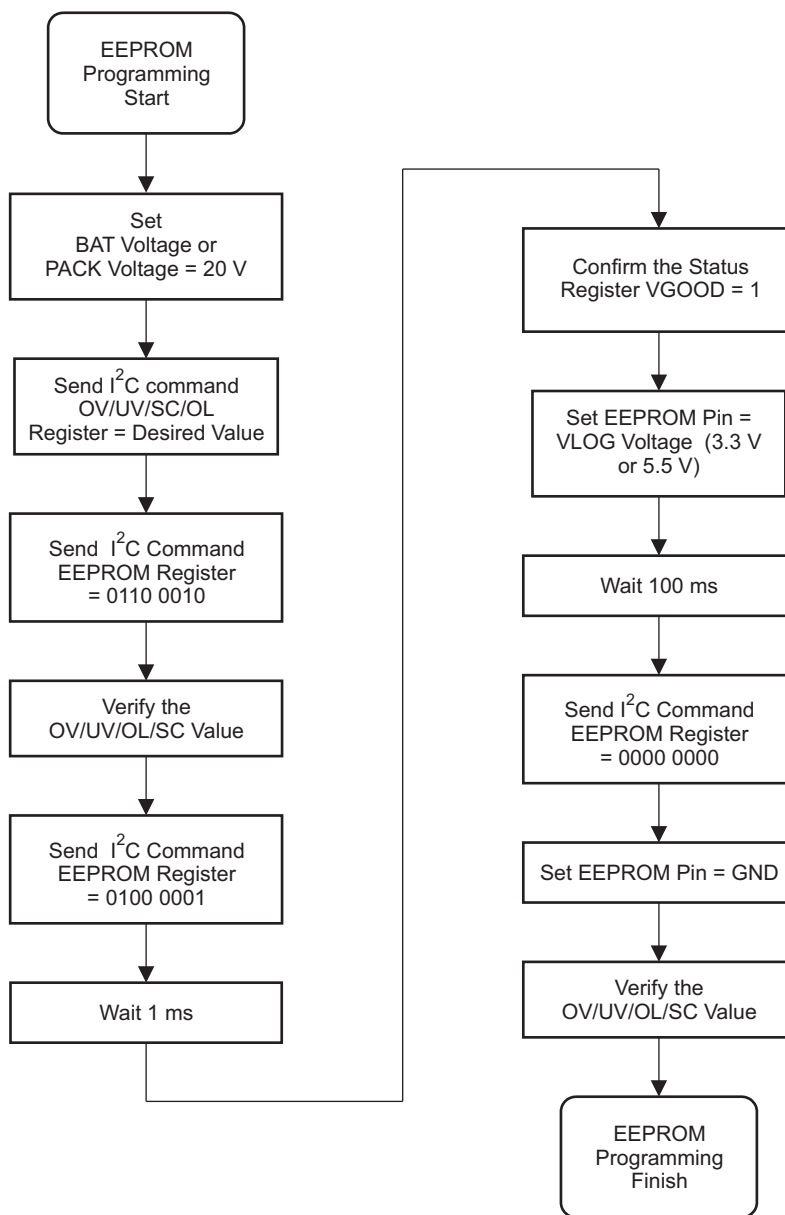
## EEPROM Write Sequence

The bq77PL900 has integrated configuration EEPROM for OV, UV, OCD, and SCD thresholds and delays. The appropriate configuration data is programmed to the configuration registers, and then 0xe2 is sent to the EEPROM register to enable the programming supply voltage. By driving the EEPROM pin (set high and then low), the data is written to the EEPROM.

When supplying BAT, care should be taken not to exceed  $V_{Cn} - V_{C(n+1)}$ , ( $n = 1$  to  $10$ )  $> 5$  V. If BAT and VC1 are connected onboard, it is recommended that all cell-balance FETs be ON where each input voltage is divided with the internal cell-balance ON resistance.

The recommended voltage at BAT or PACK for EEPROM writing is 20 V. When supplying VBAT, care is needed to ensure VBAT does not exceed the  $V_{Cn} - V_{C(n+1)}$ , ( $n = 1$  to  $10$ ) *absolute maximum voltage*. If BAT and VC1 are connected onboard, supplying 7.5 V is recommended to activate the bq77PL900 and turn ON all cell-balance FETs.

Then increase the power supply up to 20 V. By this method, each input voltage is divided with the internal cell-balance ON resistance.



F0038-01

Figure 23. EEPROM Data-Writing Flow Chart

## Power Modes

The bq77PL900 has two power modes, normal and shutdown. Table 9 outlines the operational functions during the two power modes.

**Table 9. Power Modes**

POWER MODE	TO ENTER NORMAL MODE	MODE DESCRIPTION
Normal		The battery is in normal operation with protection, power management, and battery monitoring functions available and operating. The supply current of this mode varies, as the host can enable and disable various features.
Shutdown	Add supply at the $V_{PACK} < V_{WAKE}$	When undervoltage is detected in stand-alone mode, or shutdown command at host-control mode, the bq77PL900 goes into shutdown: all outputs and interfaces are OFF and memory is not valid.

### Shutdown Mode

In host-control mode, the bq77PL900 enters shutdown mode when it receives the shutdown command, *STATE\_CONTROL [SHDN]* set. First, the DSG FET is turned OFF, and then after the pack voltage goes to 0 V, the bq77PL900 enters shutdown mode, which stops all functions of the bq77PL900.

In stand-alone mode the bq77PL900 enters shutdown when the battery voltage falls and UV is detected. It turns the DSG FET OFF, and after the pack voltage goes to 0 V, the bq77PL900 enters shutdown mode, which stops all functions.

### Exit From Shutdown

If a voltage greater than  $V_{STARTUP}$  is applied to the PACK pin, then the bq77PL900 exits from shutdown and enters normal mode.

### Parity Check

The bq77PL900 uses EEPROM for storage of protection thresholds, delay times, etc. The EEPROM is also used to store internal trimming data. For safety reasons, the bq77PL900 uses a column parity error checking scheme. If the column parity bit is changed from the written value, then *OUT\_CONTROL [PFALT]* is set to 1 and XALERT driven low. In stand-alone mode, both DSG and CHG outputs are driven high, turning OFF the DSG and CHG FETs. The GPOD output is also turned off.

In host-control mode, only *OUT\_CONTROL [PFALT]* and the XALERT output are changed, allowing the microprocessor host to control bq77PL900 operation.

## Communications

The I<sup>2</sup>C-like communication provides read and write access to the bq77PL900 data area. The data is clocked via separate data (SDATA) and clock (SCLK) pins. The bq77PL900 acts as a slave device and does not generate clock pulses. Communication to the bq77PL900 can be provided from the GPIO pins of a host controller. The slave address for the bq77PL900 is 7 bits and the value is 0010 000.

	(MSB) I <sup>2</sup> C Address + R/W Bit (LSB)						
	(MSB) I <sup>2</sup> C Address (LSB)						
Write	0	0	1	0	0	0	0
Read							1

The bq77PL900 does NOT have the following functions compatible with the I<sup>2</sup>C specification.

- The bq77PL900 is always regarded as a slave.
- The bq77PL900 does not support the general code of the I<sup>2</sup>C specification and therefore does not return an ACK, but may return a NACK.
- The bq77PL900 does not support the address auto-increment, which allows continuous reading and writing.
- The bq77PL900 allows data to be written to or read from the same location without resending the location address.

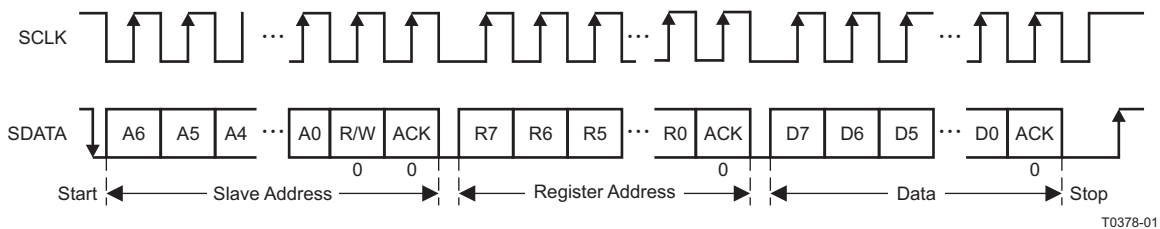


Figure 24. I<sup>2</sup>C-Bus Write to bq77PL900

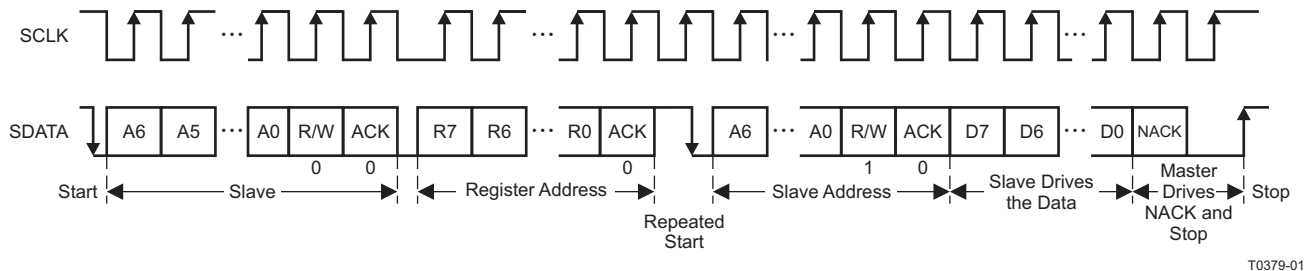


Figure 25. I<sup>2</sup>C-Bus Read From bq77PL900: Protocol A

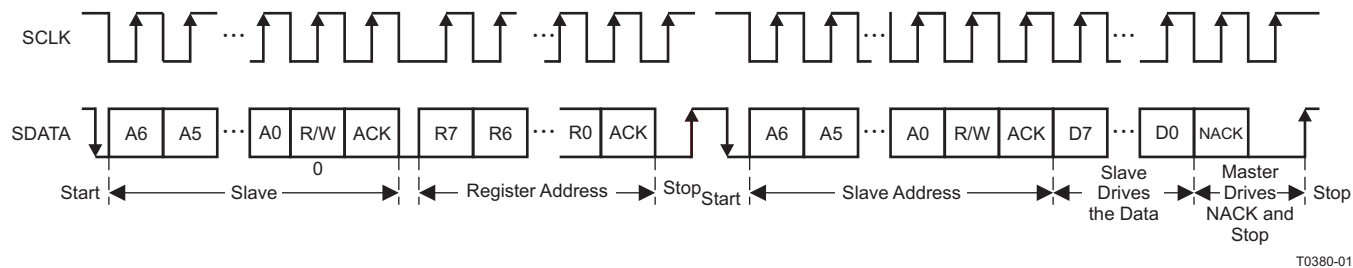


Figure 26. I<sup>2</sup>C-Bus Read From bq77PL900: Protocol B

### Register Set

The bq77PL900 has 12 addressable registers. These registers provide status, control, and configuration information for the battery protection system.

**Table 10. Register Descriptions**

NAME	TEST PIN	ADDR	MEMORY	R/W	DESCRIPTION
STATUS	X	0x00	Read	R	Status register
OUTPUT_CONTROL	X	0x01	RAM	R/W	Output pin control from system host-control mode and external pin status
STATE_CONTROL	X	0x02	RAM	R/W	State control from system host and external pin status
FUNCTION_CONTROL	X	0x03	RAM	R/W	Function control from system host and external pin status
CELL_BALANCE	X	0x04	RAM	R/W	Battery cell select for balance bypass
CELL_SEL	X	0x05	RAM	R/W	Battery cell select for balance bypass and for analog output voltage
OV_CFG	X	0x06	EEPROM	R/W <sup>(1)</sup>	Overvoltage level and delay time register
UV_LEVEL	X	0x07	EEPROM	R/W <sup>(1)</sup>	Undervoltage level register
OCV & UV DELAY	X	0x08	EEPROM	R/W <sup>(1)</sup>	Overload voltage level and undervoltage delay time register
OCDELAY	X	0x09	EEPROM	R/W <sup>(1)</sup>	Overload delay time register
SCD_CFG	X	0x0a	EEPROM	R/W <sup>(1)</sup>	Short-circuit in discharge current level and delay time register
EEPROM	X	0x0b	RAM	R/W	EEPROM read and write enable register

(1) Write and read data will be match after write EEPROM writing procedure.

**Table 11. Register Map**

NAME	I <sup>2</sup> C ADDR	B7	B6	B5	B4	B3	B2	B1	B0	
STATUS	0x00	CHG	DSG	VGOOD	OVTEMP	UV	OV	OCD	SCD	
OUTPUT_CONTROL	0x01	FS	PFALT	0	0	GPOD	CHG	DSG	LTCLR	
STATE_CONTROL	0x02	IGAIN	VGAIN	0	0	0	0	HOST	SHDN	
FUNCTION_CONTROL [Cell(9,10) balance register]	0x03	CBAL10	CBAL9	TOUT	BAT	PACK	IACAL	IAEN	VAEN	
CELL_BALANCE	0x04	CBAL8	CBAL7	CBAL6	CBAL5	CBAL4	CBAL3	CBAL2	CBAL1	
CELL_SEL	0x05	0	CAL2	CAL1	CAL0	CELL4	CELL3	CELL2	CELL1	
OV_CFG	0x06	OVD2	OVD1	OVD0	OVH1	OVH0	OV2	OV1	OV0	
UV_CFG	0x07	0	UVFET_DIS	UVH1	UVH0	UV3	UV2	UV1	UV0	
OCV&UV_DELAY	0x08	UVD3	UVD2	UVD1	UVD0	OCD3	OCD2	OCD1	OCD0	
OCD_CFG	0x09	CBEN	ZVC	SOR	OCDD4	OCDD3	OCDD2	OCDD1	OCDD0	
SCD_CFG	0x0a	SCDD3	SCDD2	SCDD1	SCDD0	SCD3	SCD2	SCD1	SCD0	
EEPROM	Read-writing	0x0b	0	1	1	0	0	0	1	0
	Writing (0x41)		0	1	0	0	0	0	0	1
	Reading (except above)		0	0	0	0	0	0	0	0

## Register Control

0x01 to 0x05 should be controlled during host-control mode.

### **STATUS: Status Register**

STATUS REGISTER (0x00)							
7	6	5	4	3	2	1	0
CHG	DSG	VGOOD	OVTEMP	UV	OV	OCD	SCD

The STATUS register provides information about the current state of the bq77PL900.

STATUS b0 (SCD): This bit indicates a short-circuit in discharge condition.

0 = Current is below the short-circuit in discharge threshold (default).

1 = Current is greater than or equal to the short-circuit in discharge threshold.

STATUS b1 (OCD): This bit indicates an overload condition.

0 = Current is less than or equal to the overload threshold (default).

1 = Current is greater than the overload threshold.

STATUS b2 (OV): This bit indicates an overvoltage condition.

0 = Voltage is less than or equal to the overvoltage threshold (default).

1 = Voltage is greater than the overvoltage threshold.

STATUS b3 (UV): This bit indicates an undervoltage condition.

0 = Voltage is greater than or equal to the undervoltage threshold (default).

1 = Voltage is less than the undervoltage threshold.

STATUS b4 (OVTEMP): This bit indicates an overtemperature condition.

0 = Temperature is lower than or equal to the overtemperature threshold (default).

1 = Temperature is higher than the overtemperature threshold.

STATUS b5 (VGOOD): This bit indicates a valid EEPROM power-supply voltage condition.

0 = Voltage is smaller than specified EEPROM power-supply voltage (default).

1 = Voltage is greater than or equal to the specified EEPROM power-supply voltage.

STATUS b6 (DSG): This bit reports the external discharge FET state.

0 = Discharge FET is off.

1 = Discharge FET is on.

STATUS b7 (CHG): This bit reports the external charge FET state.

0 = Charge FET is off.

1 = Charge FET is on.

**OUTPUT\_CONTROL: Output Control Register**

OUTPUT_CONTROL REGISTER (0x01)							
7	6	5	4	3	2	1	0
FS	PFALT	0	0	GPOD	CHG	DSG	LTCLR

The OUTPUT\_CONTROL register controls some of the outputs of the bq77PL900 and can show the state of the external pin corresponding to the control.

OUTPUT\_CONTROL b0 (LTCLR): When a fault is latched, this bit releases the fault latch when toggled (default).

0→1→0 clears the fault latches, allowing STATUS to be cleared on its next read.

OUTPUT\_CONTROL b1 (DSG): This bit controls the external discharge FET.

0 = Discharge FET is OFF in host-control mode.

1 = Discharge FET is ON in host-control mode.

OUTPUT\_CONTROL b2 (CHG): This bit controls the external charge FET.

0 = Charge FET is OFF in host-control mode.

1 = Charge FET is ON in host-control mode.

OUTPUT\_CONTROL b3 (GPOD): This bit enables or disables the GPOD output.

0 = GPOD output is high impedance (default).

1 = GPOD output is active (GND).

OUTPUT\_CONTROL b6 (PFALT): This bit indicates a parity error in the EEPROM. This bit is read-only.

0 = No parity error (default)

1 = A parity error has occurred.

OUTPUT\_CONTROL b7 (FS): This bit selects the undervoltage detection sampling time.

0 = Sampling time is 50 ms/cell (typ) (default).

1 = Sampling time is 100  $\mu$ s/cell (typ)

OUTPUT\_CONTROL b6-b4: These bits are not used and should be set to 0.

**STATE\_CONTROL: State Control Register**

STATE_CONTROL REGISTER (0x02)							
7	6	5	4	3	2	1	0
IGAIN	VGAIN	0	0	0	0	HOST	SHDN

The STATE\_CONTROL register controls the states of the bq77PL900.

STATE\_CONTROL b0 (SHDN): This bit enables or disables the shut down mode in host mode.

0 = Disable shutdown mode (default).

1 = Enable shutdown mode (if PACK voltage = 0 V).

STATE\_CONTROL b1 (HOST): This bit selects stand-alone mode or host-control mode.

0 = Stand-alone mode (default)

1 = Host control mode

STATE\_CONTROL b6 (VGAIN): This bit controls the cell amplifier scale.

0 = SCALE is 0.15 (default).

1 = SCALE is 0.2.

STATE\_CONTROL b7 (IGAIN): This bit controls the current monitor amplifier gain.

0 = GAIN is 10 (default).

1 = GAIN is 50.

STATE\_CONTROL b5-b2: These bits are not used and should be set to 0.

**FUNCTION\_CONTROL: Function Control Register, [Cell (9, 10) Balance Register]**

FUNCTION CONTROL REGISTER (0x03)							
7	6	5	4	3	2	1	0
CBAL10	CBAL9	TOUT	BAT	PACK	IACAL	IAEN	VAEN

The FUNCTION\_CONTROL register controls some features of the bq77PL900.

FUNCTION\_CONTROL b0 (VAEN): This bit controls the internal cell-voltage amplifier.

- 0 = Disable cell-voltage amplifier (default).
- 1 = Enable cell-voltage amplifier.

FUNCTION\_CONTROL b1 (IAEN): This bit controls the internal current-monitor amplifier.

- 0 = Disable current-monitor amplifier (default).
- 1 = Enable current-monitor amplifier.

FUNCTION\_CONTROL b2 (IACAL): This bit controls the internal current-monitor amplifier offset-voltage output.

- 0 = Disable offset voltage output (default).
- 1 = Enable offset voltage output.

FUNCTION\_CONTROL b3 (PACK): When VAEN = 1, PACK input is divided by 50 and presented on VCELL

- 0 = Disable pack total voltage output (default).
- 1 = Enable pack total voltage output.

FUNCTION\_CONTROL b4 (BAT): When VAEN = 1, BAT input is divided by 50 and presented on VCELL.

- 0 = Disable pack total voltage output (default).
- 1 = Enable pack total voltage output.

This bit priority is higher than PACK(b3).

FUNCTION\_CONTROL b5 (TOUT): This bit controls the power to the thermistor.

- 0 = Thermistor power is off in host-control mode (default).
- 1 = Thermistor power is on in host-control mode.

FUNCTION\_CONTROL b7–b6 (CELL10–9): This bit enables or disables the cell 9 and cell 10 balance charge bypass path

- 0 = Disable bottom series cell 9 or cell 10 balance charge bypass path (default).
- 1 = Enable bottom series cell 9 or cell 10 balance charge bypass path.

**CELL\_BALANCE: Cell (1 to 8) Balance Register**

CELL_BALANCE REGISTER (0x04)							
7	6	5	4	3	2	1	0
CBAL8	CBAL7	CBAL6	CELL5	CBAL4	CBAL3	CBAL2	CBAL1

The CELL\_BALANCE register controls cell balancing of the bq77PL900.

CELL\_BALANCE b7(CBAL8): This bit enables VC3–VC4 cell balance charge bypass path.

CELL\_BALANCE b6(CBAL7): This bit enables VC4–VC5 cell balance charge bypass path.

CELL\_BALANCE b5(CBAL6): This bit enables VC5–VC6 cell balance charge bypass path.

CELL\_BALANCE b4(CBAL5): This bit enables VC6–VC7 cell balance charge bypass path.

CELL\_BALANCE b3(CBAL4): This bit enables VC7–VC8 cell balance charge bypass path.

CELL\_BALANCE b2(CBAL3): This bit enables VC8–VC9 cell balance charge bypass path.

CELL\_BALANCE b1(CBAL2): This bit enables VC9–VC10 cell balance charge bypass path.

CELL\_BALANCE b0(CBAL1): This bit enables VC10–VC11 cell balance charge bypass path.

0 = Disable series cell balance charge bypass path (default).

1 = Enable series cell balance charge bypass path.

**CELL\_SEL: Cell Translation Selection and Cell Translation Status Register**

CELL_SEL REGISTER (0x05)							
7	6	5	4	3	2	1	0
0	CAL2	CAL1	CAL0	CELL4	CELL3	CELL2	CELL1

The CELL\_SEL register determines the cell selection for voltage measurement and translation. The register also determines operation mode of the cell voltage monitoring.

The CELL\_SEL b6–b4 (CAL2–CAL0) bits should be 0 when VAEN(b0) in register 3 is changed from 0 to 1 or the VOUT pin will not go active.

This register is don't care when either BAT(b4) or PACK(b3) is set or VAEN(b0) is cleared in register 3.

CELL\_SEL b3–b0 (CELL4–1): These four bits select the series cell for voltage measurement translation. These are don't care when CAL2–0 are not equal to 0x0.

CELL4	CELL3	CELL2	CELL1	SELECTED CELL
0	0	0	0	VC10–VC11, Bottom series element (default)
0	0	0	1	VC9–VC10, Second-lowest series element
0	0	1	0	VC8–VC9, Third-lowest series element
0	0	1	1	VC7–VC8, Fourth-lowest series element
0	1	0	0	VC6–VC7, Fifth-lowest series element
0	1	0	1	VC5–VC6, Sixth-highest series element
0	1	1	0	VC4–VC5, Seventh-highest series element
0	1	1	1	VC3–VC4, Eighth-highest series element
1	0	0	0	VC2–VC3, Ninth-highest series element
1	0	0	1	VC1–VC2, Top series element
Other				VC10–VC11, Bottom series element

CELL\_SEL b6–b4 (CAL2–0): These three bits determine the mode of the voltage monitor block.

CAL2	CAL1	CAL0	SELECTED MODE
0	0	0	Cell translation for selected cell (default), VO <sub>UT</sub> output depends on <i>CELL4–1</i> .
0	0	1	Monitor offset of differential amplifier (both inputs of differential amplifier are connected to GND).
0	1	0	Monitor the scaled V <sub>REF</sub> <sup>(1)</sup> value.
0	1	1	Monitor V <sub>REF</sub> <sup>(1)</sup> directly.
1	0	0	Monitor the scaled 2.5-V value to the measured 2.5 V.
1	0	1	Monitor V <sub>REF</sub> –0 V, through the sample-and-hold circuit. <sup>(1)</sup>
1	1	0	Monitor 2.5 V–0 V through the sample-and-hold circuit.
1	1	1	Monitor 2.5 V–1.2 V through the sample-and-hold circuit.

(1) When VGAIN = 0, VREF = 0.975 V; when VGAIN = 1, VREF = 1.2 V.

CELL\_SEL b7: These bits are not used and should be set to 0.

### OV\_CFG: Overvoltage Delay Time, Hysteresis, and Threshold Configuration Register

OV_CFG REGISTER (0x06)							
7	6	5	4	3	2	1	0
OVD2	OVD1	OVD0	OVH1	OVH0	OV2	OV1	OV0

The OV register determines cell overvoltage threshold, hysteresis voltage, and detection delay time.

OV\_CFG b2–b0 (OV2–0) configuration bits with corresponding voltage threshold with a default of 000. Resolution is 50 mV.

0x00	4.15 V	0x02	4.25 V	0x04	4.35 V	0x06	4.45 V
0x01	4.2 V	0x03	4.3 V	0x05	4.4 V	0x07	4.5 V

OV\_CFG b4–b3 (OVH1–0) configuration bits with corresponding hysteresis voltage with a default of 00. Resolution is 100 mV.

0x00	0.1 V	0x01	0.2 V	0x02	0.3 V	0x03	0 V
------	-------	------	-------	------	-------	------	-----

OV\_CFG b7–b5 (OVD2–0) configuration bits with corresponding delay time for overvoltage with a default of 000. Resolution is 250 ms.

0x00	0.5 s	0x02	1 s	0x04	1.5 s	0x06	2 s
0x01	0.75 s	0x03	1.25 s	0x05	1.75 s	0x07	2.25 s

**UV\_CFG: Undervoltage Hysteresis and Threshold Configuration Register**

UV LEVEL REGISTER (0x07)							
7	6	5	4	3	2	1	0
0	UVFET _DIS	UVH1	UVH0	UV3	UV2	UV1	UV0

The UV register determines the cell undervoltage threshold, hysteresis voltage, and detection delay time.

UV\_CFG b2–b0 (UV3–0) configuration bits with corresponding voltage threshold with a default of 000. Resolution is 100 mV.

0x00	1.4 V	0x04	1.8 V	0x08	2.2 V	0x0c	2.6 V
0x01	1.5 V	0x05	1.9 V	0x09	2.3 V	0x0d	2.7 V
0x02	1.6 V	0x06	2 V	0x0a	2.4 V	0x0e	2.8 V
0x03	1.7 V	0x07	2.1 V	0x0b	2.5 V	0x0f	2.9 V

UV\_CFG b5–b4 (UVH1–0) configuration bits with corresponding hysteresis voltage with a default of 00. Resolution is 200 mV.

0x00	0.2 V	0x01	0.4 V	0x02	0.8 V	0x03	1.2 V
------	-------	------	-------	------	-------	------	-------

When the undervoltage threshold and the hysteresis values are high, then undervoltage recovery may not occur. To avoid this, [Table 12](#) should be used for assistance in configuration.

**Table 12. Combination of UV Release Voltage vs Hysteresis**

		HYSTERESIS			
		0.2 V	0.4 V	0.8 V	1.2 V
Cell undervoltage (V)	1.4	1.6	1.8	2.2	2.6
	1.5	1.7	1.9	2.3	2.7
	1.6	1.8	2	2.4	2.8
	1.7	1.9	2.1	2.5	2.9
	1.8	2	2.2	2.6	3
	1.9	2.1	2.3	2.7	3.1
	2	2.2	2.4	2.8	3.2
	2.1	2.3	2.5	2.9	3.3
	2.2	2.4	2.6	3	3.3
	2.3	2.5	2.7	3.1	3.3
	2.4	2.6	2.8	3.2	3.3
	2.5	2.7	2.9	3.3	3.3
	2.6	2.8	3	3.3	3.3
	2.7	2.9	3.1	3.3	3.3
2.8	3	3.2	3.3	3.3	
2.9	3.1	3.3	3.3	3.3	

UV\_CFG b6 (UVFET\_DIS): This bit disable automatically turns off the DSG output when UV is detected in host-control mode.

0 = DSG output changes to OFF when UV is detected (default).

1 = DSG output does not change to OFF when UV is detected.

But the UV bit of the status register (0x00) is changed, even if this bit = 1.

UV\_CFG b7: This bit should be set to 0, so that the bq77PL900 protects battery cell safety.

**OC&UV\_DELAY: Overcurrent and Undervoltage Delay Register**

OC&UVDELAY REGISTER (0x08)							
7	6	5	4	3	2	1	0
UVD3	UVD2	UVD1	UVD0	OCD3	OCD2	OCD1	OCD0

The FUNCTION and OCDV CFG register determines overcurrent in discharge voltage threshold and controls functions.

OC&UV\_DELAY b3–b0 (OCD3–0) configuration bits with corresponding voltage threshold. Resolution is 5 mV.

0x00	10 mV	0x04	30 mV	0x08	50 mV	0x0c	70 mV
0x01	15 mV	0x05	35 mV	0x09	55 mV	0x0c	75 mV
0x02	20 mV	0x06	40 mV	0x0a	60 mV	0x0e	80 mV
0x03	25 mV	0x07	45 mV	0x0b	65 mV	0x0f	85 mV

OC&UVDELAY b7–hb4 (UVD3–0) configuration bits with corresponding delay time for undervoltage with a default of 000. Resolution is 1 s when the FS bit = 0.

OC&UVDELAY b7-b4 (UVD3-0)	FS bit (OUTPUT_CONTROL b7 )	
	1	0
0x00	See the following table.	1 s
0x01		2 s
0x02		3 s
0x03		4 s
0x04		5 s
0x05		6 s
0x06		7 s
0x07		8 s
0x08	1 s	1 s
0x09	2 s	2 s
0x0a	3 s	3 s
0x0b	4 s	4 s
0x0c	5 s	5 s
0x0d	6 s	6 s
0x0e	7 s	7 s
0x0f	8 s	8 s

UVD<3:0>	Internal Count	DELAY TIME (ms), FS = 1					
		5 Cells	6 Cells	7 Cells	8 Cells	9 Cells	10 Cells
0x00	0	0	0	0	0	0	0
0x01	2	1.25	1.5	1.75	2	2.25	2.5
0x02	4	2.5	3	3.5	4	4.5	5
0x03	8	5	6	7	8	9	10
0x04	10	6.25	7.5	8.75	10	11.25	12.5
0x05	12	7.5	9	10.5	12	13.5	15
0x06	16	10	12	14	16	18	20
0x07	24	15	18	21	24	27	30

**OCD\_CFG: Overcurrent in Discharge Configuration Register**

OCD_CFG REGISTER (0x09)							
7	6	5	4	3	2	1	0
CBEN	ZVC	SOR	OCDD4	OCDD3	OCDD2	OCDD1	OCDD0

The FUNCTION & OCD\_CFG register determines function and overload-detection delay time.

OCD\_CFG b4–b0 (OCDD4–0) configuration bits with corresponding delay time. Units are in ms and resolution is 20 ms or 100 ms.

0x00	20 ms	0x08	180 ms	0x10	100 ms	0x18	900 ms
0x01	40 ms	0x09	200 ms	0x11	200 ms	0x19	1000 ms
0x02	60 ms	0x0a	220 ms	0x12	300 ms	0x1a	1100 ms
0x03	80 ms	0x0b	240 ms	0x13	400 ms	0x1b	1200 ms
0x04	100 ms	0x0c	260 ms	0x14	500 ms	0x1c	1300 ms
0x05	120 ms	0x0d	280 ms	0x15	600 ms	0x1d	1400 ms
0x06	140 ms	0x0e	300 ms	0x16	700 ms	0x1e	1500 ms
0x07	160 ms	0x0f	320 ms	0x17	800 ms	0x1f	1600 ms

OCD\_CFG b5 (SOR): Recover condition from SC and OC with stand-alone mode

0 = Recover by attaching a charger. Recover comparator is active after 12.8 s for OC/SC detection (default).

1 = Recover by SC/OC condition released. Recovery from OC/SC after 12.8 s.

OCD\_CFG b6 (ZVC): This bit controls the 0-V/precharge of the GPOD output.

0 = Disable the GPOD output 0-V/precharge mode with stand-alone (default).

1 = Enable the GPOD output 0-V/precharge mode with stand-alone.

OCD\_CFG b7 (CBEN): This bit controls cell balancing.

0 = Disable the cell balancing function (default)

1 = Enable the cell balancing function.

**SCD\_CFG: Short-Circuit in Discharge Configuration Register**

SCD_CFG REGISTER (0x0a)							
7	6	5	4	3	2	1	0
SCDD3	SCDD2	SCDD1	SCDD0	SCD3	SCD2	SCD1	SCD0

The SCD\_CFG register determines the short-circuit voltage threshold and detection delay time.

SCD\_CFG b3–b0 (SCD3–0): These lower-nibble bits select the value of the short-circuit in discharge voltage threshold with 0000 as the default, units in mV, and a resolution of 5 mV.

0x00	60 mV	0x04	80 mV	0x08	100 mV	0x0c	120 mV
0x01	65 mV	0x05	85 mV	0x09	105 mV	0x0d	125 mV
0x02	70 mV	0x06	90 mV	0x0a	110 mV	0x0e	130 mV
0x03	75 mV	0x07	95 mV	0x0b	115 mV	0x0f	135 mV

SCD\_CFG b7–b4 (SCDD3–0): These upper nibble bits select the value of the short circuit in discharge delay time. 0000 is the default, units of  $\mu$ s and a resolution of 60 $\mu$ s.

0x00	0 $\mu$ s	0x04	240 $\mu$ s	0x08	480 $\mu$ s	0x0c	720 $\mu$ s
0x01	60 $\mu$ s	0x05	300 $\mu$ s	0x09	540 $\mu$ s	0x0d	780 $\mu$ s
0x02	120 $\mu$ s	0x06	360 $\mu$ s	0x0a	600 $\mu$ s	0x0e	840 $\mu$ s
0x03	180 $\mu$ s	0x07	420 $\mu$ s	0x0b	660 $\mu$ s	0x0f	900 $\mu$ s

**EEPROM: EEPROM Write Enable and Configuration Register**

EEPROM REGISTER (0x0b)							
7	6	5	4	3	2	1	0
EEPROM7	EEPROM6	EEPROM5	EEPROM4	EEPROM3	EEPROM2	EEPROM1	EEPROM0

EEPROM b7–b0 (EEPROM7–0):

These bits enable data write to EEPROM(0x06–0x9a) with 0100 0001 (0x41).

Prewriting data is available by setting these bits with 0110 0010 (0x62).

Default is 0000 0000 (0x00).

**Zero-Volt Charging**

In order to charge cells, the CHG FET must be turned on to create a current path. When the battery voltage ( $V_{BAT}$ ) is low and the CHG is ON, the pack voltage ( $V_{PACK}$ ) is as low as the battery voltage. In cases where the level is below the supply voltage for the bq77PL900 is too low to operate, there are two configurations to provide the appropriate 0-V/precharge function.

Common FET mode does not require a dedicated 0-V/precharge FET. The CHG FET is ON. This method is suitable for a charger that has a 0-V/precharge function. The second mode is to use a 0-V/precharge FET which establishes a dedicated 0-V/precharge current path by using an additional open drain (GPOD output) for driving an external FET (PCHG FET). This configuration sustains the PACK+ voltage level. Any type of charger can be used with this configuration.

**Table 13. 0-V Charge Summary**

PROTECTION MODE	0-V CHARGE TYPE	DEMANDED CHARGE FUNCTION	APPLICATION CIRCUIT
Host-control mode	Common FET (1)	Fast charge Precharge	PMS = PACK GPOD output not used
	0-V/precharge FET (2)	Fast charge	PMS = GND GPOD output: Drives 0-V charge FET (PCHG FET)
Stand-alone mode	Common FET (1)	Fast charge Precharge	PMS = PACK GPOD output not used
	0-V/precharge FET (2)	Fast charge	PMS = GND GPOD output: Drives 0-V charge FET (PCHG FET)

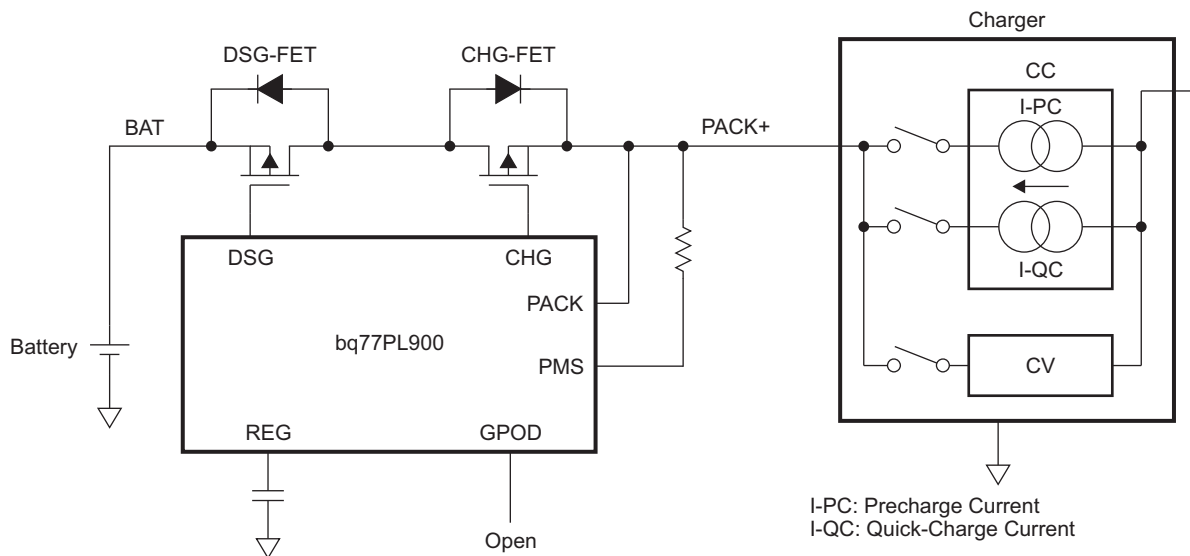
### Common FET

In this mode, the PMS pin is connected to PACK+. In this configuration, the charger must have a 0-V/precharging function which is typically controlled as follows:

- The cell voltage is lower than a certain constant voltage (normally about 3 V/cell).
  - Apply 0-V/precharging current.
- The cell voltage is higher than a certain constant voltage (normally about 3 V/cell).
  - Apply fast-charging current.

When the charger is connected and VPMS is greater than or equal to 0.7 V, the CHG FET is turned ON. The charging current flows through the CHG FET and the back diode of the DSG.

$$V_{PACK+} = V_{BAT} + 0.7 \text{ V (VF: forward voltage of a DSG-FET back diode)} + V_{DS}(\text{CHG-FET})$$

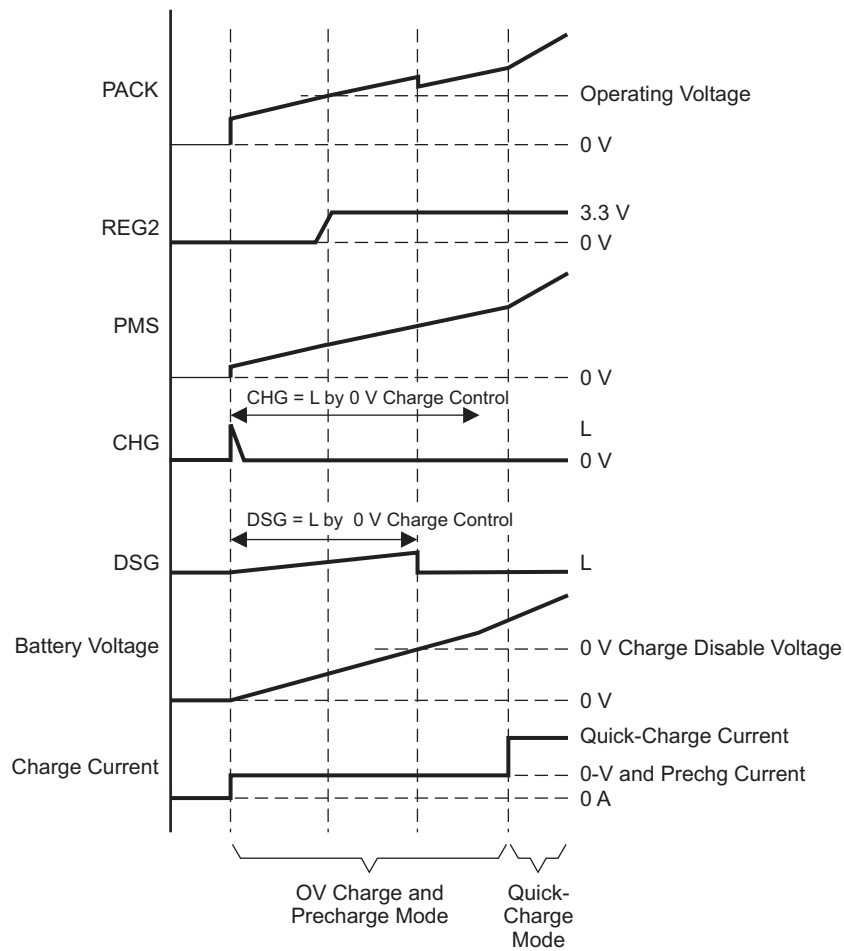


S0353-01

**Figure 27. Common FET Circuit Diagram**

When the PACK pin voltage is maintained at higher than 0.7 V and the precharging current is maintained, the PACK voltage and BAT voltage are under the minimum bq77PL900 supply voltage, so the regulator is inactive.

When the BAT voltage rises and the PACK pin voltage reaches the bq77PL900 minimum supply voltage, an internal 3.3-V regulator is turned ON. Then, the CHG FET state is controlled by UVP and OVP functions. When the all the cell voltages reach fast-charge voltage (about 3 V per cell), the charger starts the fast-charging mode.



T0381-01

Figure 28. Signal Timing of Pins During 0-V/Precharging

8.22.2 0-V/Precharge FET in Host Control Mode

In this configuration, the charger does not have a requirement to support a precharge function. Thus, the host controller and bq77PL900 must limit the fast charging current to a suitable 0-V/precharge level.

The PMS pin is connected to GND and a 0-V/precharge current flows through a dedicated 0-V/precharge FET (PCHG FET).



During the 0-V/precharge, the CHG FET is turned OFF and the PCHG FET is turned ON. When the host controller detects that all the cell voltages have reached the fast-charge threshold, it then turns ON the CHG FET and turns OFF the PCHG FET. The signal timing is shown in Figure 31.

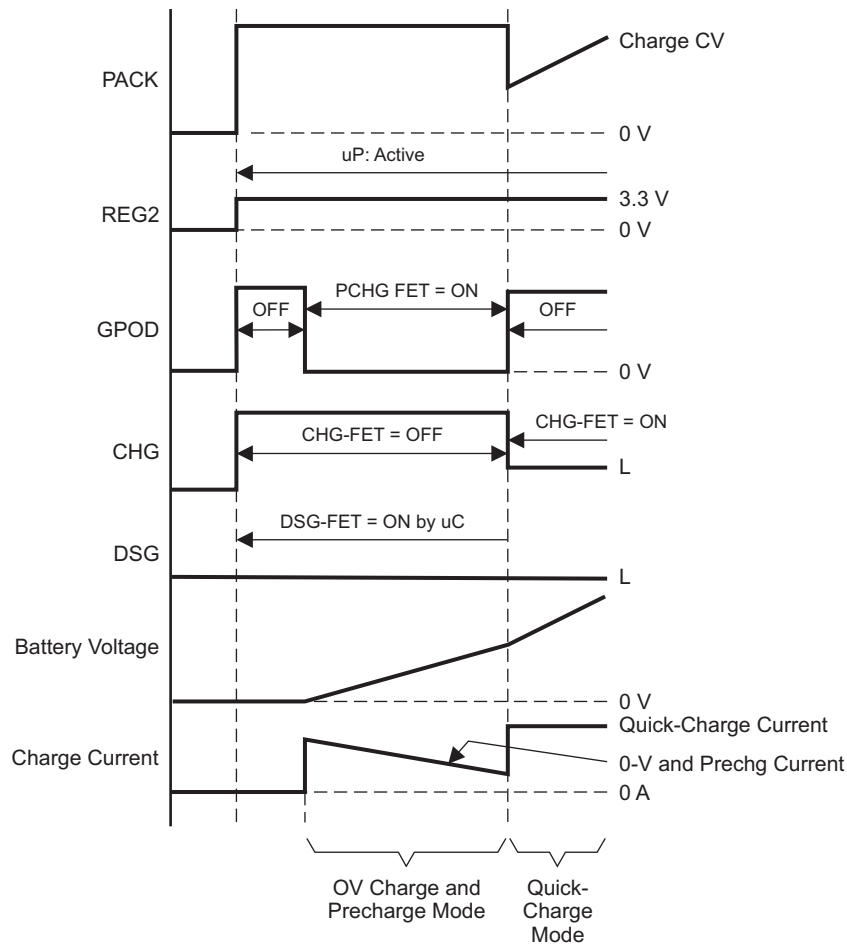
The CHG, DSG and PCHG FETs are turned OFF when the charger is connected. Then, the charger applies its maximum output voltage (constant-voltage-mode output voltage) to the PACK+ pin. Then, the bq77PL900 3.3-V regulator becomes active and supplies power to the host controller. As the host controller starts up, it turns on the GPOD output and the 0-V/precharge current begins to flow.

In this configuration, attention is needed to control high power consumption at the PCHG FET and the series resistor ( $R_p$ ). The highest power is consumed at 0-V cell voltage (highest voltage between PACK+ and BAT pins) and it results in highest heat generation. For example, the power consumption in 10 series batteries with 42-V fast charge voltage and 1-k $\Omega$   $R_p$  is expressed as follows.

$$I_{OV/PCHG} = (42\text{ V} - 0\text{ V}) / 1\text{ k}\Omega = 42\text{ mA}$$

$$(\text{Power consumption at } R_p) = 42\text{ V} \times 42\text{ mA} = 1.6\text{ W}$$

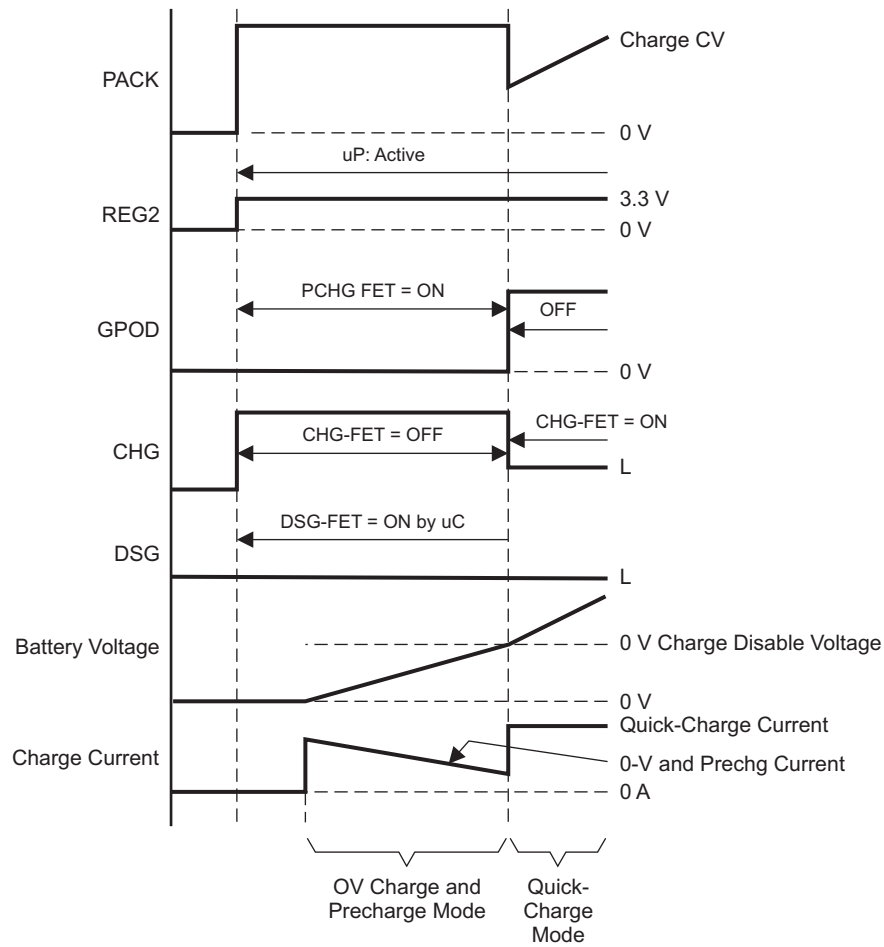
It is recommended to combine the resistor ( $R_p$ ) and the thermistor to reduce the consumption. Once the cell voltage reaches the fast-charge threshold, the host controller turns ON the CHG and DSG FETs and also turns OFF the PCHG FET.



T0382-01

**Figure 31. Signal Timing of Pins During 0-V Charging and Precharging (Precharge FET) With Host-Control Mode**





T0383-01

Figure 33. Signal Timing of Pins During 0-V/Precharging (PCHG FET) In Stand-Alone Mode

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ77PL900DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 100	BQ77PL900	<a href="#">Samples</a>
BQ77PL900DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 100	BQ77PL900	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

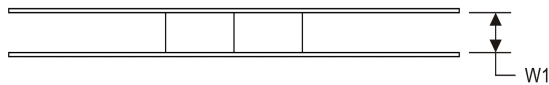
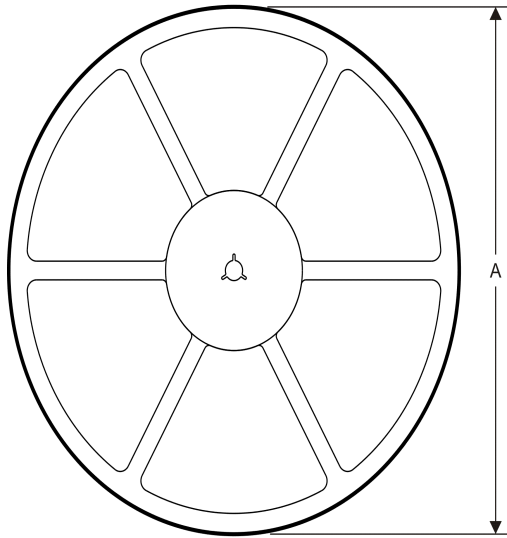
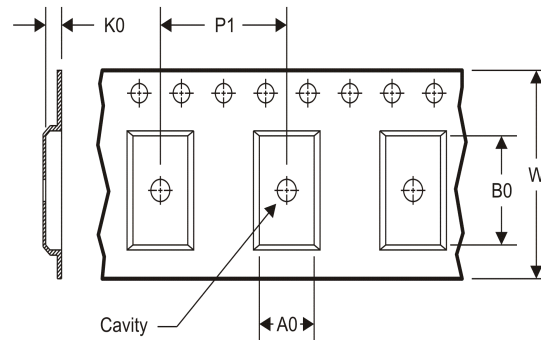
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


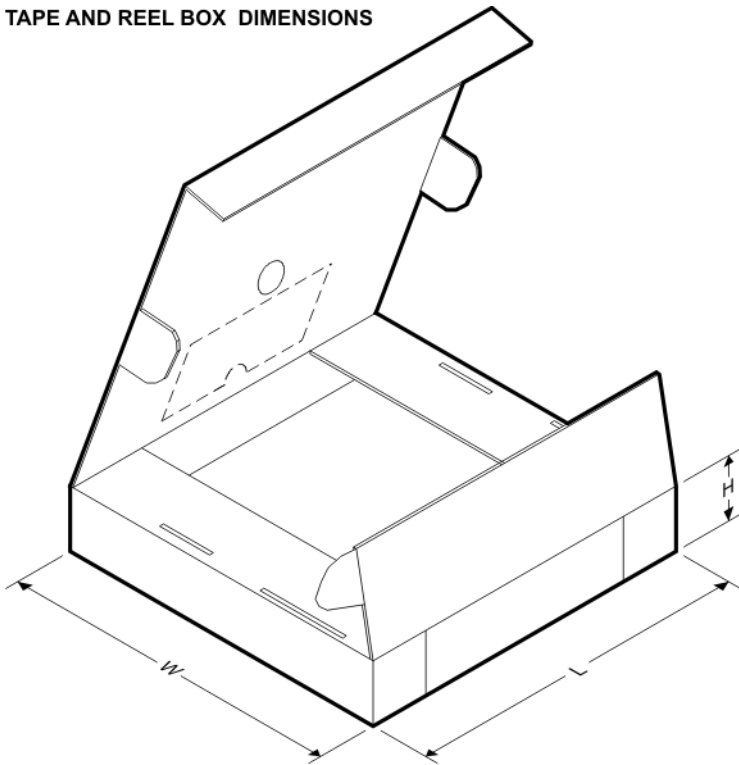
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ77PL900DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



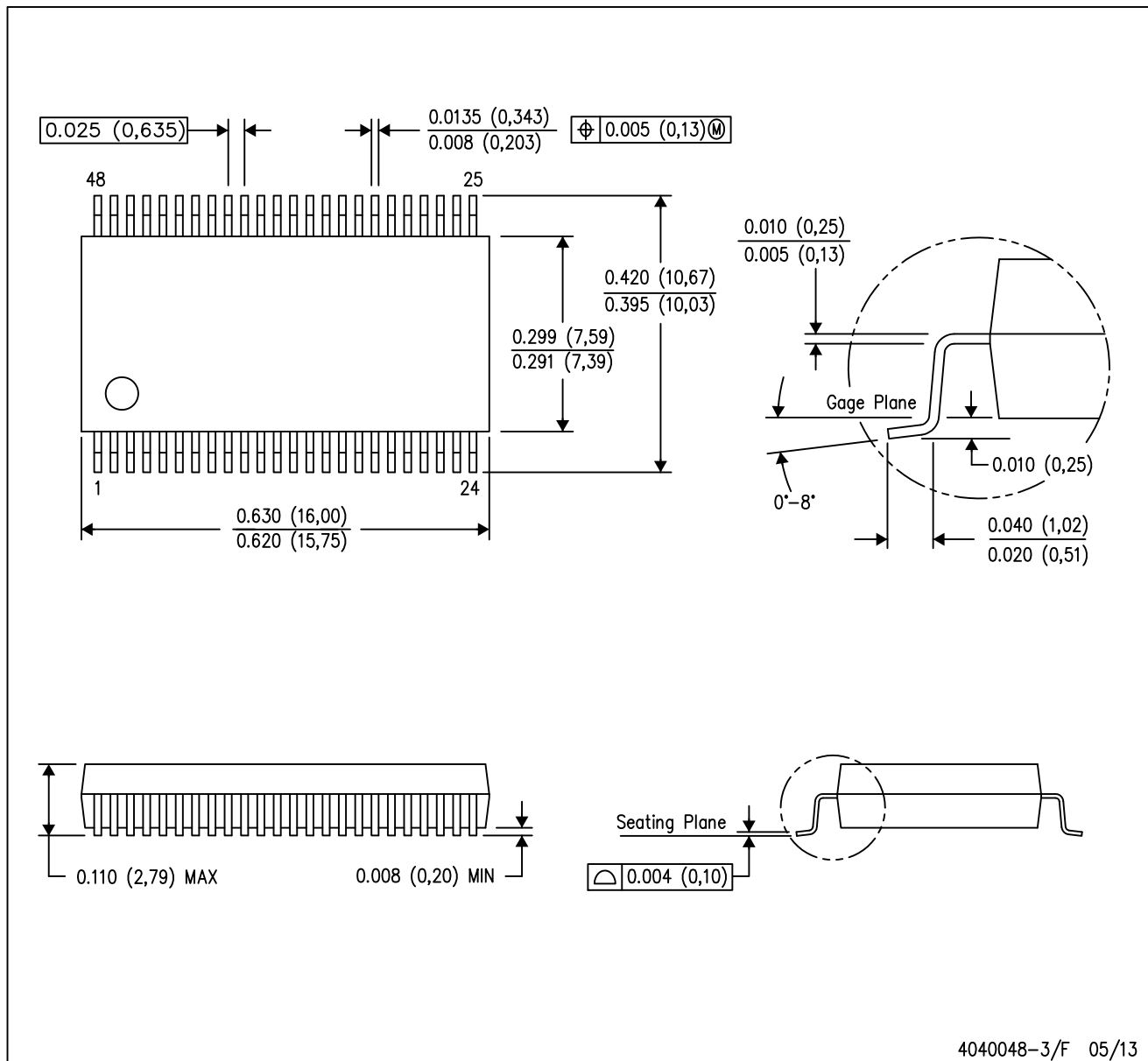
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ77PL900DLR	SSOP	DL	48	1000	367.0	367.0	55.0

# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View BQ77PL900EVM-001](#) on WIN SOURCE

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management