



**THE DATASHEET OF  
BQ3285P-SB2E3**



## Real-Time Clock (RTC)

### Features

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Functionally compatible with the DS1285
  - Closely matches MC146818A pin configuration
- 114 bytes of general nonvolatile storage
- 160ns cycle time allows fast bus operation
- Selectable Intel or Motorola bus timing
- Less than 0.5µA load under battery operation
- 14 bytes for clock/calendar and control
- BCD or binary format for clock and calendar data

- Calendar in day of the week, day of the month, months, and years, with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- Programmable square wave output
- Three individually maskable interrupt event flags:
  - Periodic rates from 122µs to 500ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle
- 24-pin plastic DIP or SOIC

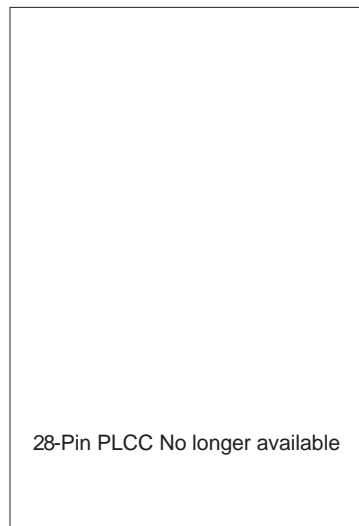
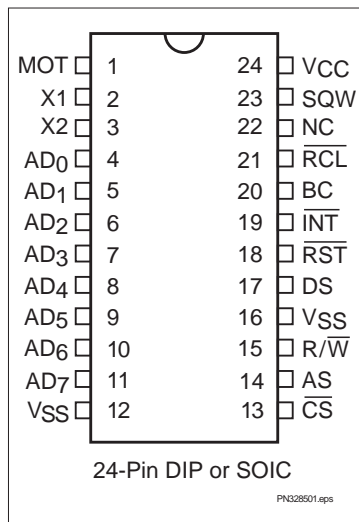
### General Description

The CMOS bq3285 is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. Other features include three maskable interrupt sources, square wave output, and 114 bytes of general nonvolatile storage.

The bq3285 write-protects the clock, calendar, and storage registers during power failure. A backup battery then maintains data and operates the clock and calendar.

The bq3285 is a fully compatible real-time clock for IBM AT compatible computers and other applications. The only external components are a 32.768kHz crystal and a backup battery

### Pin Connections

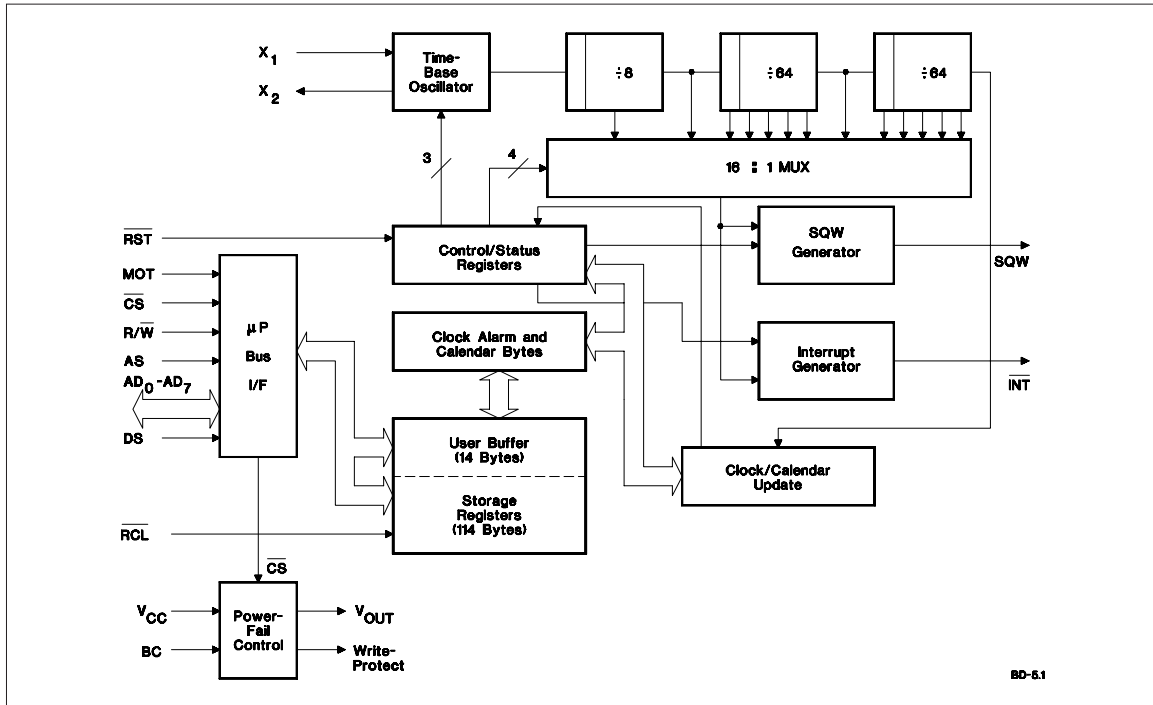


### Pin Names

AD <sub>0</sub> -AD <sub>7</sub>	Multiplexed address/data input/output
MOT	Bus type select input
CS	Chip select input
AS	Address strobe input
DS	Data strobe input
R/W	Read/write input
INT	Interrupt request output
RST	Reset input
SQW	Square wave output
RCL	RAM clear input
BC	3V backup cell input
X1-X2	Crystal inputs
NC	No connect
V <sub>CC</sub>	+5V supply
V <sub>SS</sub>	Ground

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## Block Diagram



## Pin Descriptions

### MOT Bus type select input

MOT selects bus timing for either Motorola or Intel architecture. This pin should be tied to  $V_{CC}$  for Motorola timing or to  $V_{SS}$  for Intel timing (see Table 1). The setting should not be changed during system operation. MOT is internally pulled low by a 30K $\Omega$  resistor.

Table 1. Bus Setup

Bus Type	MOT Level	DS Equivalent	R/W Equivalent	AS Equivalent
Motorola	$V_{CC}$	DS, E, or $\Phi 2$	$R/\overline{W}$	AS
Intel	$V_{SS}$	$\overline{RD}$ , $\overline{MEMR}$ , or I/OR	$\overline{WR}$ , $\overline{MEMW}$ , or I/OW	ALE

### AD<sub>0</sub>-AD<sub>7</sub> Multiplexed address/data input/output

The bq3285 bus cycle consists of two phases: the address phase and the data-transfer phase. The address phase precedes the data-transfer phase. During the address phase, an address placed on AD<sub>0</sub>-AD<sub>7</sub> is latched into the bq3285 on the falling edge of the AS signal. During the data-transfer phase of the bus cycle, the AD<sub>0</sub>-AD<sub>7</sub> pins serve as a bidirectional data bus.

### AS Address strobe input

AS serves to demultiplex the address/data bus. The falling edge of AS latches the address on AD<sub>0</sub>-AD<sub>7</sub>. This demultiplexing process is independent of the CS signal. For DIP and SOIC packages with MOT =  $V_{CC}$ , the AS input is provided a signal similar to ALE in an Intel-based system.

<b>DS</b>	<b>Data strobe input</b>	<b><math>\overline{\text{RCL}}</math></b>	<b>RAM clear input</b>
	When $\text{MOT} = \text{V}_{\text{CC}}$ , DS controls data transfer during a bq3285 bus cycle. During a read cycle, the bq3285 drives the bus after the rising edge on DS. During a write cycle, the falling edge on DS is used to latch write data into the chip.		A low level on the $\overline{\text{RCL}}$ pin causes the contents of each of the 114 storage bytes to be set to FF(hex). The contents of the clock and control registers are unaffected. This pin should be used as a user-interface input (pushbutton to ground) and not connected to the output of any active component. RCL input is only recognized when held low for at least 125ms in the presence of $\text{V}_{\text{CC}}$ when the oscillator is running. Using RAM clear does not affect the battery load. This pin is connected internally to a 30K $\Omega$ pull-up resistor.
	When $\text{MOT} = \text{V}_{\text{SS}}$ , the DS input is provided a signal similar to $\overline{\text{RD}}$ , $\overline{\text{MEMR}}$ , or $\overline{\text{I/OR}}$ in an Intel-based system. The falling edge on DS is used to enable the outputs during a read cycle.		
<b><math>\overline{\text{R/W}}</math></b>	<b>Read/write input</b>	<b>BC</b>	<b>3V backup cell input</b>
	When $\text{MOT} = \text{V}_{\text{CC}}$ , the level on $\overline{\text{R/W}}$ identifies the direction of data transfer. A high level on $\overline{\text{R/W}}$ indicates a read bus cycle, whereas a low on this pin indicates a write bus cycle.		BC should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of power. When $\text{V}_{\text{CC}}$ slews down past $\text{V}_{\text{BC}}$ (3V typical), the integral control circuitry switches the power source to BC. When $\text{V}_{\text{CC}}$ returns above $\text{V}_{\text{BC}}$ , the power source is switched to $\text{V}_{\text{CC}}$ .
	When $\text{MOT} = \text{V}_{\text{SS}}$ , $\overline{\text{R/W}}$ is provided a signal similar to $\overline{\text{WR}}$ , $\overline{\text{MEMW}}$ , or $\overline{\text{I/OW}}$ in an Intel-based system. The rising edge on $\overline{\text{R/W}}$ latches data into the bq3285.		Upon power-up, a voltage within the $\text{V}_{\text{BC}}$ range must be present on the BC pin for the oscillator to start up.
<b><math>\overline{\text{CS}}</math></b>	<b>Chip select input</b>	<b><math>\overline{\text{RST}}</math></b>	<b>Reset input</b>
	$\overline{\text{CS}}$ should be driven low and held stable during the data-transfer phase of a bus cycle accessing the bq3285.		The bq3285 is reset when $\overline{\text{RST}}$ is pulled low. When reset, $\overline{\text{INT}}$ becomes high-impedance, and the bq3285 is not accessible. Table 4 in the Control/Status Registers section lists the register bits that are cleared by a reset.
<b><math>\overline{\text{INT}}</math></b>	<b>Interrupt request output</b>		Reset may be disabled by connecting $\overline{\text{RST}}$ to $\text{V}_{\text{CC}}$ . This allows the control bits to retain their states through power-down/power-up cycles.
	$\overline{\text{INT}}$ is an open-drain output. $\overline{\text{INT}}$ is asserted low when any event flag is set and the corresponding event enable bit is also set. $\overline{\text{INT}}$ becomes high-impedance whenever register C is read (see the Control/Status Registers section).		
<b>SQW</b>	<b>Square-wave output</b>	<b>X1-X2</b>	<b>Crystal inputs</b>
	SQW may output a programmable frequency square-wave signal during normal ( $\text{V}_{\text{CC}}$ valid) system operation. Any one of the 13 specific frequencies may be selected through register A. This pin is held low when the square-wave enable bit (SQWE) in register B is 0 (see the Control/Status Registers section).		The X1-X2 inputs are provided for an external 32.768KHz quartz crystal, Daiwa DT-26 or equivalent, with 6pF load capacitance. A trimming capacitor may be necessary for extremely precise time-base generation.
			In the absence of a crystal, an oscillated output of 32.768kHz can be fed into the X1 input.

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## Functional Description

### Address Map

The bq3285 provides 14 bytes of clock and control/status registers and 114 bytes of general nonvolatile storage. Figure 1 illustrates the address map for the bq3285.

### Update Period

The update period for the bq3285 is one second. The bq3285 updates the contents of the clock and calendar locations during the update cycle at the end of each up-

date period (see Figure 2). The alarm flag bit may also be set during the update cycle.

The bq3285 copies the local register updates into the user buffer accessed by the host processor. When a 1 is written to the update transfer inhibit bit (UTI) in register B, the user copy of the clock and calendar bytes remains unchanged, while the local copy of the same bytes continues to be updated every second.

The update-in-progress bit (UIP) in register A is set  $t_{BUC}$  time before the beginning of an update cycle (see Figure 2). This bit is cleared and the update-complete flag (UF) is set at the end of the update cycle.

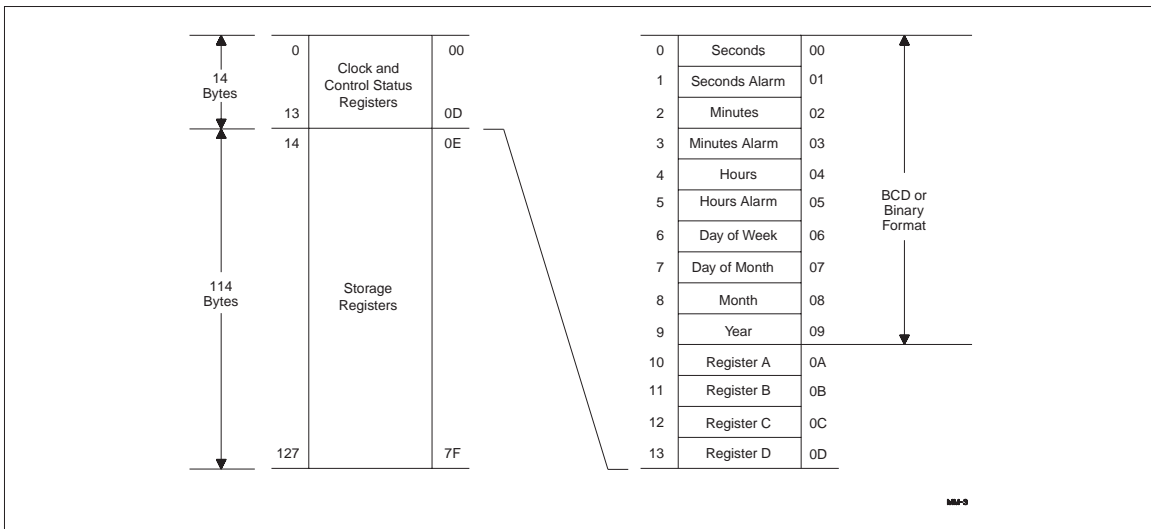


Figure 1. Address Map

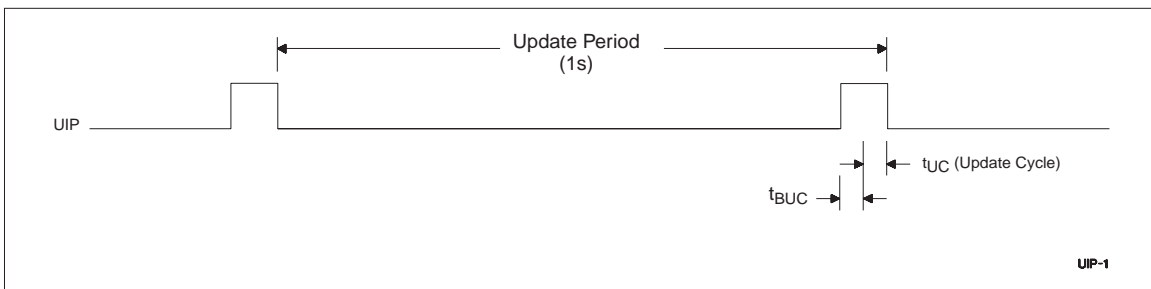


Figure 2. Update Period Timing and UIP

## Programming the RTC

The time-of-day, alarm, and calendar bytes can be written in either the BCD or binary format (see Table 2).

These steps may be followed to program the time, alarm, and calendar:

1. Modify the contents of register B:
  - a. Write a 1 to the UTI bit to prevent transfers between RTC bytes and user buffer.
  - b. Write the appropriate value to the data format (DF) bit to select BCD or binary format for all time, alarm, and calendar bytes.
2. Write new values to all the time, alarm, and calendar locations.
3. Clear the UTI bit to allow update transfers.

On the next update cycle, the RTC updates all 10 bytes in the selected format.

**Table 2. Time, Alarm, and Calendar Formats**

Address	RTC Bytes	Range		
		Decimal	Binary	Binary-Coded Decimal
0	Seconds	0–59	00H–3BH	00H–59H
1	Seconds alarm	0–59	00H–3BH	00H–59H
2	Minutes	0–59	00H–3BH	00H–59H
3	Minutes alarm	0–59	00H–3BH	00H–59H
4	Hours, 12-hour format	1–12	01H–0CH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours, 24-hour format	0–23	00H–17H	00H–23H
5	Hours alarm, 12-hour format	1–12	01H–0CH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours alarm, 24-hour format	0–23	00H–17H	00H–23H
6	Day of week (1=Sunday)	1–7	01H–07H	01H–07H
7	Day of month	1–31	01H–1FH	01H–31H
8	Month	1–12	01H–0CH	01H–12H
9	Year	0–99	00H–63H	00H–99H

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## Square-Wave Output

The bq3285 divides the 32.768kHz oscillator frequency to produce the 1Hz update frequency for the clock and calendar. Thirteen taps from the frequency divider are fed to a 16:1 multiplexer circuit. The output of this mux is fed to the SQW output and periodic interrupt generation circuitry. The four least-significant bits of register A, RS0–RS3, select among the 13 taps (see Table 3). The square-wave output is enabled by writing a 1 to the square-wave enable bit (SQWE) in register B.

## Interrupts

The bq3285 allows three individually selected interrupt events to generate an interrupt request. These three interrupt events are:

- The periodic interrupt, programmable to occur once every 122 $\mu$ s to 500ms
- The alarm interrupt, programmable to occur once per second to once per day

- The update-ended interrupt, which occurs at the end of each update cycle

Each of the three interrupt events is enabled by an individual interrupt-enable bit in register B. When an event occurs, its event flag bit in register C is set. If the corresponding event enable bit is also set, then an interrupt request is generated. The interrupt request flag bit (INTF) of register C is set with every interrupt request. Reading register C clears all flag bits, including INTF, and makes INT high-impedance.

Two methods can be used to process bq3285 interrupt events:

- Enable interrupt events and use the interrupt request output to invoke an interrupt service routine.
- Do not enable the interrupts and use a polling routine to periodically check the status of the flag bits.

The individual interrupt sources are described in detail in the following sections.

**Table 3. Square-Wave Frequency/Periodic Interrupt Rate**

Register A Bits				Square Wave		Periodic Interrupt	
RS3	RS2	RS1	RS0	Frequency	Units	Period	Units
0	0	0	0	None		None	
0	0	0	1	256	Hz	3.90625	ms
0	0	1	0	128	Hz	7.8125	ms
0	0	1	1	8.192	kHz	122.070	$\mu$ s
0	1	0	0	4.096	kHz	244.141	$\mu$ s
0	1	0	1	2.048	kHz	488.281	$\mu$ s
0	1	1	0	1.024	kHz	976.5625	$\mu$ s
0	1	1	1	512	Hz	1.95315	ms
1	0	0	0	256	Hz	3.90625	ms
1	0	0	1	128	Hz	7.8125	ms
1	0	1	0	64	Hz	15.625	ms
1	0	1	1	32	Hz	31.25	ms
1	1	0	0	16	Hz	62.5	ms
1	1	0	1	8	Hz	125	ms
1	1	1	0	4	Hz	250	ms
1	1	1	1	2	Hz	500	ms

## Periodic Interrupt

The mux output used to drive the SQW output also drives the interrupt-generation circuitry. If the periodic interrupt event is enabled by writing a 1 to the periodic interrupt enable bit (PIE) in register C, an interrupt request is generated once every 122 $\mu$ s to 500ms. The period between interrupts is selected by the same bits in register A that select the square wave frequency (see Table 3).

## Alarm Interrupt

During each update cycle, the RTC compares the hours, minutes, and seconds bytes with the three corresponding alarm bytes. If a match of all bytes is found, the alarm interrupt event flag bit, AF in register C, is set to 1. If the alarm event is enabled, an interrupt request is generated.

An alarm byte may be removed from the comparison by setting it to a “don’t care” state. An alarm byte is set to a “don’t care” state by writing a 1 to each of its two most-significant bits. A “don’t care” state may be used to select the frequency of alarm interrupt events as follows:

- If none of the three alarm bytes is “don’t care,” the frequency is once per day, when hours, minutes, and seconds match.
- If only the hour alarm byte is “don’t care,” the frequency is once per hour, when minutes and seconds match.
- If only the hour and minute alarm bytes are “don’t care,” the frequency is once per minute, when seconds match.
- If the hour, minute, and second alarm bytes are “don’t care,” the frequency is once per second.

## Update Cycle Interrupt

The update cycle ended flag bit (UF) in register C is set to a 1 at the end of an update cycle. If the update interrupt enable bit (UIE) of register B is 1, and the update transfer inhibit bit (UTI) in register B is 0, then an interrupt request is generated at the end of each update cycle.

## Accessing RTC bytes

Time and calendar bytes read during an update cycle may be in error. Three methods to access the time and calendar bytes without ambiguity are:

- Enable the update interrupt event to generate interrupt requests at the end of the update cycle. The interrupt handler has a maximum of 999ms to access the clock bytes before the next update cycle begins (see Figure 3).
- Poll the update-in-progress bit (UIP) in register A. If UIP = 0, the polling routine has a minimum of  $t_{BUC}$  time to access the clock bytes (see Figure 3).
- Use the periodic interrupt event to generate interrupt requests every  $t_{PI}$  time, such that UIP = 1 always occurs between the periodic interrupts. The interrupt handler has a minimum of  $t_{PI}/2 + t_{BUC}$  time to access the clock bytes (see Figure 3).

## Oscillator Control

When power is first applied to the bq3285 and  $V_{CC}$  is above  $V_{PPD}$ , the internal oscillator and frequency divider are turned on by writing a 010 pattern to bits 4 through 6 of register A. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. Any other pattern to these bits keeps the oscillator off.

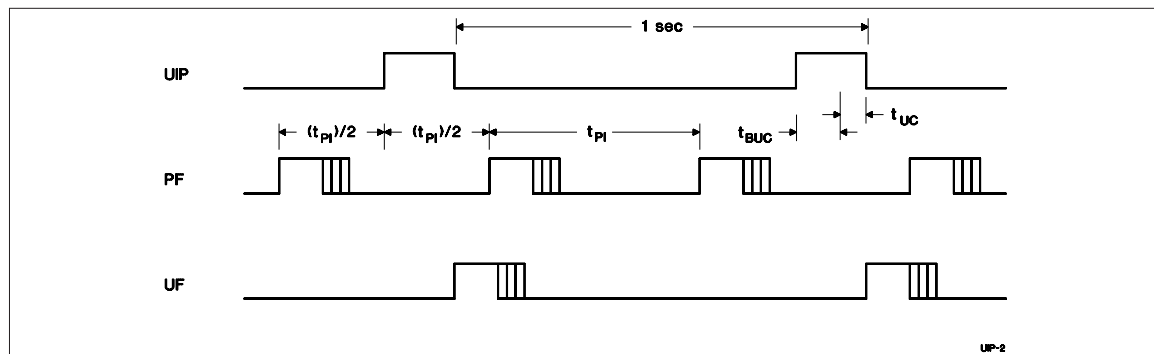


Figure 3. Update-Ended/Periodic Interrupt Relationship

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## Power-Down/Power-Up Cycle

The bq3285 continuously monitors  $V_{CC}$  for out-of-tolerance. During a power failure, when  $V_{CC}$  falls below  $V_{PFD}$  (4.17V typical), the bq3285 write-protects the clock and storage registers. When  $V_{CC}$  is below  $V_{BC}$  (3V typical), the power source is switched to BC. RTC operation and storage data are sustained by a valid backup energy source. When  $V_{CC}$  is above  $V_{BC}$ , the power source is  $V_{CC}$ . Write-protection continues for  $t_{CSR}$  time after  $V_{CC}$  rises above  $V_{PFD}$ .

## Control/Status Registers

The four control/status registers of the bq3285 are accessible regardless of the status of the update cycle (see Table 4).

### Register A

Register A Bits							
7	6	5	4	3	2	1	0
UIP	OS2	OS1	OS0	RS3	RS2	RS1	RS0

Register A programs:

- The frequency of the square-wave and the periodic event rate.
- Oscillator operation.

Register A provides:

- Status of the update cycle.

### RS0–RS3 - Frequency Select

7	6	5	4	3	2	1	0
-	-	-	-	RS3	RS2	RS1	RS0

These bits select one of the 13 frequencies for the SQW output and the periodic interrupt rate, as shown in Table 3.

### OS0–OS2 - Oscillator Control

7	6	5	4	3	2	1	0
-	OS2	OS1	OS0	-	-	-	-

These three bits control the state of the oscillator and divider stages. A pattern of 010 enables RTC operation by turning on the oscillator and enabling the frequency divider. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. When 010 is written, the RTC begins its first update after 500ms.

### UIP - Update Cycle Status

7	6	5	4	3	2	1	0
UIP	-	-	-	-	-	-	-

This read-only bit is set prior to the update cycle. When UIP equals 1, an RTC update cycle may be in progress. UIP is cleared at the end of each update cycle. This bit is also cleared when the update transfer inhibit (UTI) bit in register B is 1.

**Table 4. Control/Status Registers**

Reg.	Loc. (Hex)	Read	Write	Bit Name and State on Reset															
				7 (MSB)	6	5	4	3	2	1	0 (LSB)								
A	0A	Yes	Yes <sup>1</sup>	UIP	na	OS2	na	OS1	na	OS0	na	RS3	na	RS2	na	RS1	na	RS0	na
B	0B	Yes	Yes	UTI	na	PIE	0	AIE	0	UIE	0	SQWE	0	DF	na	HF	na	DSE	na
C	0C	Yes	No	INTF	0	PF	0	AF	0	UF	0	-	0	-	0	-	0	-	0
D	0D	Yes	No	VRT	na	-	0	-	0	-	0	-	0	-	0	-	0	-	0

- Notes:**
1. Except bit 7.
  2. na = not affected

**Register B**

Register B Bits							
7	6	5	4	3	2	1	0
UTI	PIE	AIE	UIE	SQWE	DF	HF	DSE

Register B enables:

- Update cycle transfer operation
- Square-wave output
- Interrupt events
- Daylight saving adjustment

Register B selects:

- Clock and calendar data formats

All bits of register B are read/write.

**DSE - Daylight Saving Enable**

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DSE

This bit enables daylight-saving time adjustments when written to 1:

- On the last Sunday in October, the first time the bq3285 increments past 1:59:59 AM, the time falls back to 1:00:00 AM.
- On the first Sunday in April, the time springs forward from 2:00:00 AM to 3:00:00 AM.

**HF - Hour Format**

7	6	5	4	3	2	1	0
-	-	-	-	-	-	HF	-

This bit selects the time-of-day and alarm hour format:

- 1 = 24-hour format
- 0 = 12-hour format

**DF - Data Format**

7	6	5	4	3	2	1	0
-	-	-	-	-	DF	-	-

This bit selects the numeric format in which the time, alarm, and calendar bytes are represented:

- 1 = Binary
- 0 = BCD

**SQWE - Square-Wave Enable**

7	6	5	4	3	2	1	0
-	-	-	-	SQWE	-	-	-

This bit enables the square-wave output:

- 1 = Enabled
- 0 = Disabled and held low

**UIE - Update Cycle Interrupt Enable**

7	6	5	4	3	2	1	0
-	-	-	UIE	-	-	-	-

This bit enables an interrupt request due to an update ended interrupt event:

- 1 = Enabled
- 0 = Disabled

The UIE bit is automatically cleared when the UTI bit equals 1.

**AIE - Alarm Interrupt Enable**

*This bit enables an interrupt request due to an alarm*

7	6	5	4	3	2	1	0
-	-	AIE	-	-	-	-	-

interrupt event:

- 1 = Enabled
- 0 = Disabled

**PIE - Periodic Interrupt Enable**

This bit enables an interrupt request due to a periodic

7	6	5	4	3	2	1	0
-	PIE	-	-	-	-	-	-

interrupt event:

- 1 = Enabled
- 0 = Disabled

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## UTI - Update Transfer Inhibit

7	6	5	4	3	2	1	0
UTI	-	-	-	-	-	-	-

This bit inhibits the transfer of RTC bytes to the user buffer:

1 = Inhibits transfer and clears UIE

0 = Allows transfer

## Register C

Register C Bits							
7	6	5	4	3	2	1	0
INTF	PF	AF	UF	0	0	0	0

Register C is the read-only event status register.

### Bits 0–3 - Unused Bits

7	6	5	4	3	2	1	0
-	-	-	-	0	0	0	0

These bits are always set to 0.

### UF - Update Event Flag

7	6	5	4	3	2	1	0
-	-	-	UF	-	-	-	-

This bit is set to a 1 at the end of the update cycle. Reading register C clears this bit.

### AF - Alarm Event Flag

7	6	5	4	3	2	1	0
-	-	AF	-	-	-	-	-

This bit is set to a 1 when an alarm event occurs. Reading register C clears this bit.

### PF - Periodic Event Flag

7	6	5	4	3	2	1	0
-	PF	-	-	-	-	-	-

This bit is set to a 1 every  $t_{PI}$  time, where  $t_{PI}$  is the time period selected by the settings of RS0–RS3 in register A. Reading register C clears this bit.

## INTF - Interrupt Request Flag

7	6	5	4	3	2	1	0
INTF	-	-	-	-	-	-	-

This flag is set to a 1 when any of the following is true:

AIE = 1 and AF = 1

PIE = 1 and PF = 1

UIE = 1 and UF = 1

Reading register C clears this bit.

## Register D

7	6	5	4	3	2	1	0
VRT	-	-	-	-	-	-	-

Register D is the read-only data integrity status register.

### Bits 0–6 - Unused Bits

7	6	5	4	3	2	1	0
-	0	0	0	0	0	0	0

These bits are always set to 0.

### VRT - Valid RAM and Time

Register D Bits							
7	6	5	4	3	2	1	0
VRT	0	0	0	0	0	0	0

1 = Valid backup energy source

0 = Backup energy source is depleted

When the backup energy source is depleted (VRT = 0), data integrity of the RTC and storage registers is not guaranteed.

## Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V <sub>CC</sub>	DC voltage applied on V <sub>CC</sub> relative to V <sub>SS</sub>	-0.3 to 7.0	V	
V <sub>T</sub>	DC voltage applied on any pin excluding V <sub>CC</sub> relative to V <sub>SS</sub>	-0.3 to 7.0	V	V <sub>T</sub> ≤ V <sub>CC</sub> + 0.3
T <sub>OPR</sub>	Operating temperature	0 to +70	°C	Commercial
T <sub>STG</sub>	Storage temperature	-55 to +125	°C	
T <sub>BIAS</sub>	Temperature under bias	-40 to +85	°C	
T <sub>SOLDER</sub>	Soldering temperature	260	°C	For 10 seconds

**Note:** Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

## Recommended DC Operating Conditions (T<sub>A</sub> = T<sub>OPR</sub>)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>SS</sub>	Supply voltage	0	0	0	V
V <sub>IL</sub>	Input low voltage	-0.3	-	0.8	V
V <sub>IH</sub>	Input high voltage	2.2	-	V <sub>CC</sub> + 0.3	V
V <sub>BC</sub>	Backup cell voltage	2.5	-	4.0	V

**Note:** Typical values indicate operation at T<sub>A</sub> = 25°C.

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### DC Electrical Characteristics ( $T_A = T_{OPR}$ , $V_{CC} = 5V \pm 10\%$ )

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I <sub>LI</sub>	Input leakage current	-	-	± 1	μA	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>
I <sub>LO</sub>	Output leakage current	-	-	± 1	μA	AD <sub>0</sub> –AD <sub>7</sub> , $\overline{INT}$ , and SQW in high impedance, V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub>
V <sub>OH</sub>	Output high voltage	2.4	-	-	V	I <sub>OH</sub> = -2.0 mA
V <sub>OL</sub>	Output low voltage	-	-	0.4	V	I <sub>OL</sub> = 4.0 mA
I <sub>CC</sub>	Operating supply current	-	7	15	mA	Min. cycle, duty = 100%, I <sub>OH</sub> = 0mA, I <sub>OL</sub> = 0mA
V <sub>SO</sub>	Supply switch-over voltage	-	V <sub>BC</sub>	-	V	
I <sub>CCB</sub>	Battery operation current	-	0.3	0.5	μA	V <sub>BC</sub> = 3V, T <sub>A</sub> = 25°C
V <sub>PFD</sub>	Power-fail-detect voltage	4.0	4.17	4.35	V	
I <sub>RCL</sub>	Input current when $\overline{RCL} = V_{SS}$ .	-	-	185	μA	Internal 30K pull-up
I <sub>MOTH</sub>	Input current when MOT = V <sub>CC</sub>	-	-	-185	μA	Internal 30K pull-down

Notes: Typical values indicate operation at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5V or V<sub>BC</sub> = 3V.

### Crystal Specifications (DT-26 or Equivalent)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f <sub>0</sub>	Oscillation frequency	-	32.768	-	kHz
C <sub>L</sub>	Load capacitance	-	6	-	pF
T <sub>P</sub>	Temperature turnover point	20	25	30	°C
k	Parabolic curvature constant	-	-	-0.042	ppm/°C
Q	Quality factor	40,000	70,000	-	
R <sub>1</sub>	Series resistance	-	-	45	KΩ
C <sub>0</sub>	Shunt capacitance	-	1.1	1.8	pF
C <sub>0</sub> /C <sub>1</sub>	Capacitance ratio	-	430	600	
D <sub>L</sub>	Drive level	-	-	1	μW
Δf/f <sub>0</sub>	Aging (first year at 25°C)	-	1	-	ppm

**Capacitance** ( $T_A = 25^\circ\text{C}$ ,  $F = 1\text{MHz}$ ,  $V_{CC} = 5.0\text{V}$ )

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{LO}$	Input/output capacitance	-	-	7	pF	$V_{OUT} = 0\text{V}$
$C_{IN}$	Input capacitance	-	-	5	pF	$V_{IN} = 0\text{V}$

**AC Test Conditions**

Parameter	Test Conditions
Input pulse levels	0 to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

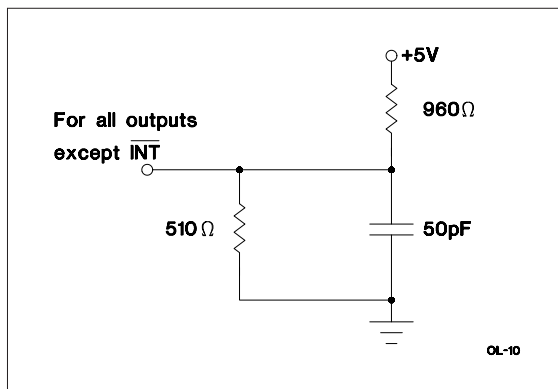


Figure 4. Output Load A

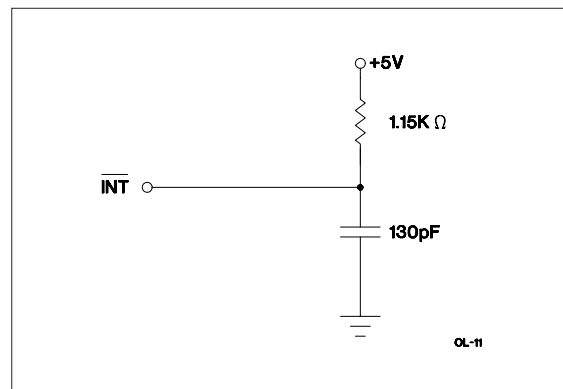


Figure 5. Output Load B

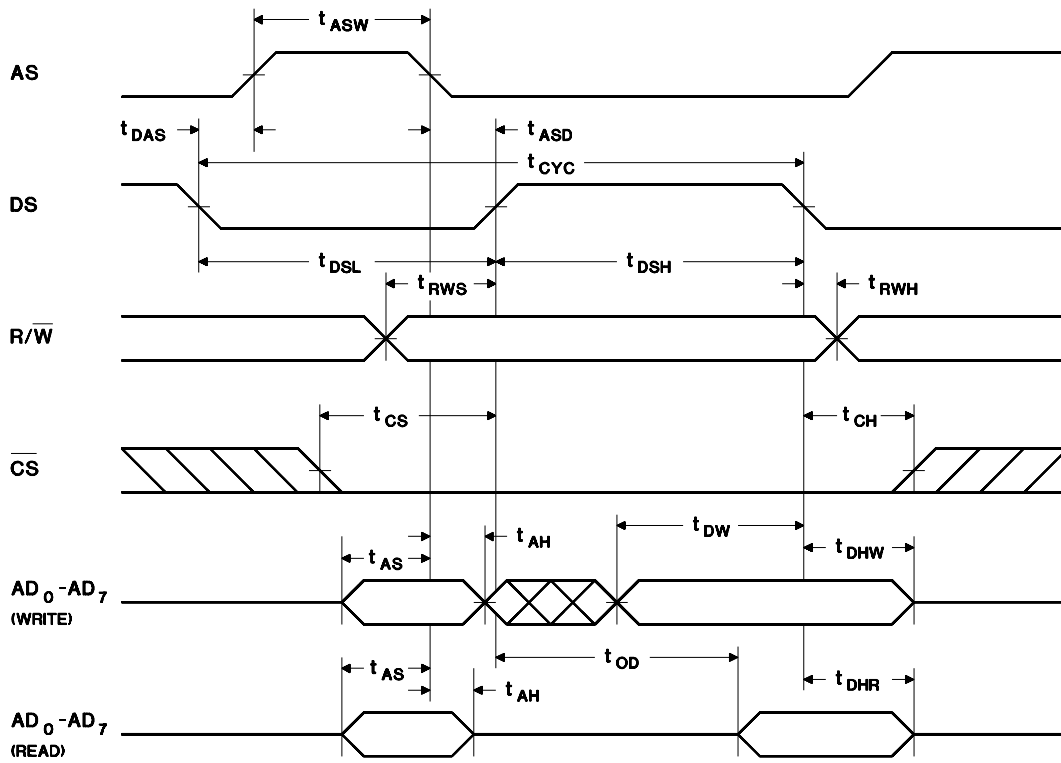
## bq3285

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### Read/Write Timing ( $T_A = T_{OPR}$ , $V_{CC} = 5V \pm 10\%$ )

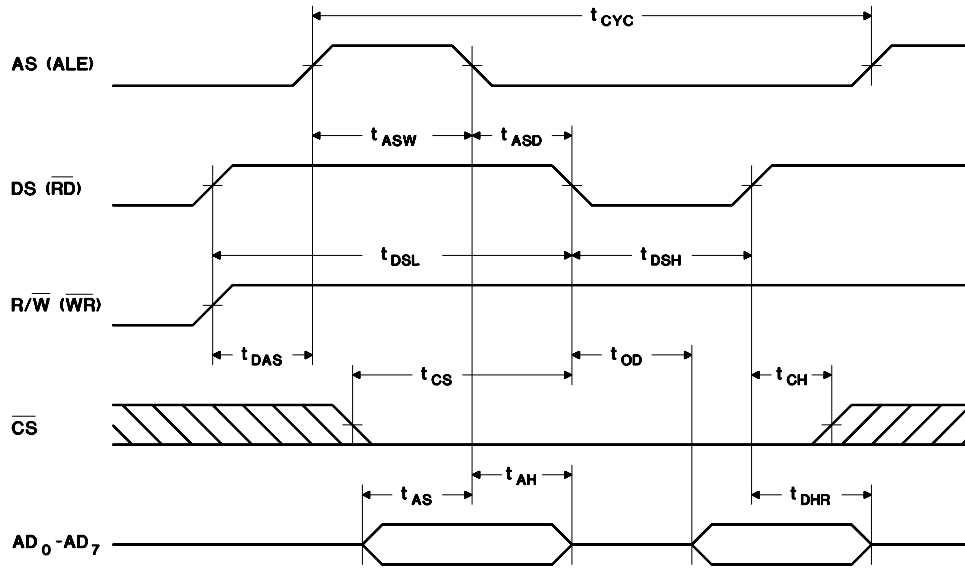
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t <sub>CYC</sub>	Cycle time	160	-	-	ns	
t <sub>DSL</sub>	DS low or $\overline{RD}/\overline{WR}$ high time	80	-	-	ns	
t <sub>DSH</sub>	DS high or $\overline{RD}/\overline{WR}$ low time	55	-	-	ns	
t <sub>RWH</sub>	$R/\overline{W}$ hold time	0	-	-	ns	
t <sub>RWS</sub>	$R/\overline{W}$ setup time	10	-	-	ns	
t <sub>CS</sub>	Chip select setup time	5	-	-	ns	
t <sub>CH</sub>	Chip select hold time	0	-	-	ns	
t <sub>DHR</sub>	Read data hold time	0	-	25	ns	
t <sub>DHW</sub>	Write data hold time	0	-	-	ns	
t <sub>AS</sub>	Address setup time	20	-	-	ns	
t <sub>AH</sub>	Address hold time	5	-	-	ns	
t <sub>DAS</sub>	Delay time, DS to AS rise	10	-	-	ns	
t <sub>ASW</sub>	Pulse width, AS high	30	-	-	ns	
t <sub>ASD</sub>	Delay time, AS to DS rise ( $\overline{RD}/\overline{WR}$ fall)	35	-	-	ns	
t <sub>OD</sub>	Output data delay time from DS rise (RD fall)	-	-	50	ns	
t <sub>DW</sub>	Write data setup time	30	-	-	ns	
t <sub>BUC</sub>	Delay time before update cycle	-	244	-	$\mu$ s	
t <sub>PI</sub>	Periodic interrupt time interval	-	-	-	-	See Table 3
t <sub>UC</sub>	Time of update cycle	-	1	-	$\mu$ s	

Motorola Bus Read/Write Timing



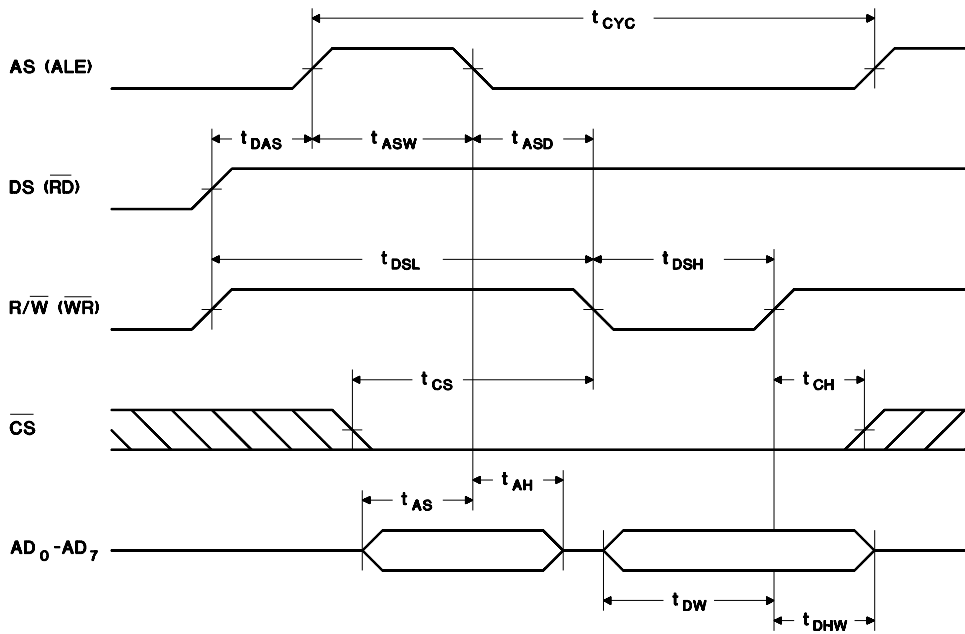
RC-4

Intel Bus Read Timing



RC-5

Intel Bus Write Timing

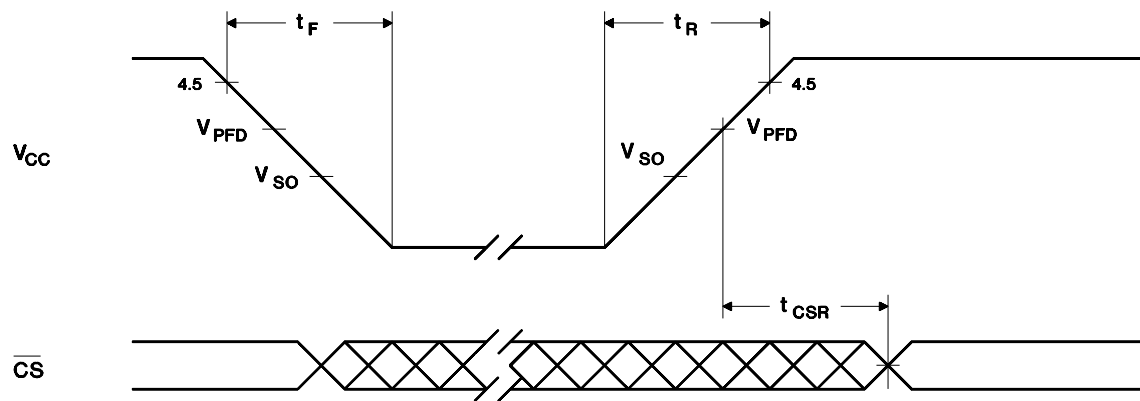


WC-5

**Power-Down/Power-Up Timing** ( $T_A = T_{OPR}$ )

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$t_F$	$V_{CC}$ slew from 4.5V to 0V	300	-	-	$\mu s$	
$t_R$	$V_{CC}$ slew from 0V to 4.5V	100	-	-	$\mu s$	
$t_{CSR}$	$\overline{CS}$ at $V_{IH}$ after power-up	20	-	200	ms	Internal write-protection period after $V_{CC}$ passes $V_{PFD}$ on power-up.

**Power-Down/Power-Up Timing**



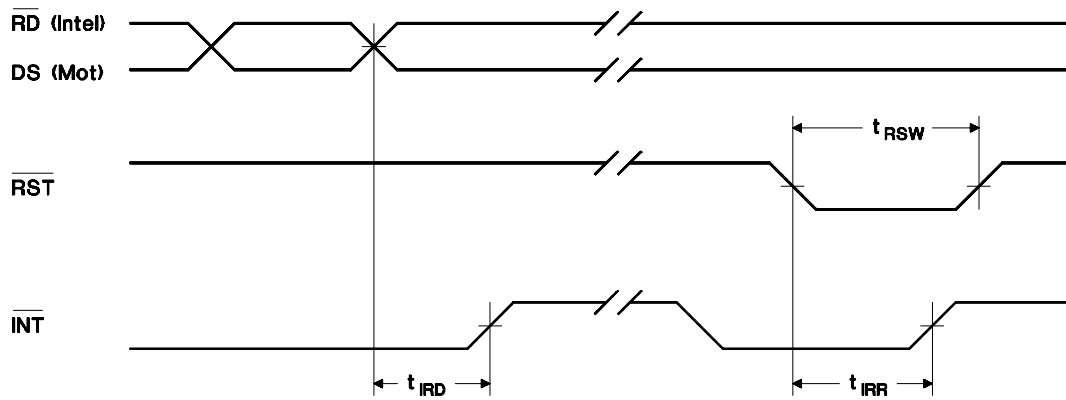
PD-4A

# bq3285

## Interrupt Delay Timing ( $T_A = T_{OPR}$ )

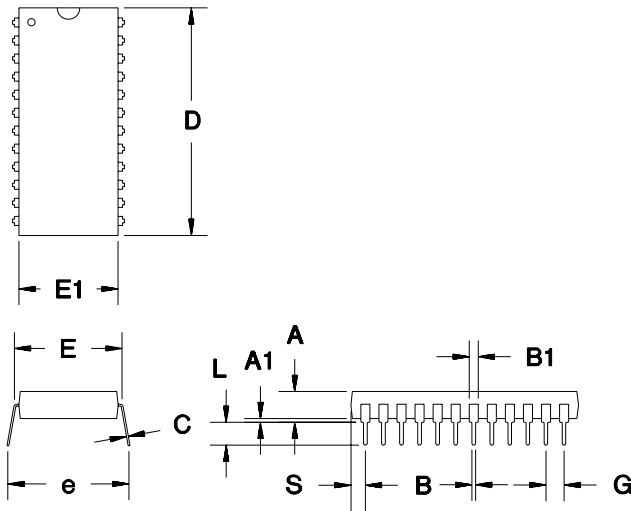
Symbol	Parameter	Minimum	Typical	Maximum	Unit
$t_{RSW}$	Reset pulse width	5	-	-	$\mu s$
$t_{IRR}$	$\overline{INT}$ release from $\overline{RST}$	-	-	2	$\mu s$
$t_{IRD}$	$\overline{INT}$ release from DS ( $\overline{RD}$ )	-	-	2	$\mu s$

## Interrupt Delay Timing



INT-1

24-Pin DIP (P)

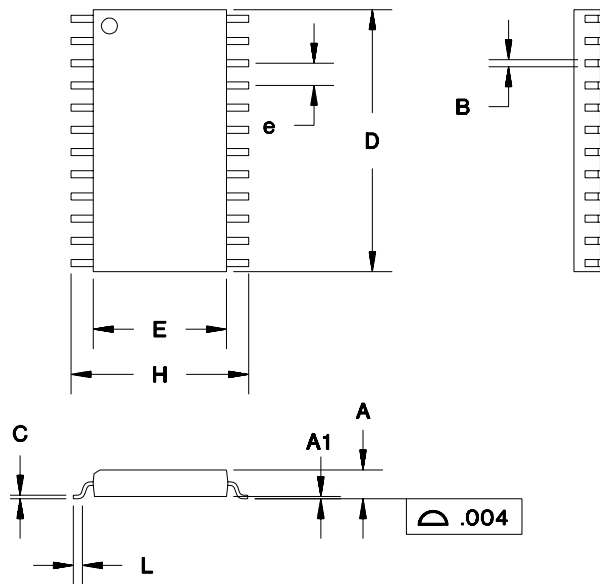


24-Pin DIP (P)

Dimension	Minimum	Maximum
A	0.160	0.190
A1	0.015	0.040
B	0.015	0.022
B1	0.045	0.065
C	0.008	0.013
D	1.240	1.280
E	0.600	0.625
E1	0.530	0.570
e	0.600	0.670
G	0.090	0.110
L	0.115	0.150
S	0.070	0.090

All dimensions are in inches.

24-Pin SOIC (S)



24-Pin SOIC (S)

Dimension	Minimum	Maximum
A	0.095	0.105
A1	0.004	0.012
B	0.013	0.020
C	0.008	0.013
D	0.600	0.615
E	0.290	0.305
e	0.045	0.055
H	0.395	0.415
L	0.020	0.040

All dimensions are in inches.

## bq3285

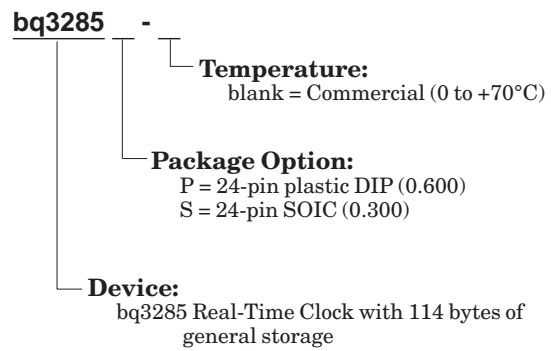
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### Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	2	Address strobe input	Clarification
1	11	Backup cell voltage $V_{BC}$	Was 2.0 min; is 2.5 min
1	12	Power-fail detect voltage $V_{PFD}$	Was 4.1 min, 4.25 max; in 4.0 mi, 4.35 max
2	3, 12	crystal type Daiwa DT-26 (not DT-26S)	Clarification
3	12	Changed value in first table	$I_{RCL}$ max. was 275; is now 185
3	12	Changed value in first table	$I_{MOTH}$ max. was -275; is now -185
3	12	Changed values for conditions of $I_{RCL}$ , $I_{MOTH}$	Was 20K; is now 30K
4	1, 8, 20	PLCC last time buy and Reg A update	Reg A labeling corrected
5	1, 8, 20	PLCC package option removed	PLCC reached end of Last Time Buy

**Note:** Change 1 = Nov. 1992 B changes from June 1991 A.  
Change 2 = Nov. 1993 C changes from Nov. 1992 B  
Change 3 = Sept. 1996 D changes from Nov. 1993 C  
Change 4 = Jan. 1999 E changes from Sept. 1996 D  
Change 5 = May 2004 (SLUS028A) changes from Jan. 1999 E

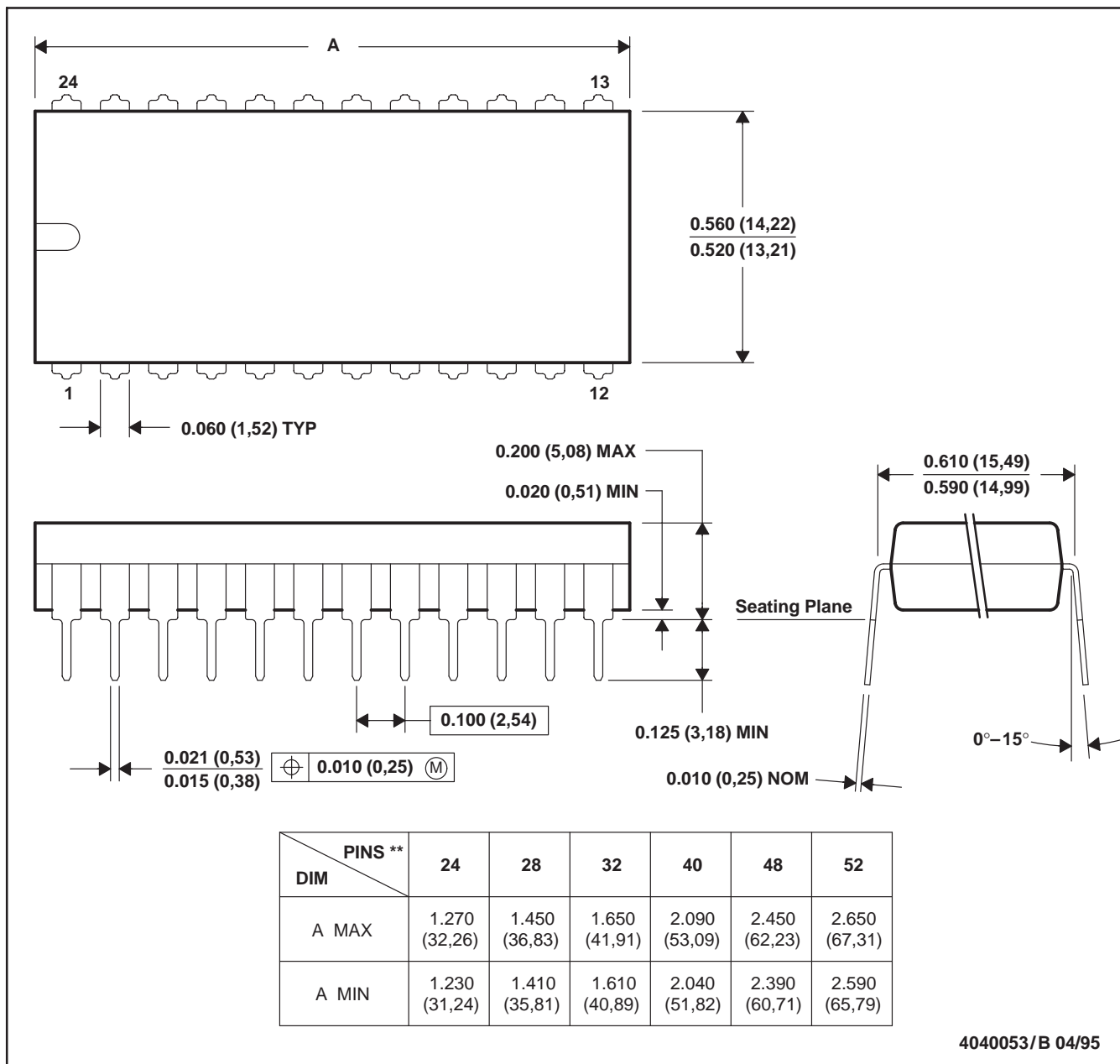
## Ordering Information



**N (R-PDIP-T\*\*)**

**PLASTIC DUAL-IN-LINE PACKAGE**

24 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-011  
 D. Falls within JEDEC MS-015 (32 pin only)

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ3285S-SB2	NRND	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3285S -SB2	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

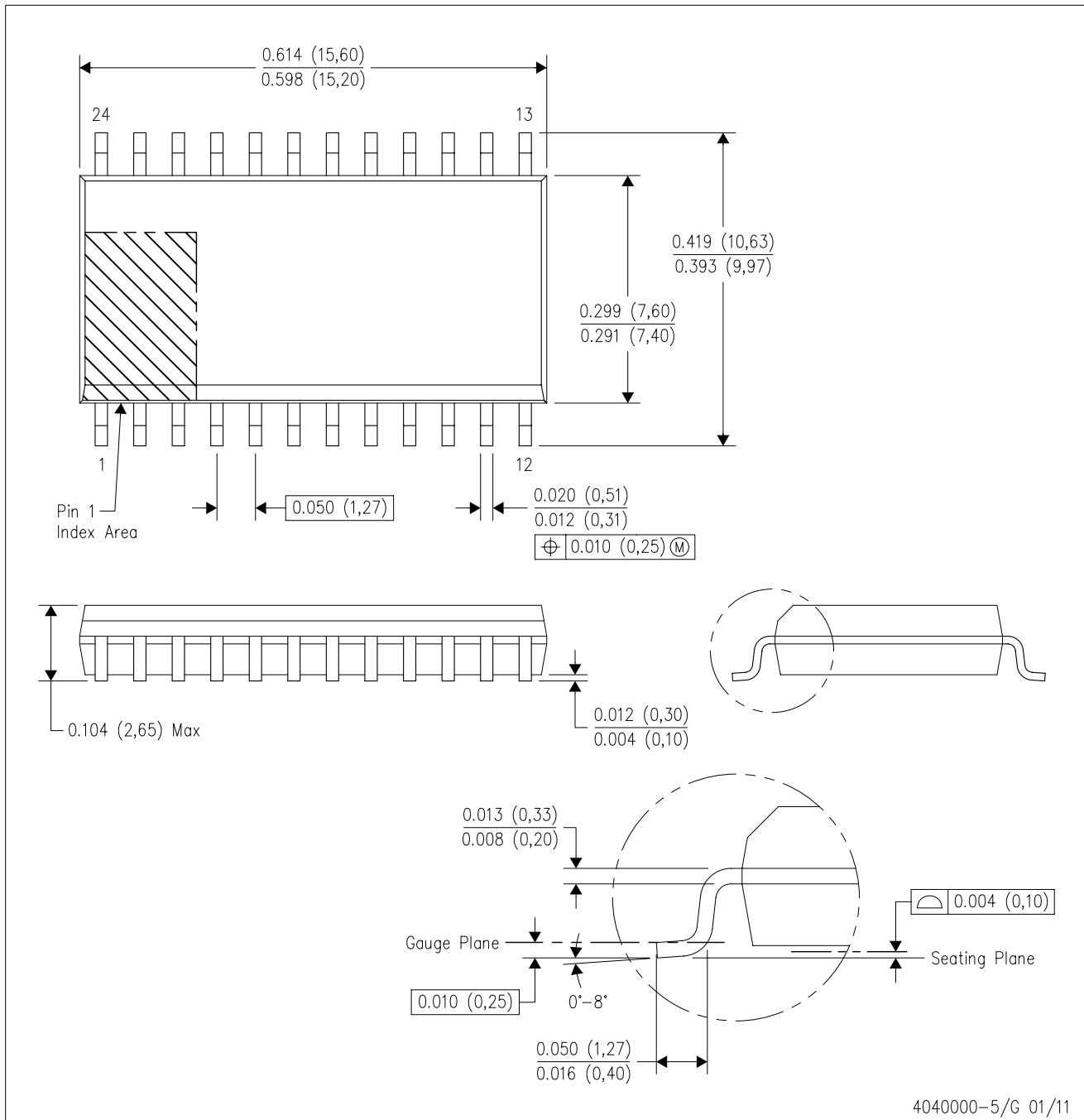
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
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  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AD.

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